EV2797-0000/0002-FP-00B

7-Cell to 16-Cell, High-Accuracy, I²C/SPI Monitor and Protector with Coulomb Counting Evaluation Board

DESCRIPTION

The EV2797-0000-FP-00B and EV2797-0002-FP-00B evaluation boards are designed to demonstrate the capabilities of the MP2797, a complete analog front-end (AFE) monitoring and protection IC. The MP2797 supports 7-cell to 16-cell series battery packs with outstanding voltage and current measurement accuracy, as well as a complete set of protection features.

The MP2797 measures each cell's voltage and synchronously measures the charge/discharge current and Coulomb counting via an external current-sense resistor. The MP2797 includes high-side MOSFET (HS-FET) drivers for charge and discharge control. It measures the die temperature and cell temperature via 4 NTC thermistor inputs. The MP2797 contains internal passive balancing MOSFETs capable of driving up to 58mA, and is also capable of driving external balancing transistors for a higher current.

The discharge (DSG) MOSFET driver includes a configurable soft start (SS) that provides a controlled turn-on, eliminating the need for an external pre-charge circuit. The MOSFET drivers also incorporate over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high/low-temperature protection. All of these protections have configurable thresholds.

This evaluation board combines the MP2797 with power MOSFETs and a current-sense resistor to support up to 70A of charge/discharge current. The board also includes placeholders to add external MOSFETs for a higher balancing current, if needed.

PERFORMANCE SUMMARY

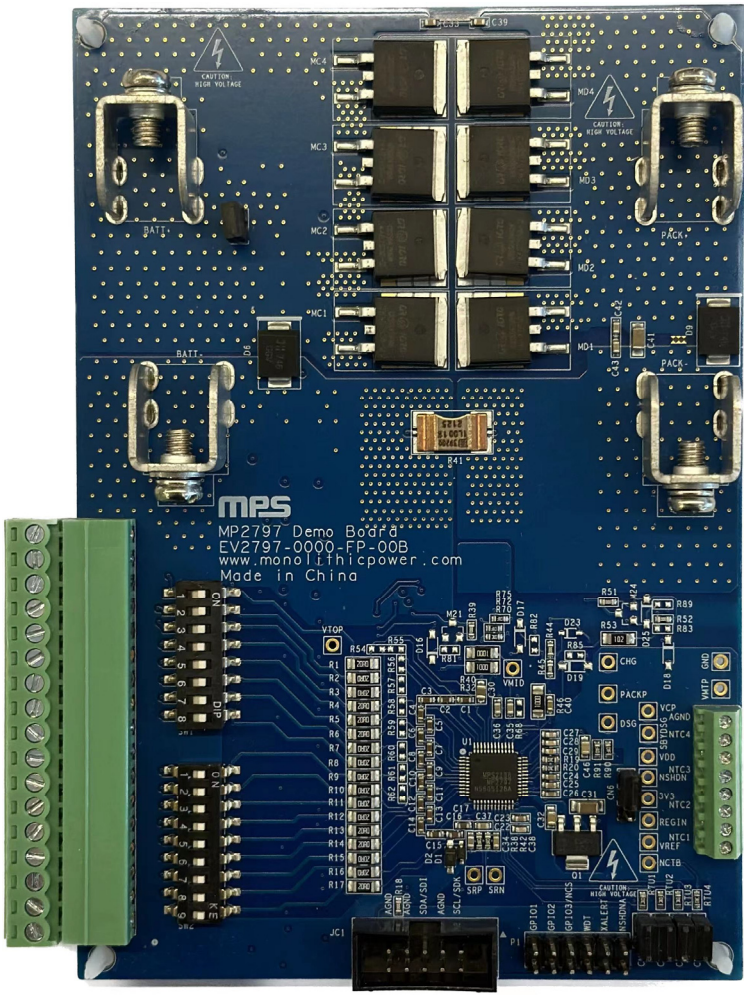
Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage range		18V to 75.2V
Cell voltage range		0V to 5V
Continuous charge current		0A to 70A
Continuous discharge current		0A to 70A
Internal balancing current	V_{BATT} = 4V, T_A = 25°C	58mA
External balancing current (1)	V_{BATT} = 4V, T_A = 25°C, R_{BAL} = 30Ω	130mA
Supported cells in series		7 to 16

Note:

1) A higher balancing current is possible when external balancing transistors are installed. Refer to the Configuration for External or Internal Cell-Balancing section in the MP2797 datasheet for details.

EVALUATION BOARDS



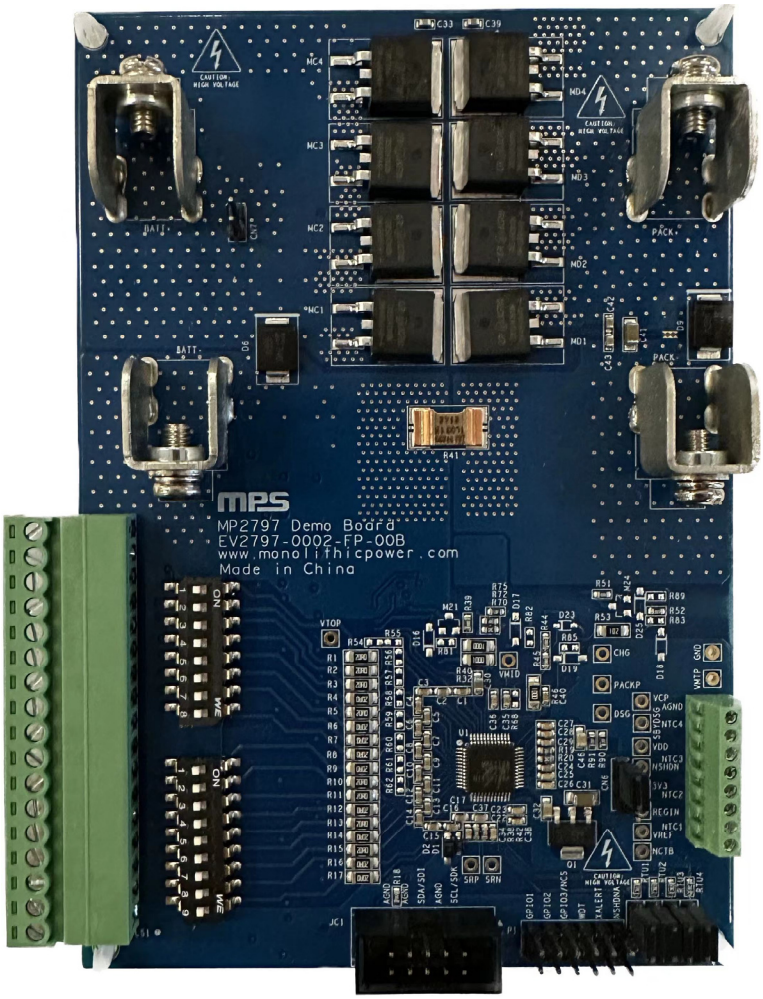
LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number	Description
EV2797-0000-FP-00B	MP2797DFP-0000 (2)	Supports I²C communication interface

Note:

2) "-0000" is the register setting option. For custom options, contact an MPS FAE to obtain an "-xxxx" value.

EVALUATION BOARDS *(continued)*



LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number	Description
EV2797-0002-FP-00B	MP2797DFP-0002 (3)	Supports SPI communication interface

Note:

3) "-0002" is the register setting option. For custom options, contact an MPS FAE to obtain an "-xxxx" value.

QUICK START GUIDE

The EV2797-0000/0002-FP-00B is designed for evaluation of the MP2797 and can be configured to support 7-cell to 16-cell series connections. This board incorporates the MP2797, power MOSFETs, a current-sense resistor, and other components. These evaluation boards include placeholders to add external MOSFETs and balancing resistors to support >58mA of balancing current, if needed. The EV2797-0000/0002-FP-00B includes protection capabilities with configurable thresholds for the following conditions: over-current (OC), short-circuit (SC), under-voltage (UV), over-voltage (OV), unbalanced cell(s), and high/low temperature.

Evaluation Platform Preparation

To use the evaluation platform, the following is required: a computer with at least one USB port, a USB cable, and a communication kit. The MP2797 programming tool must also be properly installed. This evaluation graphical user interface (GUI) software can be downloaded from the MPS website.

1. Use the USB-to-I²C communication kit (EVKT-USBI2C-02) if using the EV2797-0000-FP-00B (see Figure 1).

Figure 1: USB-to-I²C Communication Kit

2. Use the USB-to-SPI communication kit (EVKT-USBSPI-00) if using the EV2797-0002-FP-00B (see Figure 2).

Figure 2: USB-to-SPI Communication Kit

3. To check the software, double-click on the MP2797 evaluation kit .exe file, then open the software. The software is supported by Windows XP, 7, and later versions.
4. Using the cell simulator shunt (short CN7, turn the SW1 and SW2 channels on), set up the board quickly without a real battery pack.
5. Apply a DC power supply between BATT+ and BATT-, then adjust the power supply to be about 60V/1A.
6. Connect the USB-to-I²C kit to JC1 and consider the position of SCL and SDA. If connecting the USB-to-SPI kit to JC1, consider the position of NCS, SCK, SDO, and SDI.

   Figure 3 on page 5 shows the original test set-up for the MP2797DFP-0000.

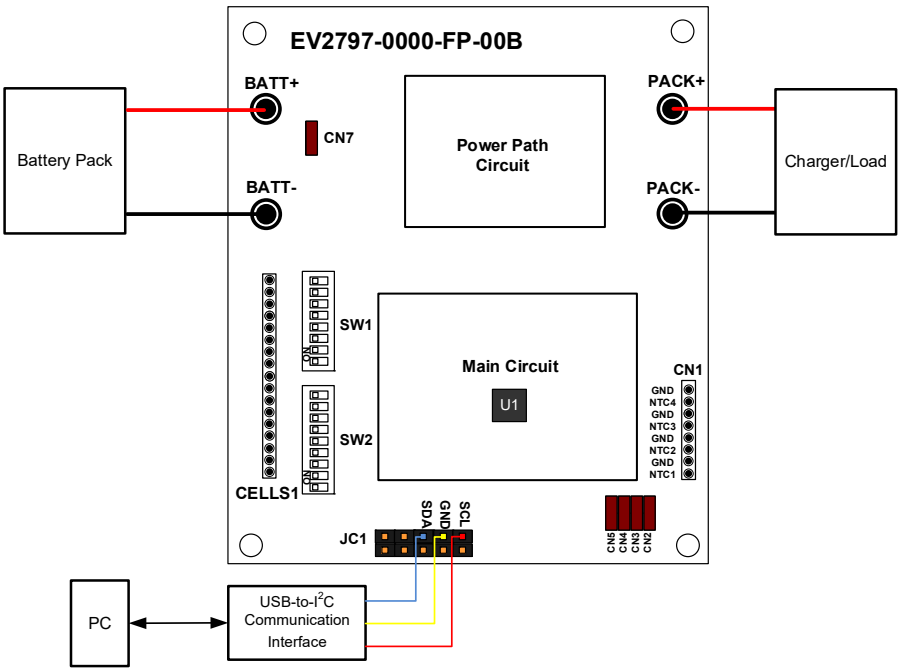


Figure 3: Test Set-Up for the MP2797DFP-0000

Figure 4 shows the original test set-up for the MP2797DFP-0002.

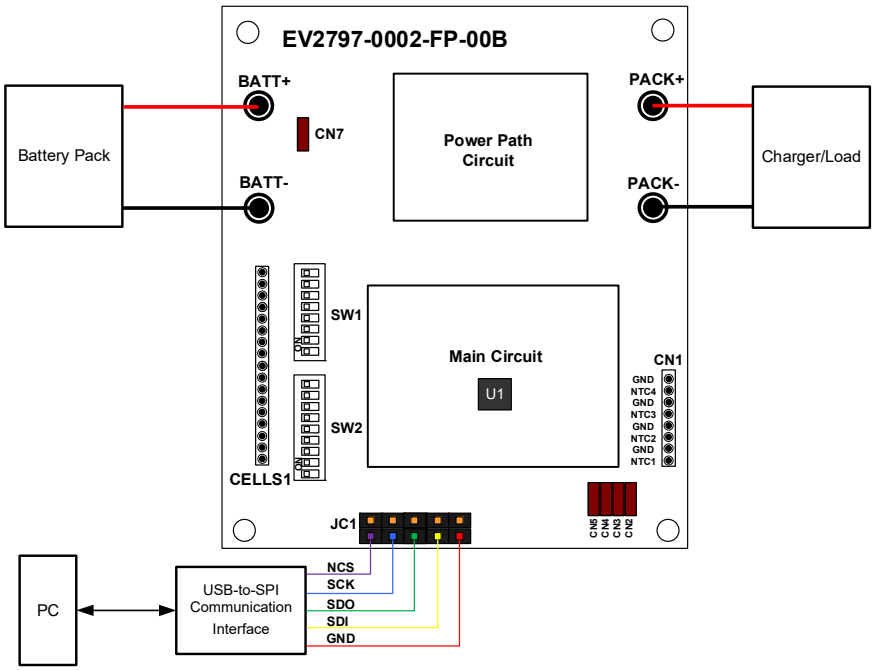


Figure 4: Test Set-Up for the MP2797DFP-0002

7. By default, this board has 16 cells in series. To use the cell simulator shunt and evaluate the device at a lower series number, short circuit the corresponding channels.

   Figure 5 shows the 10-cell series connection with the cell simulator shunt. Note that the DC power supply voltage between BATT+ and BATT- should be decreased depending on the number of cells in series.

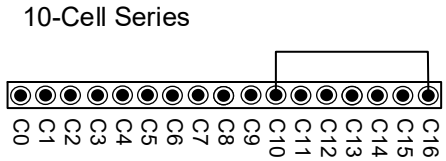


Figure 5: 10 Cells in Series Connection

8. Use a real battery pack to test the open-wire and cell balance functions, as these functions cannot be tested using the cell simulator shunt.

   Figure 6 shows the MP2797DFP-0000 test set-up with a battery pack.

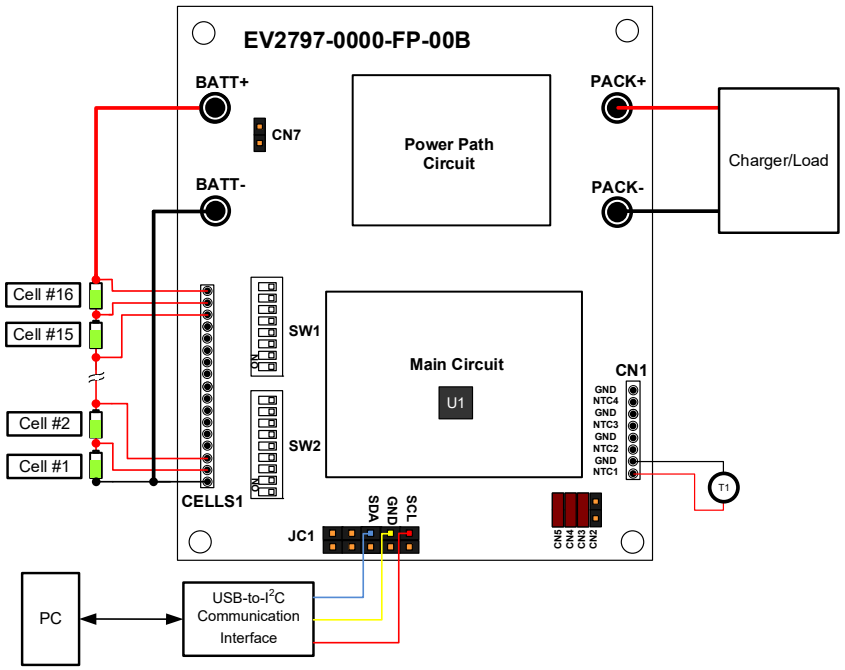


Figure 6: Test Set-Up for the MP2797DFP-0000 with a Battery Pack

Figure 7 on page 7 shows the MP2797DFP-0002 test set-up with a battery pack.

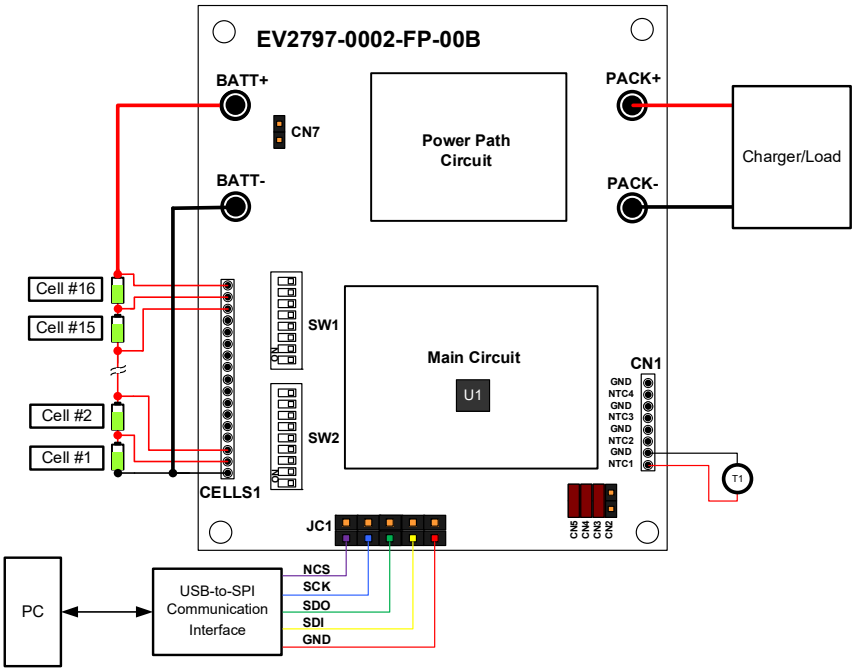


Figure 7: Test Set-Up for the MP2797DFP-0002 with a Battery Pack

9. Remove the CN7 jumper, then turn off the SW1 and SW2 channels.
10. If the application has less than 16 cells in series, use 0Ω resistors to short all unused cell channels (C_X) to the practical maximum cell channel. For example, when only 10 cells in series are used, short C10, C11, C12, C13, C14, C15, and C16 together by adding 0Ω resistors to R59, R58, R57, R56, R55 and R54. If the application has 16 cells in series, skip the shorting step.
11. Connect the cell terminals (CELLS1) to each cell-sensing point. If the number of cells in the battery pack is below 16, float the connectors' higher channels.
12. Connect the battery terminals to:
    a. Positive (+): BATT+
    b. Negative (-): BATT-
13. The EV2797-0000/0002-FP-00B has a bypass P-channel MOSFET (P-FET). In safe mode, turn on the P-FET using GPIO2 to power PACK with low power consumption. When $V_{PACK} < V_{TOP}$ - 2V, the P-FET current capacity is about 25mA. When $V_{PACK} > V_{TOP}$ - 2V, the P-FET can bypass about a 1A current. If this function is not used, set the GPIO2 output to a low level.

    It is recommended to use GPIOHV1 to control the bypass P-FET. Set the GPIOHV1 output to Hi-Z to turn the P-FET off.
14. Remove CN2, CN3, CN4, and CN5.
15. Connect and locate the temperature sensors to support up to 4 NTCs.
16. Connect the charger (or the load) terminals to:
    a. Positive (+): PACK+
    b. Negative (-): PACK-
17. Connect SDA, SCL, and GND to the USB-to-I²C communication interface. Carefully consider where SCL and SDA are positioned. If using the USB-to-SPI communication interface, connect NCS, SCK, SDO, SDI and GND instead. Carefully consider where NCS, SCK, SDO, and SDI are positioned.

18. Connect the communication interface to the PC, turn on the computer, and launch the MP2797 GUI evaluation software. Figure 8 shows the software's main window.

    If the previous steps are correct, "MP2797 Demo board: Connected" should be listed in the lower left corner. Otherwise, this area should read, "MP2797 Demo board: Disconnected!"

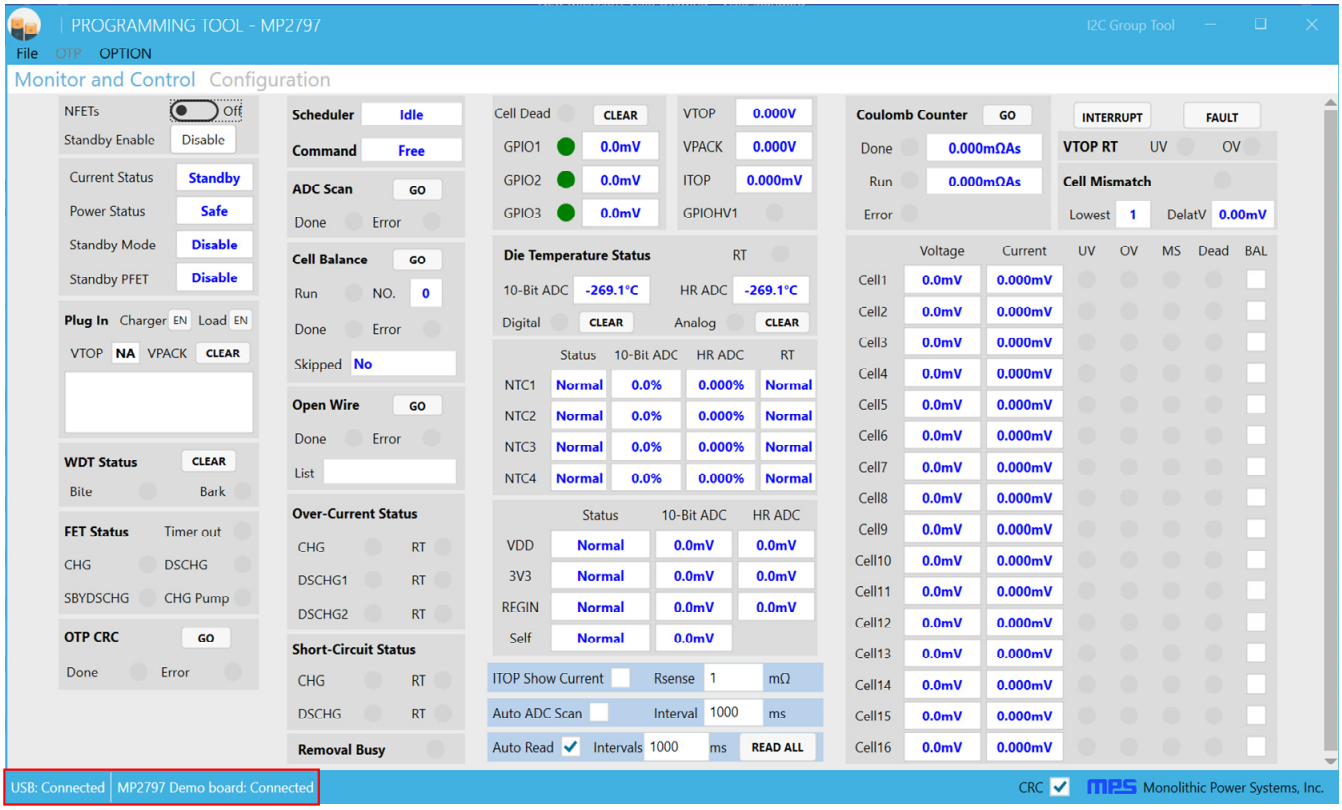


Figure 8: MP2797 Evaluation Software

PROCEDURE

Ensure that all the connections (e.g. between the USB-to-I²C/SPI communication kit and the EV2797-0000/0002-FP-00B) are successful.

1. Click the “Configuration” tab to view the configurations (see Figure 9). The software should automatically read all the configurations. Items with a lock symbol can be configured to be read-only.

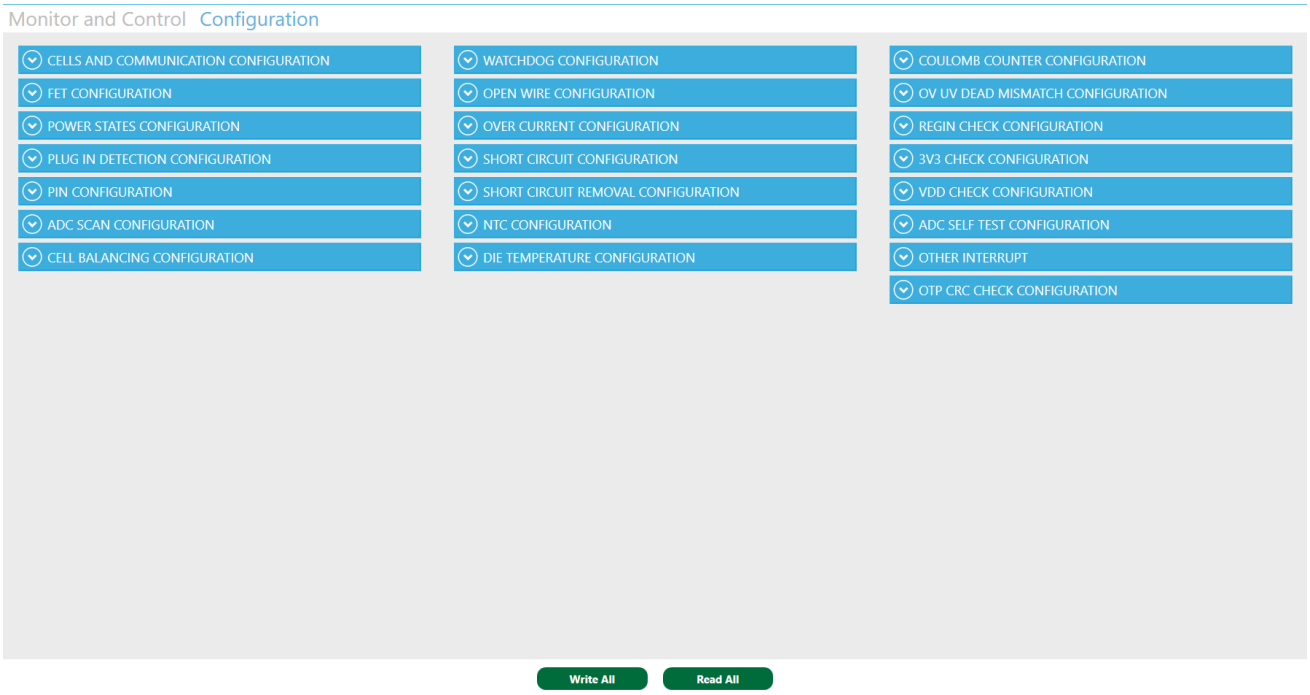


Figure 9: Configuration View

2. Configure the protection thresholds, enable all relevant functions, and set the corresponding faults.
3. Click the “Write All” button to write configurations into the register, then click the Monitor and Control tabs to switch the view.
4. Turn on the N-channel MOSFETs (N-FETs) then click the “Read All” button. The N-FET status should be displayed in green for CHG, DSG, and CHG Pump, and the power status should be set to active (see Figure 8 on page 8).
5. Click the “Read All” button. The updated values should be displayed in the GUI. If the “Auto Read” checkbox is checked, it is not required to click the “Read All” button.
6. Configure the cells and their communication (see Figure 10 on page 10).

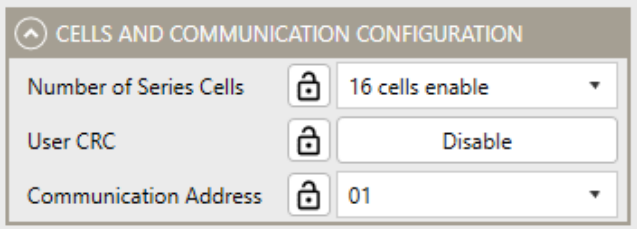


Figure 10: Cell and Communication Configuration

a. Number of Series Cells: Can be between 7 and 16.

b. User CRC: To enable the cyclic redundancy check (CRC) function, check the “CRC” checkbox at the bottom right of the GUI window. Otherwise, the value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address range is 00h to 7Fh. After changing this value, the new address should be used for the next communication. For devices with different “-xxxx” suffixes, the default address may be different. The GUI automatically scans the address, though this function can be disabled by unchecking “Monitor chip connection” in the “Option” tab.

7. Configure the FET (see Figure 11).

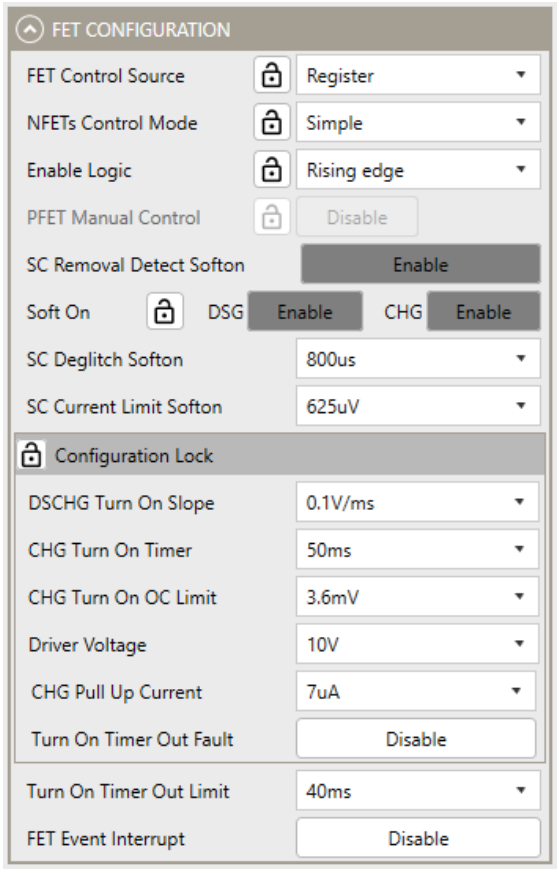


Figure 11: FET Configuration

a. FET Control Source: Can be set to GIPO control or register control.

b. NFETs Control Mode: Can be set to simple or direct mode. In direct mode with GPIO control, GPIO1 controls the DSG FET, while GPIO2 controls the CHG FET.

c. Enable Logic: Can be set to rising edge active or level active.

d. SC Removal Detect Soft Start (SS): Enables the short-circuit detection sequence that occurs before the DSCHG FET turns on.

e. SC Deglitch SS and SC Current Limit SS: When enabled, the DSG FET is protected from inrush current when charging a large capacitive load. These two settings protect the DSG FET while it ramps up during SS.

f. DSCHG Turn-On Slope: Can be set between 0.1V/ms and 1.6V/ms.

g. CHG Turn-On OC Limit: Selects the OC threshold that is applied during SS. The threshold can be set to 3.6mV or 4.8mV.

h. Driver Voltage: Defines the gate-to-source voltage (V_{GS}) for the CHG and DSCHG FETs. V_{GS} can be between 7V and 12V.

i. CHG Pull-Up Current: Sets the CHG pin's output current during the CHG soft start period to control the rising slope of the CHG FET's driver voltage. Can be between 3µA and 10µA.

8. Configure the power status (see Figure 12).

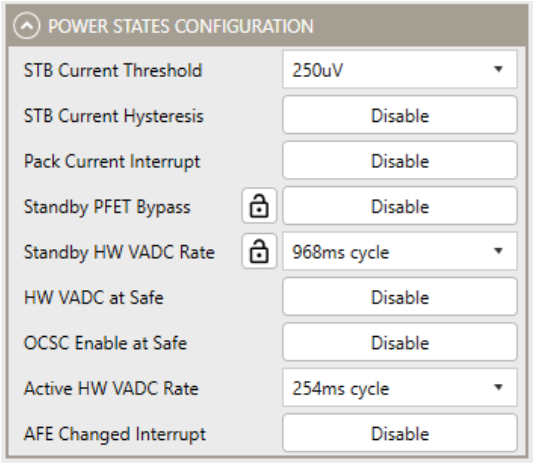


Figure 12: Power Status Configuration

a. HW VADC at Safe: If protections are required in safe mode, enable this function to ensure that the voltage can be monitored for protections.

b. Standby HW VADC Rate: Can be used with voltage protection monitoring to refresh the analog-to-digital converter (ADC) result while in safe or standby mode. This rate can be configured to refresh the voltage protection reading every 254ms, 492ms, or 968ms.

c. Active HW VADC Rate: Can be used with voltage protection monitoring to refresh the ADC result while in active mode. Can be configured to refresh the voltage protection reading every 135ms or 254ms.

9. Configure the plug-in parameters (see Figure 13).

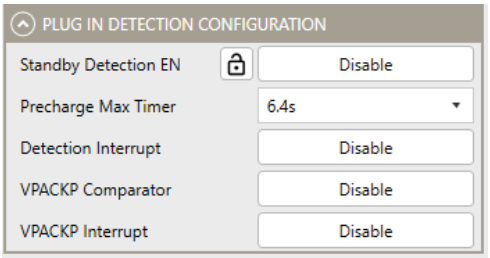


Figure 13: Plug-In Configuration

a. Pre-Charge Max Timer: Selects the PACKP pre-charge expiration timer, which ranges between 0.2s and 24s.

b. VPACKP Comparator: Enables the PACK vs. V_{TOP} comparator. When disabled, the comparator can still be internally enabled for other functions, such as plug-in detection.

10. Configure the GPIO pins (see Figure 14).

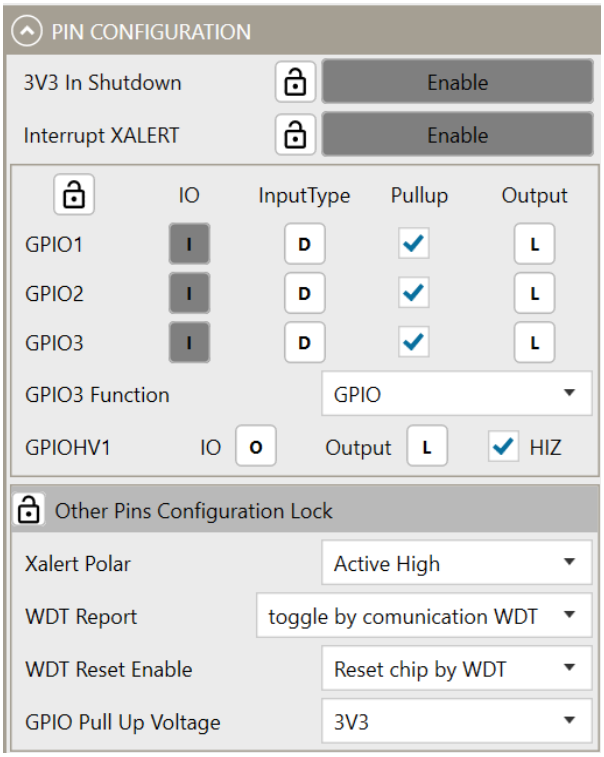


Figure 14: Pin Configuration

a. IO: Defines whether GPIO1~GPIO3 are set to act as inputs or outputs. If they are set to inputs, they cannot be left floating and must be connected to a high or low level. Otherwise, GPIO1~GPIO3 can consume excess power. GPIO2 can be used to control the bypass P-FET. Pull up GPIO2 to turn on the P-FET and set the GPIO2 output low to turn the P-FET off.

b. Input Type: Defines whether the input type for GPIO1~GPIO3 is a digital input or a buffered ADC input.

c. Pull-Up: Enables the GPIO1~GPIO3 pull-up capability. When enabled, a 20kΩ pull-up is applied.

d. Output: Sets the target output level for GPIO1~GPIO3 to be high or low. This configuration bit is only effective when the corresponding GPIO is used as a digital output.

e. GPIO3 Function (I²C version only): Can be configured as a GPIO or fault indicator. Valid when GPIO3 is set as an output.

f. GPIOHV1: Sets the GPIOHV1's target level to be high or low. This configuration bit is only effective when GPIOHV1 is used as a digital output and GPIOHV1_HIZ = 0. If "HIZ" is selected, then GPIOHV1 is in Hi-Z mode. In this mode, the MP2797 ignores GPIOHV1_O and the bypass P-FET is turned off. If "HIZ" is not selected, the GPIOHV1 is controlled in output mode following GPIOHV1_O, and the bypass P-FET turns on when the output is low. It is recommended to use GPIOHV1 to control the bypass P-FET.

g. GPIO Pull-Up Voltage: Sets the GPIO pull-up voltage to 3V3 or REGIN.

11. Configure the ADC scan parameters (see Figure 15).

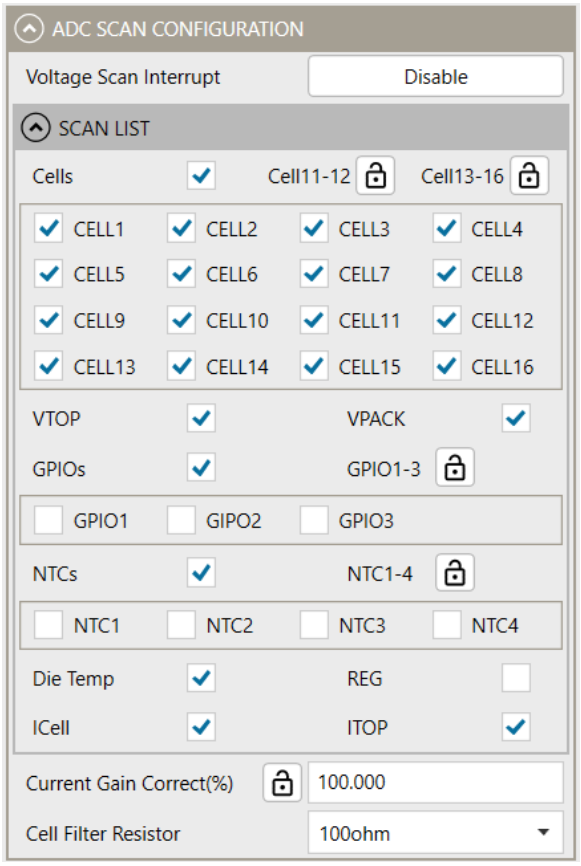


Figure 15: ADC Scan Configuration

a. Select a checkbox to enable the related parameter. If a parameter is enabled, that parameter is read and updated during the high-resolution VADC scan. If disabled, the parameter is excluded from the high-resolution VADC scan.

b. Current Gain Correct (%): Compensates for the sense resistor and SMT variation. The correction is applied to both Coulomb counting and the current ADC readings. The correction is not applied to short-circuit and over-current detection. The configuration range is between 87.5% and 112.476%.

c. Cell Filter Resistor: The default value is 100Ω, and the ADC cell readings are not compensated. This configuration should be set to 1kΩ when a 1kΩ filtering resistor is used (e.g. for external balancing), which compensates for the ADC cell readings to remove the drop caused by the input current during ADC conversion.

12. Configure the watchdog (see Figure 16).

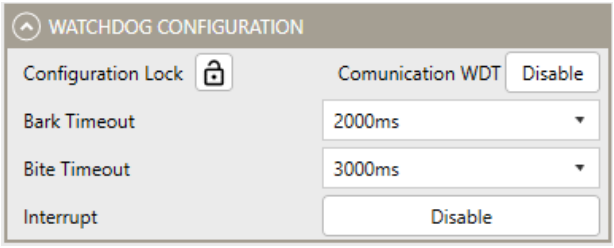


Figure 16: Watchdog Configuration

a. Bark Timeout: Defines the delay from the last watchdog reset to the bark. Ranges between 25ms and 3200ms.

b. Bite Timeout: Defines the delay from the bark to the bite. Ranges between 25ms and 3200ms.

13. Configure the open-wire parameters (see Figure 17).

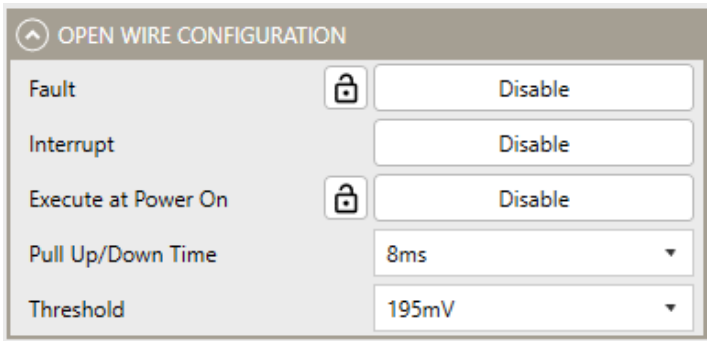


Figure 17: Open-Wire Configuration

a. Execute at Power On: Enables open-wire detection during the power-on sequence (while exiting shutdown mode).

b. Pull-Up/Down Timer: Sets the length of each pull-up and pull-down phase, which ranges between 1ms and 16ms.

c. Threshold: Sets the open-wire threshold used in the detection sequence, which ranges between 39mV and 625mV.

14. Configure the Coulomb counting parameters (see Figure 18).

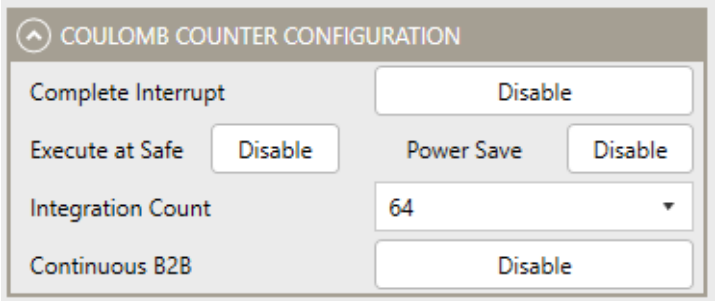


Figure 18: Coulomb Counting Configuration

a. Power Save: If enabled, the Coulomb counter operates in power-save mode; if disabled, power-save mode is not used. Power-save mode reduces overall current consumption but reduces accuracy.

b. Integration Count: Sets the Coulomb counter integration length. The length sets the number of time slots, which are each 32ms. This register should only be updated when Coulomb counting is not active. It ranges from 1 (32ms) to 64 (2048ms).

c. Continuous B2B: Enables back-to-back accumulation mode. When enabled, a new Coulomb counting conversion automatically starts after the most recent conversion is complete.

15. Configure the OC parameters (see Figure 19).

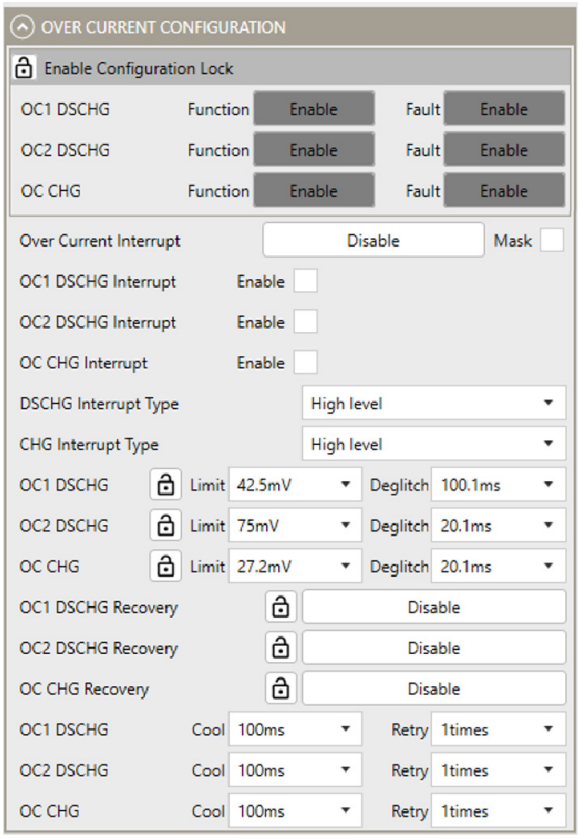


Figure 19: Over-Current Configuration

a. Select the “Over Current Interrupt Mask” checkbox to enable this function. When enabled, the OC interrupt flag is cleared and the interrupt pin goes low unless other interrupts are pending. When disabled, the OC condition can trigger the interrupt flag.

b. OC1 and OC2 DSCHG Limit: The 1x range is 2.5mV to 80mV, while the 3x range is 7.5mV to 240mV.

c. OC1 and OC2 DSCHG Deglitch: The deglitch time ranges between 0.1ms and 2520.1ms. The response time is about 100μs after the OC condition is detected.

d. OC CHG Limit: The 1x range is 1.6mV to 51.2mV, while the 3x range is 4.8mV to 153.6mV.

e. OC CHG Deglitch: The deglitch time ranges between 0.1ms and 2520.1ms. The response time is about 100μs after the OC condition is detected.

f. Recovery: The OC conditions can be enabled for automatic recovery or disabled for manual recovery.

g. Cool: The cool down time can be set to 100ms, 200ms, 500ms, or 1s.

h. Retry: The number of retry attempts can be set to 1 time, 2 times, 3 times, or keep trying.

16. Configure the SC parameters (see Figure 20).

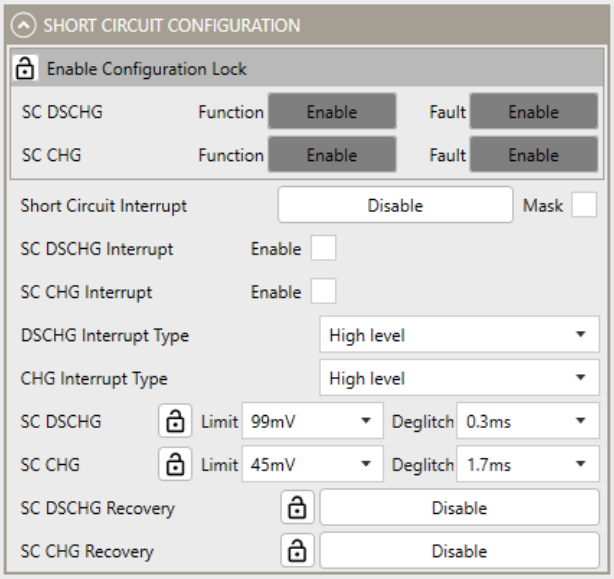


Figure 20: Short Circuit Configuration

a. Select the "Short Circuit Interrupt Mask" checkbox to enable this function. When enabled, the SC interrupt flag is cleared and the interrupt pin goes low unless other interrupts are pending. When disabled, the SC condition can trigger the interrupt flag.

b. SC DSCHG Limit: The 1x range is 5.5mV to 176mV, while the 3x range is 16.5mV to 528mV.

c. SC DSCHG Deglitch: The deglitch time ranges between 0.1ms and 25.5ms. The external filter circuit determines whether the response time is about 100μs after the SC condition is detected.

d. SC CHG Limit: The 1x range is 2.5mV to 80mV, while the 3x range is 7.5mV to 240mV.

e. SC CHG Deglitch: The deglitch time ranges between 0.1ms and 25.5ms. The external filter circuit determines whether the response time is about 100μs after the SC condition is detected.

f. Recovery: The recovery settings can be set to enable automatic recovery or manual recovery.

17. Configure short-circuit removal (see Figure 21).

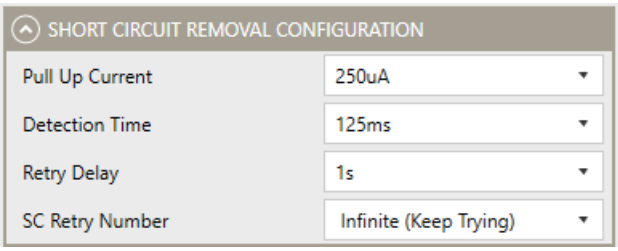


Figure 21: Short-Circuit Removal Configuration

a. Pull-Up Current: The pull-up current during SC removal detection can be set to 250μA, 500μA, or 750μA.

b. Detection Time: The detection time can be set to 125ms, 250ms, 500ms, or 1s.

c. Retry Delay: Sets the delay between SC removal detections to be between 1s and 25s.

d. SC Retry Number: Can be set to 1, 2, 4, or to keep trying.

18. Configure the NTCs (see Figure 22).

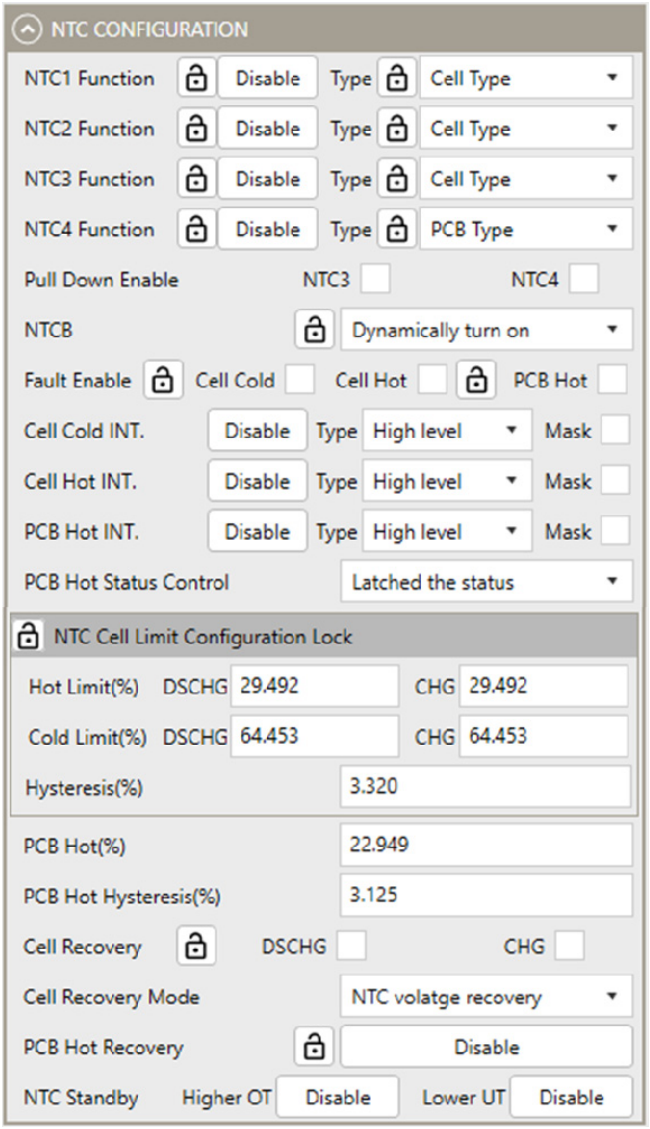


Figure 22: NTC Configuration

a. NTC Type: Can be set to cell monitor or PCB monitor.

b. Pull-Down Enable: Enables NTC3 and NTC4 to be pulled down.

c. NTCB: NTCB is set to dynamically turn on. NTCB is dynamically biased during ADC conversions of the NTC channels; if NTCB is continuously on, current consumption increases.

d. PCB Hot Status Control: Can be set to show the latched status (which goes to the interrupt controller) or show the real-time status.

e. NTC Cell Limit: Can be set to be between 0% and 99.9% of NTCB.

f. Hysteresis (%): The hysteresis threshold can be set to be between 0% and 6.055% of NTCB.

g. Cell Recovery Mode: Defines the recovery logic from NTC hot/cold conditions in charge mode. Set this bit to 0 for NTC voltage recovery. Set it to 1 for NTC voltage recovery or if the charger is removed.

h. Higher OT: Defines the selection criteria for the NTC hot threshold when the battery pack current is within the standby current range. If disabled, select the hotter threshold; if enabled, select the colder threshold.

i. Lower UT: Defines the selection criteria for the NTC cold threshold when the battery pack current is within the standby current threshold. If disabled, select the colder threshold; if enabled, select the hotter threshold.

19. Configure the die temperature parameters (see Figure 23).

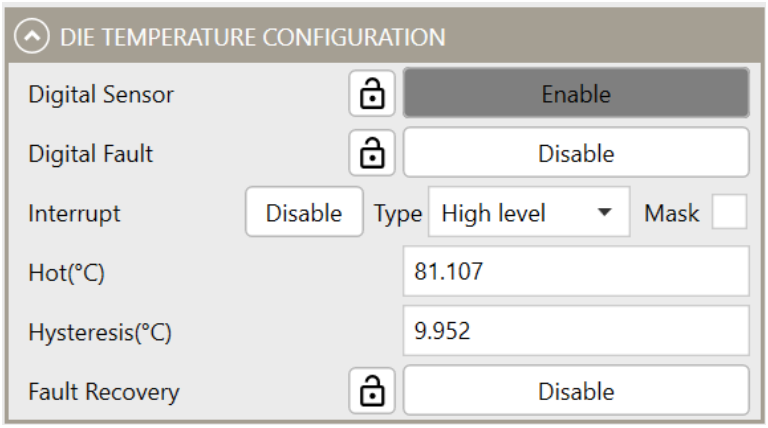


Figure 23: Die Temperature Configuration

a. Hot (°C): The resolution is 0.474°C.

b. Hysteresis (°C): Can be set between 0°C and 14.692°C.

20. Configure the cell-balancing parameters (see Figure 24).

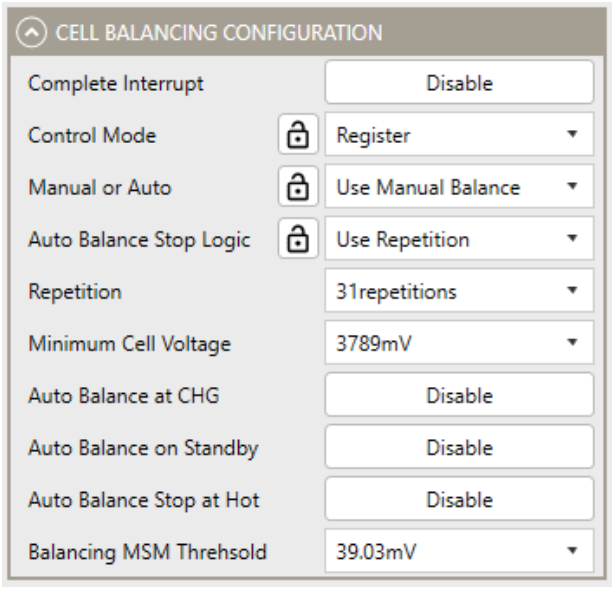


Figure 24: Cell-Balancing Configuration

a. Control Mode: Can be set to register control or GIPO3 control when using automatic balance.

b. Manual or Auto: Controls the balancing mode, which can be configured for manual balancing or automatic balancing.

c. Auto-Balance Stop Logic: Only used when automatic balance is enabled. If set to "Use Repetition," balancing uses repetition to control the number of balance iterations. When set to "Use List," balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, change this bit to disabled.

d. Repetition: Sets the number of repetitions for each execution of the balancing list, ranging between 0 and 31 repetitions. If 31 repetitions are selected, 32 balancing cycles are executed.

e. Minimum Cell Voltage: Sets the qualifying minimum cell voltage to run automatic balancing, ranging between 2500mV and 4961mV. When a cell is below this level, it is excluded from the balancing list. All other qualifying cells are balanced if they meet the criteria.

f. Balancing MSM Threshold: This value is used by the automatic balancing algorithm, and ranges between 19.5mV and 87.85mV.

21. Configure the cell over-voltage (OV) parameters (see Figure 25).

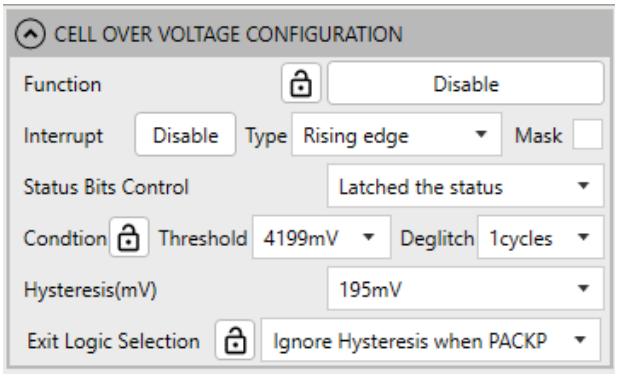


Figure 25: Cell Over-Voltage Configurations

a. Threshold: The cell OV threshold ranges between 0mV and 4980.15mV.

b. Hysteresis (mV): The OV hysteresis ranges between 0mV and 292.5mV.

c. Exit Logic Selection: Can be set to "Lower than Cell OV - Hysteresis" or "Ignore Hysteresis when PACKP < V_{TOP}".

22. Configure the cell under-voltage (UV) parameters (see Figure 26).

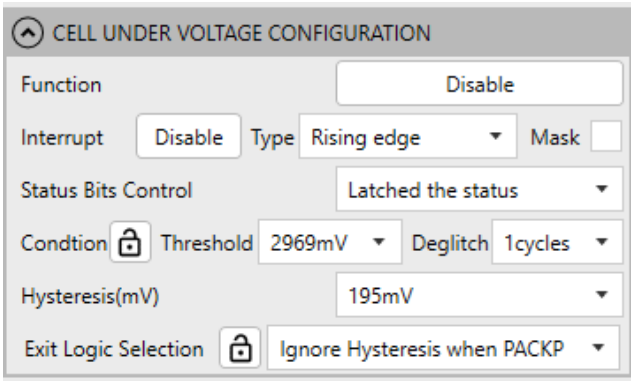


Figure 26: Cell Under-Voltage Configurations

a. Threshold: The cell UV threshold ranges between 0mV and 4980.15mV.

b. Hysteresis (mV): The UV hysteresis ranges between 0mV and 292.5mV.

c. Exit Logic Selection: Can be set to "Higher than Cell UV + Hysteresis" or "Ignore Hysteresis when PACKP > V_{TOP}".

23. Configure the mismatched cell parameters (see Figure 27).

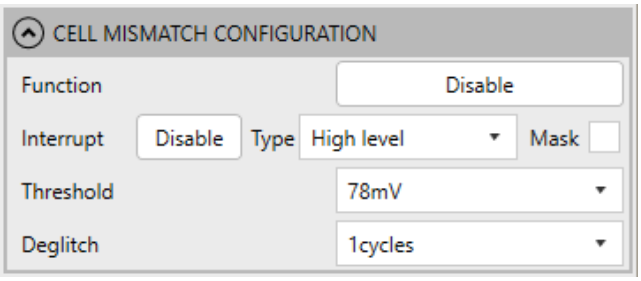


Figure 27: Cell Mismatch Configuration

Threshold: The cell mismatch threshold ranges between 0mV and 1211mV.

24. Set the dead cell parameters (see Figure 28).

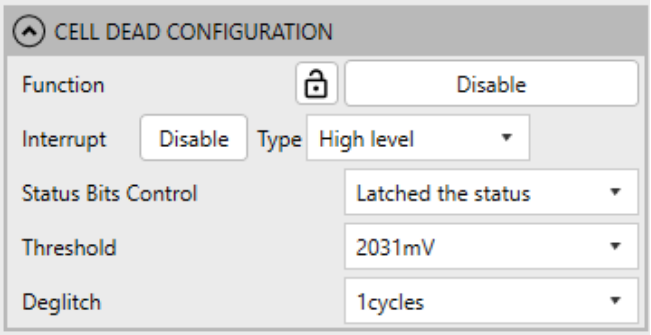


Figure 28: Cell Dead Configuration

Threshold: The cell dead threshold ranges between 0mV and 2480mV.

25. Configure the V_{TOP} UV parameters (see Figure 29).

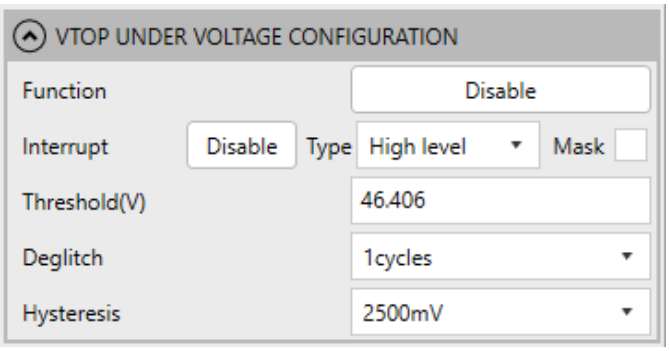


Figure 29: V_{TOP} Under-Voltage Configuration

a. Threshold (V): The V_{TOP} UV threshold ranges between 0V and 79.98V.

b. Hysteresis: Ranges between 0mV and 4922mV.

26. Configure the V_{TOP} UV parameters (see Figure 30).

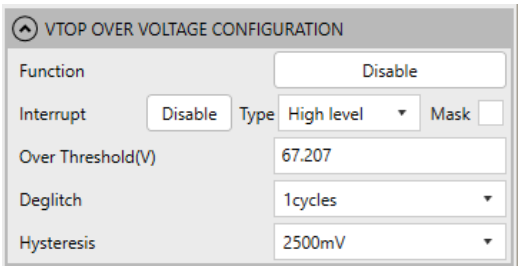


Figure 30: VTOP Over-Voltage Configuration

a. Over-Voltage Threshold (V): The V_{TOP} OV threshold ranges between 0V and 79.98V.

b. Hysteresis: Ranges between 0mV and 4922mV.

27. Configure the REGIN, 3V3, VDD, and ADC self-test checks (see Figure 31).

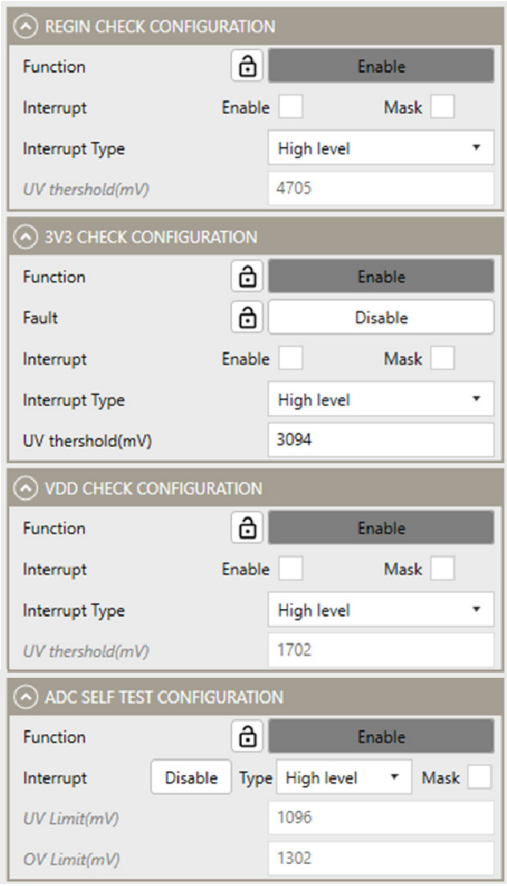


Figure 31: REGIN, 3V3, VDD, ADC Self-Test Check Configuration

28. Configure the one-time programmable (OTP) memory cyclic redundancy check (CRC) (see Figure 32).

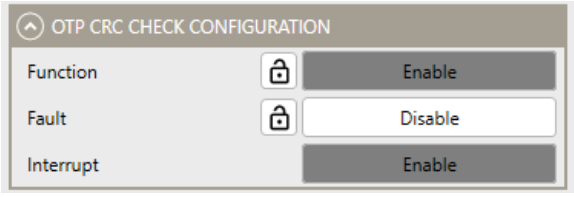


Figure 32: OTP CRC Configuration

Monitor and Control

Click on the Monitor and Control tab to view the device's statuses and faults (see Figure 8 on page 8). The software can automatically update the status, fault, and ADC measurement results by selecting "Auto ADC scan" and "Auto Read".

1. Configure simple mode N-FET control (see Figure 33).

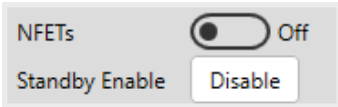


Figure 33: Simple Mode N-FET Control

2. Configure direct mode MOSFET control (see Figure 34). First modify the control mode on the configuration tab, then the options on the control tab change accordingly.

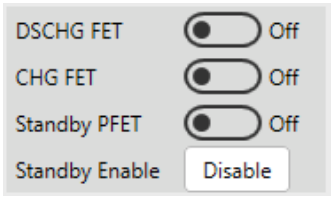


Figure 34: Direct Mode MOSFET Control

3. Check the status monitor (see Figure 35).

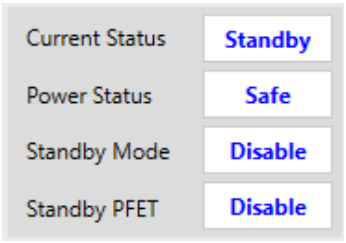


Figure 35: Status Monitor

4. Configure the plug-in detection control and monitoring parameters (see Figure 36).

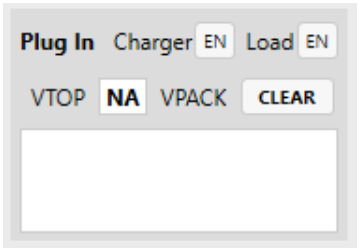


Figure 36: Plug-In Detection Control and Monitor

5. Monitor the watchdog status (see Figure 37).

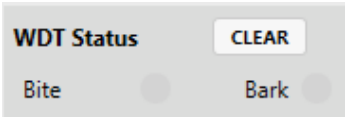


Figure 37: Watchdog Status Monitor

6. Monitor the MOSFET statuses (see Figure 38 on page 23).

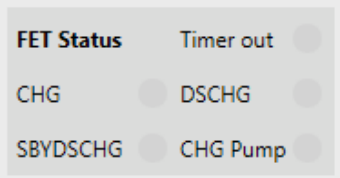


Figure 38: FET Status Monitor

7. Configure the ADC, cell balance, and open-wire control parameters (see Figure 39).

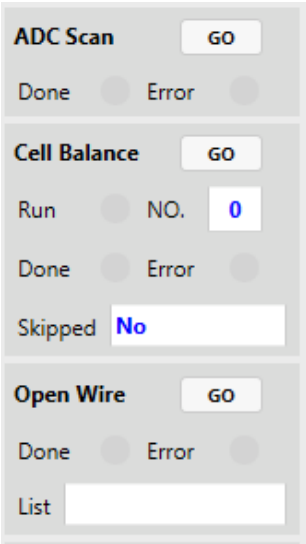


Figure 39: ADC, Cell-Balancing and Open-Wire Control and Monitor

8. Monitor the OC and SC statuses (see Figure 40).

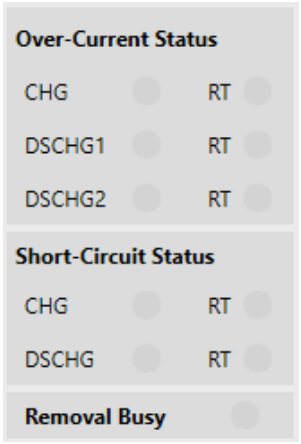


Figure 40: Over-Current and Short-Circuit Status Monitor

9. Monitor the GPIO and V_{TOP} statuses (see Figure 41).

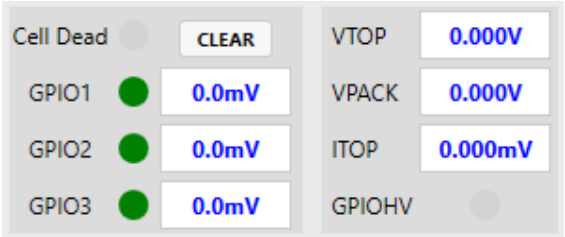


Figure 41: GPIO and VTOP Status Monitor

10. Monitor the die temperature (see Figure 42).

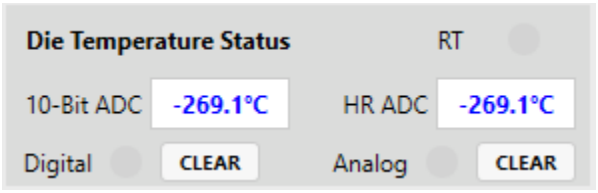


Figure 42: Die Temperature Monitor

11. Monitor the OTP CRC statuses (see Figure 43).

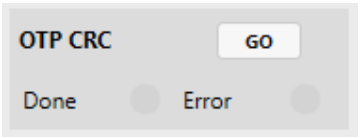
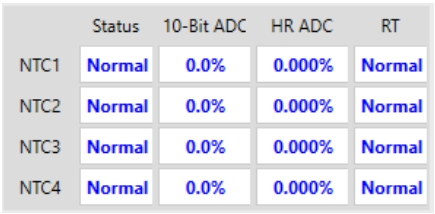


Figure 43: OTP CRC Monitor

12. Monitor the NTC statuses (see Figure 44).



	Status	10-Bit ADC	HR ADC	RT
NTC1	Normal	0.0%	0.000%	Normal
NTC2	Normal	0.0%	0.000%	Normal
NTC3	Normal	0.0%	0.000%	Normal
NTC4	Normal	0.0%	0.000%	Normal

Figure 44: NTC Monitor

Figure 45 shows the NTC functional block.

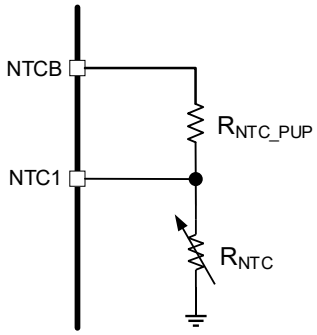


Figure 45: NTC Functional Block

R_{NTC} can be estimated using Equation (1):

$$R_{NTC} = \frac{A \times R_{NTC\_PUP}}{32768 - A} \quad (1)$$

Where *A* is the NTC ADC reading, and R_{NTC_PUP} is the NTC pull-up resistor value (10kΩ is recommended).

The ambient temperature (T, in Kelvin) can be calculated using Equation (2)

$$T = \frac{1}{\frac{1}{T_0} + \frac{1}{B} \ln \frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is the NTC resistor value when the ambient temperature is T_0 (in Kelvin), and B is the thermistor constant (in Kelvin).

For example, if the NTC ADC reading (*A*) is 9830 (0x2666) for the thermistor NCP18XH103, R_0 is 10kΩ at 25°C (298.15K), and B is 3380K, then R_{NTC} = 4.285kΩ and T = 322K. This means that if the NTC ADC reading is 9830, then the ambient temperature is about 49°C.

13. Monitor the low-dropout (LDO) regulator (see Figure 46).

	Status	10-Bit ADC	HR ADC
VDD	Normal	0.0mV	0.0mV
3V3	Normal	0.0mV	0.0mV
REGIN	Normal	0.0mV	0.0mV
Self	Normal	0.0mV	

Figure 46: LDO Monitor

14. Monitor the cells' ADC statuses (see Figure 47). To do so, click on the ADC scan "Go" button (see Figure 8 on page 8). The ADC result should be updated to the corresponding register.

	Voltage	Current	UV	OV	MS	Dead	BAL
Cell1	0.0mV	0.000mV					
Cell2	0.0mV	0.000mV					
Cell3	0.0mV	0.000mV					
Cell4	0.0mV	0.000mV					
Cell5	0.0mV	0.000mV					
Cell6	0.0mV	0.000mV					
Cell7	0.0mV	0.000mV					
Cell8	0.0mV	0.000mV					
Cell9	0.0mV	0.000mV					
Cell10	0.0mV	0.000mV					
Cell11	0.0mV	0.000mV					
Cell12	0.0mV	0.000mV					
Cell13	0.0mV	0.000mV					
Cell14	0.0mV	0.000mV					
Cell15	0.0mV	0.000mV					
Cell16	0.0mV	0.000mV					

Figure 47: Cell ADC Monitor

EVALUATION BOARD SCHEMATICS

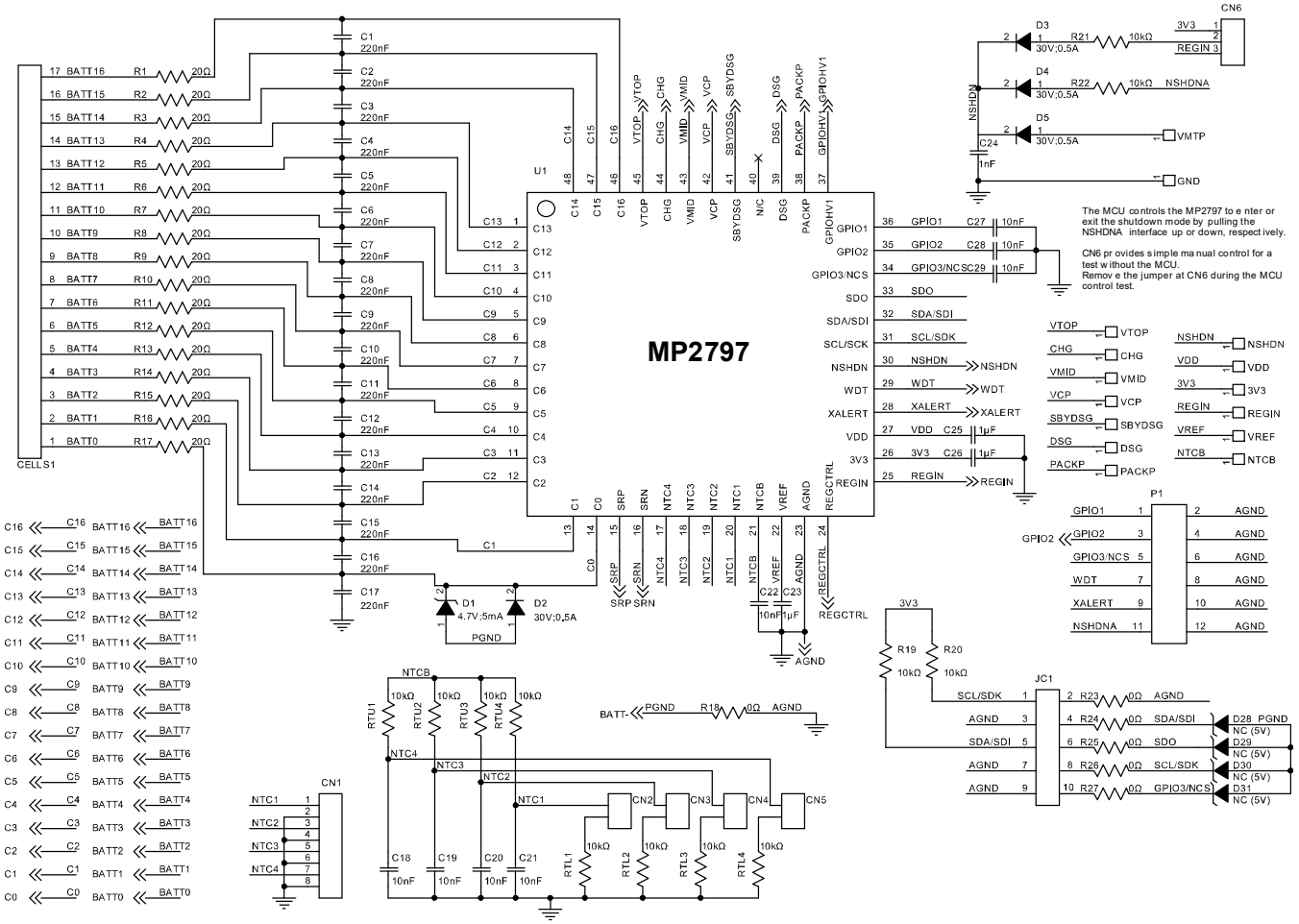


Figure 48: Evaluation Board Schematic (IC and Connector)

EVALUATION BOARD SCHEMATICS *(continued)*

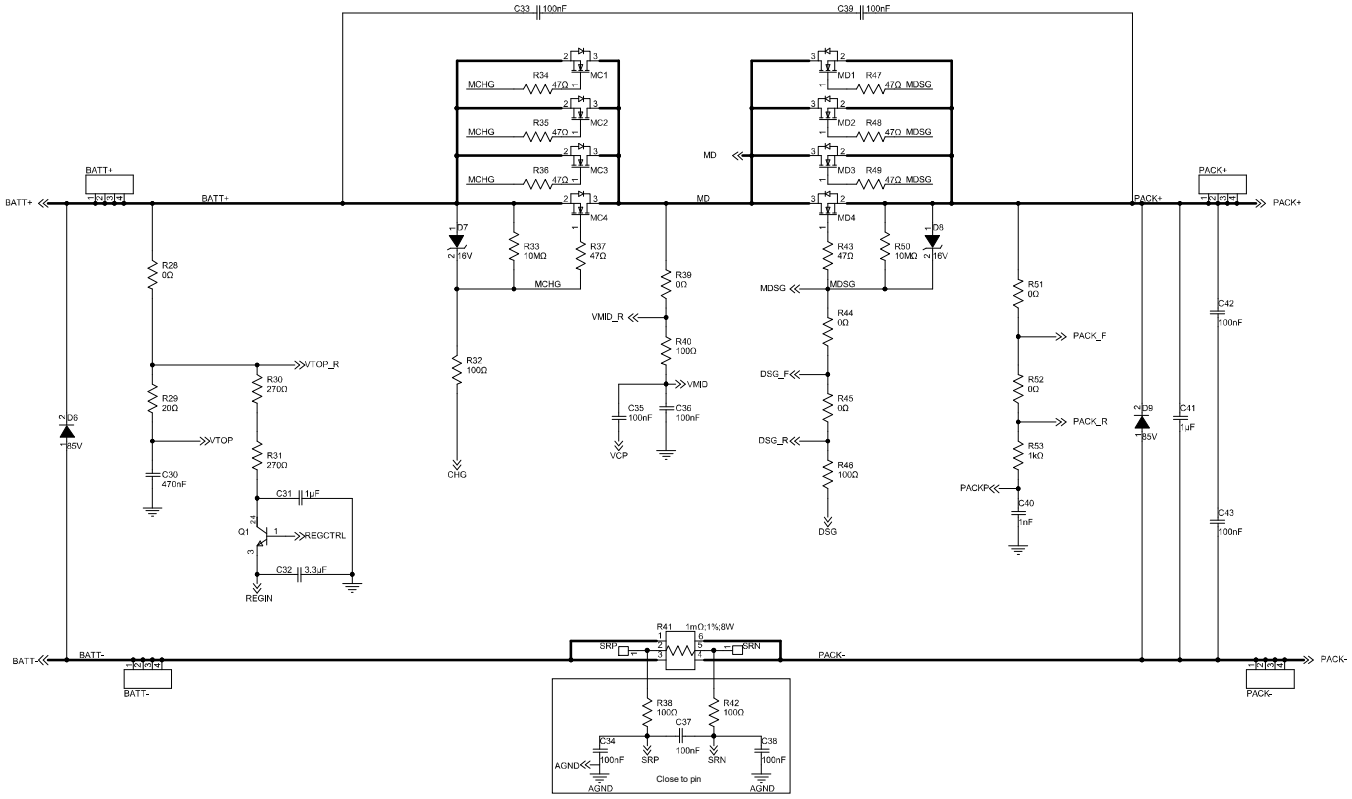


Figure 49: Evaluation Board Schematic (Power Path)

EVALUATION BOARD SCHEMATICS *(continued)*

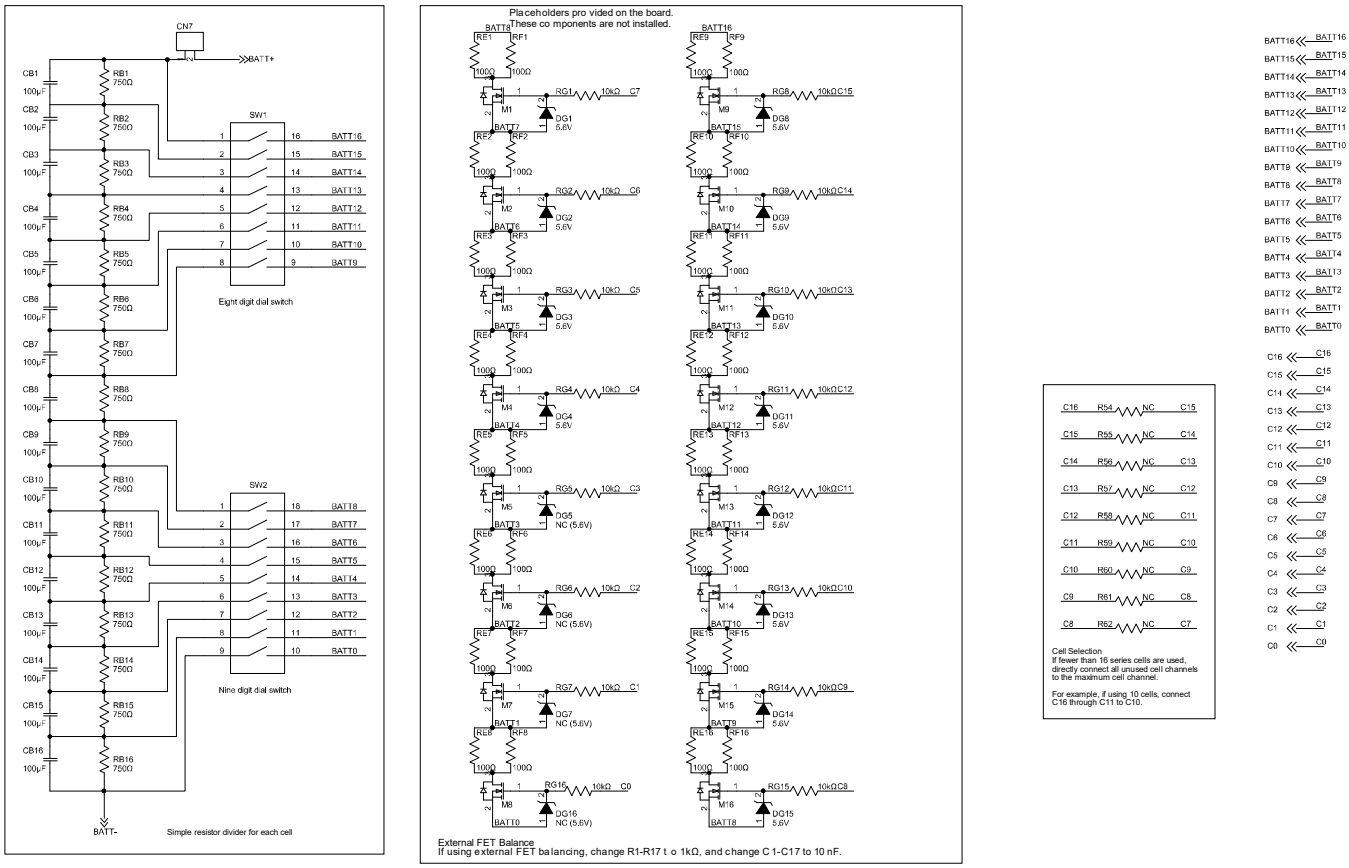


Figure 50: Evaluation Board Schematic (Battery Connection)

EVALUATION BOARD SCHEMATICS *(continued)*

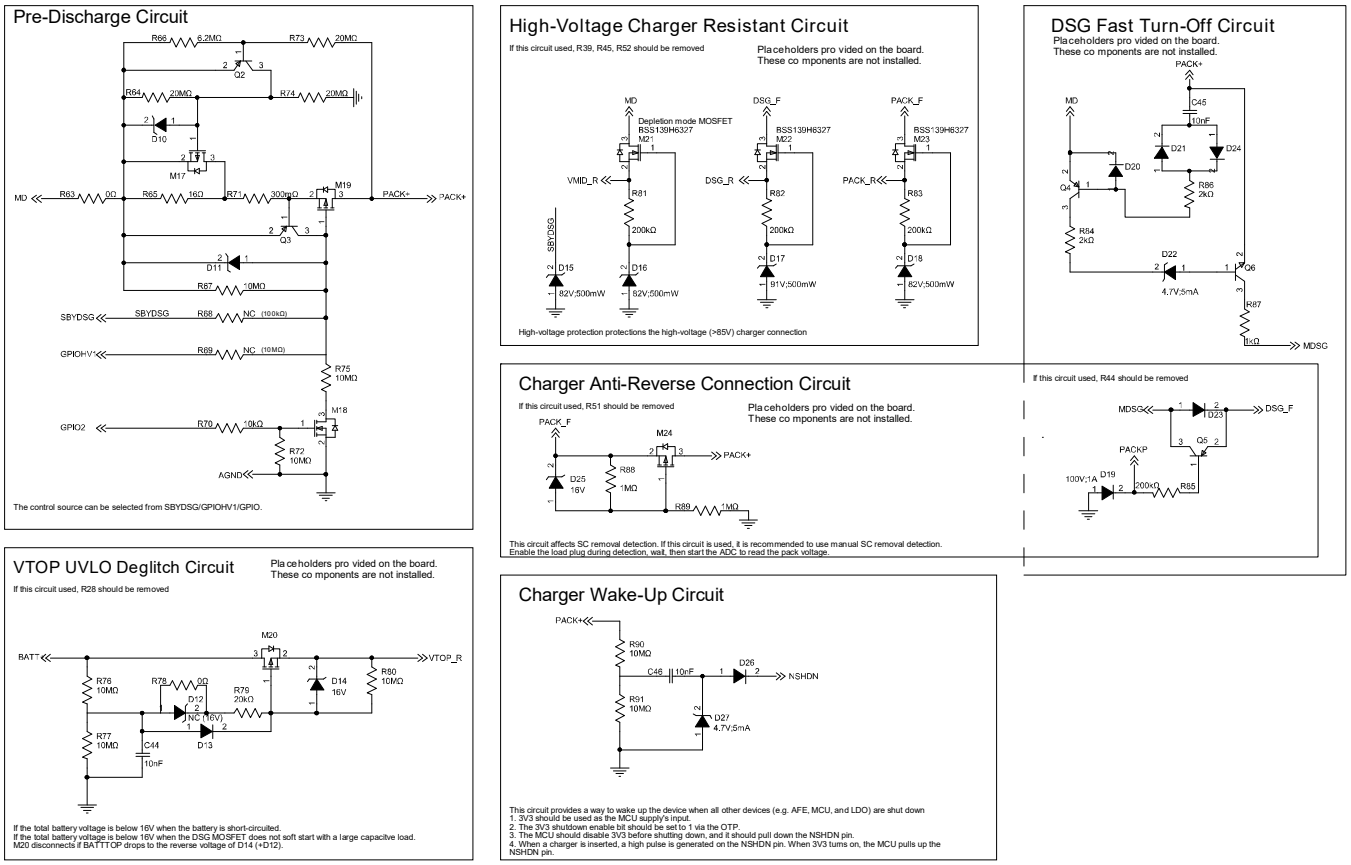


Figure 51: Evaluation Board Schematic (Additional Circuit)

EV2797-0000-FP-00B BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK-, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	zhengyou	PCB_50
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107 ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2 ,CN3, CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Wurth	60900213421
1	CN6	2.54mm	3-pin connector	DIP	Wurth	60900213421
1	CELLS1	3.5mm	17-pin connector	DIP	KEFA	KF2EDGR-3.5-17P
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224 KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102 KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474 KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A10 5KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C33 5KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103 KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	85V	TVS diode, 10.4A	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
4	D7, D8, D10, D11	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2 x 6-pin connector	DIP	Any	

EV2797-0000-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC, 120A	TO-263	CR Micro	CRSS042N10N
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-channel MOSFET, 6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D
1	Q1	100V	Transistor, NPN, 6A,3W	SOT-223	Zetex	FZT853TA
2	Q2, Q3	-20V	Transistor, PNP, 1.5A	SOT-23	JCET	SS8550LT1
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, B8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32, R40, R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor,1%	0603	Yageo	RC0603FR-0710KL
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
8	R18, R28, R39, R44, R45, R51, R52, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	0603	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Current-sense resistor, 1%	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64, R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML

EV2797-0000-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R65	16Ω	Film resistor ,1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L
1	SW1	8-pin switch	Button	SMD	Any	
1	SW2	9-pin switch	Button	SMD	Any	
1	U1	MP2797DFP-0000	7-cell to 16-cell, high-accuracy battery monitoring and protection IC	TQFP-48 (7mmx 7mm)	MPS	MP2797DFP-0000

EV2797-0002-FP-00B BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK-, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	zhengyou	PCB_50
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, B12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3, CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Wurth	60900213421
1	CN6	2.54mm	3-pin connector	DIP	Wurth	60900213421
1	CELLS1	3.5mm	17-pin connector	DIP	KEFA	KF2EDGR-3.5-17P
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	85V	TVS diode, 10.4A	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
4	D7, D8, D10, D11	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2 x 6-pin connector	DIP	Any	

EV2797-0002-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC, 120A	TO-263	CR Micro	CRSS042N10N
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-channel MOSFET, 6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-223	Zetex	FZT853TA
2	Q2, Q3	-20V	Transistor, PNP, 1.5A	SOT-23	JCET	SS8550LT1
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32, R40, R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor,1%	0603	Yageo	RC0603FR-0710KL
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
13	R18, R23, R24, R25, R26, R27, R28, R39, R44, R45, R51, R52, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	0603	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Current-sense resistor, 1%	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64, R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML

EV2797-0002-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R65	16Ω	Film resistor,1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor,1%	0603	Yageo	RC0603FR-076M2L
1	R71	300mΩ	Film resistor,1%	2512	Yageo	RL2512FK-070R3L
1	SW1	8-pin switch	Button	SMD	Any	418121270808
1	SW2	9-pin switch	Button	SMD	Any	418121270809
1	U1	MP2797DFP-0002	7-cell to 16-cell, high-accuracy battery monitoring and protection IC	TQFP-48 (7mmx 7mm)	MPS	MP2797DFP-0002

EV2797-0000/0002-FP-00B BILL OF MATERIALS

Recommended components for the external FET balance circuit (components not installed on standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
16	M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16	50V	N-channel MOSFET, 3.5mΩ, 0.2A	SOT-23	LRC	LBSS138LT1G
32	RF1, RE1, RF2, RE2, RF3, RE3, RF4, RE4, RF5, RE5, RF6, RE6, RF7, RE7, RF8, RE8, RF9, RE9, RF10, RE10, RF11, RE11, RF12, RE12, RF13, RE13, RF14, RE14, RF15, RE15, RF16, RE16	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
15	RG1, RG2, RG3, RG4, RG5, RG6, RG7, RG8, RG9, RG10, RG11, RG12, RG13, RG14, RG15	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
15	DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG8, DG9, DG10, DG11, DG12, DG13, DG14, DG15	5.6V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C5V6S-7-F

EV2797-0000/0002-FP-00B BILL OF MATERIALS

Recommended components for the V_{TOP} UVLO deglitch circuit (components not installed on standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	M20	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	D12, D14	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D13	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
3	R76, R77, R80	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
1	R78	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R79	20kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720KL
1	C44	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03

EV2797-0000/0002-FP-00B BILL OF MATERIALS

Recommended components for the DSG fast turn off and anti-reverse connection circuit (components not installed on standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C45	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
4	D20, D21, D23, D24	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	D25	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D19	100V	Schottky diode, 1A	SOD-123-2	ST	BAT41ZFILM
1	D22	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D28, D29, D30, D31	5V	ESD diode, 5V	SOD-323	NXP	PESD5V0V1BA
1	M24	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	Q4, Q5	-80V	Transistor, 0.5A, PNP	SOT-23	Diodes, Inc.	MMBTA56LT1G
1	Q6	80V	Transistor, 0.5A, NPN	SOT-23	onsemi	MMBTA06
1	R85	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
1	R87	47Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R84, R86	2kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-072KL
2	R88, R89	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML

EV2797-0000/0002-FP-00B BILL OF MATERIALS

Recommended components for the high-voltage charger circuit (components not installed on standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	D15, D16, D18	82V	Zener diode, 1.5mA	SOD-123-2	onsemi	MMSZ5268BT1G
1	D17	91V	Zener diode, 1.4mA	SOD-123-2	onsemi	MMSZ5270BT1G
3	R81, R82, R83	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
3	M21, M22, M23	250V	N-channel, 7.8mΩ, 2.3nc, 30mA	SOT-23	Infineon	BSS139H6327

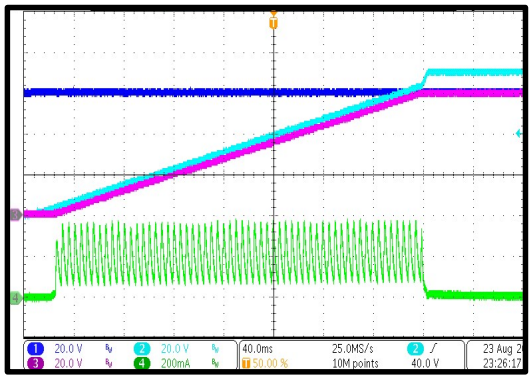
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

DSG Soft Start

PACK+ is connected to a 1mF capacitor, the DSG slope is 0.2V/ms

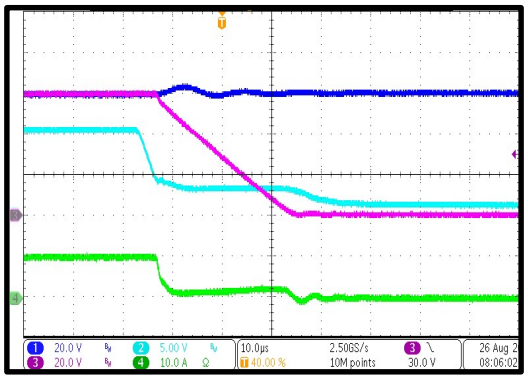
CH1: V_{MID}
CH2: V_{DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



DSG Off

CR load = 6Ω

CH1: V_{MID}
CH2: V_{GS_DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



PCB LAYOUT (MP2797-0000-FP-00B)

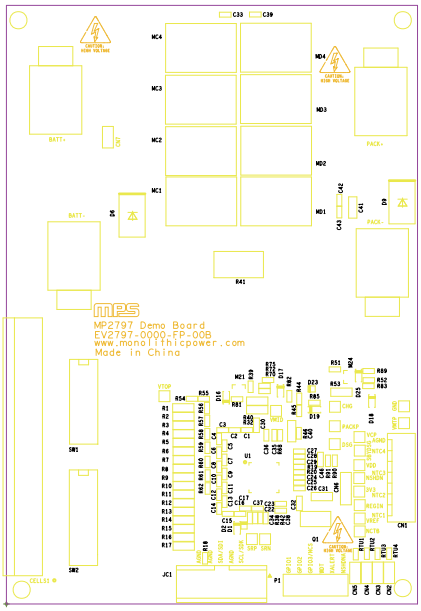


Figure 52: Top Silk

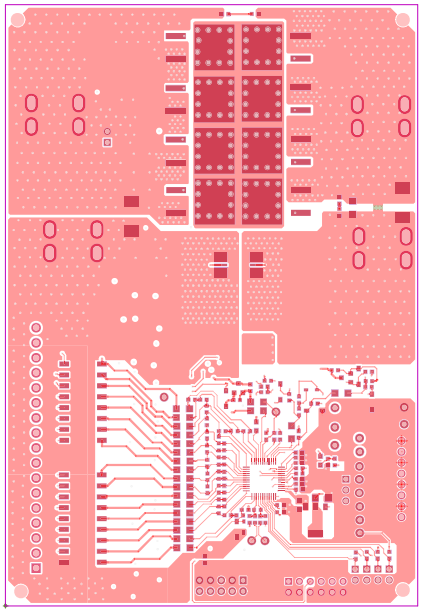


Figure 53: Top Layer

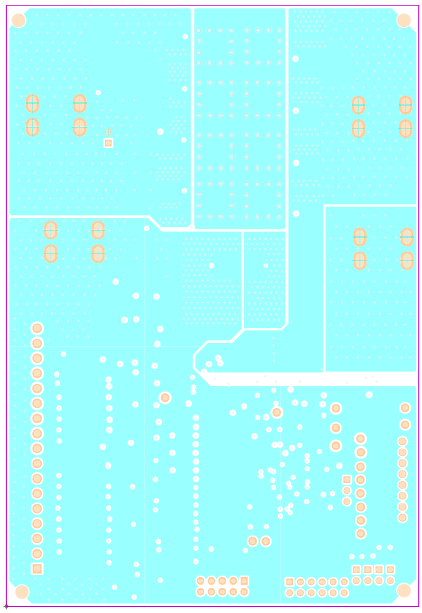


Figure 54: Mid-Layer 1

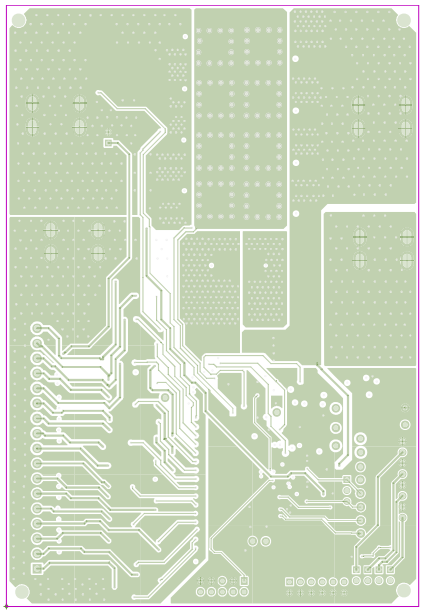


Figure 55: Mid-Layer 2

PCB LAYOUT (MP2797-0000-FP-00B) *(continued)*

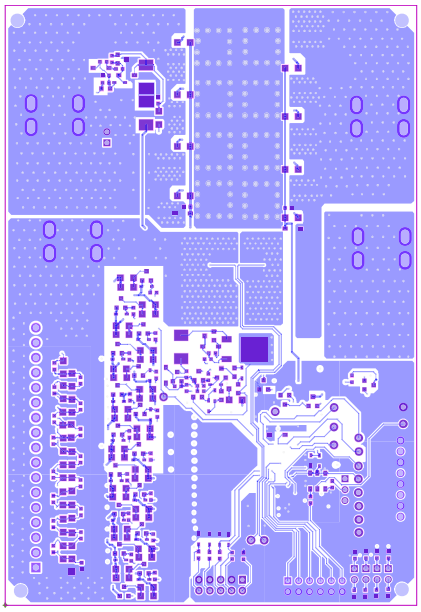


Figure 56: Bottom Layer

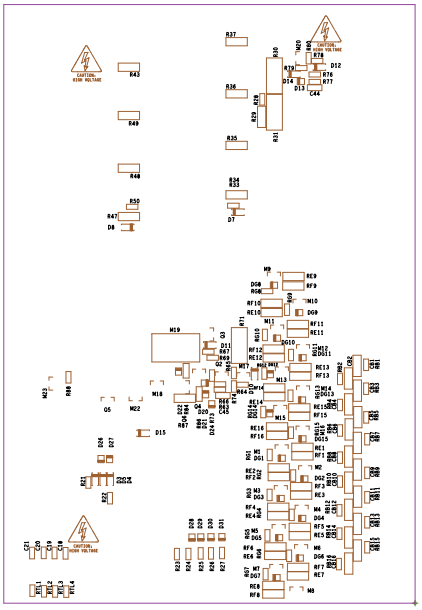


Figure 57: Bottom Silk

PCB LAYOUT (MP2797-0002-FP-00B)

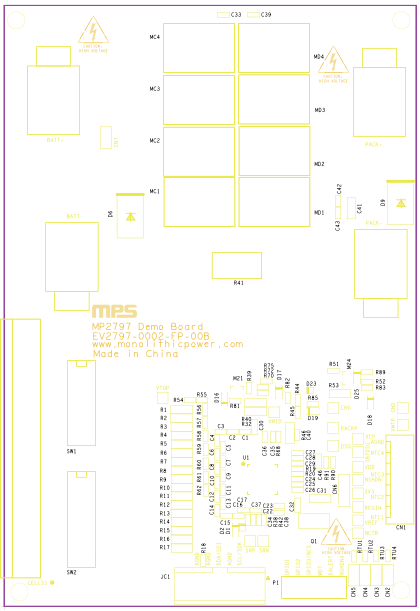


Figure 58: Top Silk

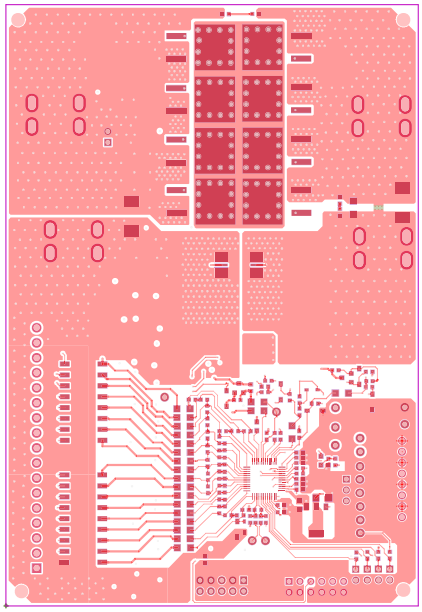


Figure 59: Top Layer

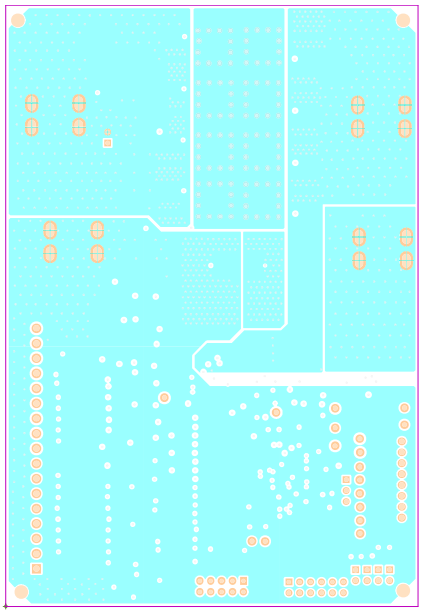


Figure 60: Mid-Layer 1

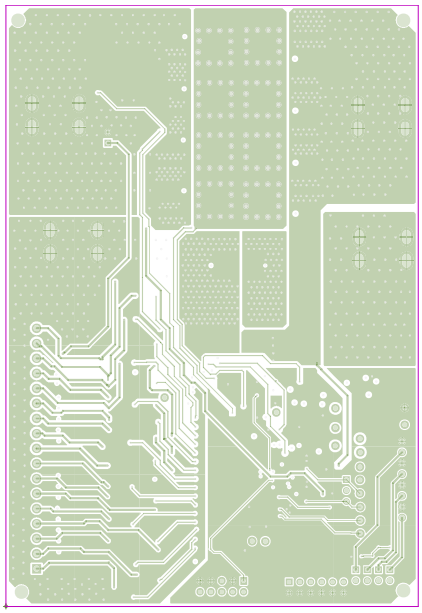


Figure 61: Mid-Layer 2

PCB LAYOUT (MP2797-0002-FP-00B) *(continued)*

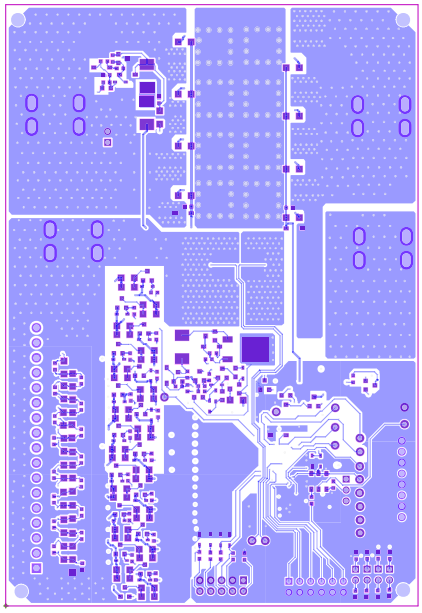


Figure 62: Bottom Layer

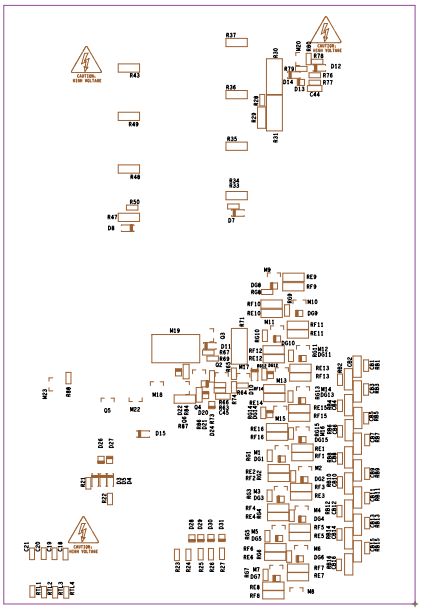


Figure 63: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/18/2023	Initial Release	-