EV2791-0000-FP-00A

7-Cell to 14-Cell, High-Accuracy, Battery Monitor and Protection IC with I²C and Coulomb Counting Evaluation Board

DESCRIPTION

The EV2791-0000-FP-00A is an evaluation board designed to demonstrate the capabilities of the MP2791, a robust battery management device. The MP2791 provides a complete solution that can monitor the analog front-end and provide protections. It is designed for battery systems with multiple cells in series. The MP2791DFP-0000 supports I²C communication.

The device supports connections for 7-cell to 14-cell series battery packs, with absolute voltages exceeding 75V on some pins.

The MP2791 integrates two separate analog-to-digital converters (ADCs). The first ADC measures each channel's differential cell voltage (up to 14 channels), die temperature, and 4-channel battery temperature via an external NTC thermistor. The second ADC measures the charge and discharge currents via an external sense resistor.

The MP2791 provides high-side MOSFET (HS-FET) drivers and many robust protections. Full protection features include over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high/low temperature protection. All of the protections have configurable thresholds.

The EV2791-0000-FP-00A includes external balancing FETs that equalize mismatched cells. The MP2791 also has integrated balancing FETs for internal cell balancing.

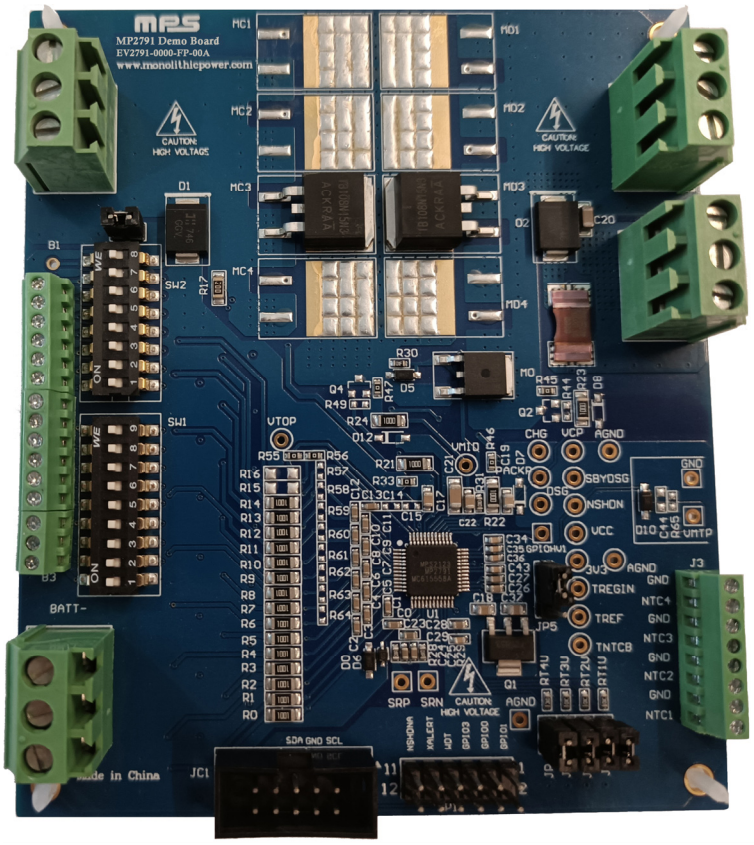
The MP2791 has an optimized baseline current consumption that depends on the operating mode. It is available in a TQFP-48 (7mmx7mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage (V_{BATT})		18V to 65.8V
Cell voltage	V_{BATT} = 18V to 65.8V	1V to 5V
Continuous charge current (I_{CHARGE})	V_{BATT} = 18V to 65.8V	0A to 60A
Continuous discharge current ($I_{DISCHARGE}$)	V_{BATT} = 18V to 65.8V	0A to 60A
Supported number of cells in series	V_{BATT} = 18V to 65.8V	7 to 14

EVALUATION BOARD



LxWxH (9.6cmx11.3cmx2.1cm)

Board Number	MPS IC Number
EV2791-0000-FP-00A	MP2791DFP-0000 (1)

Note:

1) "-0000" is the default configuration code. For other configuration options, contact an MPS FAE to obtain a custom "-xxxx" value.

QUICK START GUIDE

The EV2791-0000-FP-00A is designed to evaluate the MP2791, a robust battery management device. The MP2791 can monitor the analog front-end and provide protections. The evaluation board includes the MP2791, power MOSFETs, a current-sense resistor, a bipolar junction transistor (BJT), external balance resistors, balancing MOSFETs, and other components. The MP2791 protects the battery from the following conditions: over-current (OC), short-circuit (SC), under-voltage (UV), over-voltage (OV), unbalanced cell, and high/low temperature conditions.

This board can be set to support 7-cell to 14-cell series connections, synchronous voltage and current measurements, and robust hardware protections with configurable thresholds. The external balancing MOSFETs allow the device to support a higher balancing current.

Evaluation Board Set-Up

The following materials are required to use the evaluation board: a computer with at least one USB port, a USB cable, and a USB to I²C communication device (EVKT-USBI2C-02) (see Figure 1).

Figure 1: USB to I²C Communication Kit (EVKT-USBI2C-02)

1. Install the MP2791 GUI (2). To check that the software is installed properly, open the GUI by clicking on the “MP2791.exe” file.
2. Connect the I²C communication interface to the computer using the USB cable

Follow the steps below to set up the evaluation board without a battery pack (using a cell simulator shunt):

1. Short jumper JP0, then turn the SW1 and SW2 channels on.
2. Preset the DC power supply to 48V/1A.
3. Connect a DC power supply between BATT+ and BATT-.
4. Connect the USB to I²C communication interface to JC1. Ensure that the SCL and SDA positions are correct to avoid improper connection.
5. The evaluation board has 14 cells in series by default. To evaluate the device with a lower number of cells in series, short the channel from C14 to the practical maximum cell.

   Figure 2 shows 10 cells connected in series with a cell simulator shunt.

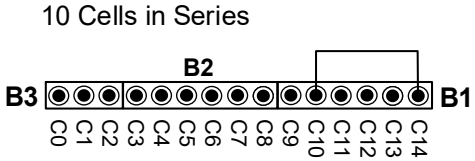


Figure 2: 10 Cells Connected in Series

6. Decrease the voltage between BATT+ and BATT- according to the number of cells in series.

Note:

2) The GUI can be downloaded from the MPS website.

Figure 3 shows the equipment set-up without a battery pack.

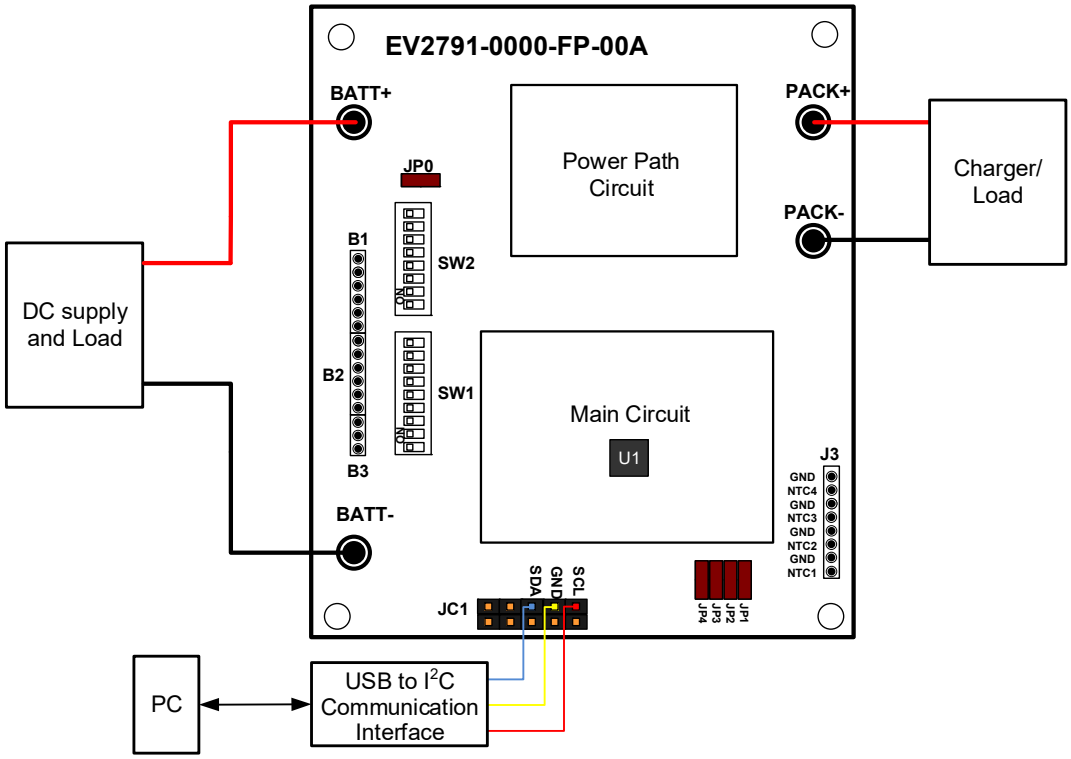


Figure 3: Equipment Set-Up without a Battery Pack

The open-wire and cell-balancing functions cannot be tested using a cell simulator shunt. A battery pack is required to evaluate these functions. Follow the steps below to set up the evaluation board with a battery pack:

1. Remove JP0, then turn the SW1 and SW2 channels off.
2. If the application has less than 14 cells in series, use 0Ω resistors to short all unused cell channels (Cx) to the practical maximum cell channel. For example, if only 10 cells are connected, then short C10, C11, C12, C13, and C14 by adding 0Ω resistors to R60, R59, R58, and R57. If the application has all 14 cells connected, then skip this step.
3. Connect the battery cell terminals (B1, B2, and B3) to each cell-sensing point. If there are less than 14 cells in the battery pack, float the high channels of the battery cell termainal.
4. Remove JP1, JP2, JP3, and JP4.
5. Connect the temperature sensors to support up to four NTCs.
6. Connect the battery terminals to:
    a. Positive (+): BATT+
    b. Negative (-): BATT-
7. Connect the charger/load terminals to:
    a. Positive (+): PACK+
    b. Negative (-): PACK-
8. Connect SDA, SCL, and GND to the USB to I²C communication interface. Ensure that the SCL and SDA position are correct to avoid improper connection.

Figure 4 shows the equipment set-up with a battery pack.

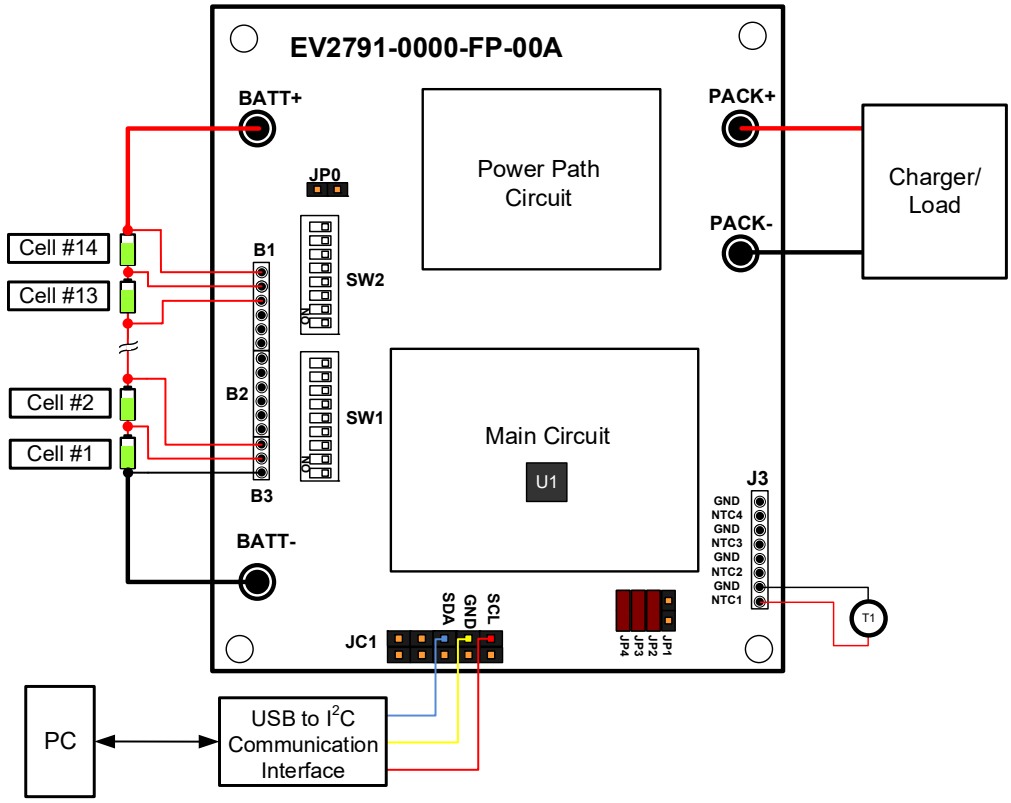


Figure 4: Equipment Set-Up with a Battery Pack

9. Open the GUI software. If the evaluation board is connected properly, then the bottom left corner of the GUI should read: “MP2791 Demo board: Connected”. If the evaluation board is not connected properly, then the bottom left corner of the GUI should read: “MP2791 Demo board: Disconnected”.
10. The evaluation board has a bypass P-channel MOSFET. In safe mode, the P-channel MOSFET is turned on via GPIO1HV to provide a small current to the load connected between PACK+ and PACK-. This consumes less power than if the N-channel MOSFET is turned on in active mode. If the PACK voltage (V_{PACK}) drops below the VTOP voltage (V_{TOP}) - 2V, then the MOSFET current capacity is about 25mA. If V_{PACK} exceeds V_{TOP} - 2V, then the MOSFET can bypass about 1A of current. Set the GPIO1HV output to a high-impedance (Hi-Z) state if the bypass function is not used.

Figure 5 shows the MP2791 evaluation GUI.

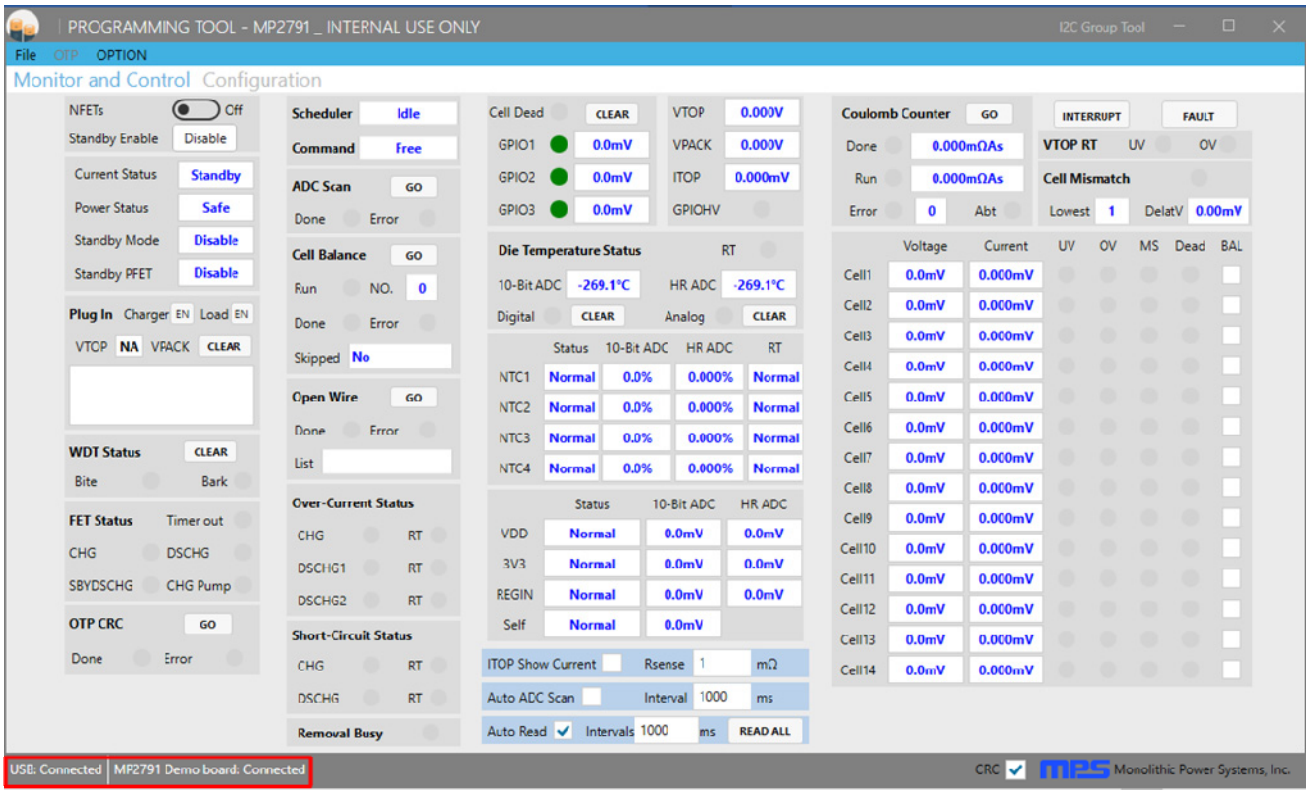


Figure 5: MP2791 Evaluation GUI

PROCEDURE

General GUI operation

Once the evaluation board is connected properly, follow the guidelines below to configure the MP2791:

1. Click on the Configuration tab in the GUI to view the device configurations (see Figure 6). The software will automatically read the device configurations when the tab is switched from Monitor and Control to Configuration. Note that the items with a lock symbol to the right can be configured as read-only.

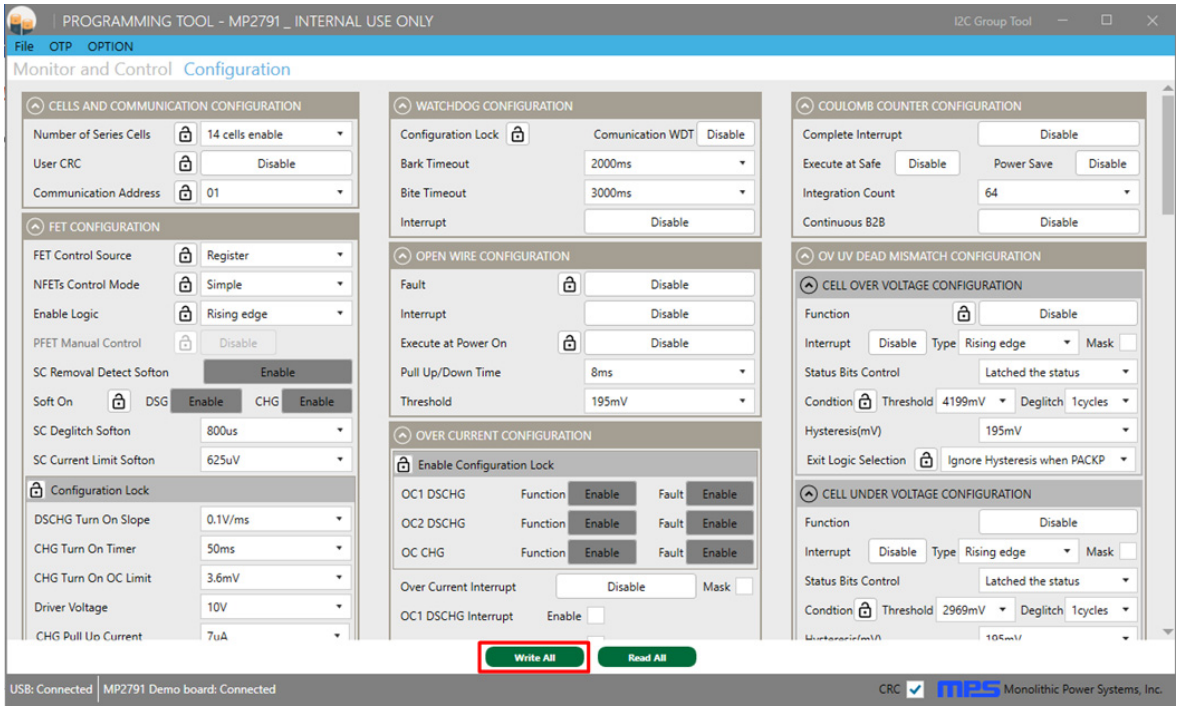


Figure 6: MP2791 Configurations

2. Configure the protection thresholds, enable the relevant functions, and set the corresponding faults and interruptions.
3. Click on the “Write All” button to write the configurations into the register. Click the “Monitor and Control” tab to switch to the “Monitor and Control” view.
4. Turn the N-channel MOSFETs on.
5. Click the “Read All” button. The power status should be set to “Active”. The “CHG”, “DSG”, and “CHG Pump” MOSFET statuses should be displayed in green.
6. Click on the “Go” button on the right side of the “ADC Scan” section to scan the ADC. The result should update to the corresponding register.
7. Click the “Read All” button again. The updated values should be displayed in the GUI. If the box labeled “Auto Read” is selected, then it is not required to click the “Read All” button after step 6.

Configuration Introduction

Some specific configuration options are described below.

1. Figure 7 shows the Cells and Communication Configuration settings in the GUI.

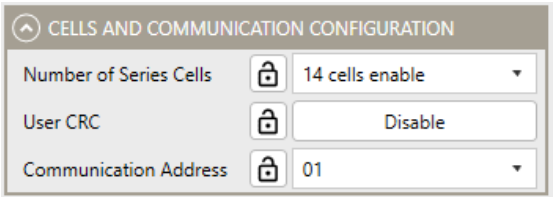


Figure 7: Cells and Communication Configuration

a. Number of Series Cells: Set the number of cells in series between 7 and 14.

b. User CRC: If the CRC is enabled, select the CRC box at the bottom right of the GUI, if the CRC box is not selected, the value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address is between 00h and 7Fh (3). The GUI scans the address automatically. This function can be disabled by deselecting “Monitor Chip Connection” in the Option tab in the top toolbar. After configuring the communication address, the new address should be used for the next communication.

Note:

3) The default address may differ for devices with custom “-xxxx” configuration codes.

2. Figure 8 shows the FET Configuration settings in the GUI.

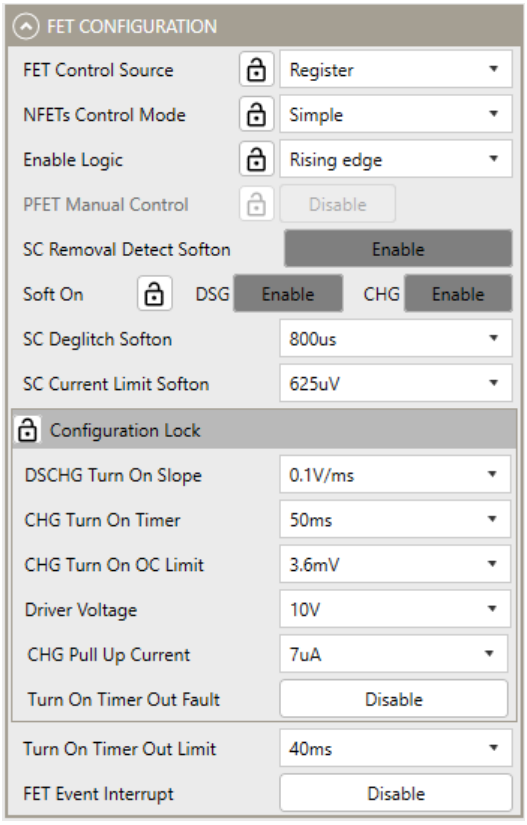


Figure 8: FET Configuration

a. FET Control Source: Set the MOSFET control source to either GIPO control or register control.

b. NFETs Control Mode: Set the N-channel MOSFET control mode to either simple mode or direct mode. In direct mode with GPIO control, GPIO1 controls the discharge MOSFET, and GPIO2 controls the charge MOSFET.

Figure 9 shows the simple mode with register control configuration.

Figure 9: Simple Mode MOSFET Register Control

Figure 10 shows the direct mode with register control configuration.

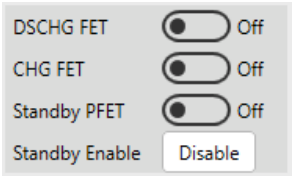


Figure 10: Direct Mode MOSFET Register Control

c. Enable Logic: Set the enable logic to either “rising edge” active or “level” active.

d. SC Removal Detect Softon: Configure the “SC Removal Detect Soft On” parameter. If SC Removal Detect Soft On is enabled, the SC detection sequence that occurs before the discharge MOSFET turns on is enabled.

e. SC Deglitch Softon and SC Current Limit Softon: Configure the “SC Deglitch Soft On” and “SC Current Limit Soft On” parameter. If “Soft On DSG” is enabled, then the discharge MOSFET is protected from inrush current while a large capacitive load is being charged. These two parameters protect the discharge MOSFET while it ramps up during the discharge N-channel MOSFET’s soft turn-on.

f. DSCHG Turn On Slope: Set the discharge start-up slope between 0.1V/ms and 1.6V/ms.

g. CHG Turn On OC Limit: Set the over-current protection (OCP) threshold during soft start to either 3.6mV or 4.8mV.

h. Driver Voltage: Set the gate to source voltage (V_{GS}) for the charge and discharge MOSFETs between 7V and 12V.

i. CHG Pull Up Current: Set CHG pin’s pull up current during the charge MOSFET’s soft-start period between 3μA and 10μA. This controls the rising slope of the charge MOSFET’s driver voltage.

3. Figure 11 shows the Power Status Configuration settings in the GUI.

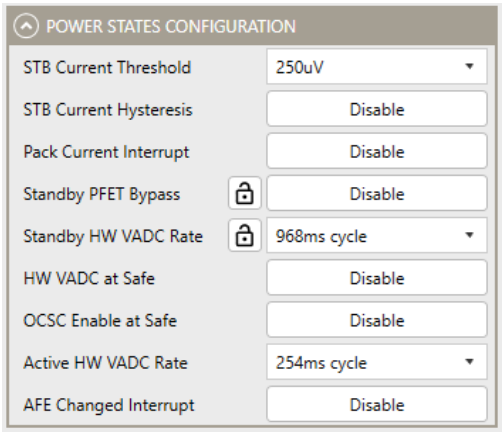


Figure 11: Power Status Configuration

a. HW VADC at Safe: If voltage ADC protection monitoring is required in safe mode, enable the HW VADC at Safe function to ensure that the hardware voltage ADC monitoring can be activated for protections.

b. Standby HW VADC Rate: The standby hardware voltage ADC monitoring rate can be used with voltage monitoring protection refresh period while the device is in safe or standby mode. Configure the standby voltage ADC rate to refresh the voltage protection reading every 254ms, 492ms, or 968ms.

c. Active HW VADC Rate: The active hardware voltage ADC monitoring rate can be used with voltage monitoring protection refresh period while in active mode. Configure the active voltage ADC rate to refresh the voltage protection reading every 254ms or 135ms.

4. Figure 12 shows the Plug-In Detection Configuration settings in the GUI.

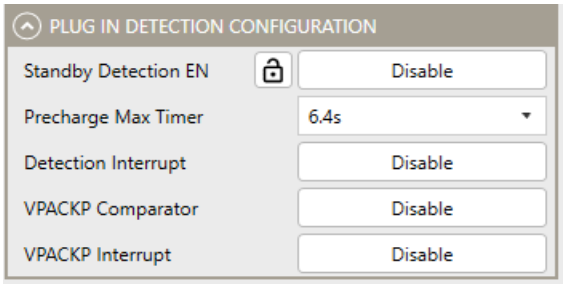


Figure 12: Plug-In Detection Configuration

a. Precharge Max Timer: Set the PACKP maximum pre-charge expiration timer between 0.2s and 24s.

b. VPACKP Comparator: The “VPACKP Comparator” parameter enables the PACK vs. VTOP comparator. If the PACK vs. VTOP comparator is disabled, the comparator still can be enabled internally by the other functions, such as plug-in detection.

5. Figure 13 shows the Pin Configuration settings in the GUI.

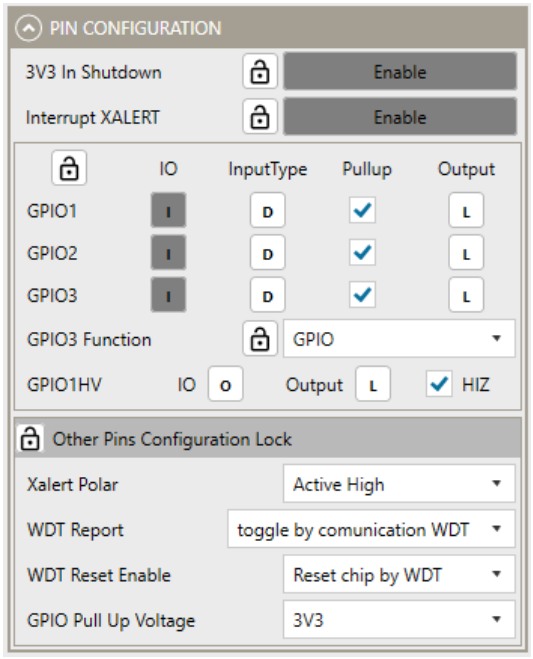


Figure 13: Pin Configuration

a. IO: The IO parameter determines whether GPIO1, GPIO2, and GPIO3 are set as inputs or outputs. If GPIOx pins are set as inputs, connect GPIOx to a high or low level. If set as an input, do not float GPIOx to reduce GPIOx power consumption.

b. Input Type: The input type determines whether the GPIO1, GPIO2, and GPIO3 inputs are digital inputs or buffered ADC inputs.

c. Pullup: The pull-up parameter enables the GPIO1, GPIO2, and GPIO3 pins' pull-up capability. If the pull-up box is selected, then the GPIOx pull-up capability is enabled, and a 20kΩ pull-up resistor is applied.

d. Output: The output parameter for GPIO1, GPIO2, and GPIO3 determines whether the GPIOx target output level is high or low. Set the GPIOx target output level to either high (H) or low (L). This bit can only be configured while the corresponding GPIOx pin is functioning as a digital output.

e. GPIO3 Function: Set GPIO3 to function as either a GPIO pin or a fault indicator. This bit can only be configured while GPIO3 is set as an output.

f. GPIO1HV: The output parameter for GPIO1HV determines whether the GPIO1HV target output level is high (H) or low (L). This bit can only be configured while GPIO1HV is functioning as a digital output and GPIO1HV_HZ = 0. If "HIZ" is selected, then GPIO1HV is in Hi-Z mode. In this mode, GPIO1HV ignores GPIO1HV_O, and the bypass P-channel MOSFET turns off. If "HIZ" is not selected, then GPIO1HV is controlled in output mode following GPIO1HV_O, and the bypass P-channel MOSFET turns on once the output is low.

g. GPIO Pull Up Voltage: Set the GPIO be pull-up voltage to either 3.3V (3V3) or V_{REGIN} (REGIN).

6. Figure 14 shows the ADC Scan Configuration settings in the GUI.

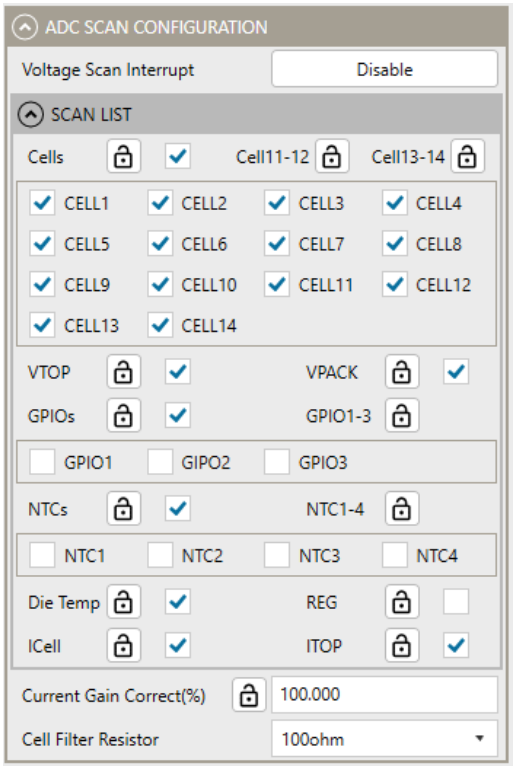


Figure 14: ADC Scan Configuration

a. Enable the desired channels by selecting the corresponding box. If a channel is enabled, then that channel is updated during the high-resolution ADC scan. If a channel is disabled, then the channel is excluded from the high-resolution ADC scan.

b. Current Gain Correct (%): The current-gain correction compensates for the sense resistor and SMT variation. The correction is applied to both Coulomb counting and synchronous current ADC readings. The correction is not applied to SC and OC detection. Set the current-gain correction between 87.5% and 112.476%.

c. Cell Filter Resistor: The default cell filter resistor value is 100Ω. When using a 1kΩ filtering resistor, set the cell filter resistor to 1kΩ (e.g. for external balancing). This compensates for the ADC cell readings to remove the drop caused by the input current during the ADC conversion.

7. Figure 15 shows the Watchdog Configuration settings in the GUI.

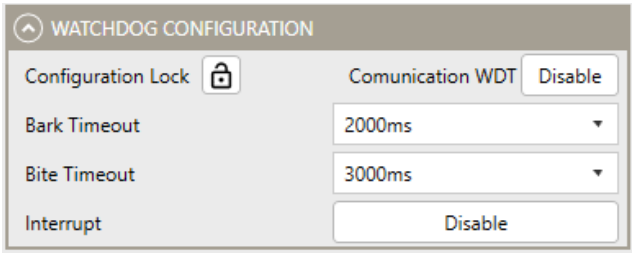


Figure 15: Watchdog Configuration

a. Bark Timeout: The bark timeout parameter determines the delay between the last watchdog reset and the bark. Set the bark timeout between 25ms and 3200ms.

b. Bite Timeout: The bite timeout parameter determines the delay between the bark and the bite. Set the bite timeout between 25ms and 3200ms.

8. Figure 16 shows the Open-Wire Configuration settings in the GUI.

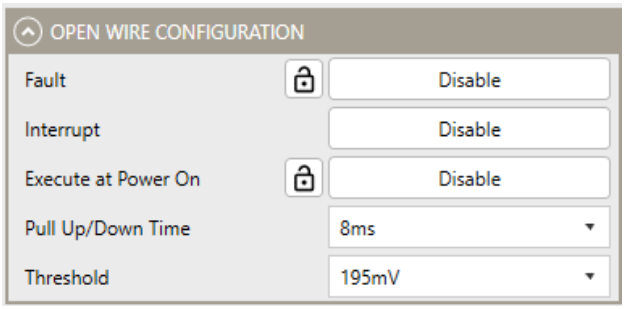


Figure 16: Open Wire Configuration

a. Execute at Power On: Set “Execute at Power On” to either “Enable” or “Disable” to execute or not to execute one time open-wire detection after leaving shutdown mode.

b. Pull Up/Down Timer: Set each pull-up and pull-down phase length between 1ms and 16ms.

c. Threshold: Set the open-wire threshold during the detection sequence between 39mV and 625mV.

9. Figure 17 shows the Coulomb Counter Configuration settings in the GUI.

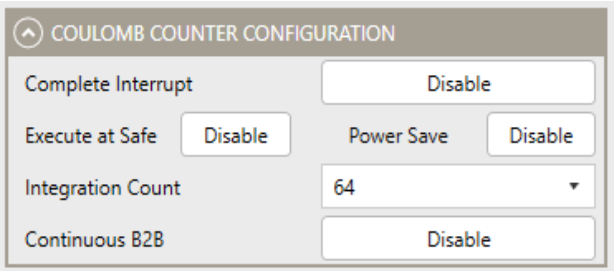


Figure 17: Coulomb Counting Configuration

a. Power Save: If the power-save mode (PSM) parameter is enabled, then the Coulomb counter operates in PSM. If Power Save is disabled, then the Coulomb counter does not operate in PSM. PSM reduces overall current consumption, but also reduces accuracy.

b. Integration Count: The Coulomb counter integration length is set as the number of time slots. Each time slot is 32ms. Set the integration length between 1 time slot (32ms) and 64 time slots (2048ms). This register should only be updated while Coulomb counting is not active.

c. Continuous B2B: If back-to-back accumulation mode is enabled, then a new Coulomb counting conversion starts automatically after the most recent conversion is complete.

10. Figure 18 shows the Over-Current Configuration settings in the GUI.

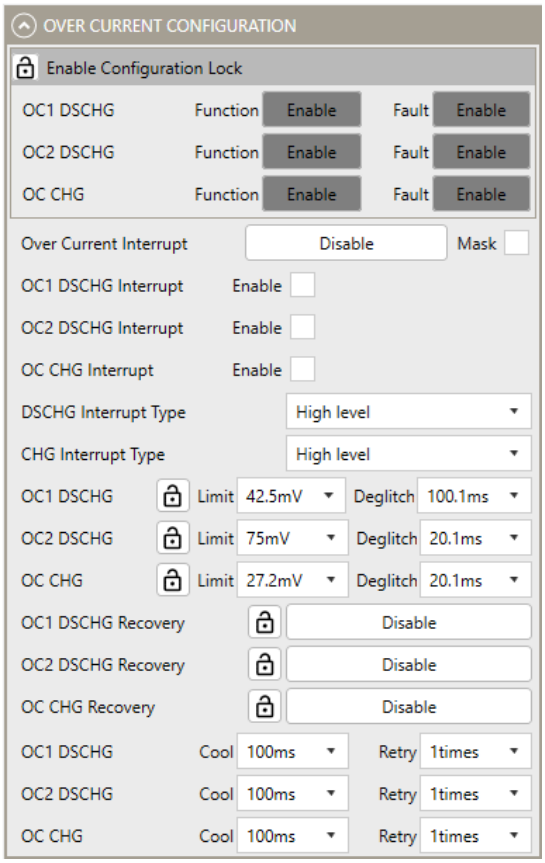


Figure 18: Over-Current Configuration

a. Mask: Select the “Mask” box to enable the OC interrupt mask function, which may be needed after the associated interrupt has triggered. If the OC interrupt mask is enabled, then the OC interrupt flag is cleared, and the interrupt pin is pulled low unless there are other pending interrupts. If the OC interrupt mask is disabled, then an OC condition can trigger the interrupt flag.

b. OC1 DSCHG Limit and OC2 DSCHG Limit: Set the OC1 discharge limit and OC2 discharge limit between 2.5mV and 240mV.

c. OC1 DSCHG Deglitch and OC2 DSCHG Deglitch: Set the OC1 discharge deglitch time and OC2 deglitch time between 0.1ms and 2520.1ms.

d. OC CHG Limit: Set the OC charge limit between 1.6mV and 153.6mV.

e. OC CHG Deglitch: Set the OC charge deglitch time between 0.1ms and 2520.1ms..

f. OC1 DSCHG Recovery, OC2 DSCHG Recovery, and OC CHG Recovery: Enable the OC recovery conditions for automatic recovery. Disable the OC recovery conditions for manual recovery.

g. OC1 DSCHG Cool, OC2 DSCHG Cool, and OC CHG Cool: Set the OC cool-down times to 100ms, 200ms, 500ms, or 1s.

h. OC1 DSCHG Retry, OC2 DSCHG Retry, and OC CHG Retry: Set the reconnection attempts to 1 time, 2 times, 3 times, or infinite (keep trying).

11. Figure 19 shows the Short-Circuit Configuration settings in the GUI.

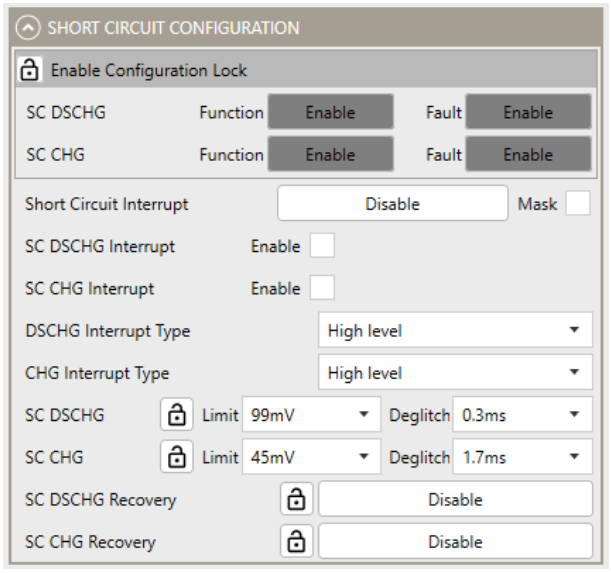


Figure 19: Short Circuit Configuration

a. Mask: Select the “Mask” box to enable the SC interrupt mask function, which may be needed after the associated interrupt has triggered. If the SC interrupt mask is enabled, then the SC interrupt flag is cleared, and the interrupt pin is pulled low unless there are other pending interrupts. If the SC interrupt mask is disabled, then an SC condition can trigger the interrupt flag.

b. SC DSCHG Limit: Set the SC discharge limit between 5.5mV and 528mV.

c. SC DSCHG Deglitch: Set the SC discharge deglitch time between 0.1ms and 25.5ms.

d. SC CHG Limit: Set the SC charge limit between 2.5mV and 240mV.

e. SC CHG Deglitch: Set the SC charge deglitch time between 0.1ms to 25.5ms.

f. SC DSCHG Recovery and SC CHG Recovery: Enable the SC recovery conditions for automatic recovery. Disable the SC recovery conditions for manual recovery.

12. Figure 20 shows the Short-Circuit Removal Configuration settings in the GUI.

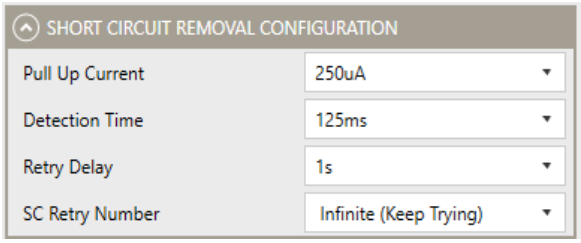


Figure 20: Short-Circuit Removal Configuration

a. Pull Up Current: Set the pull-up current during SC removal detection to 250μA, 500μA, or 750μA.

b. Detection Time: Set the detection time to 125ms, 250ms, 500ms, or 1s.

c. Retry Delay: Set the retry delay between 1s and 25s.

d. SC Retry Number: Set the number of SC retries to 1 time, 2 times, 4 times, or infinite (keep trying).

13. Figure 21 shows the NTC Configuration settings in the GUI.

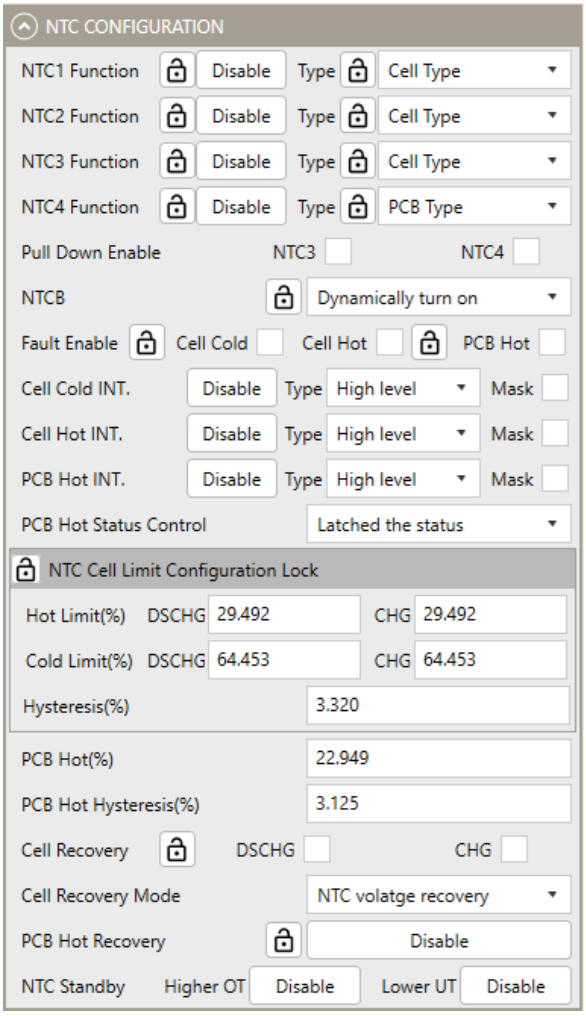


Figure 21: NTC Configuration

a. NTC Type: Set the NTC type to “cell type” for cell monitoring or “PCB type” for PCB monitoring.

b. Pull Down Enable: To allow NTC3 and NTC4 to be pulled down, selecting the “NTC3” and “NTC4” boxes to the right of “Pull Down Enable”.

c. NTCB: NTCB is set to “dynamically turn on”. NTCB is dynamically biased during ADC conversions of the NTC channels. If NTCB is on continuously, current consumption increases.

d. PCB Hot Status Control: Set the PCB hot status control to display either the latched status (which goes to the interrupt controller) or the real-time status.

e. NTC Cell Limit: Set the NTC cell limit configuration (Hot Limit(%) and Cold Limit(%)) between 0% and 99.9% of NTCB.

f. Hysteresis(%): Set the NTC cell limit configuration hysteresis between 0% and 6.055% of NTCB.

g. Cell Recovery Mode: The cell recovery mode parameter determines the recovery logic for the NTC hot/cold conditions in charge mode. Set this bit to 0 for “NTC voltage recovery”. Set this bit to 1 for “NTC voltage recovery or Charger removed”.

h. Lower UT: The “Lower UT” parameter determines the selection criteria for the NTC cold threshold while I_{BATT} is within the $I_{STANDBY}$ range. If “Lower UT” is disabled, select the colder threshold (i.e. the higher voltage). If “Lower UT” enabled, select the hotter threshold (i.e. the lower voltage).

14. Figure 22 shows the Die Temperature Configuration settings in the GUI.

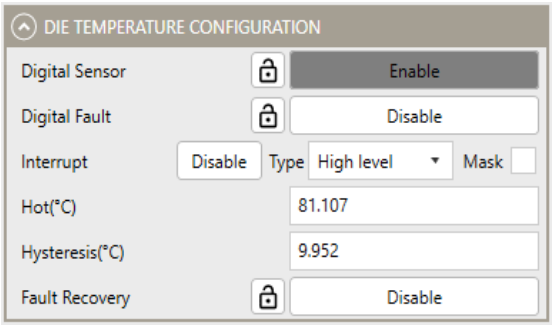


Figure 22: Die Temperature Configuration

a. Hot(°C): Set the “Hot (°C)” parameter for the digital die temperature threshold. The resolution is 0.474°C.

b. Hysteresis(°C): Set the hysteresis between 0°C and 14.692°C.

15. Figure 23 shows the Cell-Balancing Configuration settings in the GUI.

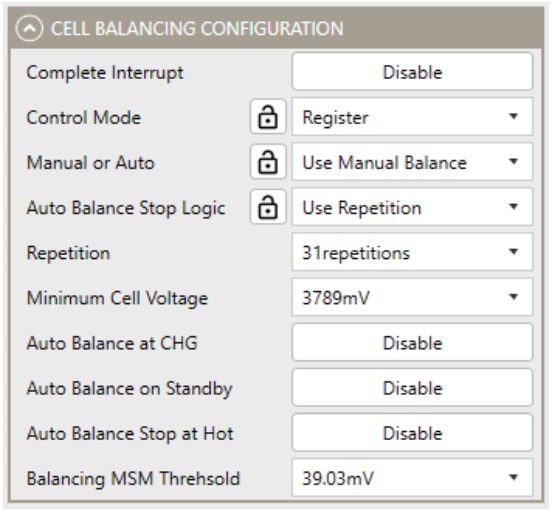


Figure 23: Cell-Balancing Configuration

a. Control Mode: Set the control mode while using automatic cell balancing to either register control mode (Register) or GIPO3 control mode (GIPO3).

b. Manual or Auto: Set the cell-balancing mode (Manual or Auto) to either manual balancing (Use Manual Balance) or automatic balancing (Use Auto Balance).

c. Auto Balance Stop Logic: The “Auto Balance Stop Logic” parameter can only be configured while automatic balance is enabled. If “Auto Balance Stop Logic” is set to “Use Repetition,” then the device uses repetition to control the number of balancing iterations. If “Auto Balance Stop Logic” is set to “Use Go or List,” then balancing continues until register BALANCE_GO is set to 0, or until the balancing list is empty.

d. Repetition: Set the balancing cycle repetitions between 0 and 31 repetitions. If 31 repetitions are selected, then 32 balancing cycles are executed.

e. Minimum Cell Voltage: Set the minimum cell voltage required to run automatic balancing between 2500mV and 4961mV. If a cell drops below this level, then it is excluded from the balancing list. All other qualifying cells are balanced.

f. Balancing MSM Threshold: The balancing MSM threshold is used by the auto-balancing algorithm. Set the balancing MSM threshold between 19.5mV and 87.85mV.

16. Figure 24 shows the Cell Over-Voltage Configuration settings in the GUI.

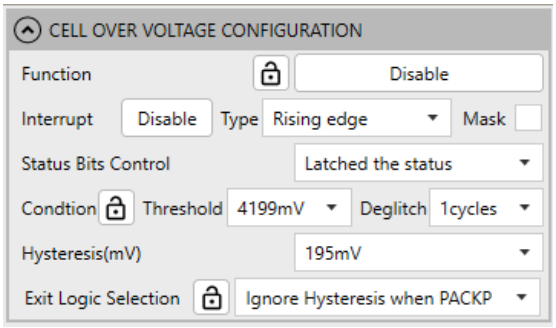


Figure 24: Cell Over-Voltage Configuration

a. Threshold: Set the cell OV threshold between 0mV and 4980.15mV.

b. Hysteresis(mV): Set the cell OV hysteresis between 0mV and 292.5mV.

c. Exit Logic Selection: Set “Exit Logic Selection” to either “Lower than Cell OV - Hysteresis” or “Ignore Hysteresis when PACKP lower than VTOP”.

17. Figure 25 shows the Cell Under-Voltage Configuration settings in the GUI.

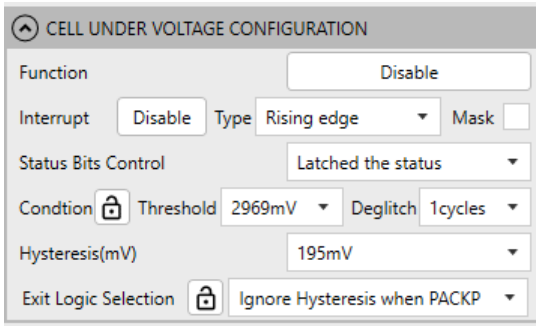


Figure 25: Cell Under-Voltage Configuration

a. Threshold: Set the cell UV threshold between 0mV and 4980.15mV.

b. Hysteresis(mV): Set the cell UV hysteresis between 0mV and 292.5mV.

c. Exit Logic Selection: Set “Exit Logic Selection” to either “Higher than Cell UV + Hysteresis” or “Ignore Hysteresis when PACKP higher than VTOP.”

18. Figure 26 shows the Cell Mismatch Configuration settings in the GUI.

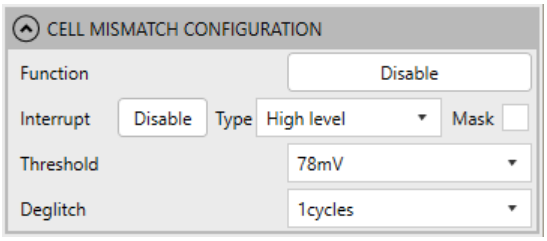


Figure 26: Cell Mismatch Configuration

Threshold: Set the cell mismatch threshold between 0mV and 1211mV.

19. Figure 27 shows the Cell Dead Configuration settings in the GUI.

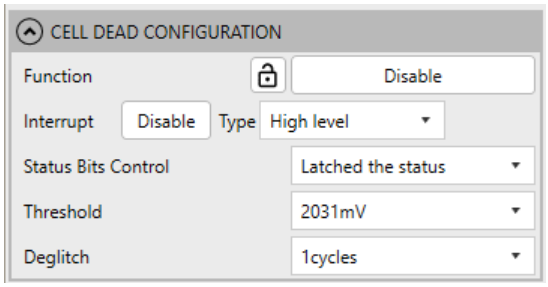


Figure 27: Cell Dead Configuration

Threshold: Set the cell dead threshold between 0mV and 2480mV.

20. Figure 28 shows the VTOP Under-Voltage Configuration settings in the GUI.

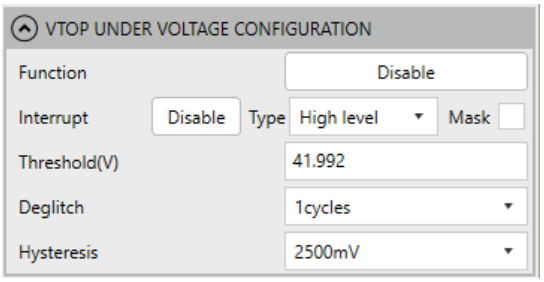


Figure 28: VTOP Under-Voltage Configuration

a. Threshold(V): Set the VTOP UV threshold between 0V and 79.98V.

b. Hysteresis: Set the VTOP UV hysteresis between 0mV and 4922mV.

21. Figure 29 shows the VTOP Over-Voltage Configuration settings in the GUI.

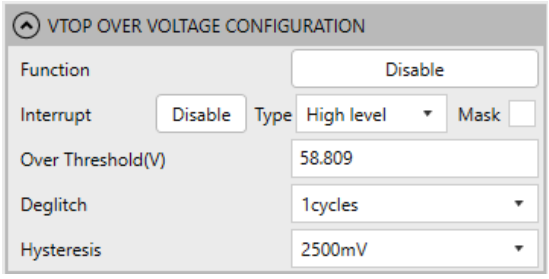


Figure 29: VTOP Over-Voltage Configuration

a. Over Threshold(V): Set the VTOP OV threshold between 0V and 79.98V.

b. Hysteresis: Set the VTOP OV hysteresis between 0mV and 4922mV.

22. Configure the REGIN Check, 3V3 Check, VDD Check, and ADC Self-Test parameters. Figure 30 shows the REGIN Check Configuration, 3V3 Check Configuration, VDD Check Configuration, and ADC Self-Test Configuration settings in the GUI.

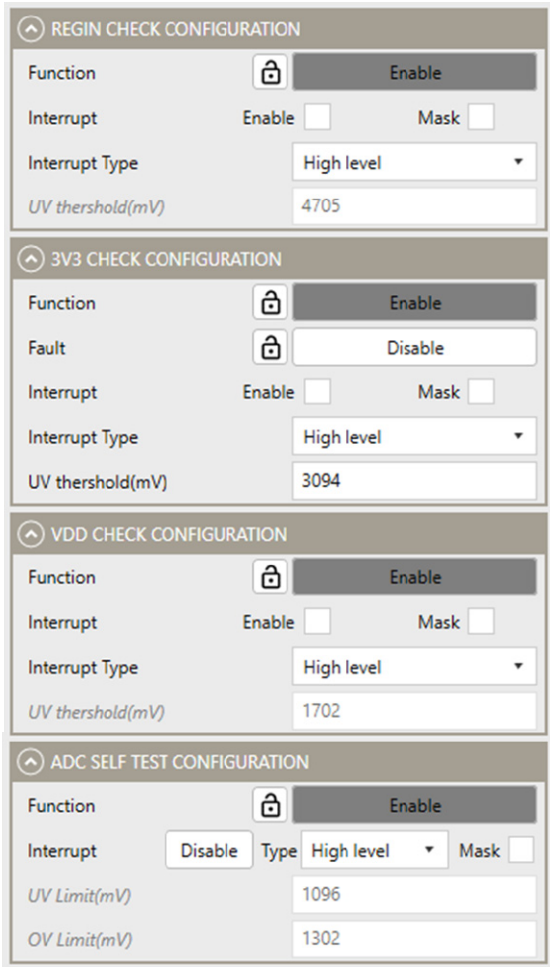


Figure 30: REGIN Check, 3V3 Check, VDD Check, and ADC Self-Test Configurations

23. Configure the one-time programmable (OTP) memory CRC check parameters. Figure 31 shows the OTP CRC Check Configuration settings in the GUI.

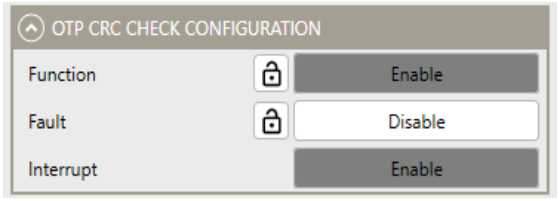


Figure 31: OTP CRC Check Configuration

Monitors and Controls

Figure 32 shows the status monitor.

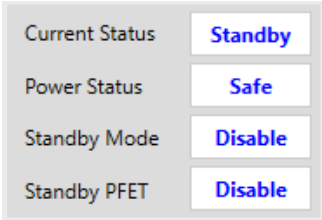


Figure 32: Status Monitor

Figure 33 shows the plug-in detection control and monitor.

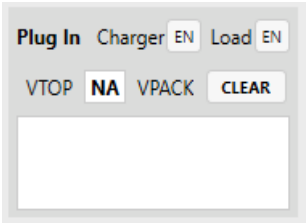


Figure 33: Plug-In Detection Control and Monitor

Figure 34 shows the watchdog status monitor.

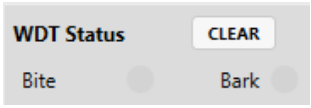


Figure 34: Watchdog Status Monitor

Figure 35 shows the MOSFET status monitor.

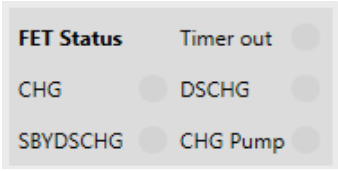


Figure 35: MOSFET Status Monitor

Figure 36 shows the configurations for the ADC scan, cell-balance, and open-wire controls and monitors.

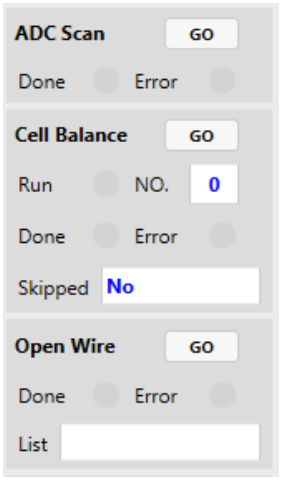


Figure 36: ADC Scan, Cell-Balance, and Open-Wire Control and Monitor Configuration

Figure 37 shows the OC and SC status monitors.

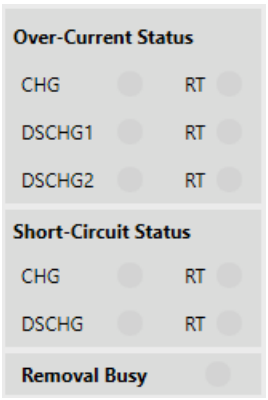


Figure 37: Over-Current and Short-Circuit Status Monitors

Figure 38 shows the GPIO and VTOP status monitors.

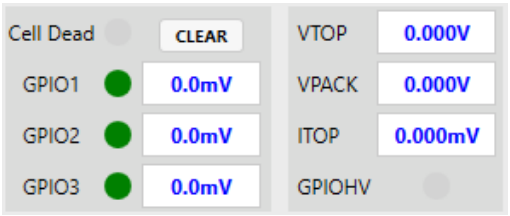


Figure 38: GPIO and VTOP Status Monitors

Figure 39 shows the die temperature status monitor.

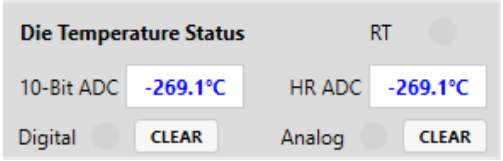


Figure 39: Die Temperature Status Monitor

Figure 40 shows the OTP CRC control and monitor.

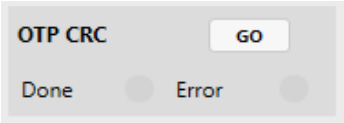


Figure 40: OTP CRC Control and Monitor

Figure 41 shows the NTC monitor.

	Status	10-Bit ADC	HR ADC	RT
NTC1	Normal	0.0%	0.000%	Normal
NTC2	Normal	0.0%	0.000%	Normal
NTC3	Normal	0.0%	0.000%	Normal
NTC4	Normal	0.0%	0.000%	Normal

Figure 41: NTC Monitor

Figure 42 shows the NTC functional block diagram.

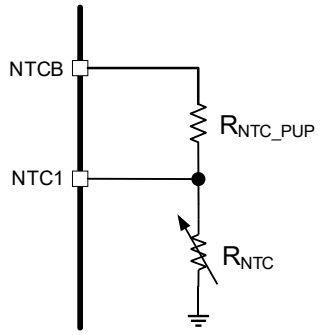


Figure 42: NTC Functional Block Diagram

The NTC resistor (R_{NTC}) can be estimated with Equation (1):

$$R_{NTC}=\frac{A \times R_{NTC\_PUP}}{32768 - A} \quad (1)$$

Where A is the NTC ADC reading, and R_{NTC_PUP} is NTC pull-up resistor (10kΩ).

The ambient temperature (T) can be calculated with Equation (2)

$$T(K) = \frac{1}{\frac{1}{T_0} + \frac{1}{B} \ln \frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is NTC resistor when $T = T_0$; B is the thermistor constant; and T, T_0, and B are in Kelvin.

For example, if the NTC ADC reading (A) is 9830 (0x2666) for the thermistor (NCP18XH103), R_0 is 10kΩ at 25°C (298.15K), and B is 3380K; then R_{NTC} is 4.285kΩ, and T is 322K. This means that if the NTC ADC reading is 9830, then the ambient temperature is about 49°C.

Figure 43 shows the LDO monitor.

	Status	10-Bit ADC	HR ADC
VDD	Normal	0.0mV	0.0mV
3V3	Normal	0.0mV	0.0mV
REGIN	Normal	0.0mV	0.0mV
Self	Normal	0.0mV	

Figure 43: LDO Monitor

Figure 44 shows the cell ADC monitor.

	Voltage	Current	UV	OV	MS	Dead	BAL
Cell1	0.0mV	0.000mV					
Cell2	0.0mV	0.000mV					
Cell3	0.0mV	0.000mV					
Cell4	0.0mV	0.000mV					
Cell5	0.0mV	0.000mV					
Cell6	0.0mV	0.000mV					
Cell7	0.0mV	0.000mV					
Cell8	0.0mV	0.000mV					
Cell9	0.0mV	0.000mV					
Cell10	0.0mV	0.000mV					
Cell11	0.0mV	0.000mV					
Cell12	0.0mV	0.000mV					
Cell13	0.0mV	0.000mV					
Cell14	0.0mV	0.000mV					

Figure 44: Cell ADC Monitor

EVALUATION BOARD SCHEMATIC

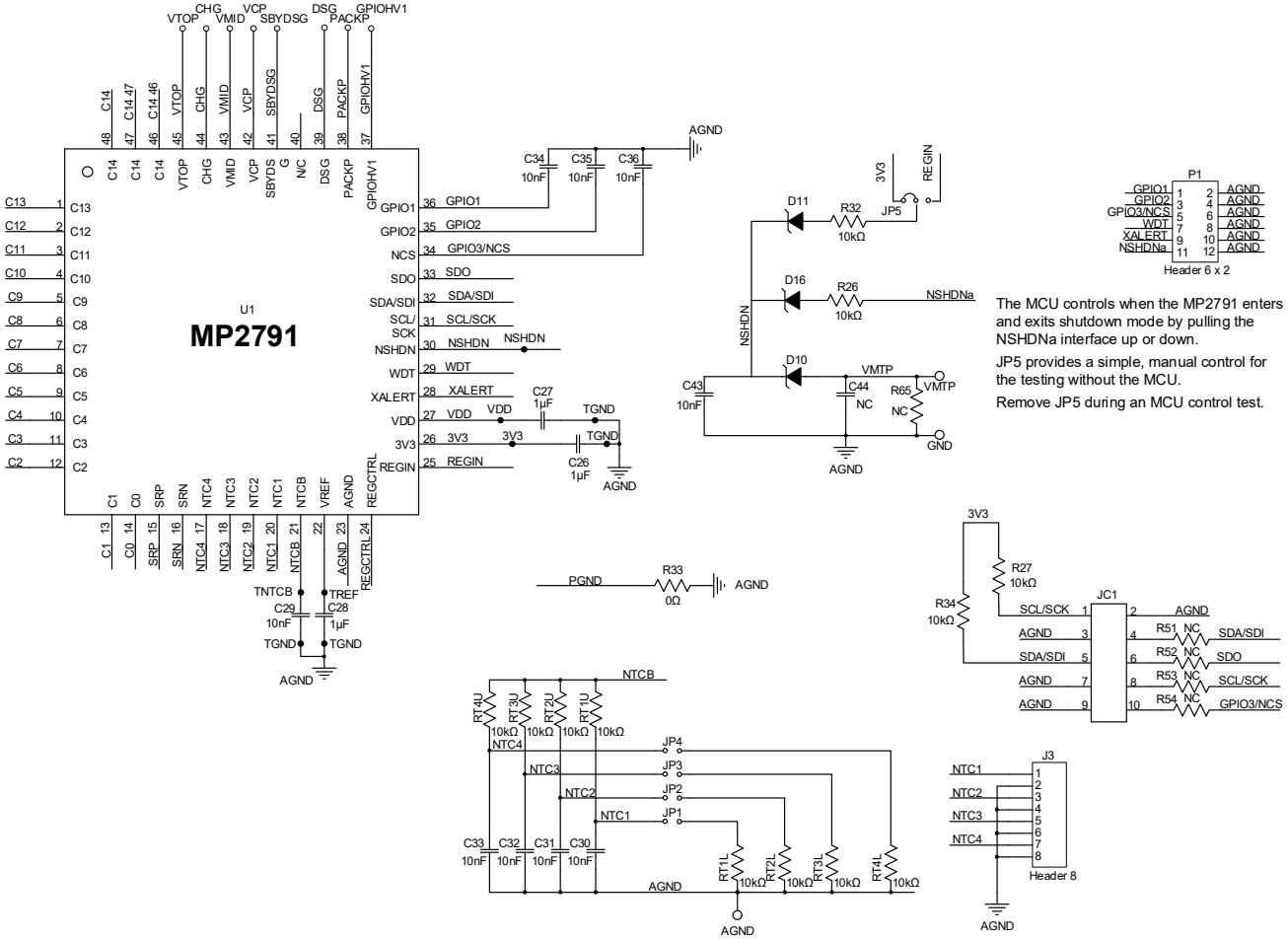


Figure 45: Evaluation Board Schematic (IC and Connector)

EVALUATION BOARD SCHEMATIC *(continued)*

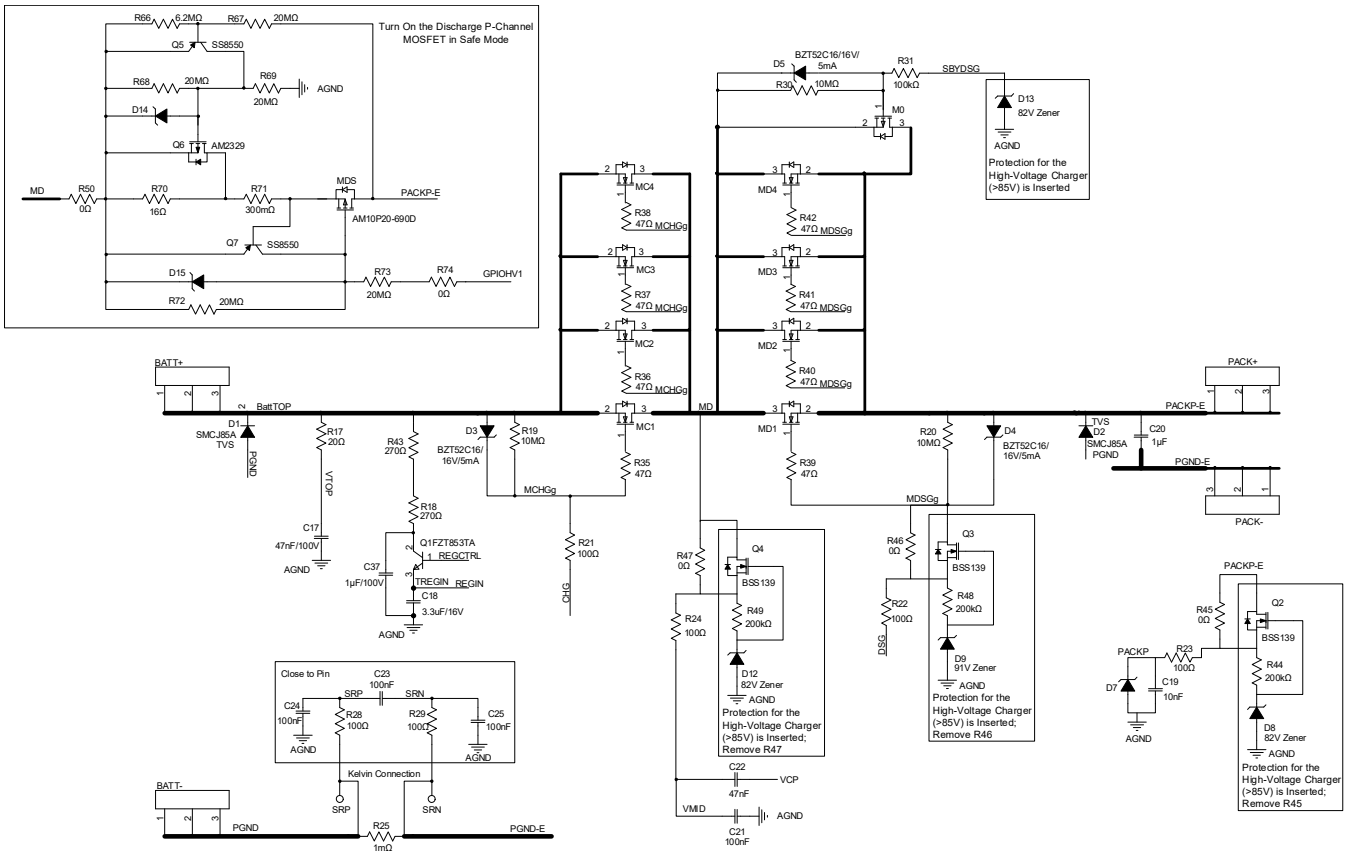
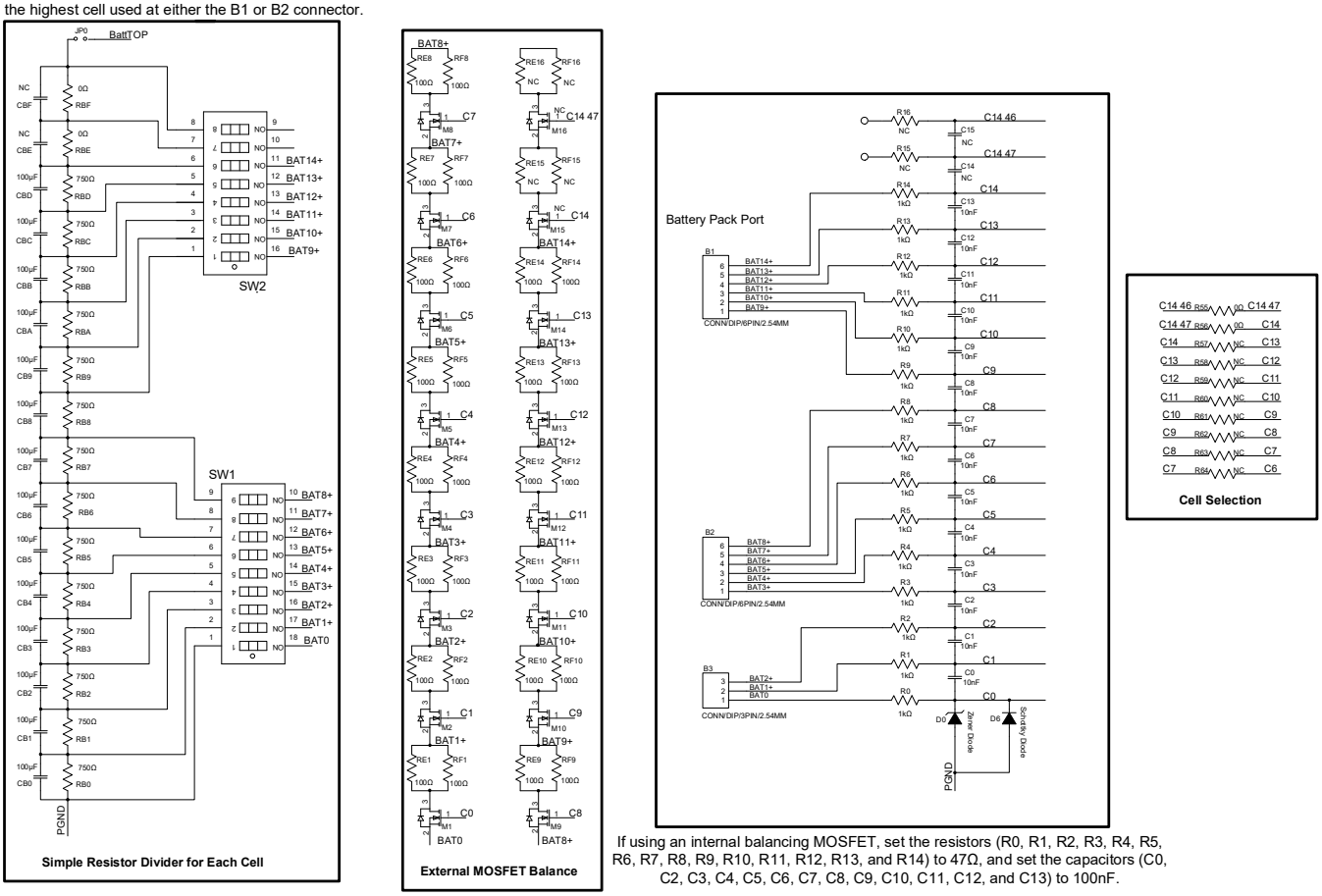


Figure 46: Evaluation Board Schematic (Power Path)

EVALUATION BOARD SCHEMATIC *(continued)*

If less than 14 cells are connected in series, short BAT14+ to the highest cell used at either the B1 or B2 connector.



If using an internal balancing MOSFET, set the resistors (R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, and R14) to 47Ω, and set the capacitors (C0, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, and C13) to 100nF.

Figure 47: Evaluation Board Schematic (Battery Connection)

EV2791-0000-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	J3	2.54mm	8-pin connector	DIP	Wurth	691210910008
2	B1,B2	2.54mm	6-pin connector	DIP	Wurth	691210910006
1	B3	2.54mm	3-pin connector	DIP	Wurth	691210910003
4	BATT+, BATT-, PACK+, PACK-	5.08mm	3-pin connector	DIP	Wurth	691236510003
14	C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13	10nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A103KA01D
3	C23, C24, C25	100nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A104KA35D
2	C17, C22	47nF	Ceramic capacitor, 100V, X7R	0805	Murata	GRM21BR72A473KA01L
1	C19	10nF	Ceramic capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
1	C18	3.3µF	Ceramic capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
1	C20	1µF	Ceramic capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C21	100nF	Ceramic capacitor, 100V, X7R	1206	Murata	GRM319R72A104KA01D
3	C26, C27, C28	1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
9	C29, C30, C31, C32, C33, C34, C35, C36, C43	10nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206065
1	C37	1µF	Ceramic capacitor, 100V, X7S	0805	TDK	C2012X7S2A105KT000N
14	CB0, CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CBA, CBB, CBC, CBD	100µF	Ceramic capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	D0	5.6V	Zener diode	SOD-123	Diodes, Inc.	BZT52C5V6
2	D1, D2	85V	TVS diode	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
5	D3, D4, D5, D14, D15	16V	Zener diode, 5mA, 500mW	SOD-123	Diodes, Inc.	BZT52C16
1	D6	100V	Schottky diode, 150mA	SOD-323	JCET	BAT46WS
3	D10, D11, D16	30V	Schottky diode, 0.5A	SOD-123	Diodes, Inc.	B0530W
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2 x 6-pin connector	DIP	Any	
5	JP0, JP1, JP2, JP3, JP4	2.54mm	2-pin connector	DIP	Any	
1	JP5	2.54mm	3-pin connector	DIP	Any	
2	M0, MDS	200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D
2	MC3, MD3	150V	N-channel MOSFET, 24mΩ, 77nC, 100A	TO-263	Analog Power	AMIB108N15N3-T1-PF

EV2791-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
14	M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14	50V	N-channel MOSFET, 600mΩ, 100mA	SOT-23	LRC	LBSS138LT1G
1	Q1	100V	NPN transistor, 6A, 3W	SOT-223	Diode, Inc.	FZT853TA
2	Q5, Q7	-25V	PNP transistor	SOT-23	JCET	SS8550LT1
1	Q6	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
15	R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
28	RE1, RE2, RE3, RE4, RE5, RE6, RE7, RE8, RE9, RE10, RE11, RE12, RE13, RE14, RF1, RF2, RF3, RF4, RF5, RF6, RF7, RF8, RF9, RF10, RF11, RF12, RF13, RF14	100Ω	Film resistor, 5%	1206	Yageo	RC1206JR-07100RL
14	RB0, RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RBA, RBB, RBC, RBD	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
1	R17	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R18, R43	270Ω	Film resistor, 5%	2512	Yageo	RC2512JR-07270RL
4	R21, R22, R23, R24	100Ω	Film resistor, 5%	1206	Yageo	RC1206JR-07100RL
3	R19, R20, R30	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
2	R28, R29	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R25	1mΩ	Current-sense resistor, 1%	3920	Bourns, Inc.	CSS2H-3920R-1L00F
1	R31	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
10	R33, R45, R46, R47, R50, R55, R56, R74, RBE, RBF	0Ω	Film Resistor, 5%	0603	Yageo	RC0603JR-070RL
8	R35, R36, R37, R38, R39, R40, R41, R42	47Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0747RL

EV2791-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
12	R26, R32, RT1L, RT1U, RT2L, RT2U, RT3L, RT3U, RT4L, RT4U, R27, R34	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L
5	R67, R68, R69, R72, R73	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
1	R70	16Ω	Film resistor, 5%	0603	LIZ	CR0603JA0160G
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L
1	SW1	9 pins	9-pin switch	SMD	Wurth	418121270809
1	SW2	8 pins	8-pin switch	SMD	Wurth	418121270808
1	U1	MP2791	7-cell to 14-cell, high-accuracy battery-monitoring and protection IC	TQFP-48 (7mmx 7mm)	MPS	MP2791DFP-0000

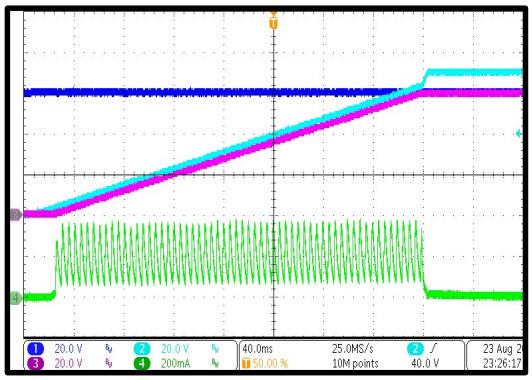
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Discharge MOSFET Soft Turn-On

PACK+ is connected to a 1mF capacitor,
DSG slope = 0.2V/ms

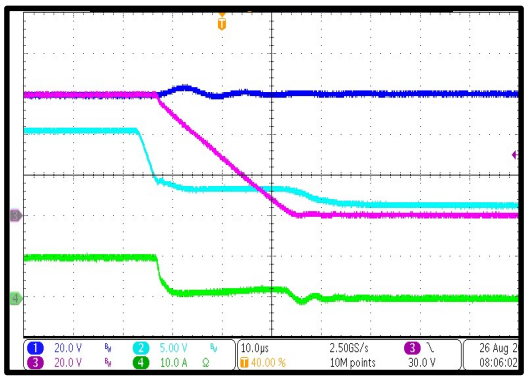
CH1: V_{MID}
CH2: V_{DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



Discharge MOSFET Turn-Off

CR load = 6Ω

CH1: V_{MID}
CH2: V_{GS_DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



PCB LAYOUT

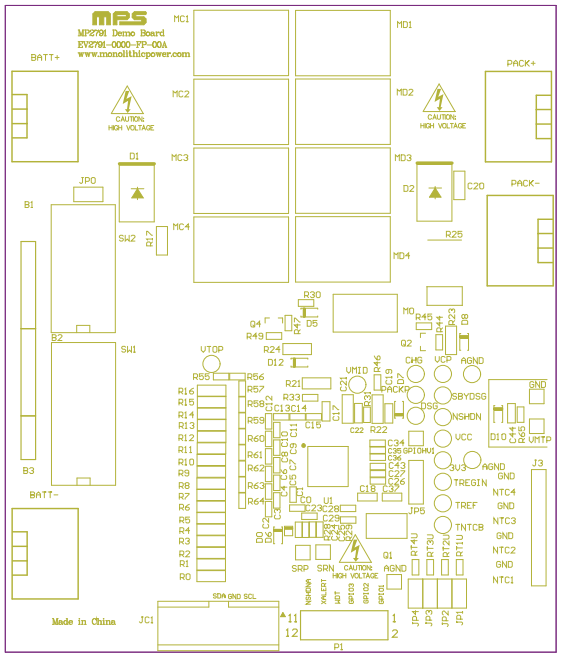


Figure 48: Top Silk

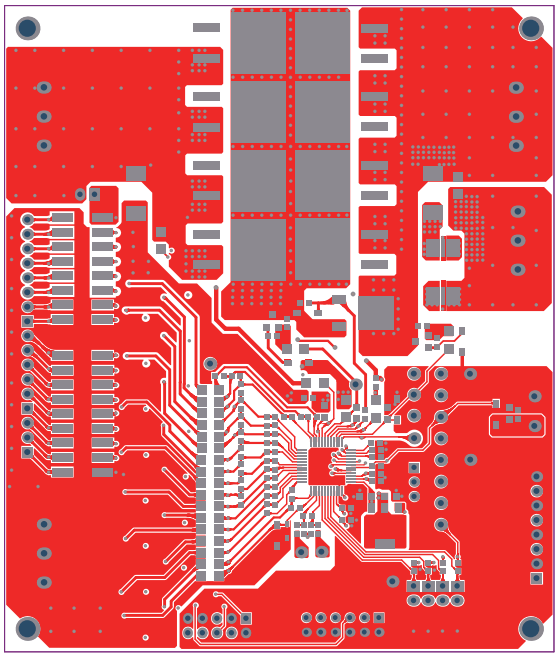


Figure 49: Top Layer

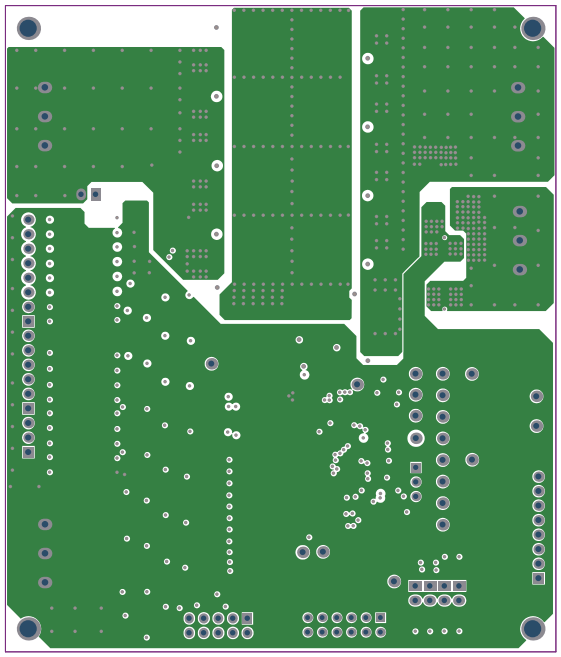


Figure 50: Mid-Layer 1

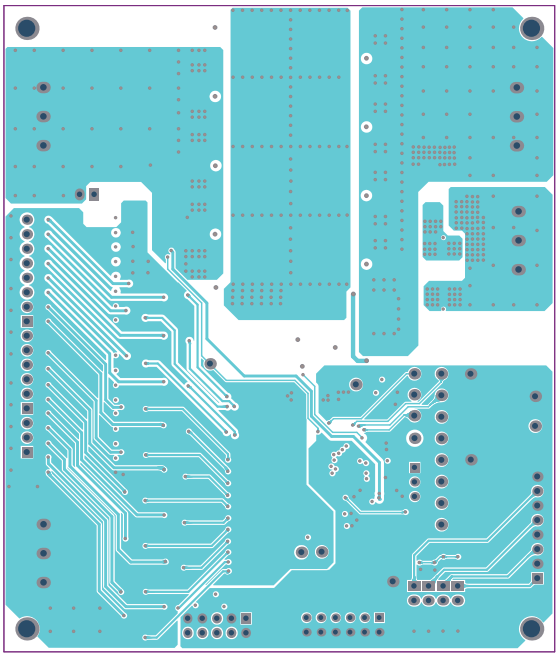


Figure 51: Mid-Layer 2

PCB LAYOUT *(continued)*

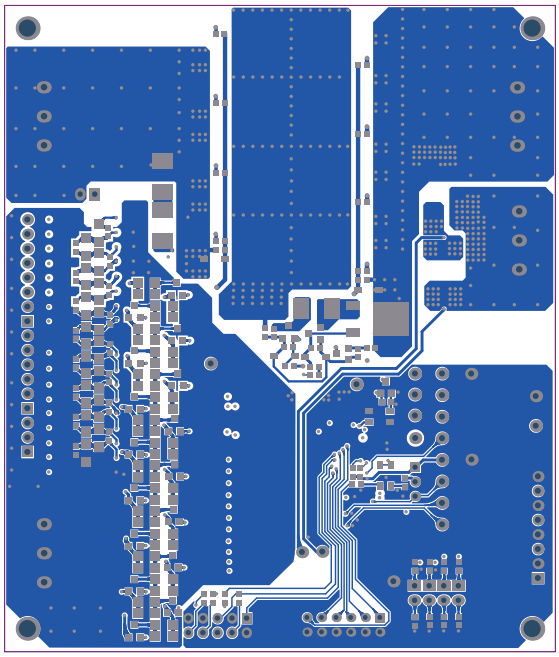


Figure 52: Bottom Layer

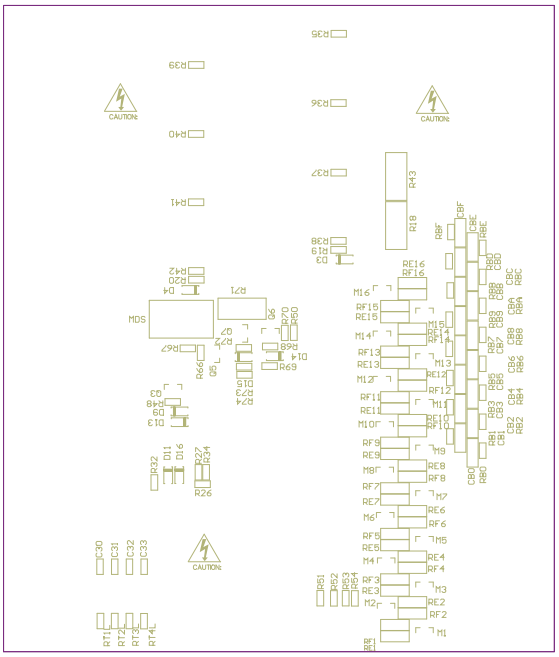


Figure 53: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/25/2022	Initial Release	-