EV2787-0000/0002-FP-00A

7-Cell to 16-Cell, High-Accuracy Battery Monitor with Coulomb Counting Evaluation Board

DESCRIPTION

The EV2787-0000-FP-00A and EV2787-0002-FP-00A evaluation boards are designed to evaluate the MP2787, a complete analog front-end (AFE) monitoring IC. The MP2787 supports 7-cell to 16-cell series battery packs with outstanding measurement accuracy.

The MP2787 measures each cell's voltage, while also synchronously measuring charge/discharge current and Coulomb counting via an external current-sense resistor. It also measures die temperature and cell temperature via four NTC thermistor inputs. The MP2787 contains internal passive balancing MOSFETs capable of driving up to 58mA, and is capable of driving external balancing transistors for higher current.

The MP2787 features robust hardware monitoring alarm functions, such as over-current (OC) interrupt, battery under-voltage (UV) interrupt, battery over-voltage (OV) interrupt, and high/low-temperature interrupt. All of these interrupts have configurable thresholds.

These evaluation boards combine the MP2787 with a current-sense resistor to support up to 70A of charge/discharge current. The board also includes placeholders to add external transistors for a higher balancing current, if needed.

The EV2787-0000/0002-FP-00A can be evaluated by connecting to an 18V to 75.2V battery pack (or simulated battery pack). These evaluation boards require a computer with an available USB port and the MPS evaluation software installed. An MPS USB-to-I^2C/SPI communication interface allows the PC to interface to the MP2787 communication port: The EV2787-0000-FP-00A has the MP2787DFP-0000 and supports I^2C communication, and the EV2787-0002-FP-00A has the MP2787DFP-0002 and supports SPI communication.

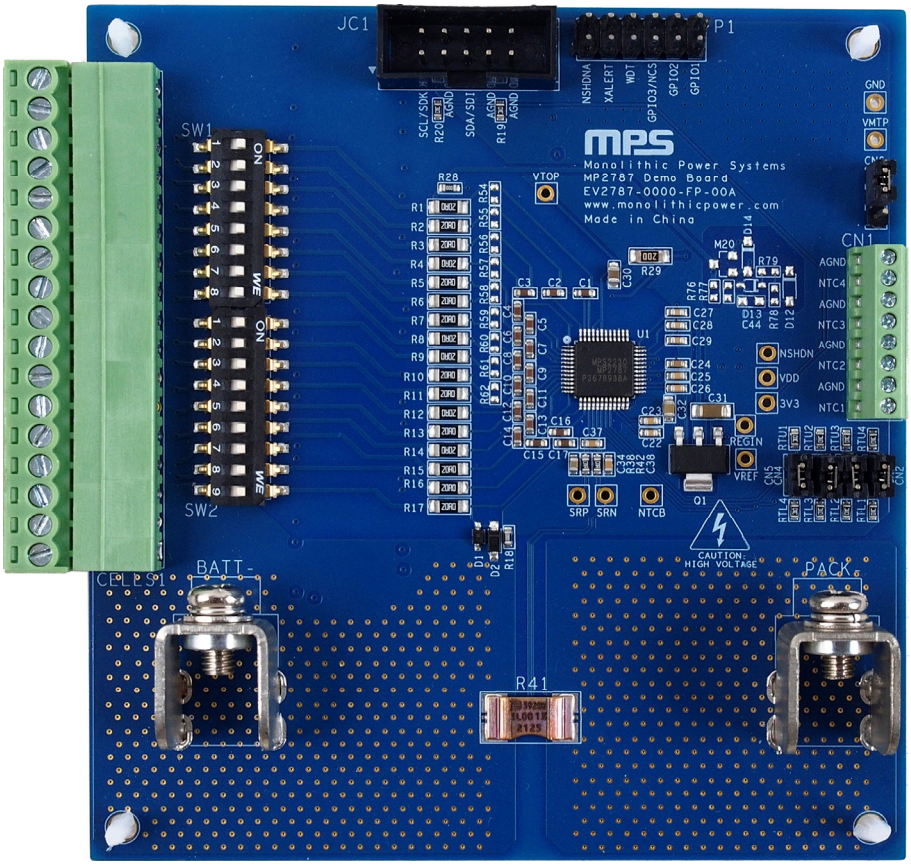
The MP2787 is available in a TQFP-48 (7mmx7mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage range		18V to 75.2V
Cell voltage (V_{CELL}) range		0V to 5V
Continuous charge current		0A to 70A
Continuous discharge current		0A to 70A
Internal balancing current	V_{BATT} = 4V, T_A = 25°C	58mA
Supported cells in series		7 to 16

EVALUATION BOARD



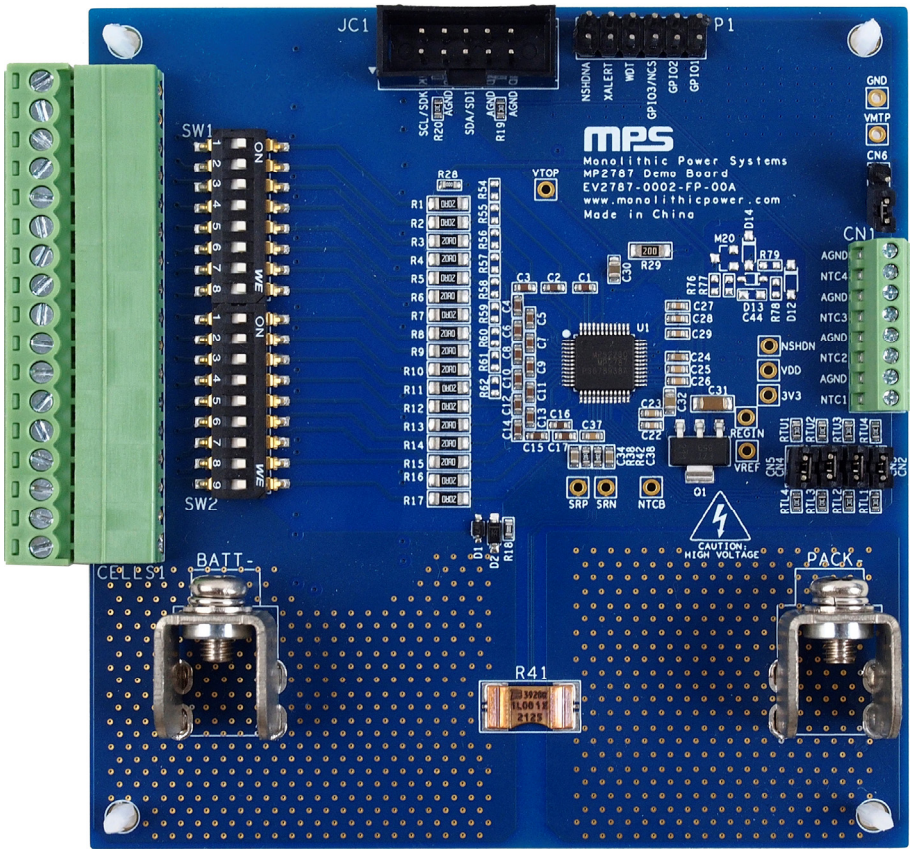
LxWxH (10.4cmx9.6cmx1.5cm)

Board Number	MPS IC Number
EV2787-0000-FP-00A	MP2787DFP-0000 (1)

Note:

1) "0000" is the register setting option that supports I^2C communication with CRC disabled. For custom options, contact an MPS FAE to obtain an "xxxx" value.

EVALUATION BOARD *(continued)*



LxWxH (10.4cmx9.6cmx1.5cm)

Board Number	MPS IC Number
EV2787-0002-FP-00A	MP2787DFP-0002 (2)

Note:

2) "0002" is the register setting option that supports SPI communication with CRC disabled. For custom options, contact an MPS FAE to obtain an "xxxx" value.

QUICK START GUIDE

The EV2787-0000/0002-FP-00A are designed to evaluate the MP2787, and can be configured to support 7-cell to 16-cell series connections. These boards incorporate the MP2787, a current-sense resistor, and other components, as well as placeholders to add external transistors and balancing resistors to support >58mA of balancing current if needed. These boards include hardware monitoring alarm capability with configurable thresholds for the following conditions: over-current (OC), under-voltage (UV), over-voltage (OV), unbalanced cell, and high/low temperature conditions.

Evaluation Platform Preparation:

1. To use the evaluation platform, which includes the evaluation kit, GUI, and related components, the following is required:
   a. A computer with at least one available USB port
   b. A USB cable
   c. A USB-to-I²C communication interface (EVKT-USBI2C-02, see Figure 1) if using the EV2787-0000-FP-00A, or a USB-to-SPI communication interface (EVKT-USBSPI-00, see Figure 2) if using the EV2787-0002-FP-00A.

   The MP2787 Programming Tool must also be properly installed. This graphical user interface (GUI) software can be downloaded from the MPS website.

Figure 1: USB-to-I²C Communication Interface

Figure 2: USB-to-SPI Communication Interface

2. To install the software, double-click on the Programming tool MP2787.exe file, then open the software. The software is supported by Windows 7 and later versions.
3. Figure 3 and Figure 4 on page 5 show the original test set-up for the MP2787DFP-0000 and MP2787DFP-0002, respectively.
   a. Use the cell simulator shunt (turn the SW1 and SW2 channels on) to set up the board quickly without a real battery pack.

b. Apply a DC power supply between BATT16 (at the top of CELLS1) and BATT-, then adjust the power supply to be about 60V/1A.

c. For the EV2787-0000-FP-00A, connect the USB-to-I²C communication interface to JC1, with careful consideration regarding where SCL and SDA are positioned. For the EV2787-0002-FP-00A, connect the USB-to-SPI communication interface to JC1, with careful consideration regarding where NCS, SCK, SDO, and SDI are positioned.

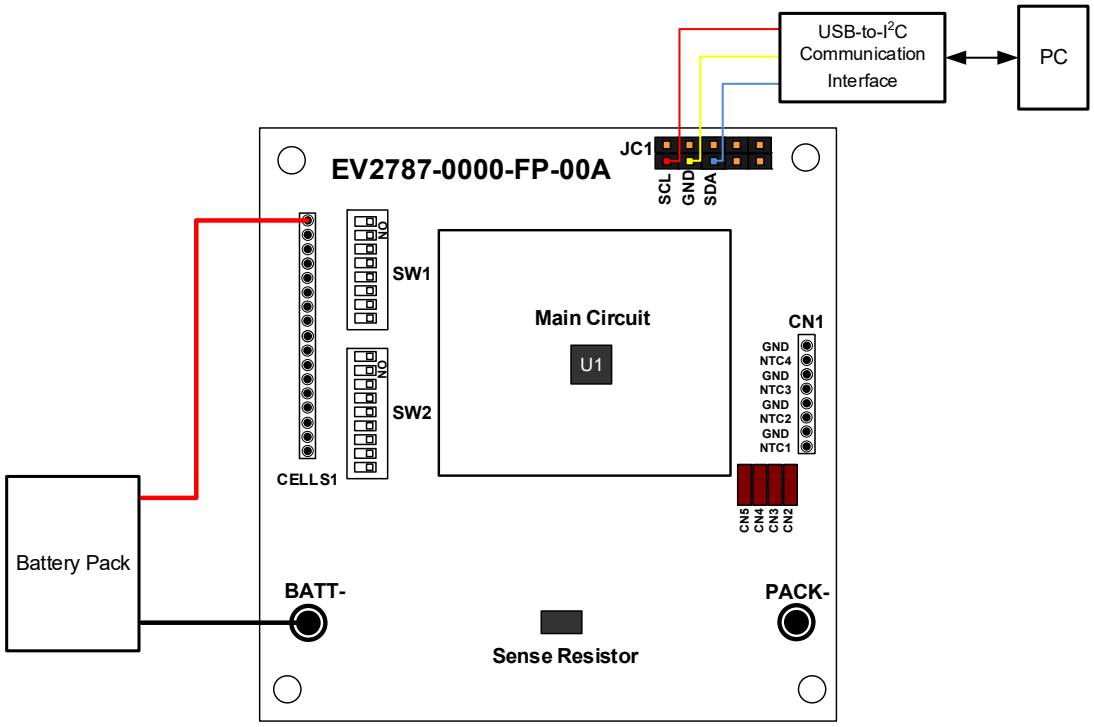


Figure 3: Test Set-Up for the MP2787DFP-0000

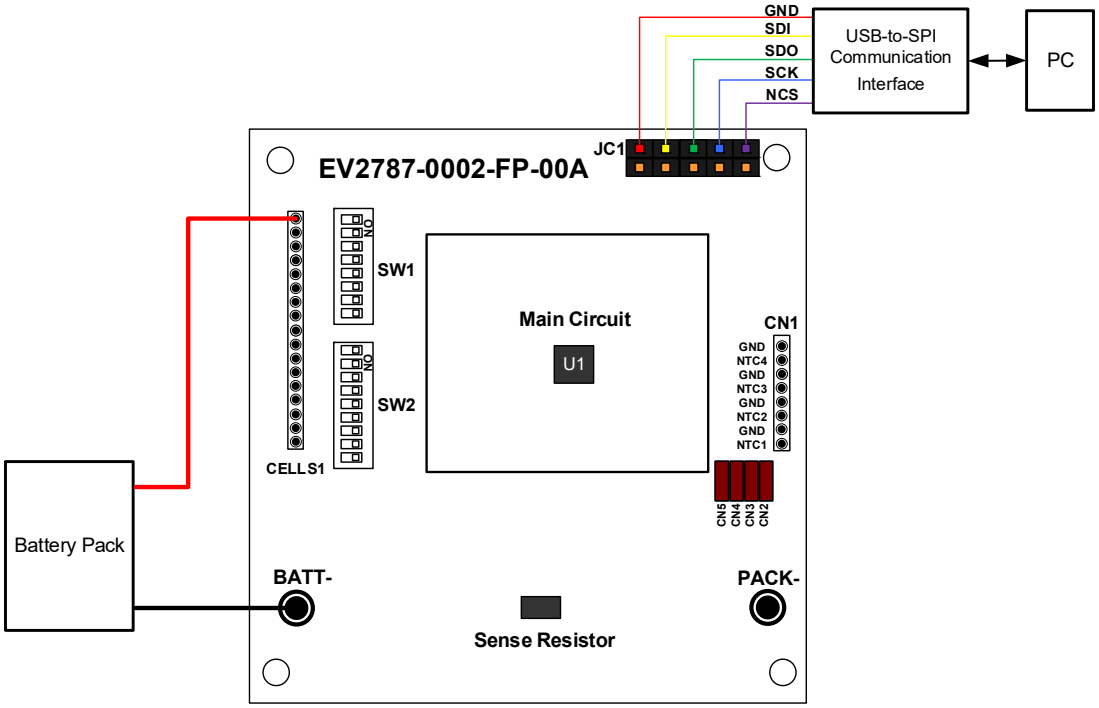


Figure 4: Test Set-Up for the MP2787DFP-0002

4. By default, this board has 16 cells in series. To use the cell simulator shunt and evaluate the device at a lower series number, short-circuit the corresponding channels. Figure 5 shows the 10-cell series connection with the cell simulator shunt. Decrease the DC power supply voltage between BATT16 and BATT- depending on the number of cells in series.

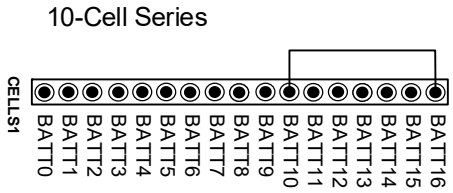


Figure 5: 10 Cells in Series Connection

5. The open-wire detection and cell-balancing functions cannot be tested using the cell simulator shunt. To evaluate these features, use a real battery pack. Figure 6 and Figure 7 on page 7 show the MP2787 test set-up with a battery pack for the EV2787-0000-FP-00A and EV2787-0002-FP-00A, respectively.

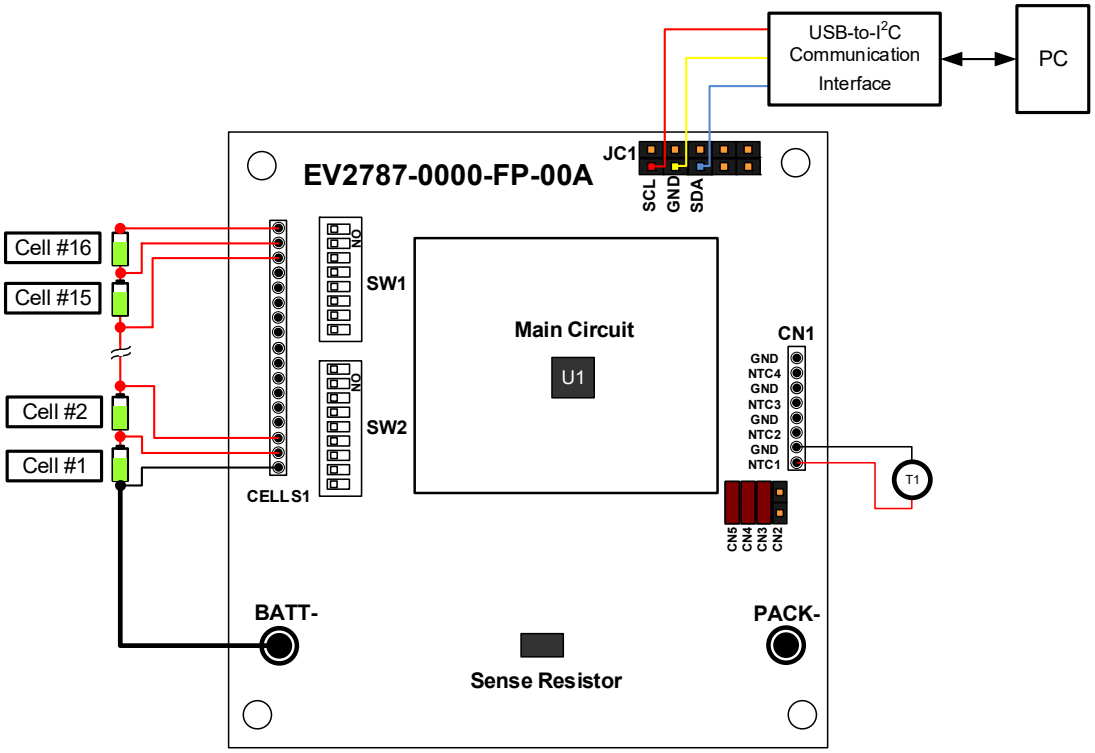


Figure 6: Test Set-Up for the MP2787DFP-0000 with a Battery Pack

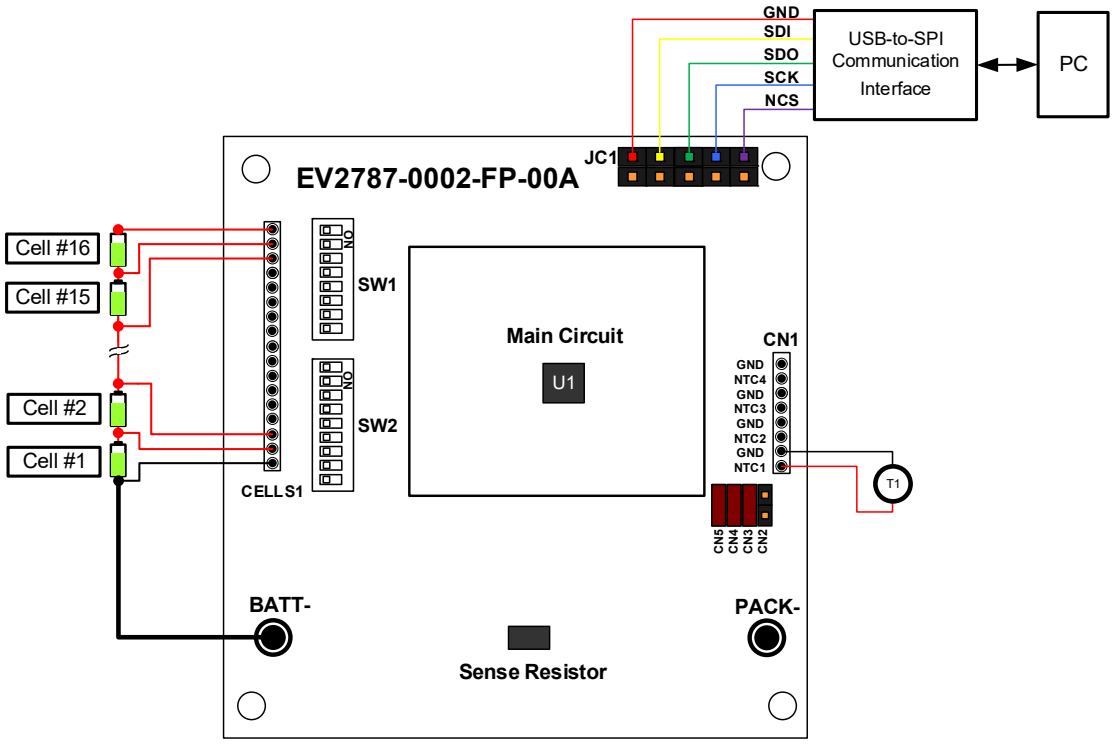


Figure 7: Test Set-Up for the MP2787DFP-0002 with a Battery Pack

6. Turn off the SW1 and SW2 channels.
7. If the application has less than 16 cells in series, use 0Ω resistors to short all unused cell channels to the practical maximum cell channel. If the application has 16 cells in series, skip this step.

   For example, if using a 10-cell series pack, add 0Ω resistors to R54, R55, R56, R57, R58, and R59.
8. Connect the cell terminals (CELLS1) to each cell-sensing point. If the number of cells in the battery pack is below 16, float the connectors' higher channels.
9. Connect the battery's negative terminals to BATT-.
10. Remove CN2, CN3, CN4, and CN5. Connect and locate the temperature sensors to support up to four NTCs.
11. Connect the charger (or the load) negative terminals to PACK-.
12. For the EV2787-0000-FP-00A, connect SDA, SCL, and GND to the USB-to-I²C communication interface, with careful consideration regarding where SCL and SDA are positioned. For the EV2787-0002-FP-00A, connect NCS, SCK, SDO, SDI and GND to the USB-to-SPI communication interface, with careful consideration regarding where NCS, SCK, SDO, and SDI are positioned.
13. Connect the USB cable to the PC, turn on the computer, and launch the MP2787 Programming Tool (GUI evaluation software). Figure 8 on page 8 shows the software's main window.

    If the previous steps are correct, "MP2787 Demo board: Connected" will be listed in the lower left corner. Otherwise, this area will read "MP2787 Demo board: Disconnected!"

Figure 8: MP2787 Programming Tool GUI Software

PROCEDURE

Ensure that all the connections (e.g. between the USB-to-I²C communication interface and the EV2787-0000-FP-00A) are successful.

1. Click the “Configuration” tab to view the configurations (see Figure 9). The software should automatically read all configurations. Items with a lock symbol can be configured as read-only.

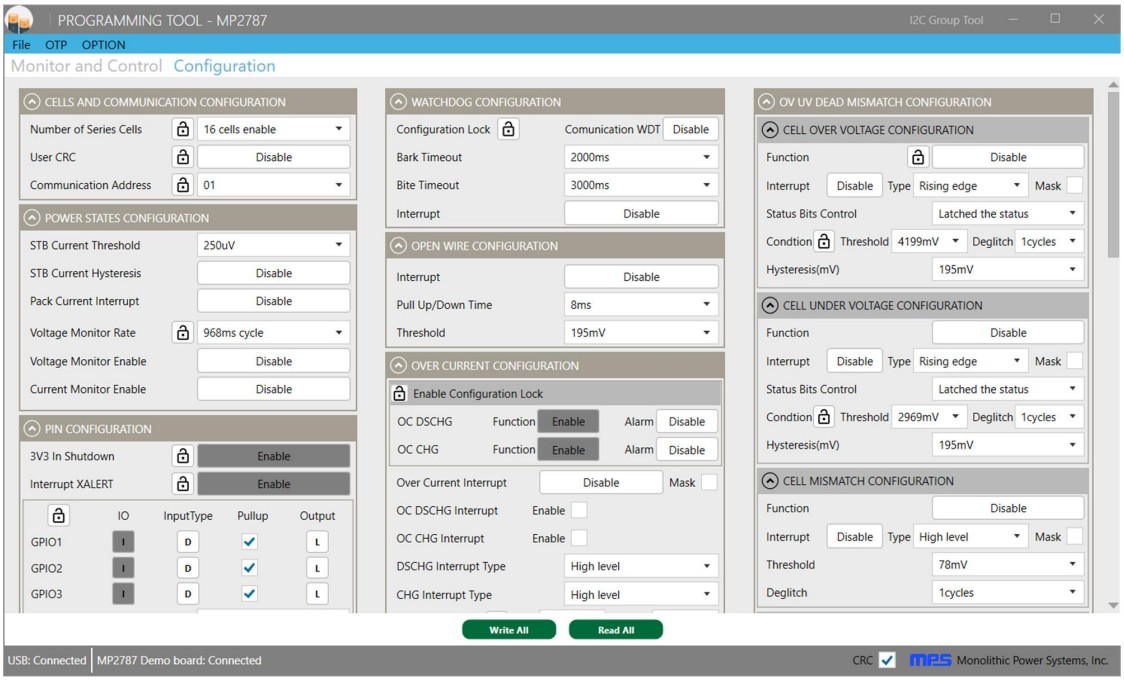


Figure 9: Configuration View

2. Configure the hardware monitoring alarm thresholds, enable all relevant functions, and set the corresponding interrupts.
3. Click the “Write All” button to write configurations to the register, then click the “Monitor and Control” tab to switch the view.
4. Click the analog-to-digital converter (ADC) scan “Go” button (see Figure 8 on page 8). The ADC result should be updated to the corresponding register.
5. Click the “Read All” button. The updated values should be displayed in the GUI. If the “Auto Read” checkbox is checked, it is not required to click the “Read All” button (see Figure 8 on page 8).
6. Figure 10 shows how to configure the cells and communication.

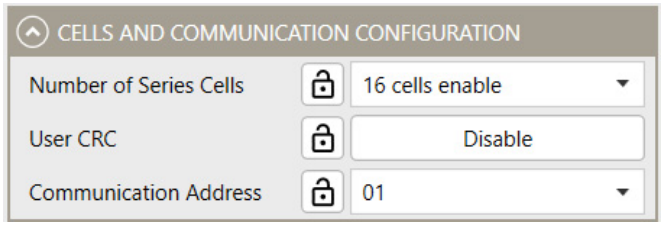


Figure 10: Cell and Communication Configuration

a. Number of Series Cells: Can be between 7 and 16.

b. User CRC: To enable cyclic redundancy check (CRC), check the “CRC” checkbox at the bottom-right of the GUI window. Otherwise, the value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address range is 00h to 7Fh. After changing this value, the new address should be used for the next communication. For devices with different “xxxx” codes, the default address may be different. The GUI automatically scans the address, though this function can be disabled by unchecking “Monitor Chip Connection” in the “OPTION” tab (see Figure 11).

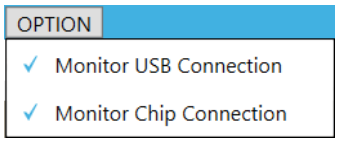


Figure 11: Option Configuration

7. Figure 12 shows how to configure the power status.

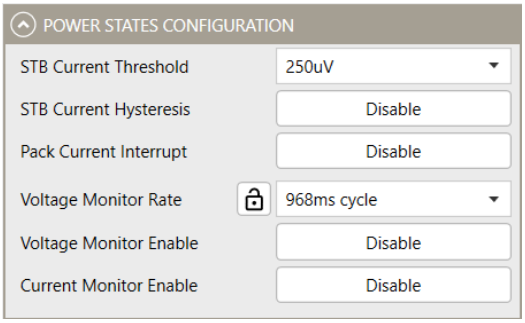


Figure 12: Power Status Configuration

a. Voltage Monitor Enable: If a hardware monitoring alarm is required, enable this function to ensure that the voltage can be monitored.

b. Voltage Monitor Rate: Can be used with voltage monitoring to refresh the ADC result. This rate can be configured to refresh the voltage reading every 254ms, 492ms, or 968ms.

8. Figure 13 shows how to configure the GPIO pins.

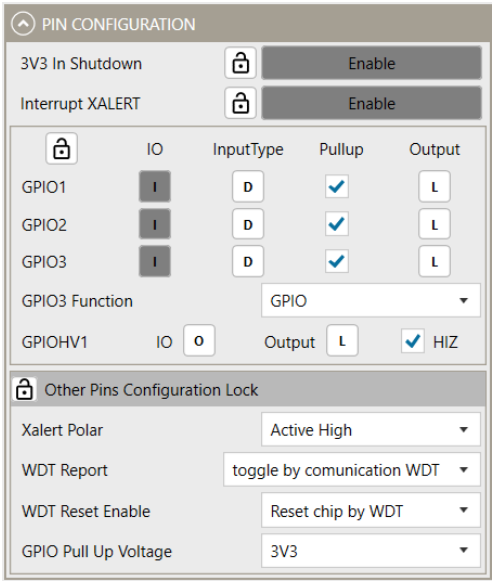


Figure 13: Pin Configuration

a. IO: The I/O setting defines whether GPIO1–3 are set to act as inputs or outputs. If they are set to inputs, they cannot be left floating and must be connected to a high or low voltage level. Otherwise, GPIO1–3 may consume excess power.

b. Input Type: Defines whether the input type for GPIO1–3 is a digital input or a buffered ADC input.

c. Pullup: Enables GPIO1–3 pull-up capability. When enabled, a 20kΩ pull-up resistance is applied.

d. Output: Sets the target output voltage level for GPIO1–3 to be high or low. This configuration bit is only effective when the corresponding GPIO is used as a digital output.

e. GPIO3 Function (I^2C version only): GPIO3 can be configured as a GPIO or OC alarm. This configuration is only valid when GPIO3 is set as an output.

f. GPIOHV1: Sets the GPIOHV1's target voltage level to be high or low. This configuration bit is only effective when GPIOHV1 is used as a digital output and GPIOHV1_HZ = 0. If "HIZ" is selected, then GPIOHV1 operates in Hi-Z mode.

g. GPIO Pull Up Voltage: Sets the GPIO pull-up voltage to the 3V3 or REGIN pin.

9. Figure 14 shows how to configure the ADC scan parameters.

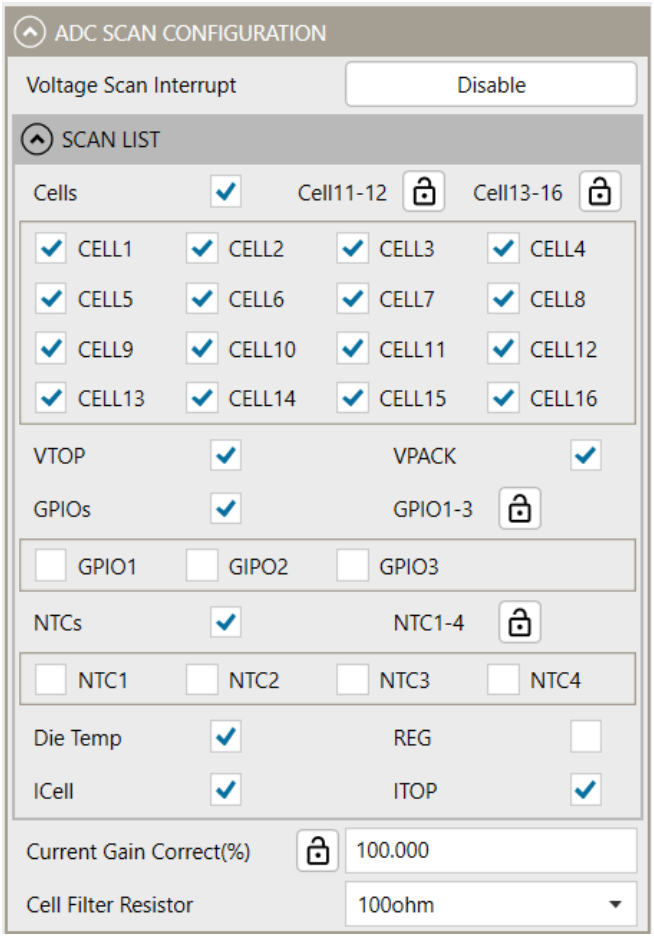


Figure 14: ADC Scan Configuration

a. Select a checkbox to enable the related parameter. If a parameter is enabled, that parameter is read and updated during the high-resolution voltage ADC (VADC) scan. If disabled, the parameter is excluded from the high-resolution VADC scan.

b. Current Gain Correct(%): Compensates for the current-sense resistor and surface-mount technology (SMT) variation. The correction is applied to both Coulomb counting and synchronous current ADC readings. The correction is not applied to OC detection. The configuration range is 87.5% to 112.476%.

c. Cell Filter Resistor: The default value is 100Ω, and the ADC cell readings are not compensated. This configuration should be set to 1kΩ when a 1kΩ filtering resistor is used (e.g. for external MOSFET balancing), which compensates for the ADC cell readings to remove the drop caused by the input current during ADC conversion.

10. Figure 15 shows how to configure the watchdog.

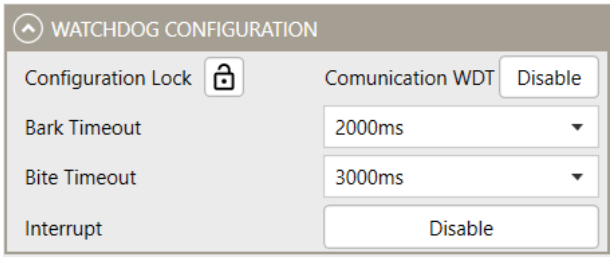


Figure 15: Watchdog Configuration

a. Bark Timeout: Defines the delay from the last watchdog reset to the bark, which ranges from 25ms to 3200ms.

b. Bite Timeout: Defines the delay from the bark to bite, which ranges from 25ms to 3200ms.

11. Figure 16 shows how to configure open-wire parameters.

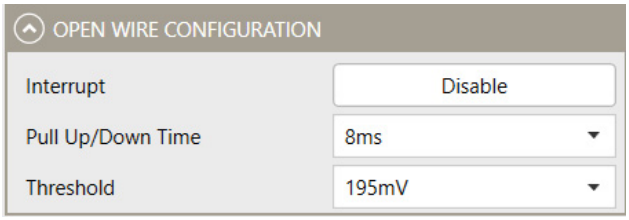


Figure 16: Open-Wire Configuration

a. Pull Up/Down Time: Sets the length of each pull-up and pull-down phase, which ranges from 1ms to 16ms.

b. Threshold: Sets the open-wire threshold used in the detection sequence, which ranges from 39mV to 625mV.

12. Figure 17 shows how to configure Coulomb counting.

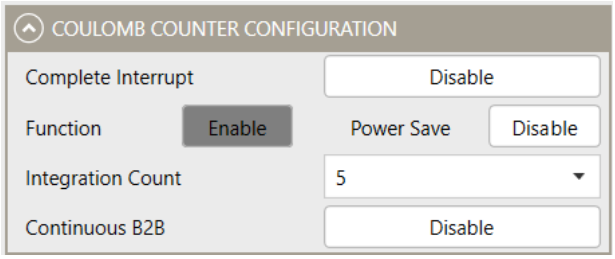


Figure 17: Coulomb Counting Configuration

a. Power Save: If enabled, the Coulomb counter operates in power-save mode; if disabled, power-save mode is not used. Power-save mode reduces overall current consumption at the expense of accuracy.

b. Integration Count: Sets the Coulomb counter integration length. The length sets the number of time slots, which are each 32ms. This register should only be updated when Coulomb counting is not active. It ranges from 1 (32ms) to 64 (2048ms).

c. Continuous B2B: Enables back-to-back accumulation mode. When enabled, a new Coulomb counting conversion starts automatically after the most recent conversion is complete.

13. Figure 18 shows how to configure the OC parameters.

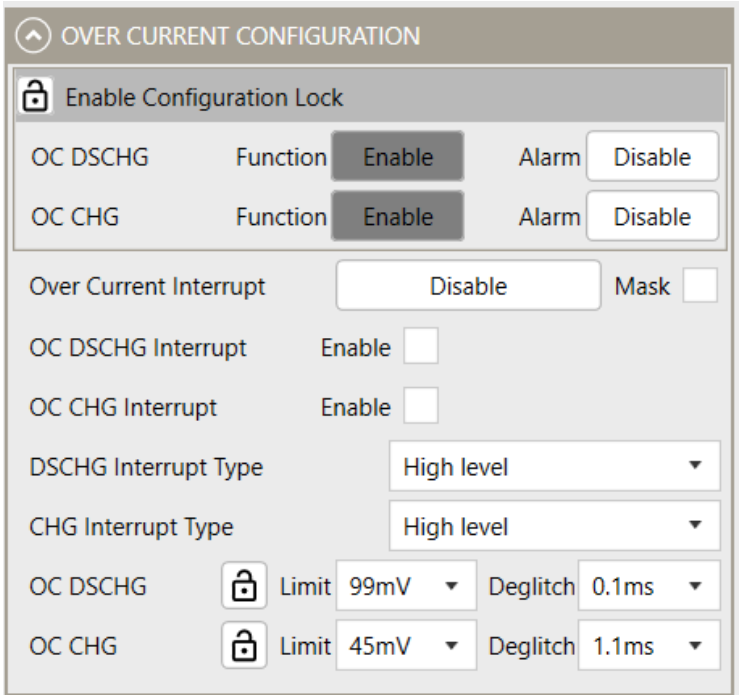


Figure 18: Over-Current (OC) Configuration

a. Select the “Over Current Interrupt Mask” checkbox to enable the related function. When enabled, the OC interrupt flag is cleared, and the interrupt pin goes low unless other interrupts are pending. When disabled, an OC condition can trigger the interrupt flag.

b. OC DSCHG Limit: The OC discharge limit 1x range is 5.5mV to 176mV, and the 3x range is 16.5mV to 528mV.

c. OC DSCHG Deglitch: The OC discharge deglitch time ranges from 0.1ms to 25.5ms. The response time is about 100μs after an OC condition is detected.

d. OC CHG Limit: The OC charge limit 1x range is 2.5mV to 80mV, and the 3x range is 7.5mV to 240mV.

e. OC CHG Deglitch: The OC charge deglitch time ranges from 0.1ms to 25.5ms. The response time is about 100μs after an OC condition is detected.

14. Figure 19 shows how to configure the negative temperature coefficient (NTC).

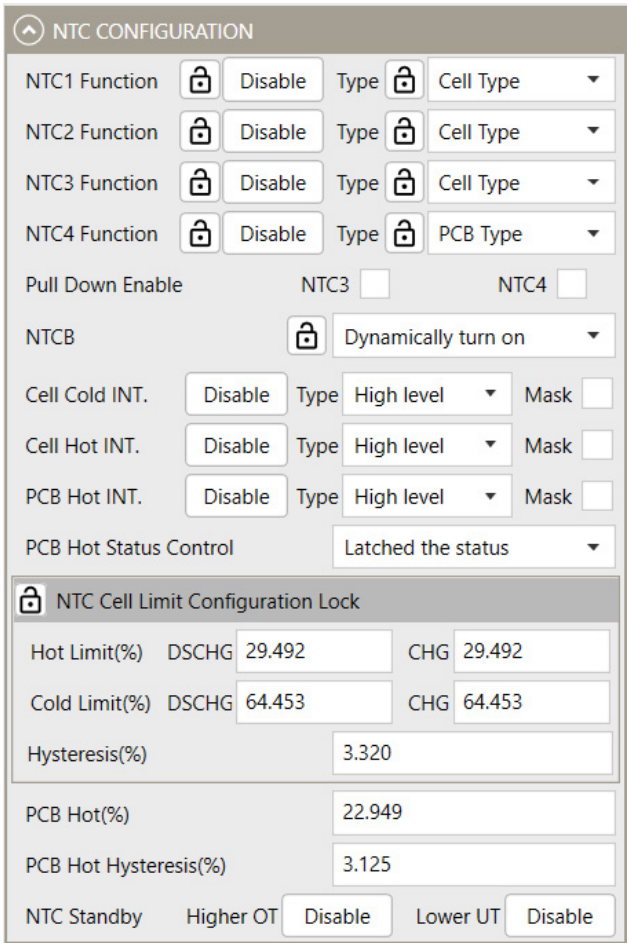


Figure 19: NTC Configuration

a. NTCx Type: The type for NTC1–4 can be set to cell monitor (“Cell Type”) or PCB monitor (“PCB Type”).

b. Pull Down Enable: Enables NTC3 and NTC4 to be pulled down.

c. NTCB: The NTCB pin is set to be enabled dynamically. NTCB is dynamically biased during ADC conversions of the NTC channels; if NTCB remains on continuously, current consumption increases.

d. PCB Hot Status Control: Can be set to show the latched status (which goes to the interrupt controller) or the real-time status.

e. NTC Cell Limit(%): The NTC hot and cold limits can be set to be between 0% and 99.9% of the NTCB value.

f. Hysteresis(%): The hysteresis threshold can be set to be between 0% and 6.055% of the NTCB value.

g. Higher Over-Temperature (OT): Defines the selection criteria for the NTC hot threshold when the battery pack current is within the standby current threshold. If disabled, select the hotter threshold; if enabled, select the colder threshold.

h. Lower Under-Temperature (UT): Defines the selection criteria for the NTC cold threshold when the battery pack current is within the standby current threshold. If disabled, select the colder threshold; if enabled, select the hotter threshold.

15. Figure 20 shows how to configure the die temperature parameters.

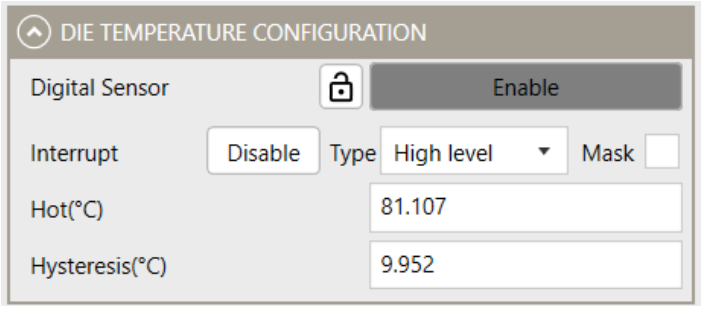


Figure 20: Die Temperature Configuration

a. Hot(°C): The resolution is 0.474°C.

b. Hysteresis(°C): Can be set between 0°C and 14.692°C.

16. Figure 21 shows how to configure the cell-balancing parameters.

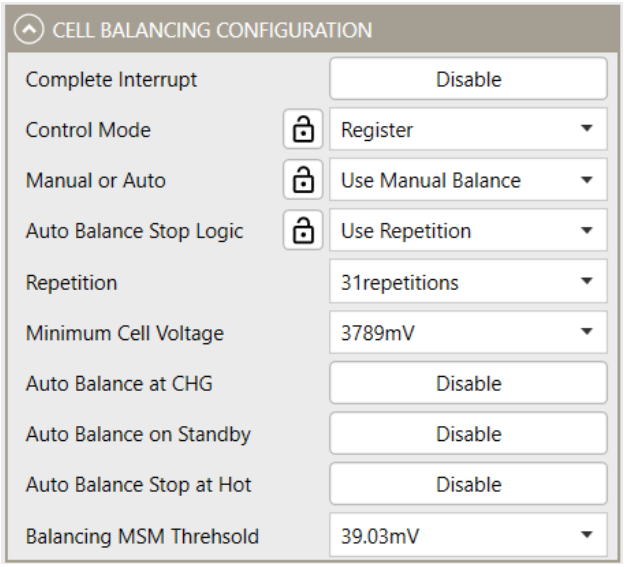


Figure 21: Cell-Balancing Configuration

a. Control Mode: Can be set to register control or GPIO3 control when using automatic balancing. This feature is only available on I^2C versions of the MP2787.

b. Manual or Auto: Controls the balancing mode, which can be configured for manual balancing or automatic balancing.

c. Auto Balance Stop Logic: Only used when automatic balancing is enabled. If set to "Use Repetition," then balancing uses repetition to control the number of balance iterations. If set to "Use List," then balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, disable this bit.

d. Repetition: Sets the number of repetitions for each execution of the balancing list, ranging between 0 and 31 repetitions. If 31 repetitions are selected, 32 balancing cycles are executed.

e. Minimum Cell Voltage: Sets the qualifying minimum cell voltage (V_{CELL}) to run automatic balancing, ranging between 2500mV and 4961mV. When a cell is below this level, it is excluded from the balancing list. All other qualifying cells are balanced if they meet the criteria.

f. Balancing MSM Threshold: This value is used by the automatic balancing algorithm, and ranges from 19.5mV to 87.85mV.

17. Figure 22 shows how to configure the cell over-voltage (OV) parameters.

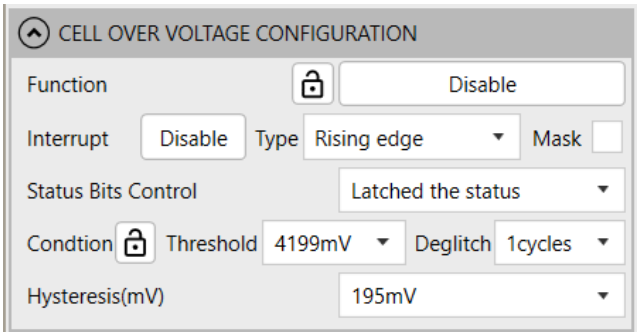


Figure 22: Cell OV Configuration

a. Threshold: The cell OV threshold ranges from 0mV to 4980.15mV.

b. Hysteresis(mV): The OV hysteresis ranges from 0mV to 292.5mV.

18. Figure 23 shows how to configure the cell under-voltage (UV) parameters.

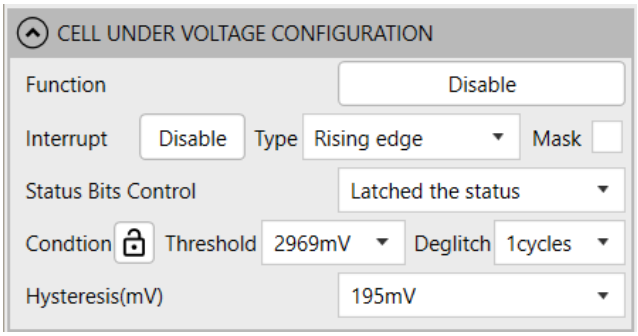


Figure 23: Cell UV Configuration

a. Threshold: The cell UV threshold ranges from 0mV to 4980.15mV.

b. Hysteresis (mV): The UV hysteresis ranges from 0mV to 292.5mV.

19. Figure 24 shows how to configure the cell mismatch parameters.

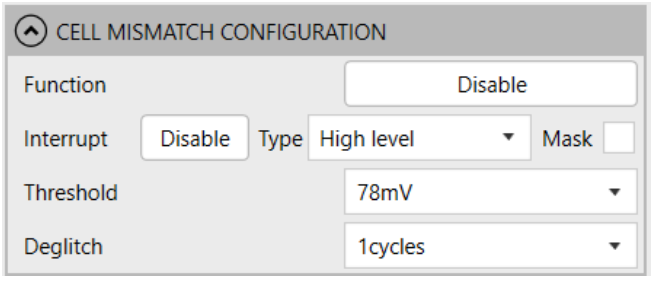


Figure 24: Cell Mismatch Configuration

a. Threshold: The cell mismatch threshold ranges from 0mV to 1211mV.

20. Figure 25 shows how to configure the cell dead parameters.

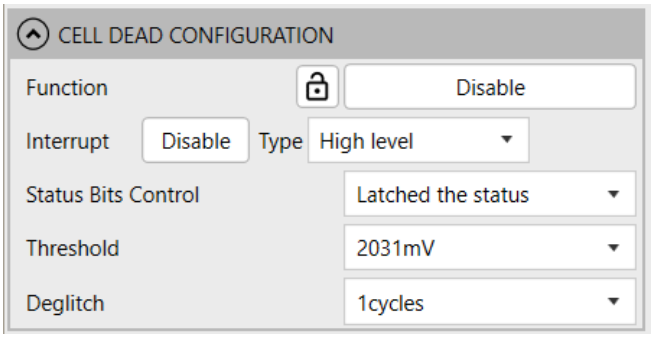


Figure 25: Cell Dead Configuration

a. Threshold: The cell dead threshold ranges from 0mV to 2480mV.

21. Figure 26 shows how to configure the VTOP pin's UV parameters.

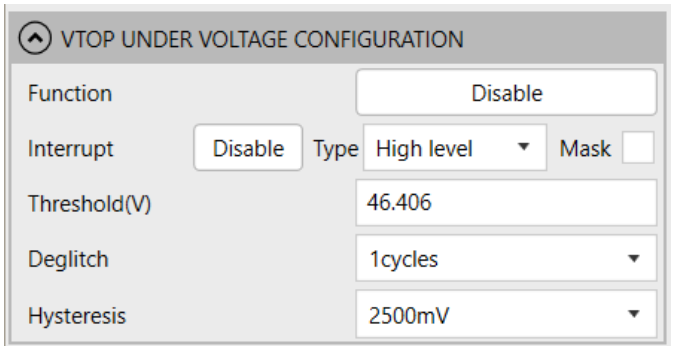


Figure 26: VTOP UV Configuration

a. Threshold(V): The VTOP UV threshold ranges from 0V to 79.98V.

b. Hysteresis: Ranges from 0mV to 4922mV.

22. Figure 27 shows how to configure the VTOP OV parameters.

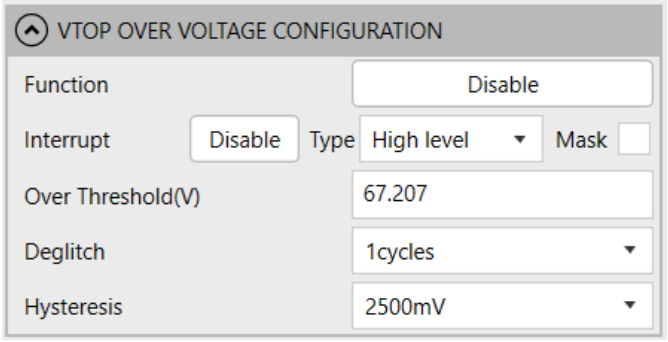


Figure 27: VTOP OV Configuration

a. OV Threshold(V): The VTOP OV threshold ranges from 0V to 79.98V.

b. Hysteresis: Ranges from 0mV to 4922mV.

23. Figure 28 shows how to configure the REGIN, 3V3, VDD, and ADC self-test check.

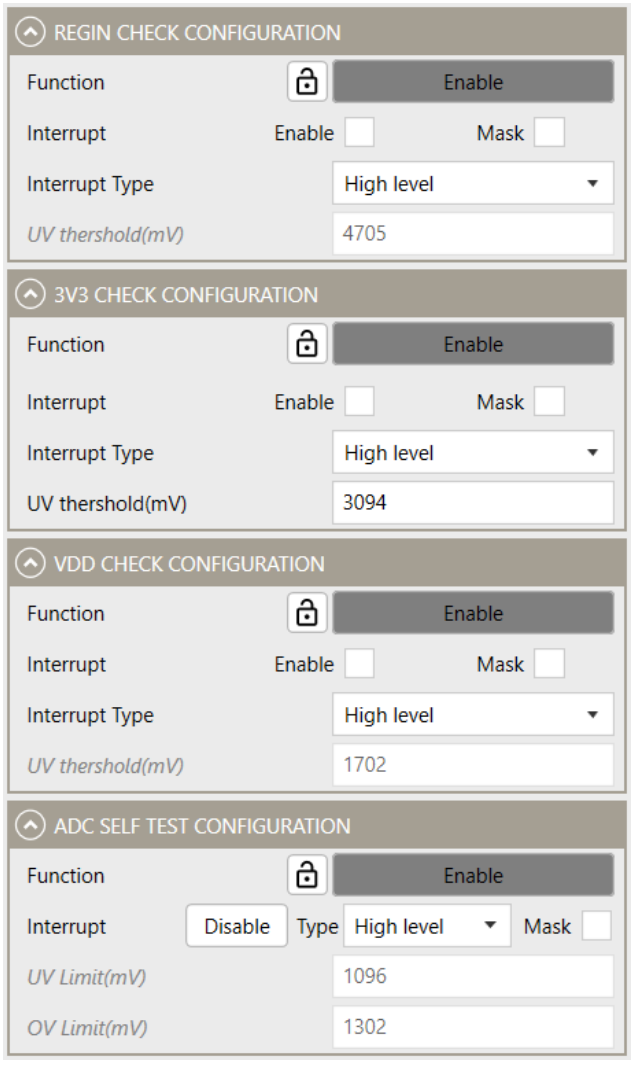


Figure 28: REGIN, 3V3, VDD, and ADC Self-Test Check Configuration

24. Figure 29 shows how to configure the one-time programmable (OTP) memory cyclic redundancy check (CRC).

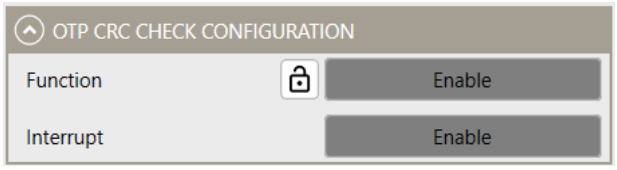


Figure 29: OTP CRC Configuration

25. Figure 30 shows the status monitor.

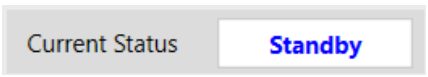


Figure 30: Status Monitor

26. Figure 31 shows the scheduler and command monitor.

Figure 31: Scheduler and Command Monitor

27. Figure 32 shows the watchdog status monitor.

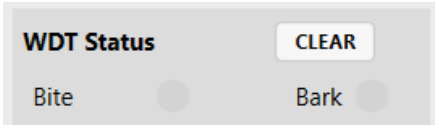


Figure 32: Watchdog Status Monitor

28. Figure 33 shows how to configure the ADC, cell-balancing, and open-wire control parameters.

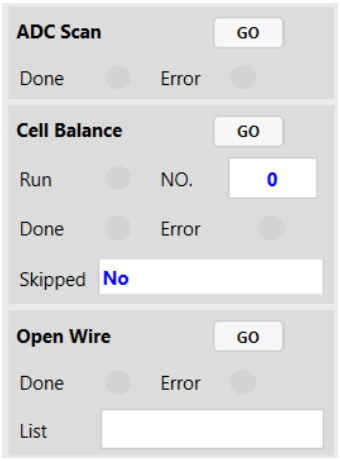


Figure 33: ADC, Cell-Balancing, and Open-Wire Control and Monitor Configuration

29. Figure 34 shows the OC status monitor.

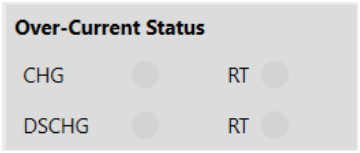


Figure 34: Over-Current Status Monitor

30. Figure 35 shows the GPIO and VTOP status monitor.

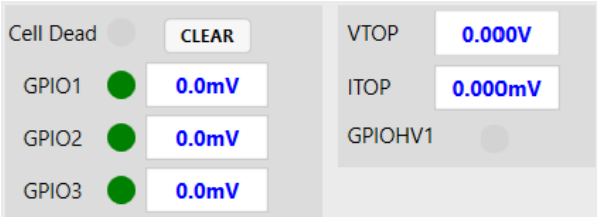


Figure 35: GPIO and VTOP Status Monitor

31. Figure 36 shows the die temperature monitor.

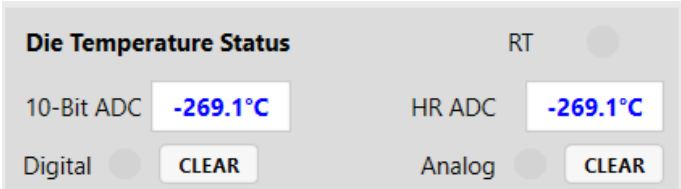


Figure 36: Die Temperature Monitor

32. Figure 37 shows the OTP CRC monitor.

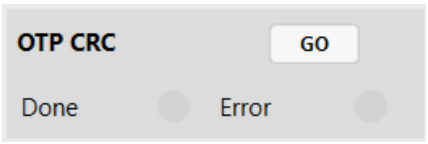


Figure 37: OTP CRC Monitor

33. Figure 38 shows the NTC monitor.

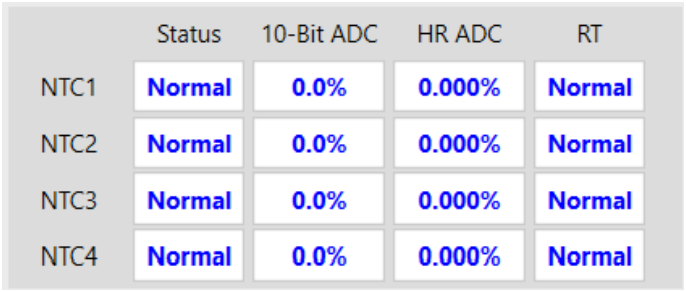


Figure 38: NTC Monitor

Figure 39 shows the NTC functional block.

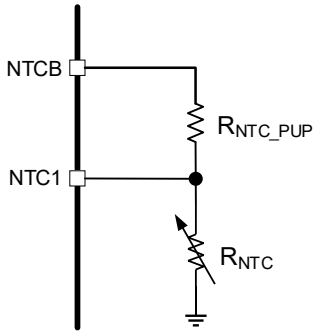


Figure 39: NTC Functional Block

The NTC resistance (R_{NTC}) can be estimated using Equation (1):

$$R_{NTC}=\frac{A \times R_{NTC\_PUP}}{32768 - A} \quad (1)$$

Where A is the NTC ADC reading, and R_{NTC_PUP} is the NTC pull-up resistance (10kΩ is recommended).

The ambient temperature (T, in Kelvin) can be calculated using Equation (2):

$$T=\frac{1}{\frac{1}{T_0}+\frac{1}{B}\ln\frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is the NTC resistor value when the ambient temperature is T_0 (in Kelvin), and B is the thermistor constant (in Kelvin).

For example, if the NTC ADC reading (A) is 9830 (0x2666) for the NCP18XH103 thermistor, R_0 is 10kΩ at 25°C (298.15K), and B is 3380K, then R_{NTC} = 4.285kΩ and T = 322K. This means that if the NTC ADC reading is 9830, then the ambient temperature (T_A) is about 49°C.

34. Figure 40 shows the low-dropout (LDO) monitor.

	Status	10-Bit ADC	HR ADC
VDD	Normal	0.0mV	0.0mV
3V3	Normal	0.0mV	0.0mV
REGIN	Normal	0.0mV	0.0mV
Self	Normal	0.0mV	

Figure 40: LDO Monitor

35. Figure 41 shows the cell ADC monitor.

	Voltage	Current	UV	OV	MS	Dead	BAL
Cell1	0.0mV	0.000mV					
Cell2	0.0mV	0.000mV					
Cell3	0.0mV	0.000mV					
Cell4	0.0mV	0.000mV					
Cell5	0.0mV	0.000mV					
Cell6	0.0mV	0.000mV					
Cell7	0.0mV	0.000mV					
Cell8	0.0mV	0.000mV					
Cell9	0.0mV	0.000mV					
Cell10	0.0mV	0.000mV					
Cell11	0.0mV	0.000mV					
Cell12	0.0mV	0.000mV					
Cell13	0.0mV	0.000mV					
Cell14	0.0mV	0.000mV					
Cell15	0.0mV	0.000mV					
Cell16	0.0mV	0.000mV					

Figure 41: Cell ADC Monitor

EVALUATION BOARD SCHEMATIC

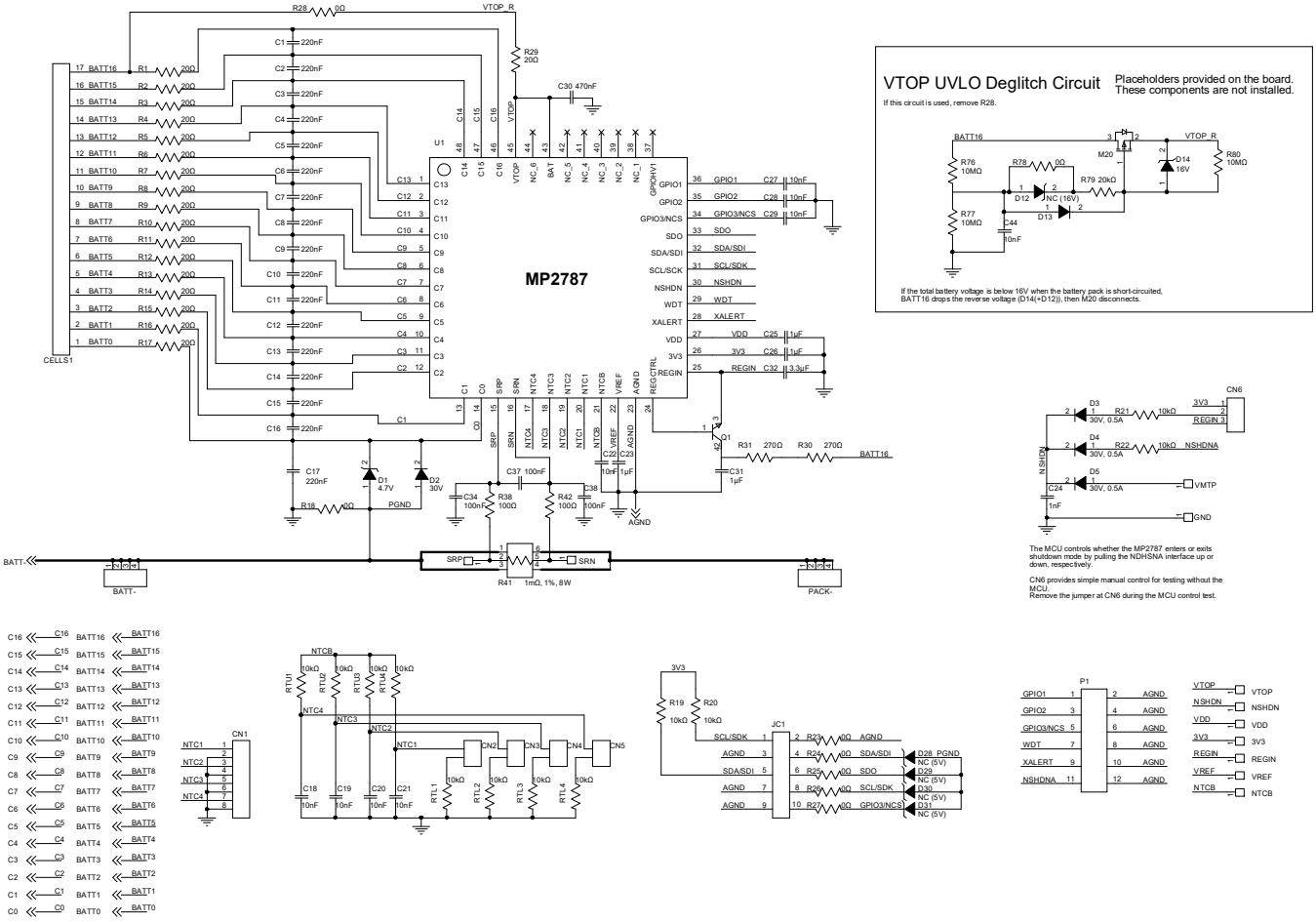


Figure 42: Evaluation Board Schematic (IC and Connector)

EVALUATION BOARD SCHEMATIC *(continued)*

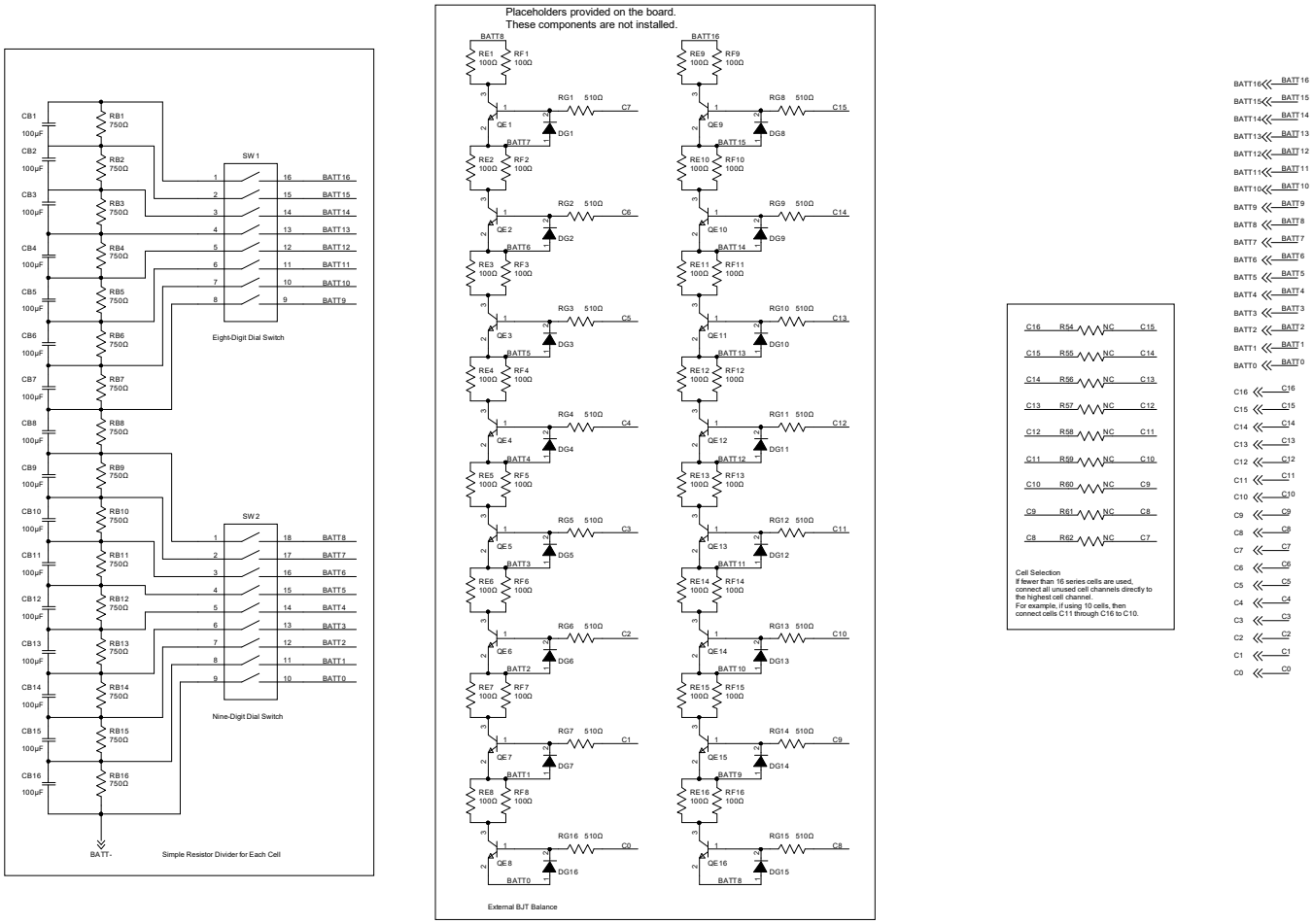


Figure 43: Evaluation Board Schematic (Battery Connection)

EV2787-0000-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	PACK-, BATT-	12mmx 18mm	Connector	DIP	Zhengyou	ZY_50
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
4	CN2, CN3, CN4, CN5	2.54mm	2-pin connector	DIP	Any	
1	CN6	2.54mm	3-pin connector	DIP	Any	
1	CELLS1	3.5mm	17-pin connector	DIP	Kefa	KF2EDGR-3.5-17P
1	JC1	2.54mm	2-row, 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2-row, 6-pin connector	DIP	Any	
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
1	C24	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
1	C31	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
3	C34, C37, C38	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	D1	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
1	Q1	100V	Transistor, 6A, 3W	SOT-223	Zetex	FZT853TA
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
12	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL

EV2787-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
2	R18, R28	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Film resistor, 1%	SMD	Bourns	CSS2H-3920R-1L00F
1	SW1	8 pins	8-pin button switch	SMD	Wurth	418121270808
1	SW2	9 pins	9-pin button switch	SMD	Wurth	418121270809
1	U1	MP2787	7-cell to 16-cell, high-accuracy battery monitor IC	TQFP-48 (7mmx 7mm)	MPS	MP2787DFP-0000

EV2787-0002-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	PACK-, BATT-	12mmx 18mm	Connector	DIP	Zhengyou	ZY_50
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
4	CN2, CN3, CN4, CN5	2.54mm	2-pin connector	DIP	Any	
1	CN6	2.54mm	3-pin connector	DIP	Any	
1	CELLS1	3.5mm	17-pin connector	DIP	Kefa	KF2EDGR-3.5-17P
1	JC1	2.54mm	2-row, 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2-row, 6-pin connector	DIP	Any	
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
1	C24	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
1	C31	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
3	C34, C37, C38	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	D1	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
1	Q1	100V	Transistor, 6A, 3W	SOT-223	Zetex	FZT853TA
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
12	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL

EV2787-0002-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
7	R18, R23, R24, R25, R26, R27, R28	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Film resistor, 1%	SMD	Bourns	CSS2H-3920R-1L00F
1	SW1	8 pins	8-pin button switch	SMD	Wurth	418121270808
1	SW2	9 pins	9-pin button switch	SMD	Wurth	418121270809
1	U1	MP2787	7-cell to 16-cell, high-accuracy battery monitor IC	TQFP-48 (7mmx 7mm)	MPS	MP2787DFP-0002

EV2787-0000/0002-FP-00A BILL OF MATERIALS

Recommended components for external BJT balance circuit (components not installed on standard board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
16	QE1, QE2, QE3, QE4, QE5, QE6, QE7, QE8, QE9, QE10, QE11, QE12, QE13, QE14, QE15, QE16	80V	Transistor, 0.5A	SOT-23	onsemi	MMBTA06LT1G
32	RF1, RE1, RF2, RE2, RF3, RE3, RF4, RE4, RF5, RE5, RF6, RE6, RF7, RE7, RF8, RE8, RF9, RE9, RF10, RE10, RF11, RE11, RF12, RE12, RF13, RE13, RF14, RE14, RF15, RE15, RF16, RE16	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
16	RG1, RG2, RG3, RG4, RG5, RG6, RG7, RG8, RG9, RG10, RG11, RG12, RG13, RG14, RG15, RG16	510Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07510RL
16	DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG8, DG9, DG10, DG11, DG12, DG13, DG14, DG15, DG16	75V	Diode, 0.15A	SOD-323	JCET	1N4148WS

EV2787-0000/0002-FP-00A BILL OF MATERIALS

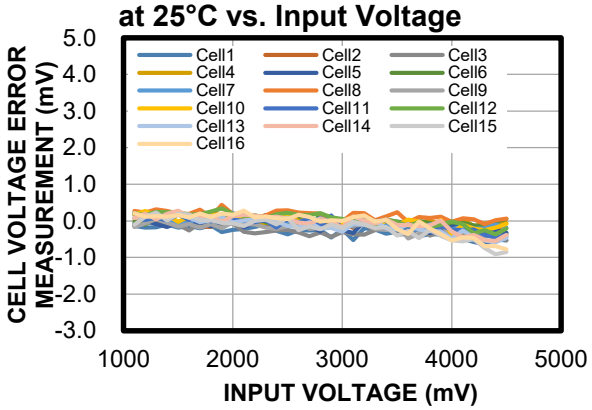
Recommended components for VTOP UVLO deglitch circuit (components not installed on standard board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	M20	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	D12, D14	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D13	75V	Diode, 0.15A	SOD-323	JCET	1N4148WS
3	R76, R77, R80	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
1	R78	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	R79	20kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720KL
1	C44	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03

EVB TEST RESULTS

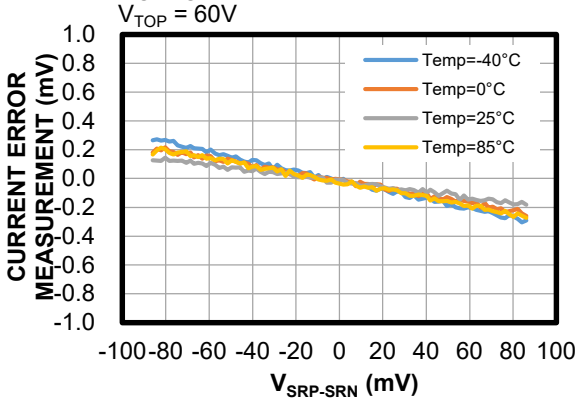
Performance curves are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Cell Voltage Error Measurement at 25°C vs. Input Voltage



Current Error Measurement vs. $V_{SRP-SRN}$

V_{TOP} = 60V



PCB LAYOUT (EV2787-0000-FP-00A)

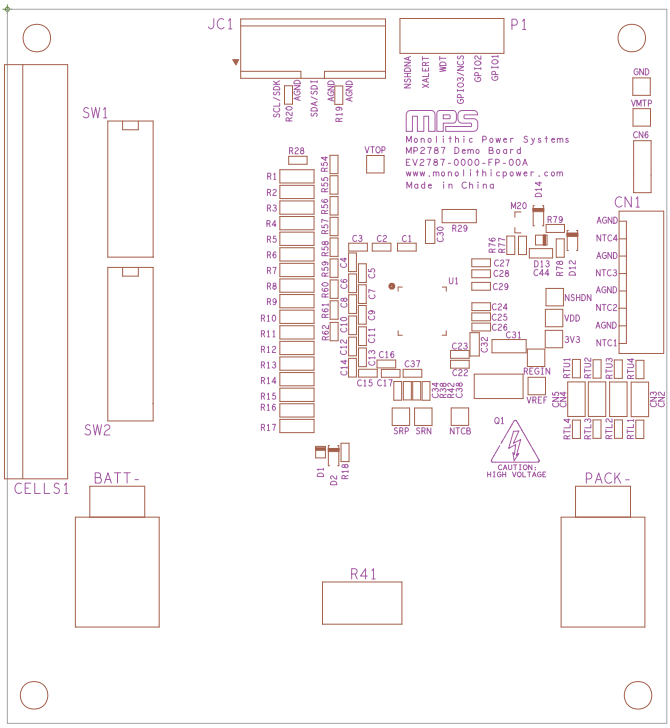


Figure 44: Top Silk

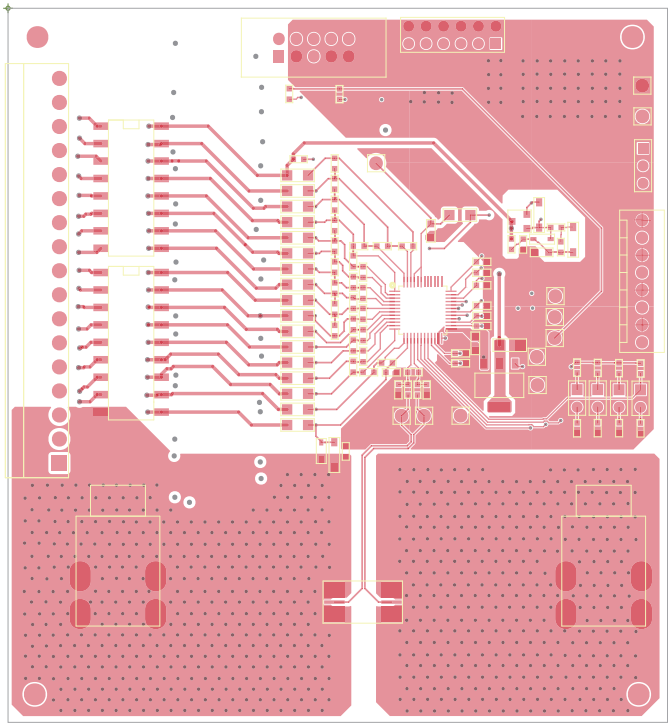


Figure 45: Top Layer

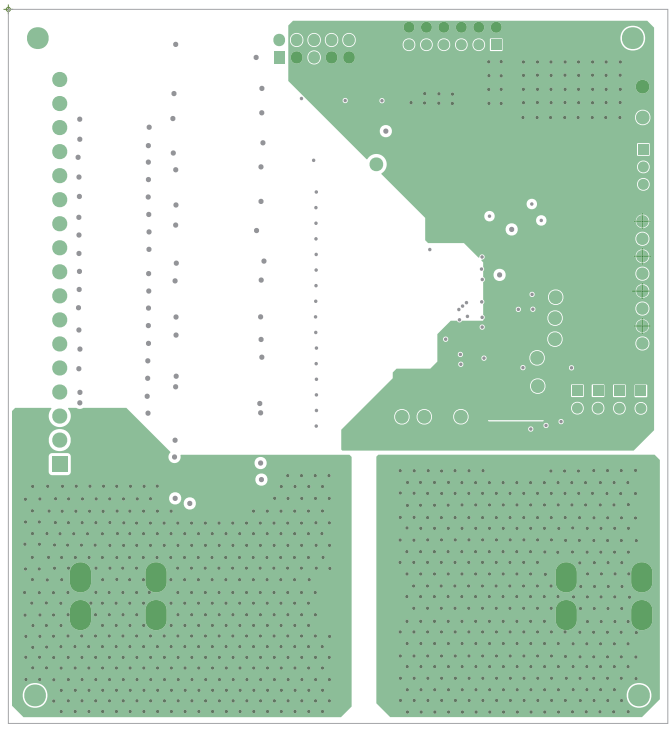


Figure 46: Mid-Layer 1

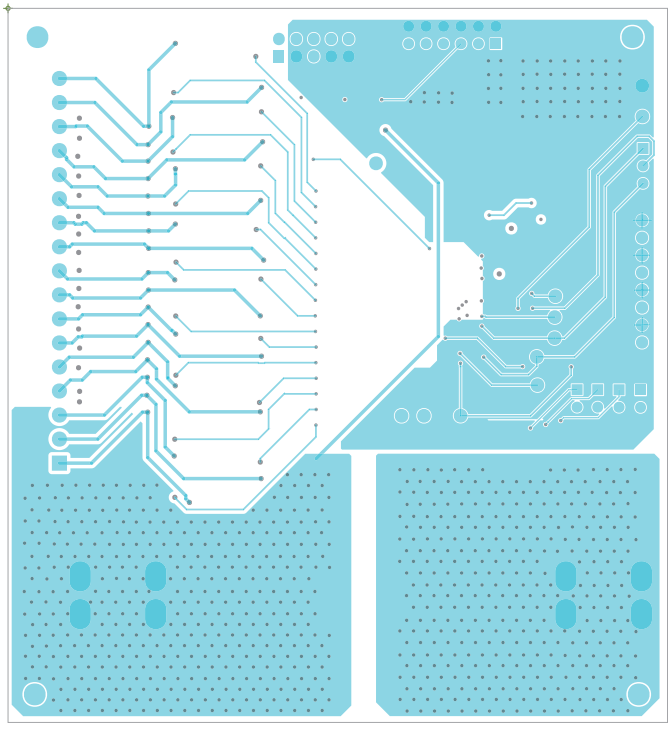


Figure 47: Mid-Layer 2

PCB LAYOUT (EV2787-0000-FP-00A) *(continued)*

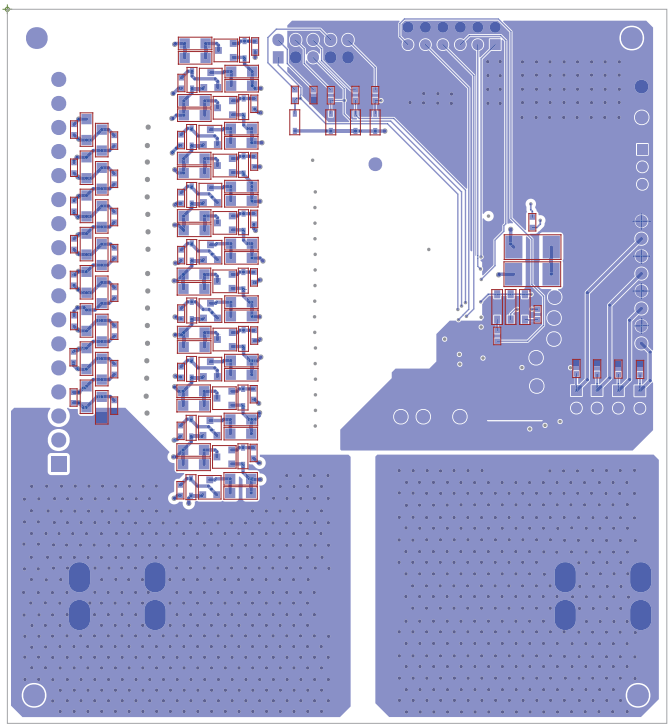


Figure 48: Bottom Layer

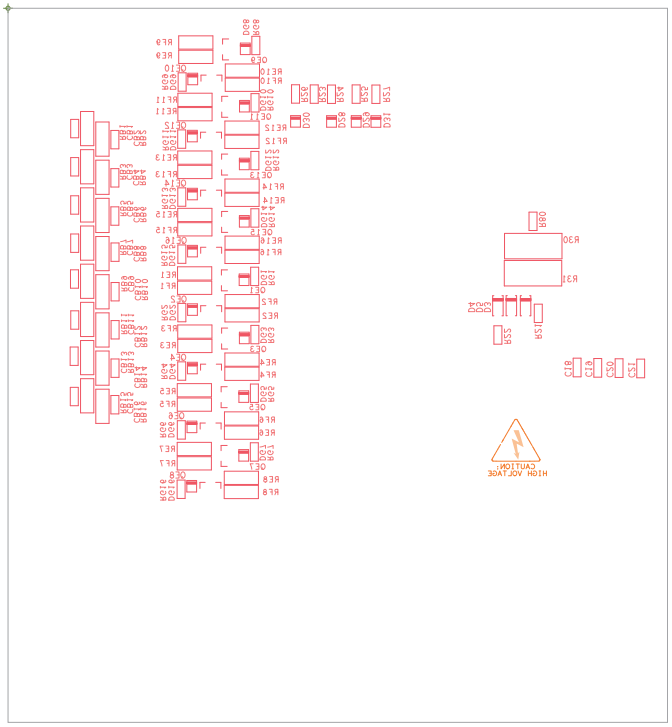


Figure 49: Bottom Silk

PCB LAYOUT (EV2787-0002-FP-00A)

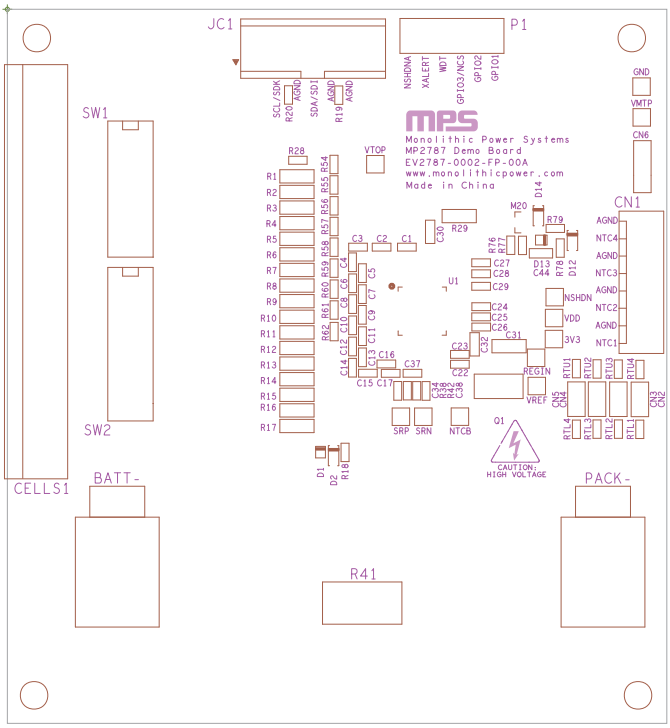


Figure 50: Top Silk

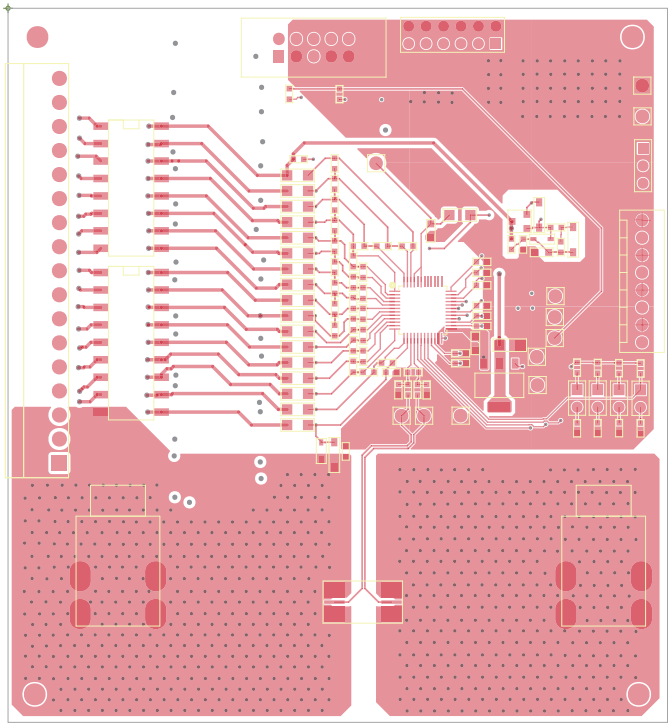


Figure 51: Top Layer

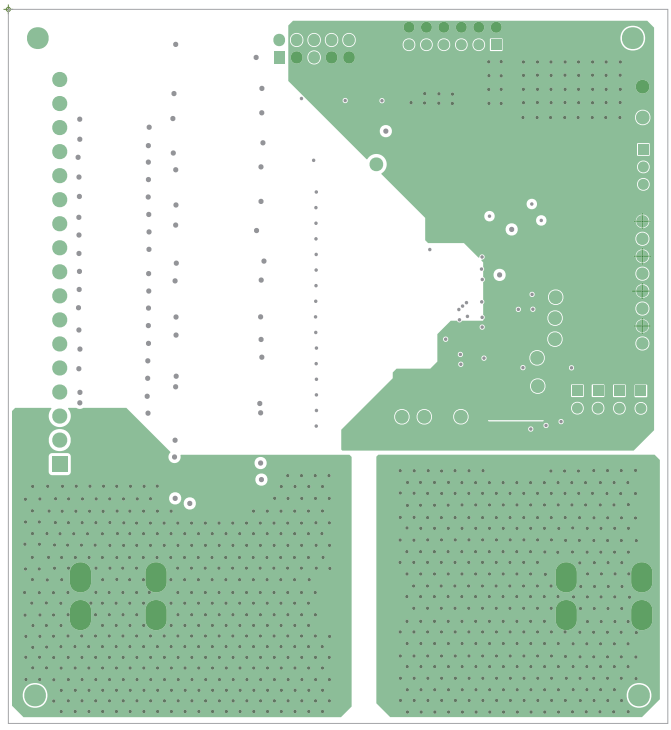


Figure 52: Mid-Layer 1

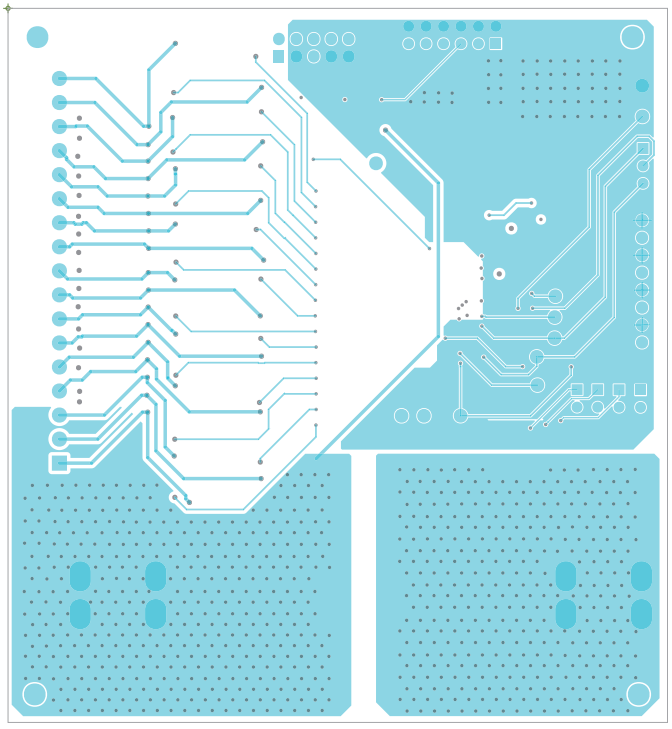


Figure 53: Mid-Layer 2

PCB LAYOUT (EV2787-0002-FP-00A) *(continued)*

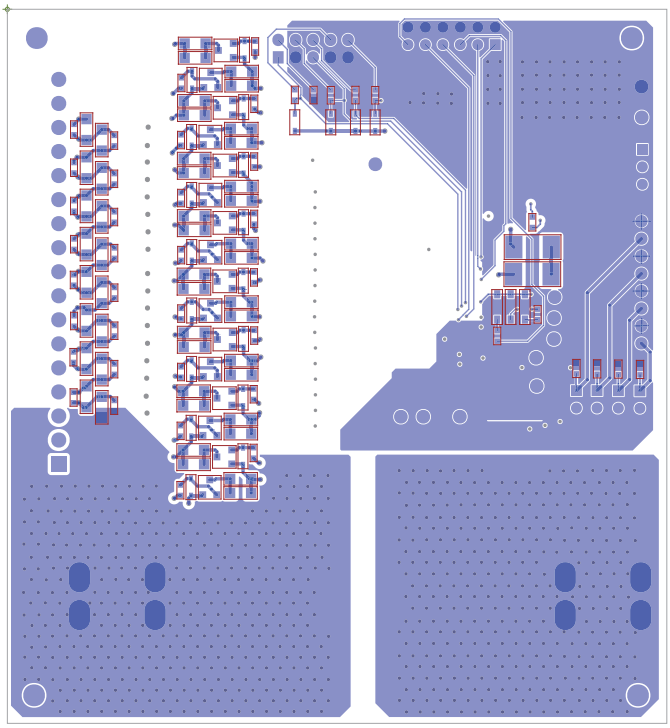


Figure 54: Bottom Layer

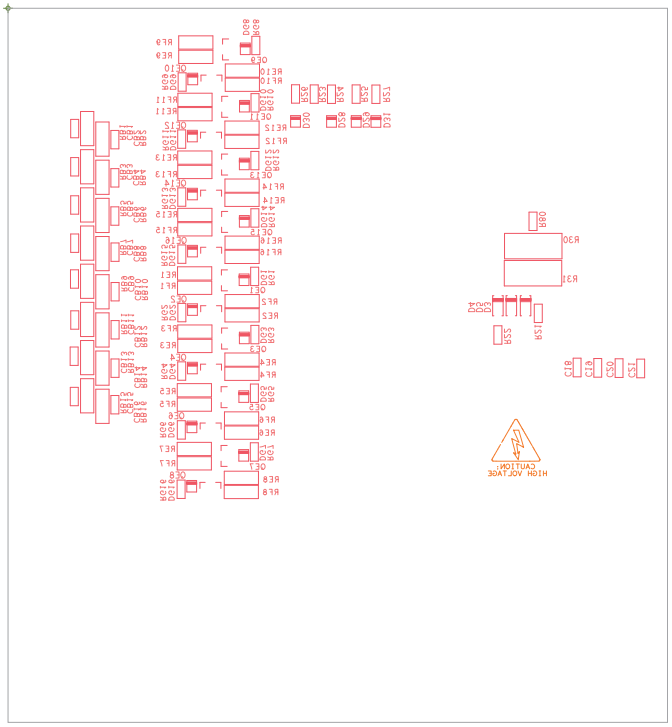


Figure 55: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/27/2023	Initial Release	-