ES_LPC407x/8x

Errata sheet LPC407x/8x

Rev. 2 — 3 June 2014 **Errata sheet**

Document information

Info	Content
Keywords	LPC4088FBD208; LPC4088FET208; LPC4088FET180; LPC4088FBD144; LPC4078FBD208; LPC4078FET208; LPC4078FET180; LPC4078FBD144; LPC4078FBD80; LPC4076FET180; LPC4076FBD144; LPC4074FBD144; LPC4074FBD80; LPC4072FBD80, LPC407x, LPC408x, errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
2	20140603	• Updated ETHERNET.1 work-around
1.3	20131126	• Added IBAT.1
1.2	20130214	• Added I2C.1
1.1	20121207	• Added ETHERNET.1
1	20120924	• Initial version

Contact information

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1. Product identification

The LPC407x/8x devices typically have the following top-side marking:

LPC40xxXXX

xxxxxxx

xxYYWWR[x]

The last digit in the last line (field 'R') will identify the device revision. Note: pre-production parts are marked differently and this system does not apply. This Errata Sheet covers the following revisions of the LPC407x/8x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ETHERNET.1	In Ethernet MII mode, the transmit data TXD3:0 and transmit enable TX_EN incorrectly reference RX_CLK in data transmission.	'-'	Section 3.1
I2C.1	In slave-transmitter mode, the device set in monitor mode must write a dummy value of 0xFF into the DAT register.	'-'	Section 3.2
IBAT.1	Typical lots have about 5 % parts with higher than normal I_{BAT} current when only V_{BAT} power is provided (VDD_{BAT} is grounded).	'-'	Section 3.3

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'-'	Section 5.1

3. Functional problems detail

3.1 ETHERNET.1

Introduction:

The Ethernet block contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration. The Ethernet block interfaces between an off-chip Ethernet PHY using the MII (Media Independent Interface) or RMII (reduced MII) protocol and the on-chip MIIM (Media Independent Interface Management) serial bus.

Problem:

In MII mode, the transmit data TXD3:0 and transmit enable TX_EN should reference the TX_CLK from the Ethernet PHY. However, due to a configuration error in the chip, the transmit data TXD3:0 and transmit enable TX_EN reference RX_CLK in data transmission. The consequence of this error is that a small percentage of packets cannot be received by the PHY.

Work-around:

None.

Note: There is no issue in RMII mode operation.

3.2 I2C.1

Introduction:

The I2C monitor mode allows the I2C module to monitor traffic on the I^2C-bus without actually participating in traffic or interfering with the I^2C-bus.

Problem:

In slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I^2C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1);     //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for slave-transmitter mode:

```
case 0xA8:      // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:      // data byte in DAT transmitted, ACK received
case 0xC0:      // (last) data byte transmitted, NACK received
case 0xC8:      // last data byte in DAT transmitted, ACK received
     DataByte = LPC_I2C->DATA_BUFFER; //Save data. Data can be processed in Main loop
     LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
     LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.3 IBAT.1

Introduction:

Two independent power domains (VDD_{REG} domain and V_{BAT} domain) are provided that allow the bulk of the device to have power removed while maintaining operation of the Real Time Clock (RTC). The V_{BAT} pin supplies power only to the RTC domain and is active when V_{BAT} is greater than VDD_{REG}. The RTC requires a minimum of power to operate, which can be supplied by an external battery (V_{BAT}). Whenever the device core power (VDD_{REG}) is greater than V_{BAT}, VDD_{REG} is used to operate the RTC. When VDD_{REG} is grounded, the I_{BAT} is typically around 1 uA.

Problem:

Typical lots have about 5 % parts with I_{BAT} current as high as about 10 uA when only V_{BAT} is applied (VDD_{REG} is grounded). This is due to a leakage current path in a level shifter in the power domain.

Work-around:

The problematic leakage path is disabled when the part is entered into Deep power-down mode. If the application allows, the customer should put the device into Deep power-down mode before the VDD_{REG} power is grounded; the BOD ISR could potentially be used for this purpose.

4. AC/DC deviations detail

n/a

5. Errata notes

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

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