Si5397/96 Reference Manual

Quad/Dual DSPLL Any-frequency, Any-output Jitter Attenuators Si5397/96 family reference manual

This Family Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5397/96 devices in end applications. The official device specifications can be found in the Si5397/96 data sheets.

The Si5397 is a high-performance, jitter-attenuating clock multiplier that integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5396 is a dual DSPLL version in a smaller package for the four output A/B/J/K grades and the larger package for the 12 output C/D/L/M grades. Each DSPLL has access to any of the four inputs and can provide low-jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency conversion with superior jitter performance. Each DSPLL supports independent free-run, holdover modes of operation, and offers automatic and hitless input clock switching. The Si5397/96 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5397/96 is made easy with Silicon Labs' ClockBuilder Pro software. Factory preprogrammed devices are available.

All devices of the 9x family offer the option of an external reference or an internal reference. Refer to the data sheet for the different device ordering options and restrictions.

RELATED DOCUMENTS

- Si5397/96 Data Sheet
- UG353: Si5397 Evaluation Board User's Guide
- UG336: Si5396J Evaluation Board User's Guide
- UG467: Si5396C/L Evaluation Board User's Guide
- Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators
- AN1178: Frequency-On-the-Fly for Silicon Labs Jitter Attenuators and Clock Generators
- AN1155: Differences between Si5342-47 and Si5392-97

Table of Contents

1. Work Flow Using ClockBuilder Pro and the Register Map . . . 6

1.1 Field Programming . . . 6

2. Family Product Comparison . . . 7

3. Functional Description . . . 8

3.1 DSPLL and MultiSynth . . . 8

3.1.1 Dividers . . . 9

3.1.2 DSPLL Loop Bandwidth . . . 10

4. Modes of Operation . . . 12

4.1 Reset and Initialization . . . 13

4.2 Dynamic PLL Changes . . . 14

4.3 NVM Programming . . . 15

4.4 Free Run Mode . . . 16

4.5 Lock Acquisition Mode . . . 16

4.6 Locked Mode . . . 16

4.7 Holdover Mode . . . 17

5. Clock Inputs . . . 20

5.1 Input Source Selection . . . 20

5.1.1 Manual Input Switching . . . 21

5.1.2 Automatic Input Switching . . . 21

5.2 Types of Inputs . . . 22

5.2.1 Unused Inputs . . . 24

5.2.2 Hitless Input Switching with Phase Buildout . . . 25

5.2.3 Use Case Scenario: Using More Than Two Inputs . . . 25

5.2.4 Ramped Input Switching . . . 26

5.2.5 Hitless Switching, LOL (Loss of Lock) and Fastlock . . . 26

5.2.6 External Clock Switching . . . 26

5.2.7 Synchronizing to Gapped Input Clocks . . . 27

5.2.8 Rise Time Considerations . . . 28

5.3 Fault Monitoring . . . 29

5.3.1 Input Loss of Signal (LOS) Fault Detection . . . 30

5.3.2 Out of Frequency (OOF) Fault Detection . . . 31

5.3.3 Loss of Lock (LOL) Fault Monitoring . . . 33

5.3.4 Interrupt Pin (INTR) . . . 35

6. Outputs . . . 37

6.1 Output Crosspoint Switch . . . 38

6.2 Output Divider (R) Synchronization . . . 39

6.3 Performance Guidelines for Outputs . . . 40

6.4 Output Signal Format . . . 41

6.4.1 Differential Output Terminations . . . 42

6.4.2 Differential Output Swing Modes 43
6.4.3 Programmable Common Mode Voltage for Differential Outputs 44
6.4.4 LVCMOS Output Terminations 44
6.4.5 LVCMOS Output Impedance and Drive Strength Selection 44
6.4.6 LVCMOS Output Signal Swing 45
6.4.7 LVCMOS Output Polarity 46
6.4.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML 47
6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes 48
6.5 Output Enable/Disable 50
6.5.1 Output Driver State When Disabled 53
6.5.2 Synchronous Output Enable/Disable Feature 53
6.6 Output Buffer Supply Voltage Selection 53
7. Digitally-Controlled Oscillator (DCO) Mode 54
7.1 Frequency Increment/Decrement Using Pin Controls 55
7.2 Frequency Increment/Decrement Using the Serial Interface 57
7.2.1 DCO with Direct Register Writes 59
8. Frequency-On-The-Fly for Si5397/96 60
9. Serial Interface 62
9.1 I^2C Interface 64
9.2 SPI Interface 66
10. XAXB References 71
10.1 External References 71
10.2 Recommended Crystals and Oscillators 71
10.3 Register Settings to Configure for External XTAL Reference 72
10.3.1 XAXB_EXTCLK_EN Reference Clock Selection Register 72
10.3.2 PXAXB Pre-scale Divide Ratio for Reference Clock Register 72
11. Internal Reference 73
12. Crystal, XO and Device Circuit Layout Recommendations 74
12.1 64-Pin QFN Si5397/96 Layout Recommendations 74
12.1.1 Si5397/96 XO Guidelines 74
12.1.2 Si5397/96 Crystal Guidelines 75
12.1.3 Si5397/96 Output Clocks 81
12.2 64-Pin LGA Si5397/96 Layout Recommendations 82
12.3 44-Pin QFN Si5396 Layout Recommendations 83
12.3.1 Si5396 XO Guidelines 83
12.3.2 Si5396 Crystal Guidelines 84
12.4 44-Pin LGA Si5396 Layout Recommendations 89
13. Power Management 90
13.1 Power Management Features 90
13.2 Power Supply Recommendations 90

13.3 Power Supply Sequencing 91
13.4 Grounding Vias 91
14. Register Map 92
14.1 Base vs. Factory Preprogrammed Devices 92
14.2 “Base” Devices (a.k.a. “Blank” Devices) 92
14.3 “Factory Preprogrammed” (Custom OPN) Devices 92
14.4 Register Map Overview and Default Settings Values 93
15. Si5397A/B Register Map 94
15.1 Page 0 Registers Si5397A/B 94
15.2 Page 1 Registers Si5397A/B 114
15.3 Page 2 Registers Si5397A/B 120
15.4 Page 3 Registers Si5397A/B 131
15.5 Page 4 Registers Si5397A/B 133
15.6 Page 5 Registers Si5397A/B 143
15.7 Page 6 Registers Si5397A/B 153
15.8 Page 7 Registers Si5397A/B 163
15.9 Page 9 Registers Si5397A/B 173
15.10 Page A Registers Si5397A/B 174
15.11 Page B Registers Si5397A/B 175
15.12 Page C Registers Si5397A/B 178
16. Si5397C/D Register Map 180
16.1 Page 0 Registers Si5397C/D 180
16.2 Page 1 Registers Si5397C/D 200
16.3 Page 2 Registers Si5397C/D 204
16.4 Page 3 Registers Si5397C/D 215
16.5 Page 4 Registers Si5397C/D 217
16.6 Page 5 Registers Si5397C/D 227
16.7 Page 6 Registers Si5397C/D 237
16.8 Page 7 Registers Si5397C/D 247
16.9 Page 9 Registers Si5397C/D 257
16.10 Page A Registers Si5397C/D 258
16.11 Page B Registers Si5397C/D 259
16.12 Page C Registers Si5397C/D 262
17. Si5396A/B Register Map 264
17.1 Page 0 Registers Si5396A/B 264
17.2 Page 1 Registers Si5396A/B 281
17.3 Page 2 Registers Si5396A/B 285

17.4 Page 3 Registers Si5396A/B 293
17.5 Page 4 Registers Si5396A/B 295
17.6 Page 5 Registers Si5396A/B 304
17.7 Page 9 Registers Si5396A/B 314
17.8 Page A Registers Si5396A/B 315
17.9 Page B Registers Si5396A/B 316
17.10 Page C Registers Si5396A/B 318
18. Si5396C/D Register Map 319
18.1 Page 0 Registers Si5396C/D 319
18.2 Page 1 Registers Si5396C/D 336
18.3 Page 2 Registers Si5396C/D 342
18.4 Page 3 Registers Si5396C/D 351
18.5 Page 4 Registers Si5396C/D 353
18.6 Page 5 Registers Si5396C/D 363
18.7 Page 9 Registers Si5396C/D 373
18.8 Page A Registers Si5396C/D 374
18.9 Page B Registers Si5396C/D 375
18.10 Page C Registers Si5396C/D 377
19. Revision History 378

1. Work Flow Using ClockBuilder Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to the applications notes and Knowledge Base articles within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is to enable use of the device without an in-depth understanding of its complexities. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

1.1 Field Programming

To simplify design and software development of systems using the Si5397/96, a field programmer is available in addition to the evaluation board. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5397/96 sample devices. Refer to www.silabs.com/CBProgrammer for information about this kit.

2. Family Product Comparison

The following table is a comparison of the different parts in the product family showing the differences in the inputs, MultiSynths, outputs and package type.

Table 2.1. Family Feature Comparison

Part Number	Internal/External Reference	Number of Inputs	Number of Multi-Synths	Number of Outputs	Package Type
Si5397A/B	External	4	4	8	64-QFN
Si5397J/K	Internal	4	4	8	64-LGA
Si5397C/D	External	4	4	4	64-QFN
Si5397L/M	Internal	4	4	4	64-LGA
Si5396A/B	External	4	2	4	44-QFN
Si5396J/K	Internal	4	2	4	44-LGA
Si5396C/D	External	4	2	12	64-QFN
Si5396L/M	Internal	4	2	12	64-LGA

3. Functional Description

The Si5397 takes advantage of Silicon Labs fourth-generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. Each DSPLL has access to any of the four inputs (IN0 to IN3) after having been divided down by the P dividers, which are either fractional or integer. Clock selection can be either manual or automatic. Any of the output clocks can be configured to any of the DSPLLs using a flexible crosspoint connection. The Si5396 is a 2 PLL device with a four output option (Si5396A/B/J/K) or a twelve output option (Si5396C/D/L/M).
The registers and features of the external reference parts match that of the internal reference parts. Throughout this document the register descriptions for labels of the external reference grades can be assumed to be the same for the internal reference grades.

3.1 DSPLL and MultiSynth

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pxn/Pxd) allow for integer or fractional division of the input frequency, but the input frequencies must be integer related to allow the DSPLL to perform hitless switching between input clocks (INx). Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. Note that a XTAL (or suitable XO reference on XA/XB) is always required and is the jitter reference for the device. The high-performance MultiSynth dividers (Nxn/Nxd) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the generated frequencies to any of the outputs. A single MultiSynth output can connect to one or more output drivers. Additional integer division (R) determines the final output frequency. The internal reference grade devices have a XTAL integrated in the package, so no external XTAL is needed. The specs for the integrated reference can be found in the data sheet.

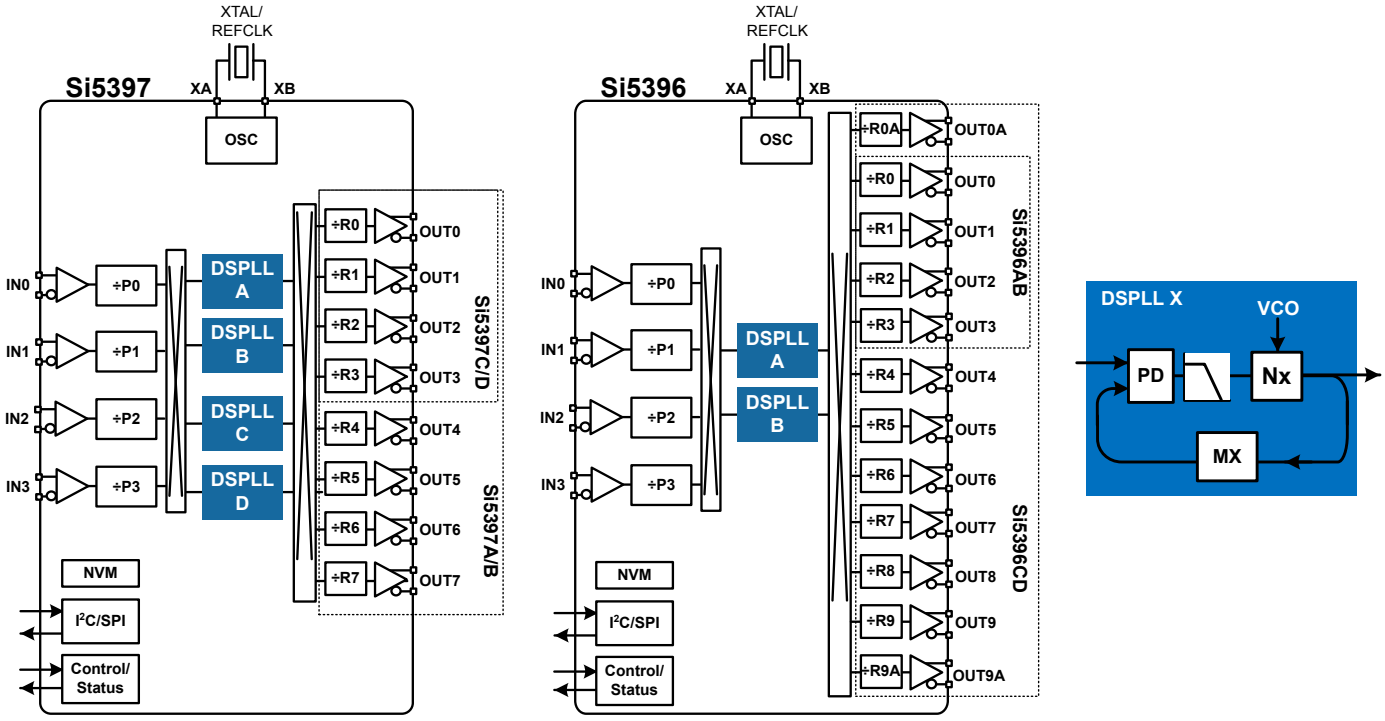


Figure 3.1. DSPLL and Multisynth System Flow Diagram

The frequency configuration of the DSPLL is programmable through the SPI or I^{2}C serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), fractional output MultiSynth division (Nn/Nd), and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro software.

3.1.1 Dividers

There are five main divider classes within the Si5397/96. Additionally, FSTEPW can be used to adjust the nominal output frequency in DCO mode. See Section 7. Digitally-Controlled Oscillator (DCO) Mode for more information and block diagrams on DCO mode.

- 1. PXAXB: Reference input divider (0x0206)
  - Divide reference clock by 1, 2, 4, or 8 to obtain an internal reference < 125 MHz
- 2. P0-P3: Input clock wide range dividers (0x0208-0x022F)
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24} (Fractional-P divisors must be > 5)
  - 48-bit numerator, 32-bit denominator
  - Practical P divider range of (Fin / 2 MHz) < P < (Fin / 8 kHz)
  - Each P divider has a separate update bit for the new divider value to take effect
- 3. MA-MD: DSPLL feedback dividers (0x0415-0x041F, 0x0515-0x051F, 0x0615-0x061F, 0x0716-0x0720)
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24} (Fractional-M divisors must be > 10)
  - 56-bit numerator, 32-bit denominator
  - Practical M divider range of (Fdco / 2 MHz) < M < (Fdco / 8 kHz)
  - Each M divider has a separate update bit for the new divider value to take effect
  - Soft reset will also update M divider values
- 4. Output N dividers N0-N3(0x0302-0x032D)
  - MultiSynth divider
  - Integer or fractional divide values
  - 44 bit numerator, 32 bit denominator
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
- 5. R0A-R9A: Output dividers (0x024A-0x026A)
  - 24-bit field
  - Min. value is 2, Max. value is 2^{25}-2
  - Only even integer divide values: 2, 4, 6, etc.
  - R Divisor = 2 x (Field + 1). For example, Field = 3 gives an R divisor of 8
- FSTEPW: DSPLL DCO step words (0x0423-0x0429, 0x0523-0x0529, 0x0623-0x0629, 0x0724-0x072A)
  - Positive Integers, where FINC/FDEC select direction
  - Min. value is 0, Max. value is 2^{24}
  - 56-bit step size, relative to 32-bit M denominator

3.1.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and wander filtering. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. The loop bandwidth is controlled digitally and remains stable with less than 0.1 dB of peaking for the loop bandwidth selected. The DSPLL loop bandwidth is set in registers 0x0408-0x040D, 0x0508-0x050D, 0x0608-0x060D, 0x0709-0x070E and are determined using ClockBuilder Pro.

The higher the PLL bandwidth is set relative to the phase detector frequency (f_{pfd}), the more chance that f_{pfd} will cause a spur in the Phase Noise plot of the output clock and increase the output jitter. To guarantee the best phase noise/jitter it is recommended that the normal PLL bandwidth be kept less than $f_{pfd}/160$ although ratios of $f_{pfd}/100$ will typically work fine.

Note: After changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414, 0x0514, 0x0614, 0x0714) must be set high to latch the new values into operation. The update bits will latch both nominal and fastlock bandwidths.

Table 3.1. PLL Bandwidth Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
BW_PLLA	0408[7:0] - 040D[7:0]	0408[7:0] - 040D[7:0]	This group of registers determine the loop bandwidth for DSPLL A, B, C, D. They are all independently selectable in the range from 0.1 Hz up to 4 kHz. Register values determined by ClockBuilderPro.
BW_PLLB	0508[7:0] - 050D[7:0]	0508[7:0] - 050D[7:0]	
BW_PLLC	0608[7:0] - 060D[7:0]	—	
BW_PLLD	0709[7:0] - 070E[7:0]	—	

3.1.2.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process to reduce lock time. Higher Fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the nominal DSPLL Loop Bandwidth setting. The Fastlock feature can be enabled or disabled independently by register control. If enabled, when LOL is asserted Fastlock will be automatically enabled. When LOL is no longer asserted, Fastlock will be automatically disabled. The loss of lock (LOL) feature is a fault monitoring mechanism. Details of the LOL feature can be found in the fault monitoring section.

Note: After changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414, 0x0514, 0x0614, 0x0714) must be set high to latch the new values into operation. This update bit will latch new values for Loop, Fastlock, and Holdover bandwidths simultaneously.

Table 3.2. PLL Fastlock Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
FASTLOCK_AUTO_EN_PLLA	042B[0]	042B[0]	Fastlock enable/disable. Fastlock is enabled by default with a bandwidth of 4 kHz.
FASTLOCK_AUTO_EN_PLLB	052B[0]	052B[0]	
FASTLOCK_AUTO_EN_PLLC	062B[0]	—	
FASTLOCK_AUTO_EN_PLLD	072C[0]	—	
FAST_BW_PLLA	040E[7:0] - 0413[7:0]	040E[7:0] - 0413[7:0]	Fastlock bandwidth is selectable in the range of 100 Hz up to 4 kHz. Register values determined using ClockBuilderPro.
FAST_BW_PLLB	050E[7:0] - 0513[7:0]	050E[7:0] - 0513[7:0]	
FAST_BW_PLLC	060E[7:0] - 0613[7:0]	—	
FAST_BW_PLLD	070F[7:0] - 0714[7:0]	—	

3.1.2.2 Holdover Exit Bandwidth

In addition to the operating loop and fastlock bandwidths, there is also a user-selectable bandwidth when exiting holdover and locking or relocking to an input clock, available when ramping is disabled (HOLD_RAMP_BYP = 1). CBPro sets this value equal to the loop bandwidth by default.

Note: The BW_UPDATE bit will latch new values for Loop, Fastlock, and Holdover bandwidths simultaneously.

Table 3.3. DSPLL Holdover Exit Bandwidth Registers

Register Name	Hex Address	Function
HOLDEXIT_BW_PLLx	049D-04A2 (PLLA) 059D–05A2 (PLLB) 069D-06A2 (PLLC) 079D-07A2 (PLLD)	Determines the Holdover Exit BW for the DSPLL. Parameters are generated by ClockBuilder Pro. See CBPro for the generated values and corresponding bandwidths.

4. Modes of Operation

Once initialization is complete, the DSPLL operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

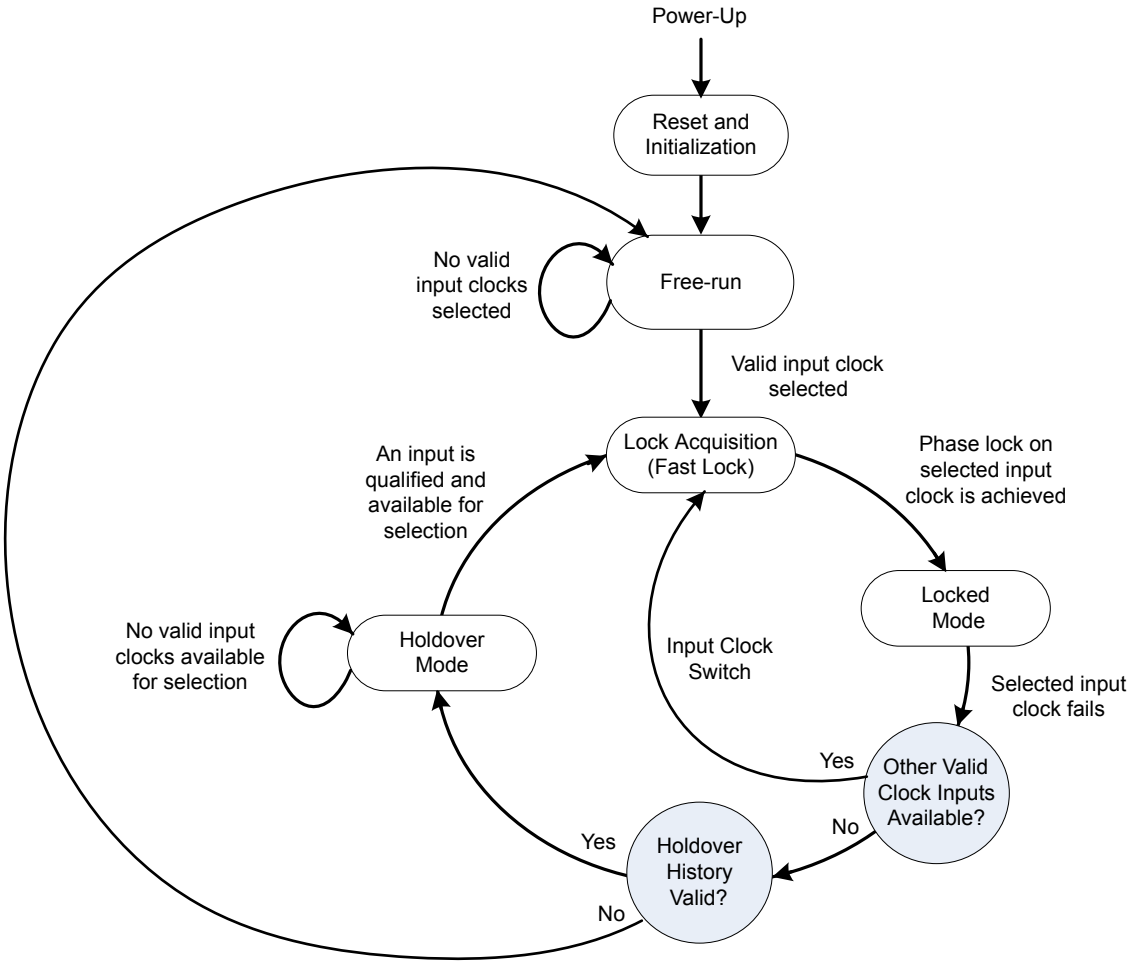


Figure 4.1. Modes of Operation

4.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from internal non-volatile memory (NVM) and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RST pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

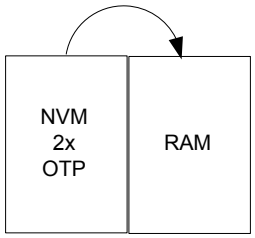


Figure 4.2. Si5397/96 Memory Configuration

Table 4.1. Reset Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
HARD_RST	001E[1]	001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST_ALL	001C[0]	001C[0]	Resets the device without re-downloading the register configuration from NVM.
SOFT_RST_PLLA	001C[1]	001C[1]	Performs a soft reset on DSPLL A only.
SOFT_RST_PLLB	001C[2]	001C[2]	Performs a soft reset on DSPLL B only.
SOFT_RST_PLLC	001C[3]	—	Performs a soft reset on DSPLL C only.
SOFT_RST_PLLD	001C[4]	—	Performs a soft reset on DSPLL D only.

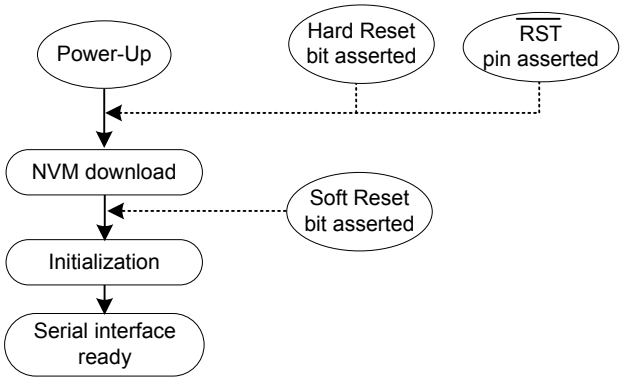


Figure 4.3. Initialization from Hard Reset and Soft Reset

The Si5397/96 is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from NVM. Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins. Neither VDDOx or VDDS supplies are required to write the NVM.

4.2 Dynamic PLL Changes

ClockBuilder Pro generates all necessary control register writes to update settings for the entire device, including the ones described below. This is the case for both “Export” generated files as well as when using the GUI. This is sufficient to cover most applications. However, in some applications it is desirable to modify only certain sections of the device while maintaining unaffected clocks on the remaining outputs. If this is the case CBPro provides some frequency changes on the fly examples.

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). Additionally, making single frequency step changes greater than ±350 ppm, either by using the DCO or by directly updating the M dividers, may also cause the PLL to become unresponsive. Changes to the following registers require this special sequence of writes:

Control	Register(s)
PXAXB	0206[1:0]
MXAXB_NUM	0235 – 023A
MXAXB_DEN	023B – 023E

PLL lockup can easily be avoided by using the following the preamble and postamble write sequence below when one of these registers is modified or large frequency steps are made. Clockbuilder Pro software adds these writes to the output file by default when Exporting Register Files.

To start, write the preamble by updating the following control bits.

Address	Value
0B24	0xC0
0B25	0x00
0B4E	0x1A

Wait 300 ms for the device state to stabilize.

Then, modify all desired control registers.

Write 0x01 to Register 0x001C (SOFT_RST_ALL) to perform a Soft Reset once modifications are complete.

Write the postamble by updating the following control bits.

Address	Value
0B24	0xC3
0B25	0x02

Note, however, that this procedure affects all DSPLLs and outputs on the device.

4.3 NVM Programming

Devices have two categories of non-volatile memory: user NVM and Factory (Silabs) NVM. Each type is segmented into NVM banks. There are three user NVM banks, one of which is used for factory programming (whether a base part or an Orderable Part Number). User NVM can be therefore be burned in the field up to two times. Factory NVM cannot be modified, and contains fixed configuration information for the device.

The ACTIVE_NVM_BANK device setting can be used to determine which user NVM bank is currently being used and therefore how many banks, if any, are available to burn. The following table describes possible values:

Table 4.2. NVM Bank Burning Values

Active NVM BANK Value (Decimal)	Number of User Banks Burned	Number of User Banks Available to Burn
3 (factory state)	1	2
15	2	1
63	3	0

Note: While polling DEVICE_READY during the procedure below, the following conditions must be met in order to ensure that the correct values are written into the NVM:

- VDD and VDDA power must both be stable throughout the process.
- No additional registers may be written or read during DEVICE_READY polling. This includes the PAGE register at address 0x01. DEVICE_READY is available on every register page, so no page change is needed to read it.
- Only the DEVICE_READY register (0xFE) should be read during this time.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed. Verify device operation before writing registers to NVM.
2. You may write to the user scratch space (Registers 0x026B to 0x0272 DESIGN_ID0-DESIGN_ID7) to identify the contents of the NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Poll DEVICE_READY until DEVICE_READY=0x0F.
5. Set NVM_READ_BANK 0x00E4[0]=1. This will load the NVM contents into non-volatile memory.
6. Poll DEVICE_READY until DEVICE_READY=0x0F.
7. Read ACTIVE_NVM_BANK and verify that the value is the next highest value in the table above. For example, from the factory it will be a 3. After NVM_WRITE, the value will be 15.

Alternatively, steps 5 and 6 can be replaced with a Hard Reset, either by RSTb pin, HARD_RST register bit, or power cycling the device to generate a POR. All of these actions will load the new NVM contents back into the device registers.

The ClockBuilder Pro Field Programmer kit is a USB attached device to program supported devices either in-system (wired to your PCB) or in-socket (by purchasing the appropriate field programmer socket). ClockBuilder Pro software is then used to burn a device configuration (project file). Learn more at https://www.silabs.com/products/development-tools/timing/cbprogrammer.

Table 4.3. NVM Programming Registers

Register Name	Hex Address [Bit Field]	Function
ACTIVE_NVM_BANK	00E2[7:0]	Identifies the active NVM bank.
NVM_WRITE	00E3[7:0]	Initiates an NVM write when written with value 0xC7.
NVM_READ_BANK	00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	00FE[7:0]	Indicates that the device is ready to accept commands when value = 0x0F.

Warning: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming and may corrupt the register contents, as they are read from NVM. Note that this includes accesses to the PAGE register.

4.4 Free Run Mode

Once power is applied to the Si5397/96 and initialization is complete, if valid input is not present, the DSPLL will automatically enter freerun mode, generating the frequencies determined by the NVM. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes. Because there is little or no jitter attenuation from the XAXB pins to the clock outputs, a low-jitter XAXB source will be needed for low-jitter clock outputs.

4.5 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.6 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. DSPLL has its LOL pin and status bit to indicate when lock is achieved. See Section 5.3.3 Loss of Lock (LOL) Fault Monitoring for more details on the operation of the loss of lock circuit.

4.7 Holdover Mode

The DSPLL programmed for holdover mode automatically enters holdover when the selected input clock becomes invalid (i.e. when either OOF or LOS are asserted) and no other valid input clocks are available for selection. The DSPLL calculates a historical average of the input frequency while in locked mode to minimize the initial frequency offset when entering the holdover mode.

The averaging circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window with the stored historical frequency data. The window size determines the amount of holdover frequency averaging. The delay value is used to ignore frequency data that may be corrupt just before the input clock failure. Both the window size and the delay are programmable as shown in the figure below.

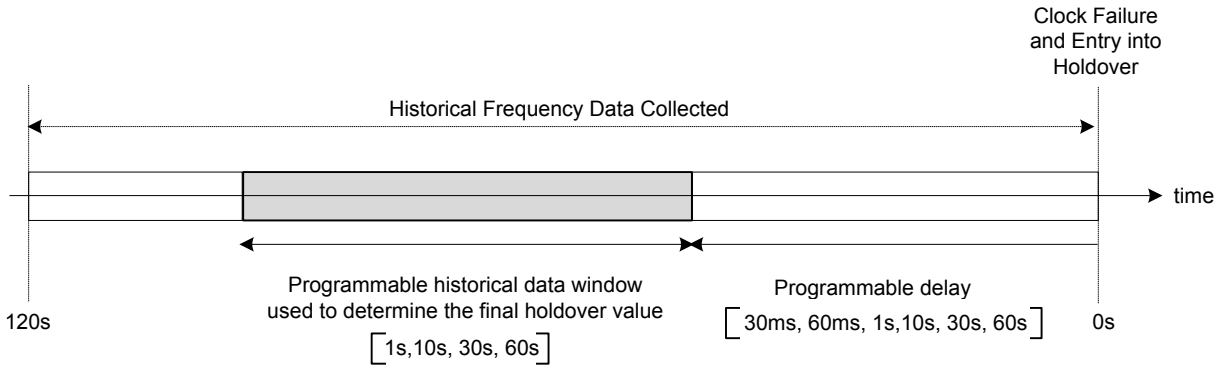


Figure 4.4. Programmable Holdover Window

When entering Holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XAXB pins. If the clock input becomes valid, the DSPLL will automatically exit the Holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. These options are register programmable.

The recommended mode of exit from holdover is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is likely that the new output clock frequency will not be the same as the holdover output frequency because the new input clock frequency might have changed and the XTAL drift might have changed the output frequency. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of approximately 40 values that are in between. The loop bandwidth values do not limit or affect the ramp rate selections and vice versa. CBPro defaults to ramped exit from holdover. Ramped exit from holdover is also used for ramped input clock switching. See Section 5.2.4 Ramped Input Switching for more information.

As shown in Figure 4.1 Modes of Operation on page 12, the Holdover and Freerun modes are closely related. The device will only enter Holdover if a valid clock has been selected long enough for the holdover history to become valid. If the clock fails before the combined holdover history length and holdover history delay time has been met, then holdover history won't be valid and the device will enter Freerun mode instead. Reducing the holdover history length and holdover history delay times will allow Holdover in less time, limited by the source clock failure and wander characteristics. Note that the Holdover history accumulation is suspended when the input clock is removed and resumes accumulating when a valid input clock is again presented to the DSPLL.

Table 4.4. Holdover Mode Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
Holdover Status			
HOLD_PLL(D,C,B,A)	000E[7:4]	000E[5:4]	Holdover status indicator. Indicates when a DSPLL is in holdover or free-run mode and is not synchronized to the input reference. The DSPLL goes into holdover only when the historical frequency data is valid, otherwise the DSPLL will be in free-run mode.
HOLD_FLG_PLL(D,C,B,A)	0013[7:4]	0013[5:4]	Holdover status monitor sticky bits. Sticky bits will remain asserted when an holdover event occurs until cleared. Writing a zero to a sticky bit will clear it.
HOLD_HIST_VALID_PLLA	043F[1]	043F[1]	Holdover historical frequency data valid. Indicates if there is enough historical frequency data collected for valid holdover value.
HOLD_HIST_VALID_PLLB	053F[1]	053F[1]	
HOLD_HIST_VALID_PLLC	063F[1]	—	
HOLD_HIST_VALID_PLLD	0740[1]	—	
Holdover Control and Settings			
HOLD_HIST_LEN_PLLA	042E[4:0]	042E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $((2^{LEN}) - 1)$*268nsec
HOLD_HIST_LEN_PLLB	052E[4:0]	052E[4:0]	
HOLD_HIST_LEN_PLLC	062E[4:0]	—	
HOLD_HIST_LEN_PLLD	072F[4:0]	—	
HOLD_HIST_DELAY_PLLA	042F[4:0]	042F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = (2^{DELAY}) x268nsec
HOLD_HIST_DELAY_PLLB	052F[4:0]	052F[4:0]	
HOLD_HIST_DELAY_PLLC	062F[4:0]	—	
HOLD_HIST_DELAY_PLLD	0730[4:0]	—	
FORCE_HOLD_PLLA	0435[0]	0435[0]	These bits allow forcing any of the DSPLLs into holdover
FORCE_HOLD_PLLB	0535[0]	0535[0]	
FORCE_HOLD_PLLC	0635[0]	—	
FORCE_HOLD_PLLD	0736[0]	—	
HOLD_EXIT_BW_SEL1_PLLA	042C[4]	042C[4]	Selects the exit from holdover bandwidth. Options are: 0: Exit of holdover using the fastlock bandwidth 1: Exit of holdover using the DSPLL loop bandwidth
HOLD_EXIT_BW_SEL1_PLLB	052C[4]	052C[4]	
HOLD_EXIT_BW_SEL1_PLLC	062C[4]	—	
HOLD_EXIT_BW_SEL1_PLLD	072D[4]	—	
HOLD_EXIT_BW_SEL0_PLLA	049B[6]	049B[6]	
HOLD_EXIT_BW_SEL0_PLLB	059B[6]	059B[6]	
HOLD_EXIT_BW_SEL0_PLLC	069B[6]	—	
HOLD_EXIT_BW_SEL0_PLLD	079B[6]	—	

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
HOLD_RAMP_EN_PLLA	042C[3]	042C[3]	Must be set to 1 for normal operation.
HOLD_RAMP_EN_PLLB	052C[3]	052C[3]	
HOLD_RAMP_EN_PLLC	062C[3]	—	
HOLD_RAMP_EN_PLLD	072D[3]	—	

5. Clock Inputs

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both standard format inputs and low duty cycle pulsed CMOS clocks. The input P dividers can be either fractional or integer. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in the figure below.

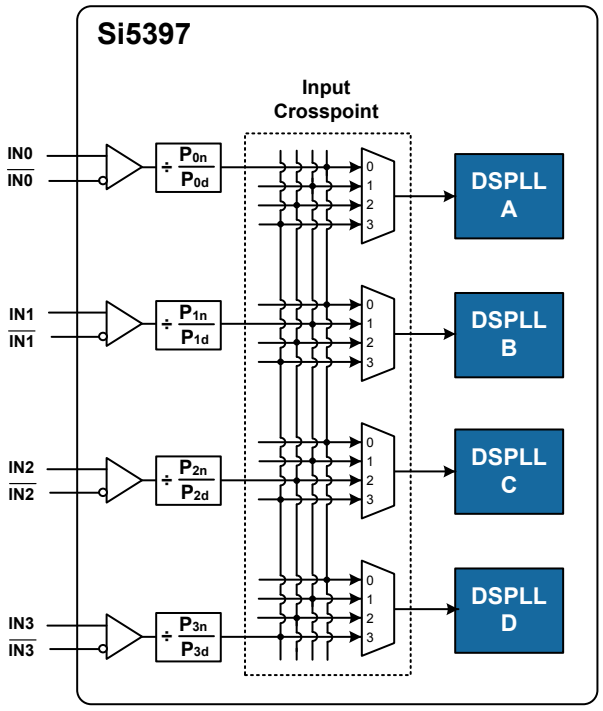


Figure 5.1. Clock Inputs Example

5.1 Input Source Selection

The inputs accept ac-coupled clocks that are differential or singled ended such as LVCMOS. In addition, the inputs also accept dc-coupled CMOS type inputs with 50% or very low input duty cycle. Input selection can be manual (pin or register controlled) or automatic with user definable priorities. There is a register to select pin or register control, and to configure the input as shown below.

Table 5.1. Manual or Automatic Input Clock Selection Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
CLK_SWITCH_MODE_PLLA	0436[1:0]	0436[1:0]	Selects manual or automatic switching mode for DSPLL A, B, C, D. 0: For manual 1: For automatic, non-revertive 2: For automatic, revertive 3: Reserved
CLK_SWITCH_MODE_PLLB	0536[1:0]	0536[1:0]	
CLK_SWITCH_MODE_PLLC	0636[1:0]	—	
CLK_SWITCH_MODE_PLLD	0737[1:0]	—	

5.1.1 Manual Input Switching

In manual mode the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode if the holdover history is valid or Freerun if it is not.

Table 5.2. Manual Input Select Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
IN_SEL_PLLA	042A[2:0]	042A[2:0]	Selects the clock input used to synchronize DSPLL A, B, C, or D. Selections are: IN0, IN1, IN2, IN3, corresponding to the values 0, 1, 2, and 3. Selections 4–7 are reserved.
IN_SEL_PLLB	052A[3:1]	052A[3:1]	
IN_SEL_PLLC	062A[2:0]	—	
IN_SEL_PLLD	072B[2:0]	—	

5.1.2 Automatic Input Switching

Automatic input switching is available in addition to the manual selection described previously. In automatic mode, the switching criteria is based on input clock qualification, input priority and the revertive option. The IN_SEL_PLLx register bits are not used in automatic input switching. Also, only input clocks that are valid (i.e., with no active fault indicators) can be selected by the automatic clock switching. If there are no valid input clocks available, the DSPLL will enter Holdover or Freerun mode. With Revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With Non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid, an automatic switchover to the highest priority valid input will be initiated.

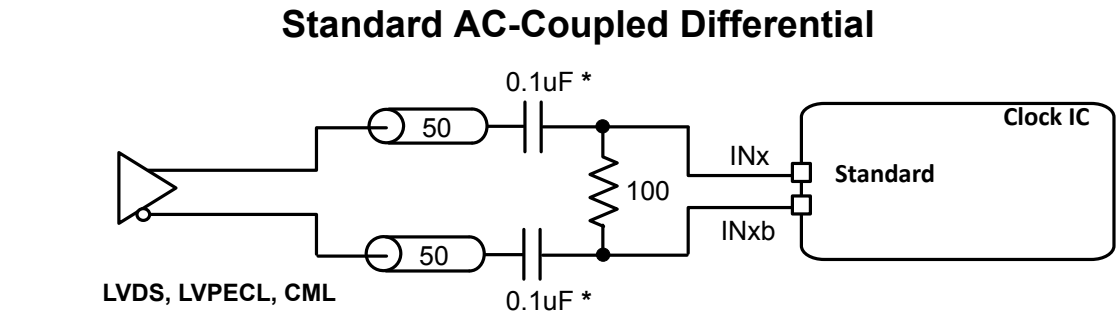
Table 5.3. Automatic Input Select Control Registers

Setting Name	Hex Address		Function
	Si5397	Si5396	
IN(3,2,1,0)_PRIORITY_PLLA	0438–0439	0438–0439	Selects the automatic selection priority for [IN3, IN2, IN1, IN0] for each DSPLL A, B, C, D. Selections are: 1st, 2nd, 3rd, 4th, or never select. Default is IN0=1st, IN1=2nd, IN2=3rd, IN3=4th.
IN(3,2,1,0)_PRIORITY_PLLB	0538–0539	0538–0539	
IN(3,2,1,0)_PRIORITY_PLLC	0638–0639	—	
IN(3,2,1,0)_PRIORITY_PLLD	0739–073A	—	
IN(3,2,1,0)_LOS_MSK_PLLA	0437	0437	Determines if the LOS status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is LOS is enabled (un-masked).
IN(3,2,1,0)_LOS_MSK_PLLB	0537	0537	
IN(3,2,1,0)_LOS_MSK_PLLC	0637	—	
IN(3,2,1,0)_LOS_MSK_PLLD	0738	—	
IN(3,2,1,0)_OOF_MSK_PLLA	0437	0437	Determines if the OOF status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is OOF enabled (un-masked).
IN(3,2,1,0)_OOF_MSK_PLLB	0537	0537	
IN(3,2,1,0)_OOF_MSK_PLLC	0637	—	
IN(3,2,1,0)_OOF_MSK_PLLD	0738	—	

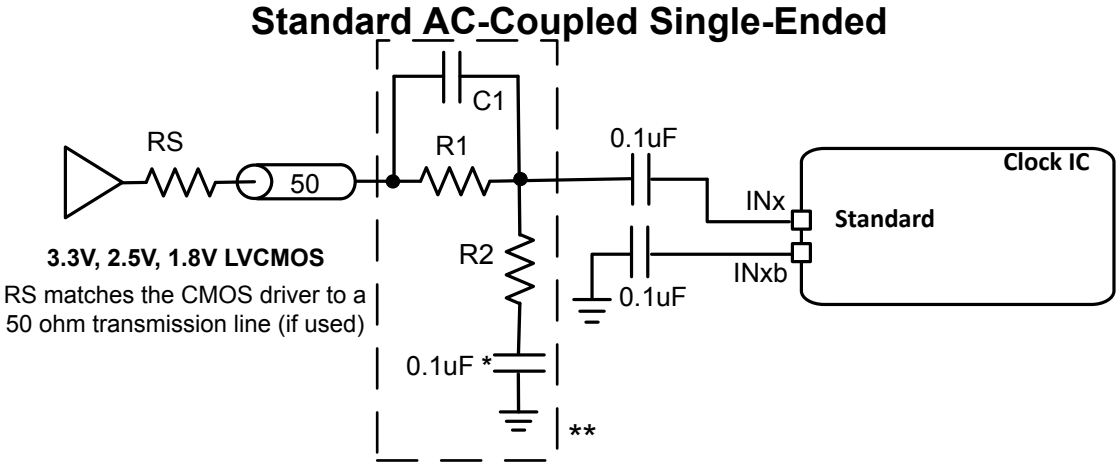
5.2 Types of Inputs

Each of the four different inputs IN0-IN3 can be configured as ac-coupled differential formats such as LVDS, LVPECL, HCSL, CML, and ac-coupled single-ended CMOS formats. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” input buffer selection as these pins are internally dc-biased to approximately 0.83 V.

Floating clock inputs are noise sensitive. Add a cap to ground for all non-CMOS unused clock inputs. To place the input into Standard Mode make sure IN_PULSED_CMOS_EN 0x949 [7:4] = 0. Bit 7 = IN3, Bit 6 = IN2, Bit 5 = IN1 and Bit 4 = IN0. Make sure the corresponding input bit is set to 0 for Standard Mode. If this bit is 1 this will turn on dc-coupled CMOS Mode. Although the name is PULSED_CMOS_EN this setting actually corresponds to enable all dc-coupled CMOS modes described further below for the Standard CMOS and Non-Standard/Pulsed CMOS inputs, which are all dc-coupled inputs.



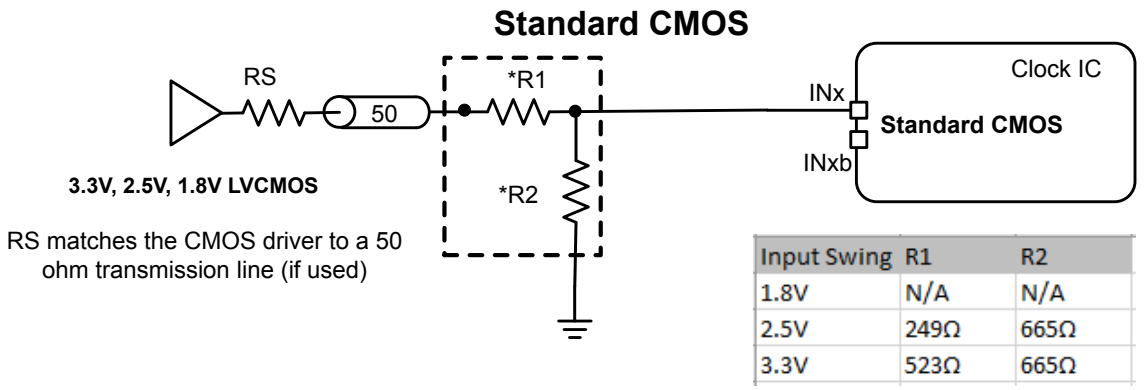
* These caps should have < ~5 ohms capacitive reactance at the clock input frequency.



*This cap should have less than ~20 ohms of capacitive reactance at the clock input frequency.
** Only when 3.3V LVCMOS driver is present, use R2 = 845 ohm and R1 = 267 ohm if needed to keep the signal at INx < 3.6 Vpp_se. Including C1 = 6 pf may improve the output jitter due to faster input slew rate at INx. If attenuation is not needed for Inx<3.6Vppse, make R1 = 0 ohm and omit C1, R2 and the capacitor below R2. C1, R1, and R2 should be physically placed as close as practicle to the device input pins.

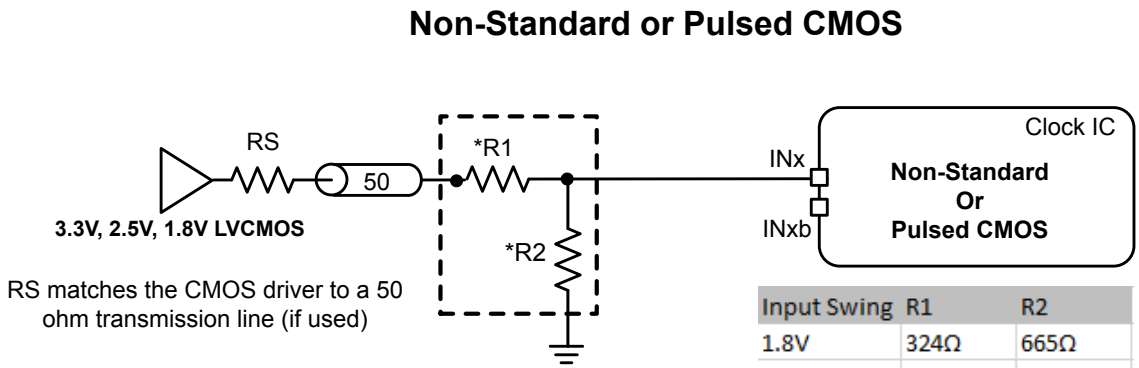
Figure 5.2. AC-coupled Standard Input Termination Diagrams

Each of the four different inputs IN0-IN3 can be configured as single-ended **dc**-coupled standard CMOS, non-standard CMOS or pulsed CMOS inputs. In all cases, the inputs should be terminated near the device input pins. In these configurations CMOS mode is enabled via register setting "IN_PULSED_CMOS_EN" = 1 for each input. Note from the data sheet that the Standard CMOS selection has higher VIL and VIH settings than the non-standard/ pulsed CMOS Input buffer selection. See the data sheet for the max VIL and min VIH values for both Standard CMOS vs Non-standard CMOS & Pulsed CMOS selection.



Input Swing	R1	R2
1.8V	N/A	N/A
2.5V	249Ω	665Ω
3.3V	523Ω	665Ω

* Attenuation circuit not required for 1.8V input or if all input specifications in datasheet are met.



Input Swing	R1	R2
1.8V	324Ω	665Ω
2.5V	665Ω	665Ω
3.3V	1.1kΩ	665Ω

* Attenuation circuit recommended but not required if input specifications in datasheet are met.

Figure 5.3. Input Terminations for DC Coupled Standard CMOS and Non-Standard/Pulsed CMOS Inputs

Standard CMOS refers to a signal with a swing of (1.8 V, 2.5 V or 3.3 V) +/- 5% that complies with the specified maximum VIL and minimum VIH specifications in the data sheet. Refer to the data sheet for the VIL and VIH specifications. For non-compliant inputs, a resistive attenuator is required as shown. It is not recommended to add the attenuation circuit for compliant inputs as it adversely affects the signal integrity at the input pins. Note that maximum input frequency cannot be guaranteed with the attenuator circuit. If an input exceeds 3.3 V +5% then the input must be attenuated before going into the chip.

Non-standard CMOS refers to a signal with a swing of (1.8 V, 2.5 V or 3.3 V) +/-5% that has been attenuated/level-shifted in order to comply with the specified non-standard maximum VIL and minimum VIH specifications. Refer to the data sheet for the VIL and VIH specifications. For non-compliant inputs, a resistive attenuator is required as shown. It is not recommended to add the attenuation circuit for compliant inputs as it adversely affects the signal integrity at the input pins. Note that maximum input frequency cannot be guaranteed with the attenuator circuit. If an input exceeds 3.3 V +5% then the input must be attenuated before going into the chip.

The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. The resistor divider values given in the diagram will work with up to 1 MHz pulsed inputs. Pulsed CMOS refers to a low-frequency (up to 1 MHz), low/high duty cycle signal with a swing of (1.8 V, 2.5 V or 3.3 V) +/-5% that has been attenuated/level-shifted in order to comply with the specified non-standard maximum VIL and minimum VIH specifications. Refer to the data sheet for the VIL and VIH specifications. Make sure to not violate the max and min specifications or use the attenuator circuit to ensure the specifications.

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for IN3 through IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected, as shown in the above figure, including the “Standard AC-coupled Single-Ended” case. In any of the CMOS modes, it is not necessary to connect the inverting INx input pin. To place the input buffer into any one of the CMOS modes, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4]. Make sure the corresponding input bit is set to 1 for DC-coupled CMOS Mode. Although the name is PULSED_CMOS_EN this setting actually corresponds to enable all dc-coupled CMOS modes. IN_CMOS_USE1P8 0x094F[7:4] determines Standard CMOS mode when the input bit is high and Non-Standard or Pulsed CMOS Mode when the input bit is low. The difference between Standard CMOS and Non-Standard/ Pulsed CMOS is the VIL/VIH settings, which should be reviewed carefully from the data sheet.

Table 5.4. Input Clock Control and Configuration Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5397/96	
IN_EN	0949[3:0]	Enable each of the input clock buffers for IN3 through IN0.
IN_PULSED_CMOS_EN	0949[7:4]	Enable CMOS mode for each input 1 = DC-coupled CMOS Mode either Standard or Non-Standard/Pulsed CMOS 0 = Standard AC-coupled Mode 7: IN3 6: IN2 5: IN1 4: IN0
IN_CMOS_USE1P8	094F[7:4]	1 = Standard DC-coupled CMOS mode 0 = Non-Standard or Pulsed DC-coupled CMOS Mode 7: IN3 6: IN2 5: IN1 4: IN0 Review data sheet for max and min VIL/VIH thresholds

5.2.1 Unused Inputs

Unused inputs can be disabled and left unconnected. Register 0x0949[3:0] defaults the input clocks to being enabled. Clearing the unused input bits will disable them. Enabled inputs not actively being driven by a clock may benefit from pull up or pull down resistors to avoid them responding to system noise.

5.2.2 Hitless Input Switching with Phase Buildout

Phase buildout, also referred to as hitless switching, prevents a phase change from propagating to the output when switching between two clock inputs with an integer related frequency and a fixed phase relationship (i.e., they are phase/frequency locked, but with a non-zero phase difference). When phase buildout is enabled, the DSPLL absorbs the phase difference between the two input clocks during a clock switch. When phase buildout is disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL loop bandwidth. Lower PLL loop bandwidth provides more filtering.

Hitless Switching with Phase Buildout should be used for applications where the input clocks are all locked to a common upstream clock, as in most synchronization systems. Hitless switching is supported for input frequencies down to 8 kHz. Gapped clocks are not recommended for use with Hitless Switching, as this may increase the phase transient on the outputs.

Table 5.5. Hitless Switching Enable Bit

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
HSW_EN_PLLA	0436[2]	0436[2]	Phase Buildout Switching Enable/Disable for DSPLL A, B, C, D. Phase Buildout Switching is enabled by default.
HSW_EN_PLLB	0536[2]	0536[2]	
HSW_EN_PLLC	0636[2]	—	
HSW_EN_PLLD	0737[2]	—	

5.2.3 Use Case Scenario: Using More Than Two Inputs

When a DSPLL uses more than two inputs there is a rare but small chance that if two of the inputs are lost at the exact same time (within 1 PFD clock period) the switch to the 3rd available input will not occur correctly, and the state machine will be stuck pointing to a lost clock causing the PLL to lose lock. It won't recover unless manually switched to an available input.

Workaround: For designs using more than two inputs with hitless switching enabled follow the below guidance.

1. Do not disable two inputs at the exact same time. If both inputs must be shut off then leave at least one clock period of delay between shutting off one input and then shut off the other input.
2. Also consider including a LOS ISR (Interrupt Service Routine) that always checks for a LOS event with the active input pointing to an input that is LOS.

Outside the ISR make sure the device is already configured for input register control mode if this is an available feature for the device. Set IN_SEL_REGCTRL[0] = 1 for devices that have the option of both pin or register control.

LOS Interrupt Service Routine Pseudo code Example:

```
Step 1. If a LOS event occurs – read and store the LOS flags LOS_FLG 0x0012[0:3]

Step 2. Read the Input Active Register(s). This is named IN_PLLx_ACTV, where x = A, B, C or D depending on the
PLL.  Compare this to the LOS flags asserted in step 1. This is done to determine if the device is pointing to
an input that is LOS asserted.

Step 3. If the input points to a LOS input then set the input switch to manual mode.
Set CLK_SWITCH_MODE_PLLx[1:0]  = 0, where x= A, B, C, or D depending on the PLL.

Step 4. Change the input to an available active input.
Set IN_SEL_PLLx in the multi PLL devices where x = A, B, C or D depending on the PLL.  Set to 0, 1, 2 or 3
whichever is the available active input.

Step 5. Verify IN_PLLx_ACTV to make sure the input is now pointing to the active input as expected.

Step 6. Go back to automatic mode
Set CLK_SWITCH_MODE_PLLx[1:0] = 1 for Automatic non revertive, or 2 for automatic revertive
```

For further guidance and workarounds please contact Silicon Labs.

5.2.4 Ramped Input Switching

When switching between input clocks that are not synchronized to the same upstream clock source (i.e. are plesiochronous) there will be differences in frequency between clocks. Ramped switching should be enabled in these cases to ensure a smooth frequency transition on the outputs. In this situation, it is also advisable to enable phase buildout, as discussed in the previous section to minimize the input-to-output clock skew after the frequency ramp has completed.

When ramped clock switching is enabled, the Si5397/96 will enter into holdover and then exit from holdover when the exit ramp has been calculated. This means that ramped switching behaves like an exit from holdover. This is particularly important when switching between two input clocks that are not the same frequency so that the transition between the two frequencies will be smooth and linear. Ramped switching is not needed for cases where the input clocks are locked to the same upstream clock source. The CBPro 'DSPLL Configure' page defaults to enable 'Ramped Exit from Holdover', but the user needs to select the 'Ramped Input Switching & Exit from Holdover' option when switching between non-synchronized input clocks.The same ramp rate settings are used for both exit from holdover and clock switching. For more information on ramped exit from holdover including the ramp rate, see Section 4.7 Holdover Mode. To ensure that Hitless Input Switching and Ramped Input Switching are optimally configured for a given application, it is strongly advised to use the Hitless Switching Assistant in the "Hitless Input Switching Assistant" page of ClockBuilder Pro.

Table 5.6. Ramped Switching Decision Matrix

Frequency Difference between Input Frequencies	f_{Pfd} > 500 kHz	f_{Pfd} < 500 kHz
Zero PPM	Select "Ramped Exit from Holdover"	
Non-Zero PPM	If difference is: • Less than 10 ppm, select "Ramped Exit from Holdover". • More than 10 ppm, select "Ramped input switching and Ramped Exit from Holdover".	Select "Ramped input switching and Ramped Exit from Holdover".

Table 5.7. Ramped Input Switching Control Registers

Setting Name	Hex Address [Bit Field]	Function
RAMP_SWITCH_EN_PLLA	04A6[3]	Enable frequency ramping on an input switch
RAMP_SWITCH_EN_PLLB	05A6[3]	
RAMP_SWITCH_EN_PLLC	06A6[3]	
RAMP_SWITCH_EN_PLLD	07A6[3]	
HSW_MODE_PLLA	043A[1:0]	Input switching mode select
HSW_MODE_PLLB	053A[1:0]	
HSW_MODE_PLLC	063A[1:0]	
HSW_MODE_PLLD	073A[1:0]	

5.2.5 Hitless Switching, LOL (Loss of Lock) and Fastlock

When doing a clock switch between clock inputs that are frequency locked, LOL may be momentarily asserted. In such cases, the assertion of LOL will invoke Fastlock. Because Fastlock temporarily increases the loop BW by asynchronously inserting new filter parameters into the DSPLL's closed loop, there may be transients at the clock outputs when Fastlock is entered or exited. For this reason, it is suggested that automatic entry into Fastlock be disabled by writing a zero to FASTLOCK_AUTO_EN_PLLx whenever a clock switch might occur.

5.2.6 External Clock Switching

When applications require an external switch, it is difficult for the PLL to predict when that switch will occur. The Si5397/96 will temporarily go into holdover and then exit in a controlled manner to have a minimum phase/frequency transient. If expansion beyond the maximum number of inputs is required, please see AN1111: DSPLL Input Clock Expander which describes how an external FPGA can be used for this purpose.

5.2.7 Synchronizing to Gapped Input Clocks

The DSPLL supports locking to an input clock with missing clock edges. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its edges. Gapping a clock significantly increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of 2 missing cycles out of every 8. Gapped input clocks are not recommended for use with Hitless Switching, as the output phase transients may be significantly higher.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification for a maximum phase transient, when the switch occurs during a gap in either input clocks. The following figure shows a 100 MHz clock with one cycle removed every 10 cycles, which results in a 90 MHz periodic non-gapped output clock.

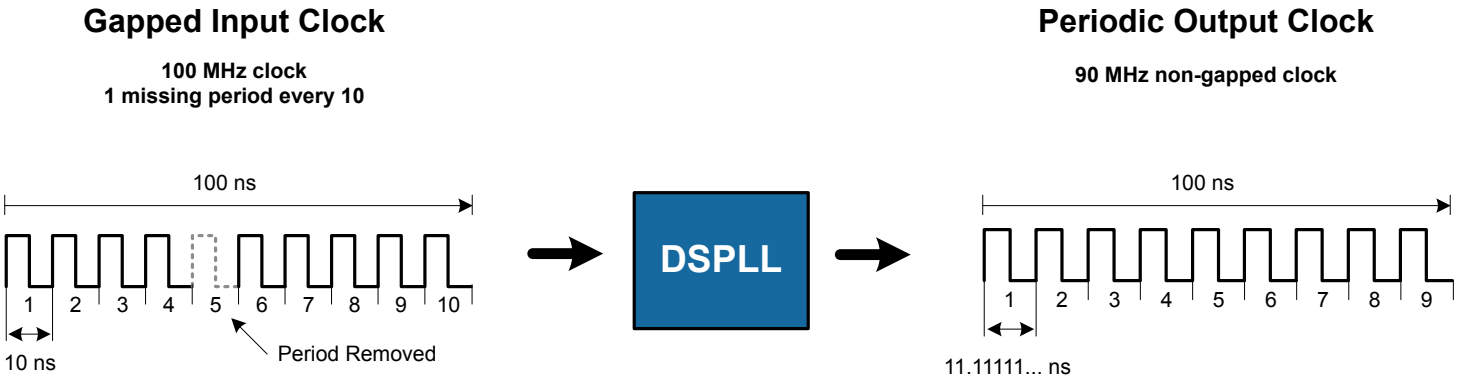


Figure 5.4. Gapped Input Clock Use

5.2.8 Rise Time Considerations

It is well known that slow rise time signals with low slew rates are a cause of increased jitter. Although the low loop BW of the Si5397/96 will attenuate a good portion of the jitter that is associated with a slow rise time clock input, if the slew rate is low enough, the output jitter will increase. The following figure shows the effect of a low slew rate on RMS jitter for a differential clock input. It shows the relative increase in the amount of RMS jitter due to slow rise time and is not intended to show absolute jitter values.

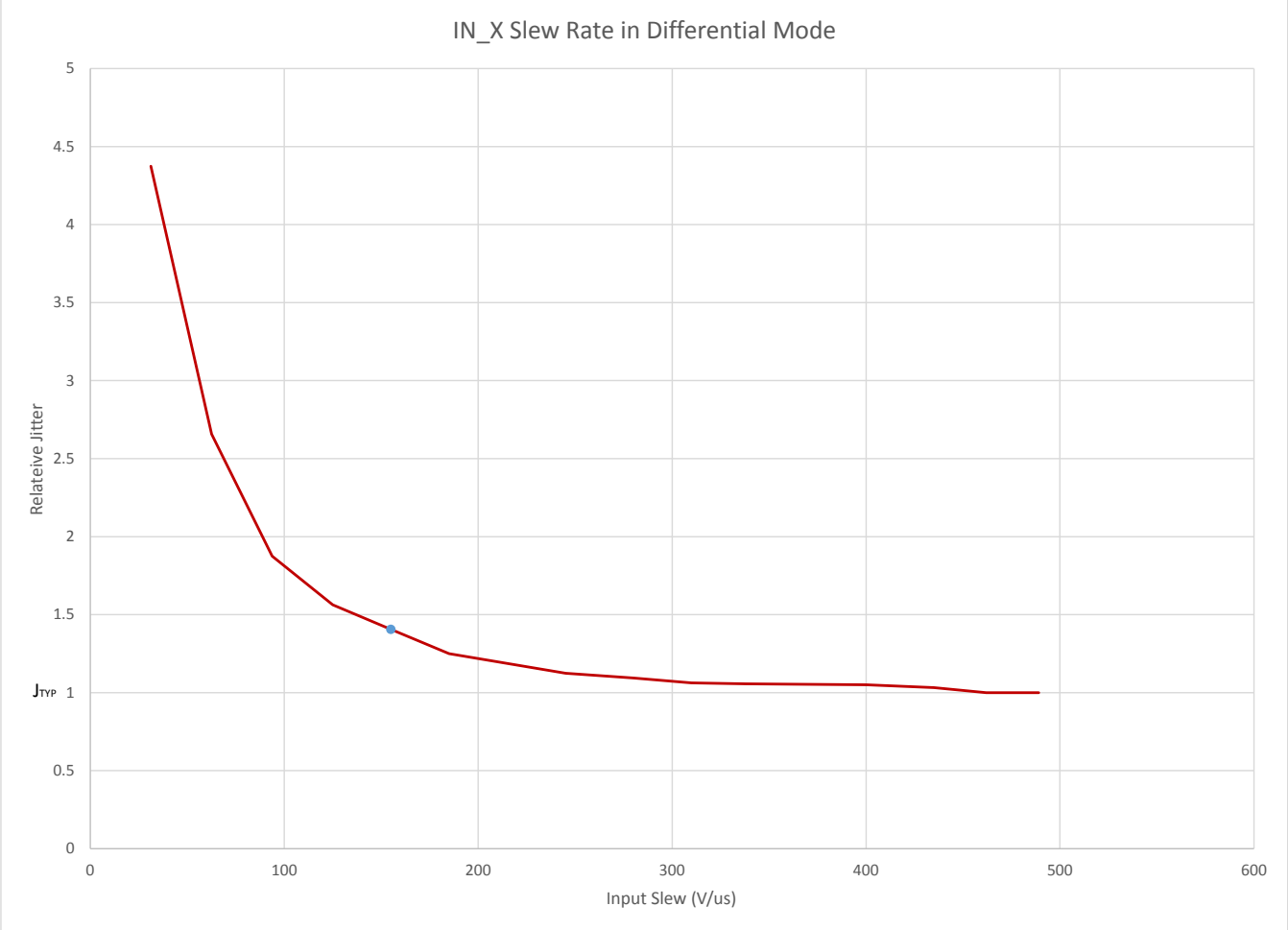


Figure 5.5. Effect of Low Slew Rate on RMS Jitter

5.3 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. There is a Loss Of Lock (LOL) indicator asserted when the DSPLL loses synchronization with its reference input.

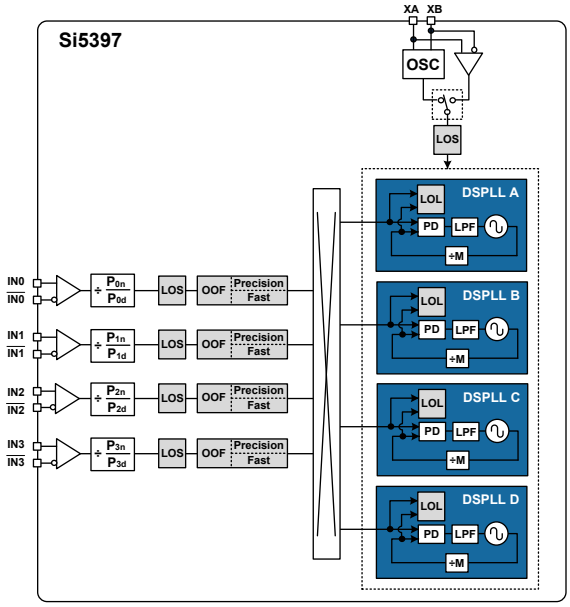


Figure 5.6. Fault Monitors

5.3.1 Input Loss of Signal (LOS) Fault Detection

The loss of signal monitor qualifies the input signal with the following criteria to determine if a valid signal is present. The loss of signal monitor measures the period of each phase detector input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits compares the measured phase detector input period to a maximum and minimum period thresholds. LOS asserts if the maximum input period threshold is exceeded or if the input period is less than the minimum input period threshold. The thresholds for assert and de-assert of LOS are specified in a number of corresponding clock cycles at the input to the phase detector which is the input clock divided by it's corresponding P divider. This is translated to a time based on the frequency of the corresponding phase detector input clock. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

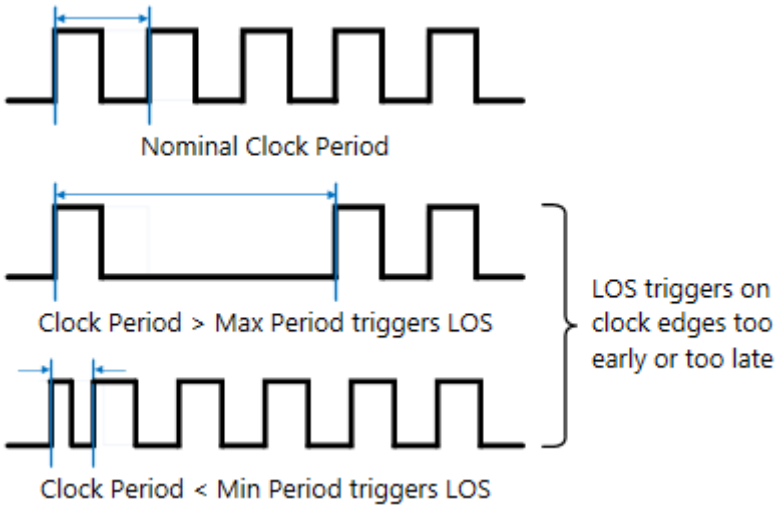


Figure 5.7. LOS Clock Maximum (Trigger) and Minimum (Clear) Period Thresholds

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register when set, always stays asserted until cleared by the user.

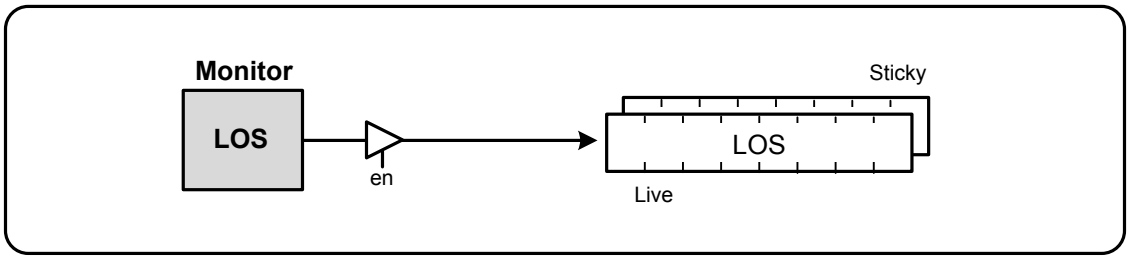


Figure 5.8. LOS Status Indicators

A LOS monitor is also available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when LOSXAXB is detected. This feature can be disabled such that the device will continue to produce output clocks even when LOSXAXB is detected. Single-ended inputs must be connected to the XA input pin with the XB pin terminated properly for LOSXAXB to function correctly. The table below lists the loss of signal status indicators and fault monitoring control registers.

Table 5.8. Loss of Signal Status Monitoring and Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
LOS Status Indicators			
LOS(3,2,1,0)	000D[3:0]	000D[3:0]	LOS status monitor for IN3, IN2, IN1, IN0. Indicates if a valid clock is detected or if a LOS condition is present.
LOSXAXB	000C[1]	000C[1]	LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
LOS(3,2,1,0)_FLG	0012[3:0]	0012[3:0]	LOS status monitor sticky bits for IN3, IN2, IN1, IN0. Sticky bits will remain asserted when an LOS event occurs until they are cleared. Writing a zero to a sticky bit will clear it.
LOSXAXB_FLG	0011[1]	0011[1]	LOS status monitor sticky bits for XAXB. Sticky bits will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS Fault Monitor Controls and Settings			
LOS(3,2,1,0)_EN	002C[3:0]	002C[3:0]	LOS monitor enable for IN3, IN2, IN1, IN0. Allows disabling the monitor if unused.
LOS(3,2,1,0)_TRG_THR	002E[7:0] - 0035[7:0]	002E[7:0] - 0035[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN3, IN2, IN1, IN0. These 16-bit values are determined with the ClockBuilder Pro utility. The trigger threshold sets the maximum period and the clear threshold sets the minimum period.
LOS(3,2,1,0)_CLR_THR	0036[7:0] - 003D[7:0]	0036[7:0] - 003D[7:0]	

5.3.2 Out of Frequency (OOF) Fault Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its 0 ppm reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure directly below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

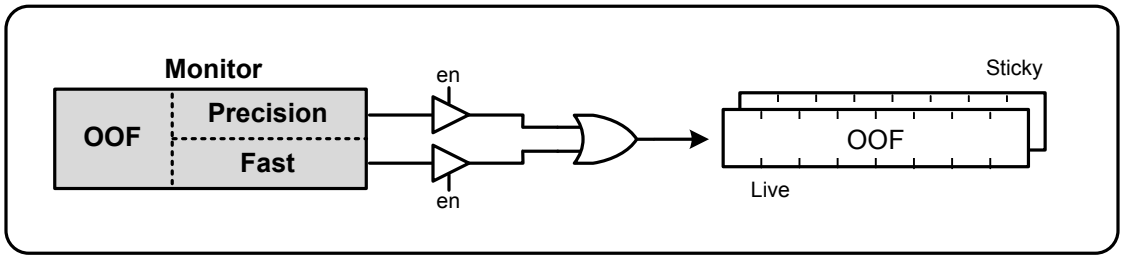


Figure 5.9. OOF Status Indicator

The Precision OOF monitor circuit measures the frequency of all input clocks to within up to ±0.0625 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of from ±0.0625 ppm to ±512 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XAXB pins is available. These options are all register configurable.

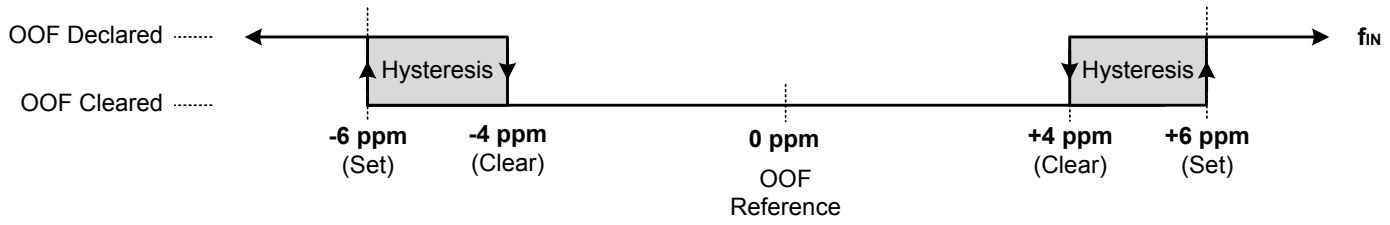


Figure 5.10. Example of Precise OOF Monitor Assertion and De-assertion Triggers

The table below lists the OOF monitoring and control registers. Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF responds more quickly and has larger thresholds.

Table 5.9. Out-of-Frequency Status Monitoring and Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
OOF Status Indicators			
OOF(3,2,1,0)	000D[7:4]	000D[7:4]	OOF status monitor for IN3, IN2, IN1, IN0. Indicates if a valid clock is detected or if a OOF condition is detected.
OOF(3,2,1,0)_FLG	0012[7:4]	0012[7:4]	OOF status monitor sticky bits for IN3, IN2, IN1, IN0. Sticky bits will remain asserted when an OOF event occurs until cleared. Writing a zero to a sticky bit will clear it.
OOF(3,2,1,0)_INTR_MSK	0018[7:4]	0018[7:4]	Marks OOF from generating INTRb interrupt for IN3-IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt
OOF Monitor Control and Settings			
OOF_REF_SEL	0040[2:0]	0040[2:0]	This selects the clock that the OOF monitors use as their “0 ppm” reference. Selections are: XA/XB, IN0, IN1, IN2, IN3.
OOF(3,2,1,0)_EN	003F[3:0]	003F[3:0]	This allows to enable/disable the precision OOF monitor for IN3, IN2, IN1, IN0.
FAST_OOF(3,2,1,0)_EN	003F[7:4]	003F[7:4]	To enable/disable the fast OOF monitor for IN3, IN2, IN1, IN0.
OOF(3,2,1,0)_SET_THR	0046[7:0] - 0049[7:0]	0046[7:0] - 0049[7:0]	Determines the OOF alarm set threshold for IN3, IN2, IN1, IN0. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm.
OOF(3,2,1,0)_CLR_THR	004A[7:0] - 004D[7:0]	004A[7:0] - 004D[7:0]	Determines the OOF alarm clear threshold for INx. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm.
FAST_OOF(3,2,1,0)_SET_THR	0051[7:0] - 0054[7:0]	0051[7:0] - 0054[7:0]	Determines the fast OOF alarm set threshold for IN3, IN2, IN1, IN0.
FAST_OOF(3,2,1,0)_ CLR_THR	0055 [7:0] - 0058[7:0]	0055 [7:0] - 0058[7:0]	Determines the fast OOF alarm clear threshold for IN3, IN2, IN1, IN0.

5.3.3 Loss of Lock (LOL) Fault Monitoring

There is a loss of lock (LOL) monitor for each of the DSPLLs. The LOL monitor asserts a LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_A, LOL_B, LOL_C, LOL_D). The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear).

A block diagram of the LOL monitor is shown below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

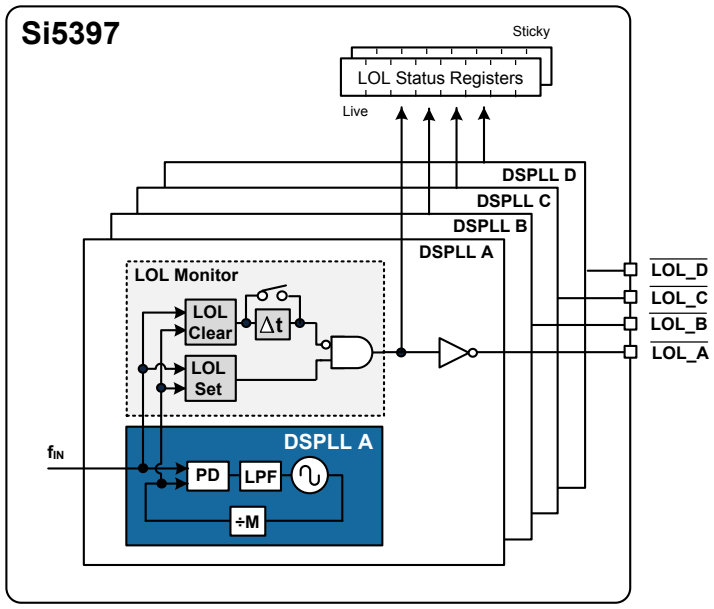


Figure 5.11. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10000 ppm. CBPro provides a wide range of set and clear thresholds for the LOL function. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration of the LOL set and clear thresholds is shown below.

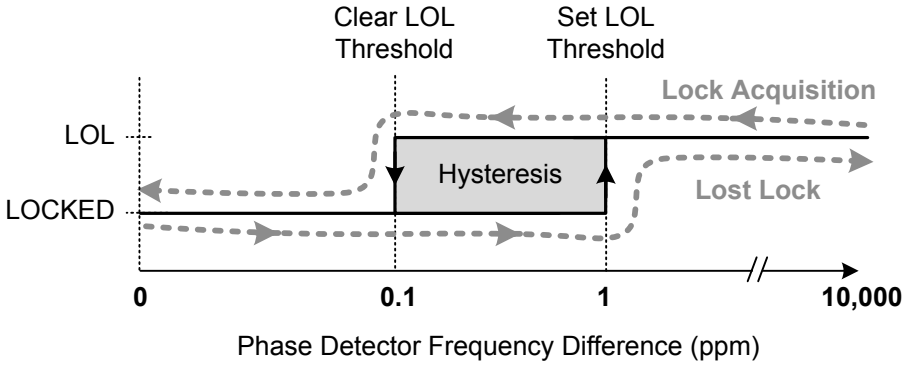


Figure 5.12. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

It is important to know that, in addition to being status bits, LOL optionally enables Fastlock.

Table 5.10. Loss of Lock Status Monitor and Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
LOL Status Indicators			
LOL_PLL(D,C,B,A)	000E[3:0]	000E[1:0]	Status bit that indicates if DSPLL A, B, C, or D is locked to an input clock.
LOL_FLG_PLL(D,C,B,A)	0013[3:0]	0013[1:0]	Sticky bits for LOL_[D,C,B,A]_STATUS register. Writing a zero to a sticky bit will clear it.
LOL Fault Monitor Controls and Settings			
LOL_SET_THR_PLL(D,C,B,A)	009E[7:0] - 009F[7:0]	009E[7:0]	Configures the loss of lock set thresholds for DSPLL A, B, C, D.
LOL_CLR_THR_PLL(D,C,B,A)	00A0[7:0] - 00A1[7:0]	00A0[7:0]	Configures the loss of lock clear thresholds for DSPLL A, B, C, D.
LOL_CLR_DE-LAY_DIV256_PLL(D,C,B,A)	00A4[7:0] - 00B6[7:0]	00A4[7:0] - 00AC[7:0]	This is a 29-bit register that configures the delay value for the LOL Clear delay. Selectable from 4 ns to over 500 seconds. This value depends on the DSPLL frequency configuration and loop bandwidth. It is calculated using the ClockBuilder Pro utility
LOL_TIMER_EN_PLL(D,C,B,A)	00A2[3:0]	00A2[1:0]	Allows bypassing the LOL Clear timer for DSPLL A, B, C, D. 0- bypassed, 1-enabled

The settings in the table above are handled by ClockBuilder Pro. Manual settings should be avoided.

5.3.4 Interrupt Pin (INTR)

An interrupt pin (INTR) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

Table 5.11. Interrupt Mask Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
LOS(3, 2, 1, 0)_INTR_MSK	0018[3:0]	0018[1:0]	Prevents IN3, IN2, IN1, IN0 LOS from asserting the INTR pin
OOF(3, 2, 1, 0)_INTR_MSK	0018[7:4]	0018[5:4]	Prevents IN3, IN2, IN1, IN0 OOF from asserting the INTR pin
LOSXAXB_INTR_MSK	0017[1]	0017[1]	Prevents XAXB LOS from asserting the INTR pin
LOL_INTR_MSK_PLL(D,C,B,A)	0019[3:0]	0019[1:0]	Prevents DSPLL D, C, B, A LOL from asserting the INTR pin
HOLD_INTR_MSK_PLL(D,C,B,A)	0019[7:4]	0019[5:4]	Prevents DSPLL D, C, B, A HOLD from asserting the INTR pin

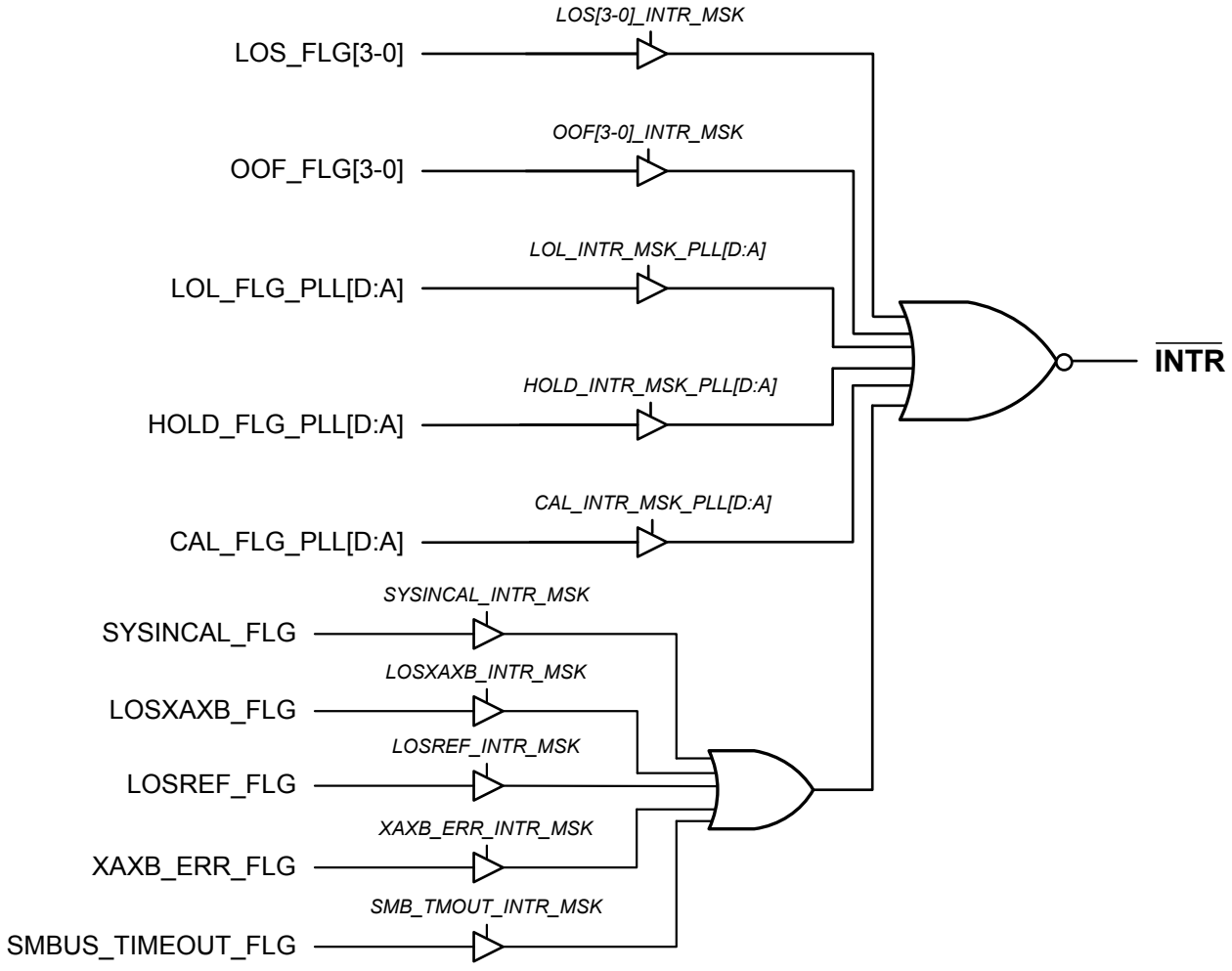


Figure 5.13. Interrupt Triggers and Masks

The _FLG bits are “sticky” versions of the alarm bits and will stay high until cleared. A _FLG bit can be cleared by writing a zero to the _FLG bit. When a _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTR pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannot be cleared.

Note: The INTR pin may toggle during reset.

6. Outputs

The Si5397 supports four or eight differential output drivers and the Si5396 supports four or twelve differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, with CML-compatible amplitudes. In addition to supporting differential signals, any of the outputs can be configured as dual single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

6.1 Output Crosspoint Switch

A crosspoint switch allows any of the output drivers to connect with any of the MultiSynths as shown in Figure 6.1 MultiSynth to Output Driver Crosspoint on page 38. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up. Any MultiSynth output can connect to multiple output drivers.

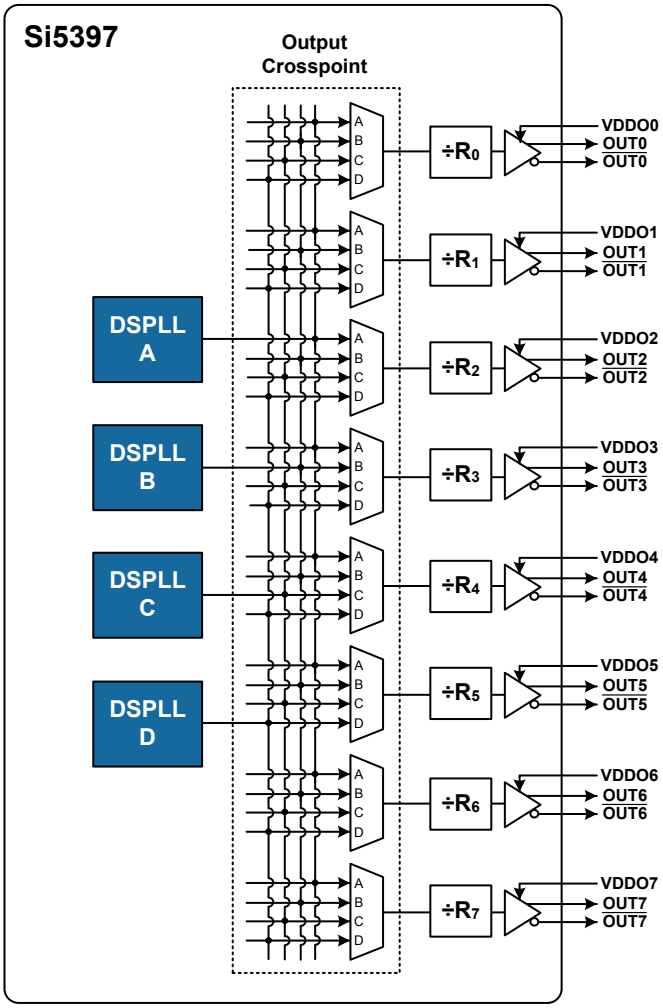


Figure 6.1. MultiSynth to Output Driver Crosspoint

The figure above is used to set up the routing from the MultiSynth frequency selection to the output.

Table 6.1. Output Driver Crosspoint Configuration Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_MUX_SEL	—	—	—	0x106[2:0]	Selects the DSPLL that each of the outputs are connected to. Options are DSPLL_A, DSPLL_B, DSPLL_C, or DSPLL_D
OUT0_MUX_SEL	010B[2:0]	010B[2:0]	0115[2:0]	010B[2:0]	
OUT1_MUX_SEL	0115[2:0]	011F[2:0]	011A[2:0]	0110[2:0]	
OUT2_MUX_SEL	011A[2:0]	0129[2:0]	0129[2:0]	0115[2:0]	
OUT3_MUX_SEL	011F[2:0]	012E[2:0]	012E[2:0]	011A[2:0]	
OUT4_MUX_SEL	0129[2:0]	—	—	011F[2:0]	
OUT5_MUX_SEL	012E[2:0]	—	—	0124[2:0]	
OUT6_MUX_SEL	0133[2:0]	—	—	0129[2:0]	
OUT7_MUX_SEL	013D[2:0]	—	—	012E[2:0]	
OUT8_MUX_SEL	—	—	—	0133[2:0]	
OUT9_MUX_SEL	—	—	—	0138[2:0]	
OUT9A_MUX_SEL	—	—	—	013D[2:0]	

6.2 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment. Resetting the device using the RST pin or asserting the hard reset bit 0x001E[1] will give the same result. Soft reset does not affect output alignment.

6.3 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another there will be some amount of crosstalk. The jitter generation of the Si5397/96 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the crosstalk will come from the Si5397/96, and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources since the Si5397/96 must be attached to a board in order to measure jitter.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in following table.

Table 6.2. Example of Output Clock Placement

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	622.08	Not used
5	625	156.25
6	Not used	156.25
7	Not used	625

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. For example, a 155.52 MHz clock should not be placed next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are allowed, and these outputs should be grouped together when possible. Noting that because 155.52 MHz x 4 = 622.08 MHz, it is okay to place the pair of these frequency values close to one another.
3. Unused outputs can be used to separate clock outputs that might otherwise interfere with one another.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, they generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided in jitter-sensitive applications. When CMOS clocks are unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see application note, AN862: Optimizing Jitter Performance in Next Generation Internet Infrastructure Systems.

The ClockBuilder Pro Clock Placement Wizard is an easy way to reduce crosstalk for a given frequency plan. This feature can be accessed on the “Define Output Clocks” page of ClockBuilder Pro in the lower left hand corner of the page. It is recommended to use this tool after each project frequency plan change.

6.4 Output Signal Format

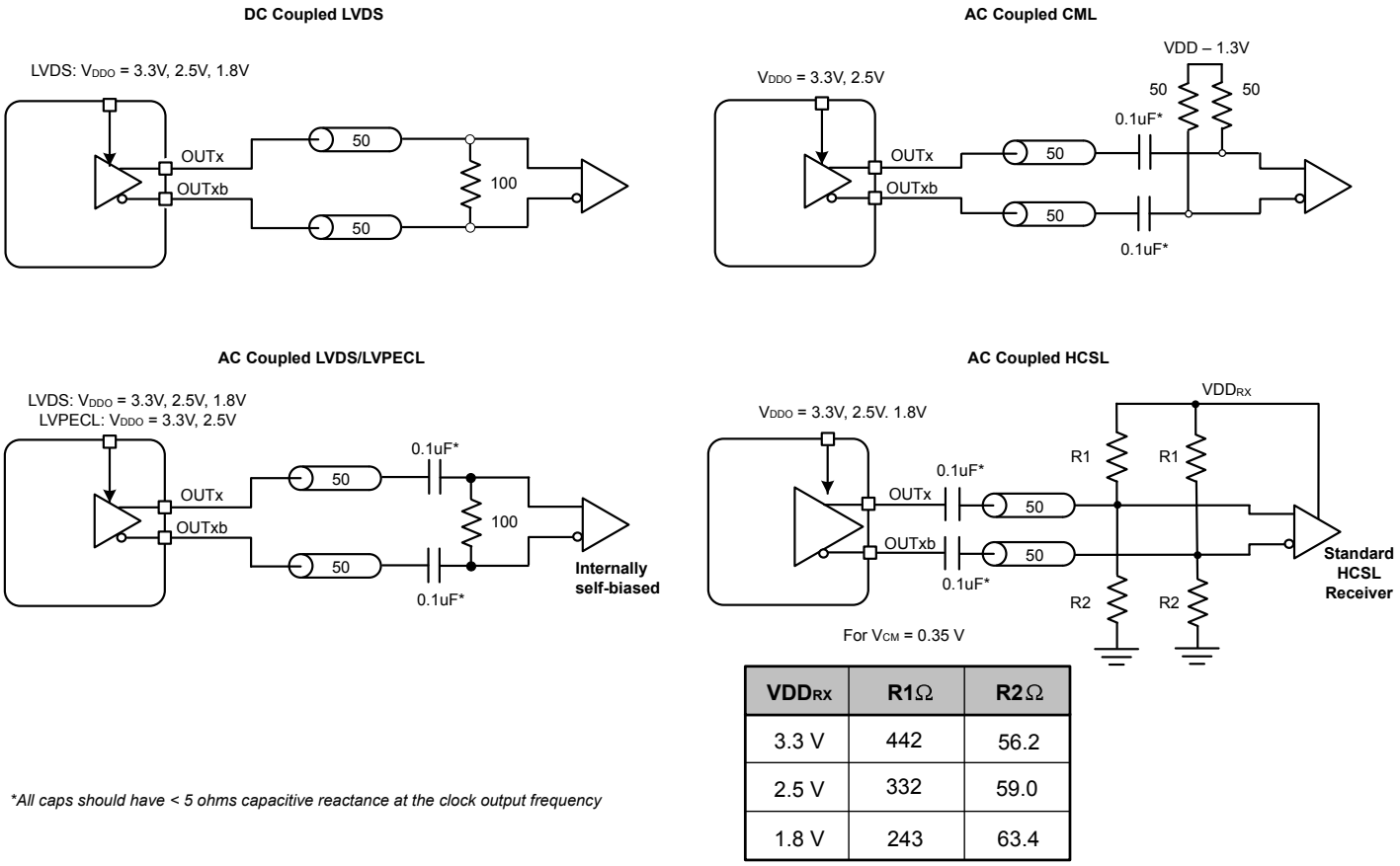
The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL, and HCSL. For CML applications, see Section 6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes. The differential formats can be either normal or low power. Low power format uses less power for the same amplitude but has the drawback of slower rise/fall times. The source impedance in low power format is much higher than 100 Ω. See Section 6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 8 (for the Si5396) single-ended outputs, or any combination of differential and single-ended outputs. Note also that CMOS output can create much more crosstalk than differential outputs so extra care must be taken in their pin replacement so that other clocks that need the lowest jitter are not on nearby pins. See AN862: Optimizing Jitter Performance in Next Generation Internet Infrastructure Systems for additional information.

Table 6.3. Output Signal Format Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_FORMAT	—	—	—	0104[2:0]	Selects the output signal format as differential or LVCMOS.
OUT0_FORMAT	0109[2:0]	0109[2:0]	0113[2:0]	0109[2:0]	
OUT1_FORMAT	0113[2:0]	011D[2:0]	0118[2:0]	010E[2:0]	
OUT2_FORMAT	0118[2:0]	0127[2:0]	0127[2:0]	0113[2:0]	
OUT3_FORMAT	011D[2:0]	012C[2:0]	012C[2:0]	0118[2:0]	
OUT4_FORMAT	0127[2:0]	—	—	011D[2:0]	
OUT5_FORMAT	012C[2:0]	—	—	0122[2:0]	
OUT6_FORMAT	0131[2:0]	—	—	0127[2:0]	
OUT7_FORMAT	013B[2:0]	—	—	012C[2:0]	
OUT8_FORMAT	—	—	—	0131[2:0]	
OUT9_FORMAT	—	—	—	0136[2:0]	
OUT9A_FORMAT	—	—	—	013B[2:0]	

6.4.1 Differential Output Terminations

The differential output drivers support both ac and dc-coupled terminations as shown in the following figure.



VDDRX	R1Ω	R2Ω
3.3 V	442	56.2
2.5 V	332	59.0
1.8 V	243	63.4

*All caps should have < 5 ohms capacitive reactance at the clock output frequency

Figure 6.2. Supported Differential Output Terminations

6.4.2 Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and High (also called low power mode). Each output can support a unique mode.

Differential Normal Swing Mode—This is the usual selection for differential outputs and should be used, unless there is a specific reason to do otherwise. When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. Differential Output Voltage Swing Control Registers lists the registers that control the output voltage swing. The output impedance in the Normal Swing Mode is 100 Ω differential. Any of the terminations shown in Figure 6.2 Supported Differential Output Terminations on page 42 are supported in this mode.

Differential High Swing Mode—When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the terminations shown in Figure 6.2 Supported Differential Output Terminations on page 42 are supported. The use of High Swing mode will result in larger pk-pk output swings that draw less power. The trade off will be slower rise and fall times.

Vpp_diff is 2 x Vpp_se as shown below.

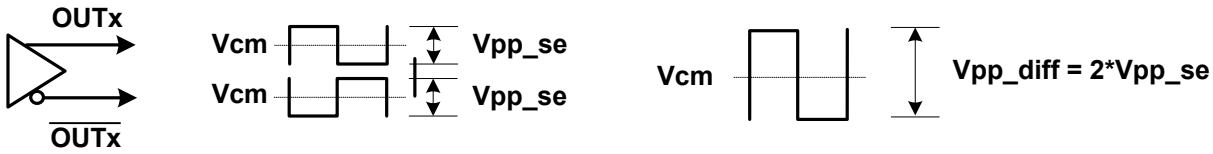


Figure 6.3. Vpp_se and Vpp_diff

Table 6.4. Differential Output Voltage Swing Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_AMPL	—	—	—	0105[6:4]	Sets the differential voltage swing (amplitude) for the output drivers in both normal and low-power modes. See Table 6.10 Settings for LVDS, LVPECL, and HCSL on page 47 for more information.
OUT0_AMPL	010A[6:4]	010A[6:4]	0114[6:4]	010A[6:4]	
OUT1_AMPL	0114[6:4]	011E[6:4]	0119[6:4]	010F[6:4]	
OUT2_AMPL	0119[6:4]	0128[6:4]	0128[6:4]	0114[6:4]	
OUT3_AMPL	011E[6:4]	012D[6:4]	012D[6:4]	0119[6:4]	
OUT4_AMPL	0128[6:4]	—	—	011E[6:4]	
OUT5_AMPL	012D[6:4]	—	—	0123[6:4]	
OUT6_AMPL	0132[6:4]	—	—	0128[6:4]	
OUT7_AMPL	013C[6:4]	—	—	012D[6:4]	
OUT8_AMPL	—	—	—	0132[6:4]	
OUT9_AMPL	—	—	—	0137[6:4]	
OUT9A_AMPL	—	—	—	013C[6:4]	

6.4.3 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc coupling the output drivers. High swing mode may also cause an increase in the rise/fall time.

Table 6.5. Differential Output Common Mode Voltage Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_CM	—	—	—	0105[3:0]	Sets the common mode voltage for the differential output driver. See Table 6.10 Settings for LVDS, LVPECL, and HCSL on page 47 for more information.
OUT0_CM	010A[3:0]	010A[3:0]	0114[3:0]	010A[3:0]	
OUT1_CM	0114[3:0]	011E[3:0]	0119[3:0]	010F[3:0]	
OUT2_CM	0119[3:0]	0128[3:0]	0128[3:0]	0114[3:0]	
OUT3_CM	011E[3:0]	012D[3:0]	012D[3:0]	0119[3:0]	
OUT4_CM	0128[3:0]	—	—	011E[3:0]	
OUT5_CM	012D[3:0]	—	—	0123[3:0]	
OUT6_CM	0132[3:0]	—	—	0128[3:0]	
OUT7_CM	013C[3:0]	—	—	012D[3:0]	
OUT8_CM	—	—	—	0132[3:0]	
OUT9_CM	—	—	—	0137[3:0]	
OUT9A_CM	—	—	—	013C[3:0]	

6.4.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in Figure 6.4 LVCMOS Output Terminations on page 44.

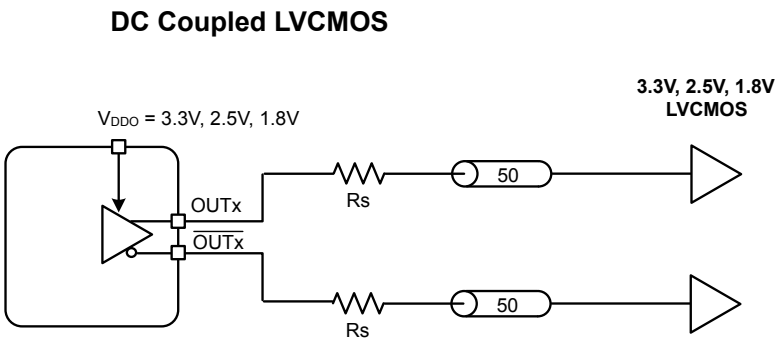


Figure 6.4. LVCMOS Output Terminations

6.4.5 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO option as shown below. The value for the OUTx_CMOS_DRIVE bits are given.

Table 6.6. Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Rs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03[1]	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03[1]	24 Ω	11 mA
1.8 V	0x03[1]	31 Ω	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages.

Table 6.7. LVCMOS Drive Strength Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_CMOS_DRV	—	—	—	0104[7:6]	LVCMOS output impedance.
OUT0_CMOS_DRV	0109[7:6]	0109[7:6]	0118[7:6]	0109[7:6]	
OUT1_CMOS_DRV	0113[7:6]	011D[7:6]	011D[7:6]	010E[7:6]	
OUT2_CMOS_DRV	0118[7:6]	0127[7:6]	0127[7:6]	0113[7:6]	
OUT3_CMOS_DRV	011D[7:6]	012C[7:6]	012C[7:6]	0118[7:6]	
OUT4_CMOS_DRV	0127[7:6]	—	—	011D[7:6]	
OUT5_CMOS_DRV	012C[7:6]	—	—	0122[7:6]	
OUT6_CMOS_DRV	0131[7:6]	—	—	0127[7:6]	
OUT7_CMOS_DRV	013B[7:6]	—	—	012C[7:6]	
OUT8_CMOS_DRV	—	—	—	0131[7:6]	
OUT9_CMOS_DRV	—	—	—	0136[7:6]	
OUT9A_CMOS_DRV	—	—	—	013B[7:6]	

6.4.6 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

6.4.7 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTx pin is generated with the same polarity (in phase) with the clock on the OUTxb pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

Table 6.8. LVCMOS Output Polarity Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_INV	—	—	—	0106[7:6]	Controls output polarity of the OUTx and OUTx pins when in LVCMOS mode.
OUT0_INV	010B[7:6]	010B[7:6]	0115[7:6]	010B[7:6]	
OUT1_INV	0115[7:6]	011F[7:6]	011A[7:6]	0110[7:6]	
OUT2_INV	011A[7:6]	0129[7:6]	0129[7:6]	0115[7:6]	
OUT3_INV	011F[7:6]	012E[7:6]	012E[7:6]	011A[7:6]	
OUT4_INV	0129[7:6]	—	—	011F[7:6]	
OUT5_INV	012E[7:6]	—	—	0124[7:6]	
OUT6_INV	0133[7:6]	—	—	0129[7:6]	
OUT7_INV	013D[7:6]	—	—	012E[7:6]	
OUT8_INV	—	—	—	0133[7:6]	
OUT9_INV	—	—	—	0138[7:6]	
OUT9A_INV	—	—	—	013D[7:6]	

Table 6.9. Output Polarity of OUTx and OUTxb Pins in LVCMOS Mode

OUTx_INV Register Settings	OUTx	OUTxb	Comment
00	CLK	CLK	Both in phase (default)
01	CLK	CLKb	OUTxb inverted
10	CLKb	CLK	OUTx and OUTxb inverted
11	CLKb	CLKb	OUTx inverted

6.4.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

- Normal or Low Power Format
- Amplitude (sometimes called Swing)
- Common Mode Voltage
- Stop High or Stop Low

The normal Format setting has a 100 Ω internal resistor between the plus and minus output pins. The Low Power Format setting removes this 100 Ω internal resistor and then the differential output resistance will be > 500 Ω. However as long as the termination impedance matches the differential impedance of the pcb traces the signal integrity across the termination impedance will be good. For the same output amplitude the Low Power Format will use less power than the Normal Format. The Low Power Format also has a lower rise/fall time than the Normal Format. See the Si5397/96 data sheet for the rise/fall time specifications. For LVPECL and LVDS standards, ClockBuilder Pro does not support the Low Power Differential Format. Stop High means that when the output driver is disabled the plus output will be high and the minus output will be low. Stop Low means that when the output driver is disabled the plus output will be low and the minus output will be high.

The Format, Amplitude and Common Mode settings for the various supported standards are shown in Table 6.10 Settings for LVDS, LVPECL, and HCSL on page 47.

Table 6.10. Settings for LVDS, LVPECL, and HCSL

OUTx_FORMAT[1]	Standard	VDDO Volts	OUTx_CM (Decimal)	OUTx_AMPL (Decimal)
001 = Normal Differential	LVPECL	3.3	11	6
001 = Normal Differential	LVPECL	2.5	11	6
002 = Low Power Differential	LVPECL	3.3	11	3
002 = Low Power Differential	LVPECL	2.5	11	3
001 = Normal Differential	LVDS	3.3	3	3
001 = Normal Differential	LVDS	2.5	11	3
001 = Normal Differential	Sub-LVDS[2]	1.8	13	3
002 = Low Power Differential	LVDS	3.3	3	1
002 = Low Power Differential	LVDS	2.5	11	1
002 = Low Power Differential	Sub-LVDS[2]	1.8	13	1
002 = Low Power Differential	HCSL[3]	3.3	11	3
002 = Low Power Differential	HCSL[3]	2.5	11	3
002 = Low Power Differential	HCSL[3]	1.8	13	3

Note:

1. The low-power format will cause the rise/fall time to increase by approximately a factor of two. See the Si5397/96 data sheet for more information.
2. The common-mode voltage produced is not compliant with LVDS standards; therefore ac coupling the driver to an LVDS receiver is highly recommended.
3. Creates HCSL compatible signal.

The output differential driver can produce a wide range of output amplitudes that includes CML amplitudes. See Section 6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes for additional information.

6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes

In some applications, it may be desirable to have larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings, as selected by CBPro. In these cases, the following information describes how to implement these amplitudes by writing to the OUTx_CM and OUTx_AMPL setting names. Contact Silicon Labs for assistance if you want your custom configured device to be programmed for any of the settings described here.

The differential output driver has a variable output amplitude capability and two basic formats, normal and low-power format. The difference between these two formats is that the normal format has an output impedance of ~100 Ω differential, and the low-power format has an output impedance of > 500 Ω differential. Note that the rise/fall time is slower when using the Low Power Differential Format. See the Si5397/96 data sheet for rise/fall time specifications.

If the standard LVDS or LVPECL compatible output amplitudes will not work for a particular application, the variable amplitude capability can be used to achieve higher or lower amplitudes. For example, a “CML” format is sometimes desired for an application. However, CML is not a defined standard, and hence the amplitude of a CML signal for one receiver may be different than that of another receiver.

When the output amplitude needs to be different than standard LVDS or LVPECL, the Common Mode Voltage settings must be set as shown in Table 6.11 Output Differential Common Mode Voltage Settings on page 48. No settings other than these are supported as the signal integrity could be compromised. In addition, the output driver should be ac-coupled to the load so that the common-mode voltage of the driver is not affected by the load.

Table 6.11. Output Differential Common Mode Voltage Settings

VDDOx (Volts)	Differential Format	OUTx_FORMAT	Common Mode Voltage (Volts)	OUTx_CM
3.3	Normal	0x1	2.0	0xB
3.3	Low Power	0x2	1.6	0x7
2.5	Normal	0x1	1.3	0xC
2.5	Low Power	0x2	1.1	0xA
1.8	Normal	0x1	0.8	0xD
1.8	Low Power	0x2	0.8	0xD

The differential amplitude can be set as shown in the following table.

Table 6.12. Typical Differential Amplitudes[1]

OUTx_AMPL	Normal Differential Format (Vpp SE mV – Typical)	Low-Power Differential Format (Vpp SE mV – Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[2]
7	920	1600[2]

Note:
1. These amplitudes are based upon a 100 Ω differential termination.
2. In low-power mode and VDDOx = 1.8 V, OUTx_AMPL may not be set to 6 or 7.

Note: High-Speed Differential Mode in ClockBuilder Pro output setting page sets OUTx_AMP to 7 in order to compensate for channel loss at high frequency.

See the register map portion of this document for additional information about OUTx_FORMAT, OUTx_CM and OUTx_AMPL. Contact Silicon Labs for assistance if you require a factory-programmed device to be configured for any of the output driver settings listed above.

6.5 Output Enable/Disable

The Si5397/96 allows enabling/disabling outputs by either pin, register control, or a combination of both. Two output enable pins are available (OE0b, OE1b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b is unmapped and has no affect until configured.

To use the pin control to map the outputs to different OE pins do the following:

1. Set register 0x0022[0] = 0 to enable using OExb pins to control the outputs.
2. Set the mask registers to map the outputs to the OExb pins. The OExb mask registers are used to configure the outputs to be controlled by the specific OExb pins (logic 1) or not controlled (logic 0). Note that the same bit of OExb mask registers should not be set at the same time otherwise the corresponding output will be disabled no matter OExb pin inputs. Registers 0x0023[0:7], 0x0024[8:15] are used to control bits 0-15 for the output masks for OEB0 and 0x0025[0:7], 0x0026[8:15] to control the same bits 0-15 for the output masks for OEB1.

Example Si5397A/B: 8 output part

OUT0-Enable to control Out 1,3,5,7 and **OUT1-Enable** to control Out 0,2,4,6

OExb Mask Registers Bits Mapping to Outputs for Si5397A/B								
	OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
	BIT11	**BIT9**	**BIT8**	**BIT7**	**BIT5**	**BIT4**	**BIT3**	**BIT1**
OE0b Mask Registers (Low byte address: 0x0023h High byte address: 0x0024h)	1	0	1	0	1	0	1	0
OE1b Mask Registers (Low byte address: 0x0025h High byte address: 0x0026h)	0	1	0	1	0	1	0	1

Example Si5397C/D: 4 output part

Out0-Enable to control Out 1,2,3 **Out 1-Enable** to control Out 0

OExb Mask Registers Bits Mapping to Outputs for Si5397C/D				
	OUT3	**OUT2**	**OUT1**	**OUT0**
	BIT8	**BIT7**	**BIT 5**	**BIT 1**
OE0b Mask Registers (Low byte address: 0x0023h High byte address: 0x0024h)	1	1	1	0
OE1b Mask Registers (Low byte address: 0x0025h High byte address: 0x0026h)	0	0	0	1

Example Si5396C/D: 12 output part

Out0-Enable to control Out 0A,6,7,8,9 **Out 1-Enable** to control Out 1,2,3,4,5,9A

OExb Mask Registers Bits Mapping to Outputs for Si5396C/D												
	OUT9A	**OUT9**	**OUT8**	**OUT7**	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**	**OUT0A**
	BIT11	**BIT10**	**BIT9**	**BIT8**	**BIT7**	**BIT6**	**BIT5**	**BIT4**	**BIT3**	**BIT2**	**BIT1**	**BIT0**
OE0b Mask Registers (Low byte address: 0x0023h High byte address: 0x0024h	0	1	1	1	1	0	0	0	0	0	0	1

OExb Mask Registers Bits Mapping to Outputs for Si5396C/D												
OE1b Mask Registers (Low byte address: 0x0025h High byte address: 0x0026h)	1	0	0	0	0	0	1	1	1	1	1	0

Example Si5396A/B: 4 output part

Out0-Enable to control Out 1,2,3 **Out 1-Enable** to control Out 0

OExb Mask Registers Bits Mapping to Outputs for Si5396AB				
	OUT3	**OUT2**	**OUT1**	**OUT0**
	DRV 8	**DRV7**	**BIT 4**	**BIT 3**
OE0b Mask Registers (Low byte address: 0x0023h High byte address: 0x0024h)	1	1	1	0
OE1b Mask Registers (Low byte address: 0x0025h High byte address: 0x0026h)	0	0	0	1

The following are the register controls for enable/disable outputs.

Table 6.13. Output Enable/Disable Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUTALL_DISABLE_LOW	0102[0]	0102[0]	0102[0]	0102[0]	Allows disabling all output drivers: 0 - all outputs disabled, 1 - all outputs controlled by the OUTx_OE bits. Note that if the OE pin is held high (disabled), then all assigned outputs will be disabled regardless of the state of this register bit.

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_OE	—	—	—	0103[1]	Allows enabling/disabling individual output drivers. Note that the OE pin must be held low in order to enable an output with these register bits.
OUT0_OE	0108[1]	0108[1]	0012[1]	0108[1]	
OUT1_OE	0112[1]	011C[1]	0117[1]	010D[1]	
OUT2_OE	0117[1]	0126[1]	0126[1]	0112[1]	
OUT3_OE	011C[1]	012B[1]	012B[1]	0117[1]	
OUT4_OE	0126[1]	—	—	011C[1]	
OUT5_OE	012B[1]	—	—	0121[1]	
OUT6_OE	0130[1]	—	—	0126[1]	
OUT7_OE	013A[1]	—	—	012B[1]	
OUT8_OE	—	—	—	0130[1]	
OUT9_OE	—	—	—	0135[1]	
OUT9A_OE	—	—	—	013A[1]	
OUT_DIS_MSK_LOL_PLL(D,C,B,A)	0142[3:0]	0142[3:0]	0142[1:0]	0142[1:0]	Determines if the outputs are disabled during an LOL condition. 0 = outputs disable on LOL, 1 = outputs remain enabled during LOL (default). This option is independently configured for each DSPLL. See DRVx_DIS_SRC registers.
OUT_DIS_MSK_LOSXAXB	0141[6]	0141[6]	0141[6]	0141[6]	Determines if outputs are disabled during an LOSXAXB condition. 0 = all outputs disabled on LOSXAXB (default), 1 = outputs remain enabled during LOSXAXB condition.
OUT0A_DIS_STATE	—	—	—	0104[5:4]	Sets the state for the outputs when they are disabled. Selectable as: Disable logic low Disable logic high
OUT0_DIS_STATE	0109[5:4]	0109[5:4]	0113[5:4]	0109[5:4]	
OUT1_DIS_STATE	0113[5:4]	011D[5:4]	0118[5:4]	010E[5:4]	
OUT2_DIS_STATE	0118[5:4]	0127[5:4]	0127[5:4]	0113[5:4]	
OUT3_DIS_STATE	011D[5:4]	012C[5:4]	012C[5:4]	0118[5:4]	
OUT4_DIS_STATE	0127[5:4]	—	—	011D[5:4]	
OUT5_DIS_STATE	012C[5:4]	—	—	0122[5:4]	
OUT6_DIS_STATE	0131[5:4]	—	—	0127[5:4]	
OUT7_DIS_STATE	013B[5:4]	—	—	012C[5:4]	
OUT8_DIS_STATE	—	—	—	0131[5:4]	
OUT9_DIS_STATE	—	—	—	0136[5:4]	
OUT9A_DIS_STATE	—	—	—	013B[5:4]	

6.5.1 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high. When the output driver is disabled, the outputs will drive either logic high or logic low, selectable by the user. The output common mode voltage is maintained while the driver is disabled, reducing enable/disable transients. By contrast, powering down the driver rather than disabling it increases output impedance and shuts off the output common mode voltage. For all output drivers connected in the system, it is recommended to use Disable rather than Powerdown to reduce enable/disable common mode transients. Unused outputs may be left unconnected, powered down to reduce current draw, and, with the corresponding VDDOx, left unconnected.

6.5.2 Synchronous Output Enable/Disable Feature

The output drivers provide a selectable synchronous enable/disable feature when OUTx_SYNC_EN = 1. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled or enabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off OUTx_SYNC_EN = 0, the output clock will disable immediately without waiting for the period to complete and will enable immediately without waiting a period to complete. The default state is for the synchronous output disable/enable to be turned on OUTx_SYNC_EN = 1 .

Table 6.14. Synchronous Disable Control Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
OUT0A_SYNC_EN	—	—	—	0104[3]	Selects Synchronous or Asynchronous output c
OUT0_SYNC_EN	0109[3]	0109[3]	0113[3]	0109[3]	ble. 1= synchronous, 0 = asynchronous. Defaul
OUT1_SYNC_EN	0113[3]	011D[3]	0118[3]	010E[3]	synchronous mode.
OUT2_SYNC_EN	0118[3]	0127[3]	0127[3]	0113[3]	
OUT3_SYNC_EN	011D[3]	012C[3]	012C[3]	0118[3]	
OUT4_SYNC_EN	0127[3]	—	—	011D[3]	
OUT5_SYNC_EN	012C[3]	—	—	0122[3]	
OUT6_SYNC_EN	0131[3]	—	—	0127[3]	
OUT7_SYNC_EN	013B[3]	—	—	012C[3]	
OUT8_SYNC_EN	—	—	—	0131[3]	
OUT9_SYNC_EN	—	—	—	0136[3]	
OUT9A_SYNC_EN	—	—	—	013B[3]	

6.6 Output Buffer Supply Voltage Selection

These power supply settings must match the actual VDDOx voltage so that the output driver operates properly.

Table 6.15. OUTx VDD Settings

Setting Name	Description
OUTx_VDD_SEL_EN	These bits are set to 1 and should not be changed
OUTx_VDD_SEL	These bits are set by CBPro to match the expected VDDOx voltage. 0: 3.3 V; 1: 1.8 V; 2: 2.5 V; 3: Reserved

7. Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps given by frequency step words (FSTEPW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in locked mode. Note that the maximum FINC/FDEC update rate, by either hardware or software, is 1 MHz. Each DSPLL being used in DCO mode should have fractional M division enabled by setting the appropriate M_FRAC_EN_PLLx = 0x3B for proper operation.

Note: DCO mode is not available when in free run or when in holdover. A large freq step can assert LOL on the relevant DSPLL. The step sizes and frequency of operation need to be considered with the LOL settings and BW.

Table 7.1. Fractional M Divider Enable Controls

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
M_FRAC_EN_PLLA	0x0421[5:0]	0x0421[5:0]	DSPLL feedback M divider fractional enable. 0x2B: Integer-only division 0x3B Fractional (or Integer) division Required for DCO operation.
M_FRAC_EN_PLLB	0x0521[5:0]	0x0521[5:0]	
M_FRAC_EN_PLLC	0x0621[5:0]	—	
M_FRAC_EN_PLLD	0x0721[5:0]	—	

7.1 Frequency Increment/Decrement Using Pin Controls

Controlling the output frequency with pin controls is available on the Si5397. This feature involves asserting the FINC or FDEC pins to increment or decrement the DSPLL frequency. The DSPLL_SEL pins select which DSPLL output frequency is affected by the frequency change. The DSPLL_SEL pin selection is in the table below and follows the same logic as the register control settings for FSTEP_PLL, register 0x0020[3:2].The frequency step words (FSTEPW) define the amount of frequency change for each FINC or FDEC. The FSTEPW may be written once or may be changed after every FINC/FDEC assertion. Note that the DSPLL_SEL pins are not available on the Si5346. Both the FINC and FDEC inputs are rising-edge-triggered and must meet the data sheet minimum pulse width (PW) specifications.

Note: When the FINC/FDEC pins on the Si5397 are unused, the FDEC pin must be pulled down with an external pull-down resistor or jumper. The FINC pin has an internal pull-down and may be left unconnected when not in use.

Table 7.2. 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	FSTEP_PLL_SINGLE	0: DSPLL_SEL[1:0] pins and bits are disabled. 1: DSPLL_SEL[1:0] pins or FSTEP_PLL bits are enabled. See FSTEP_PLL_REGCTRL
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only functions when FSTEP_PLL_SINGLE = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	3:2	R/W	FSTEP_PLL[1:0] (reg) DSPLL_SEL[1:0] (pin)	Register version of the DSPLL_SEL[1:0] pins. Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: DSPLL B M-divider 2: DSPLL C M-divider 3: DSPLL D M-divider

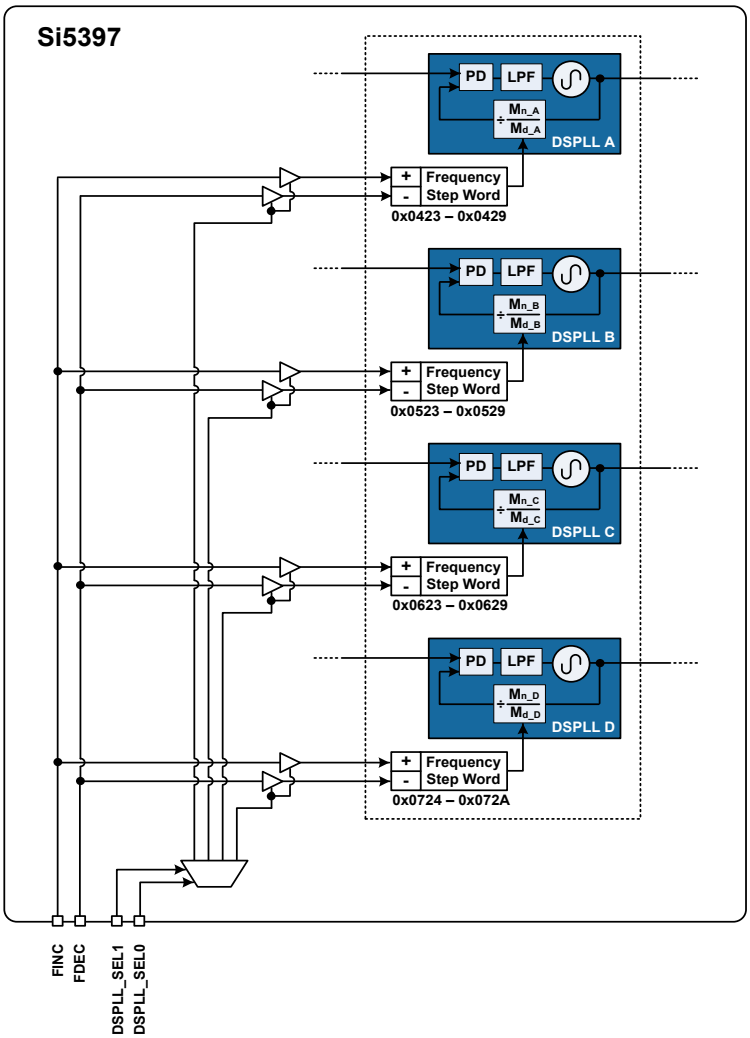


Figure 7.1. Controlling the DCO Mode By Pin Control

7.2 Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available on both the Si5397 and Si5396. This can be performed by asserting the FINC or FDEC bits to activate the frequency change defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affect by the frequency change. The FINC and FDEC pins can also be used to trigger a frequency change. Note that both the FINC and FDEC register bits are rising-edge-triggered and self-clearing.

Each DSPLL being used in DCO mode should have fractional M division enabled by setting the appropriate M_FRAC_EN_PLLx=0x3B for proper operation. See AN909: DCO Application with the Jitter Attenuators for related information.

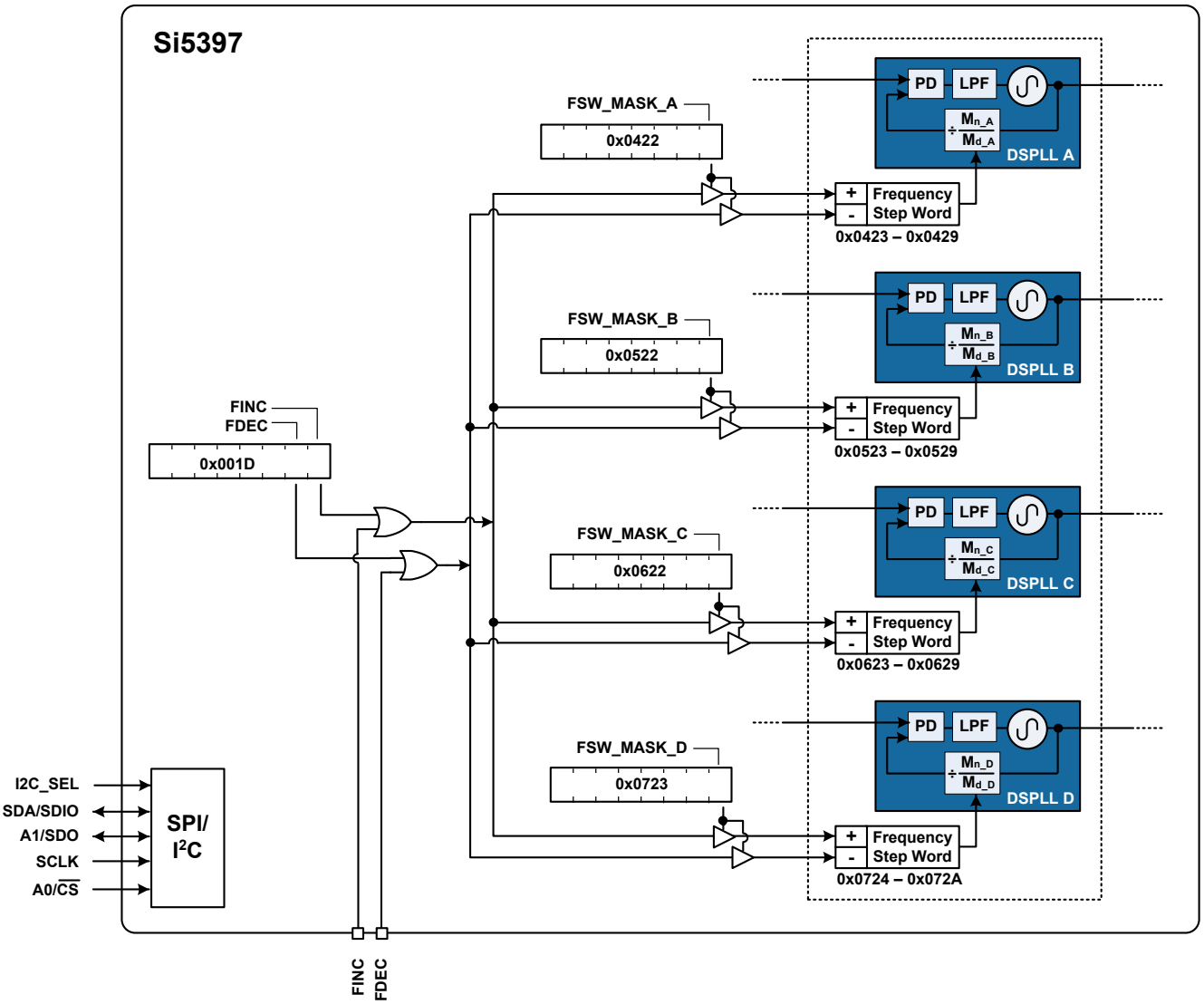


Figure 7.2. Controlling the DCO Mode Using the Serial Interface

Table 7.3. Frequency Increment/Decrement Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
FINC	001D[0]	001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	001D[1]	001D[1]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
M_FSTEPW_PLLA	0423[7:0] - 0429[7:0]	0423[7:0] - 0429[7:0]	This is a 56-bit frequency step word for DSPLL A, B, C, D. The FSTEPW will be added or subtracted to the DSPLL output frequency during assertion of the FINC/FDEC bits or pins. The FSTEPW is calculated based on the frequency configuration and is easily calculated using ClockBuilder Pro utility.
M_FSTEPW_PLLB	0523[7:0] - 0529[7:0]	0523[7:0] - 0529[7:0]	
M_FSTEPW_PLLC	0623[7:0] - 0629[7:0]	—	
M_FSTEPW_PLLD	0724[7:0] - 072A[7:0]	—	
M_FSTEP_MSK_PLLA	0422[0]	0422[0]	This mask bit determines if a FINC or FDEC affects DSPLL A, B, C, D. 0 = FINC/FDEC will increment/decrement the FSTEPW to the DSPLL. 1 = Ignores FINC/FDEC.
M_FSTEP_MSK_PLLB	0522[0]	0522[0]	
M_FSTEP_MSK_PLLC	0622[0]	—	
M_FSTEP_MSK_PLLD	0723[0]	—	
M_FRAC_EN_PLLA	0x0421[5:0]	0x0421[5:0]	DSPLL feedback M divider fractional enable.
M_FRAC_EN_PLLB	0x0521[5:0]	0x0521[5:0]	0x2B: Integer-only division
M_FRAC_EN_PLLC	0x0621[5:0]	—	0x3B: Fractional (or Integer) division
M_FRAC_EN_PLLD	0x0721[5:0]	—	Required for DCO operation.

7.2.1 DCO with Direct Register Writes

In addition to the register-based FINC/FDEC described above, updated values for the DSPLL feedback M divider value may be updated directly by the user. When the M divider numerator (Mx_NUM) and its corresponding update bit (Mx_UPDATE) is written, the new numerator value will take effect and the output frequency will change without any glitches. The M divider numerator and denominator terms (Mx_NUM and Mx_DEN) can be left and right-shifted so that the least significant bit of the numerator word represents the exact step resolution that is needed for your application. Each individual M divider has its own update bit (Mx_UPDATE) that must be written to cause the new numerator value to take effect. All M dividers can be updated at the same time by issuing a Soft Reset.

Changing the DSPLL feedback M divider value while the device is operating will not generate any glitches on affected outputs. The frequency settling to the new value will be determined by the Loop BW of the DSPLL. All other outputs generated by other DSPLLs will be unaffected by this update. It is generally recommended to avoid dynamically changing the M divider denominator (Mx_DEN) as, in some cases, a small output phase shift may be observed when the update becomes active. However, by using the proper combination of settings for the particular frequency plan, it is possible to avoid this entirely. If your application requires dynamic changes to an M divider denominator, contact Silicon Labs at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx.

Table 7.4. Direct DCO Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5397	Si5396	
M_NUM_PLLA	0x0415–0x041B	0x0415–0x041B	56-bit DSPLL feedback M divider Numerator.
M_NUM_PLLB	0x0515–0x051B	0x0515–0x051B	
M_NUM_PLLC	0x0615–0x061B	—	
M_NUM_PLLD	0x0716–0x071C	—	
M_DEN_PLLA	0x041C–0x041F	0x041C–0x041F	32-bit DSPLL feedback M divider Denominator.
M_DEN_PLLB	0x051C–0x051F	0x051C–0x051F	
M_DEN_PLLC	0x061C–0x061F	—	
M_DEN_PLLD	0x071D–0x0720	—	
M_UPDATE_PLLA	0x0420[0]	0x0420[0]	Must write a 1 to this bit to cause the individual M divider changes to take effect. Note that a corresponding SOFT_RST_PLLx or device SOFT_RST will also update the M divider values.
M_UPDATE_PLLB	0x0520[0]	0x0520[0]	
M_UPDATE_PLLC	0x0620[0]	—	
M_UPDATE_PLLD	0x0721[0]	—	

8. Frequency-On-The-Fly for Si5397/96

Some applications require characteristics like input frequency to be modified while leaving clocks from other DSPLLs unaffected. This Frequency-On-The-Fly functionality is fully supported by Si5397 hardware with the help of CBPro Command Line Interface (CLI) tool. Frequency-On-The-Fly allows user to:

- Reconfigure the input frequency, output frequency, bandwidth, and LOL/OOF thresholds of a certain DSPLL. The clock output of the target DSPLL is disabled during the reconfiguration, but the functionalities (for example, freerun, holdover, lock acquisition, hitless switching) remain the same after it is done.
- Leave all other DSPLLs undisturbed, which means that all clock functions, like phase noise and lock status, remain the same.

Detailed explanation on how to set up Frequency-On-The-Fly with CLI tool is included in these two documents: “CBPro Tools & Support for In-System Programming” & “CLI User’s Guide”

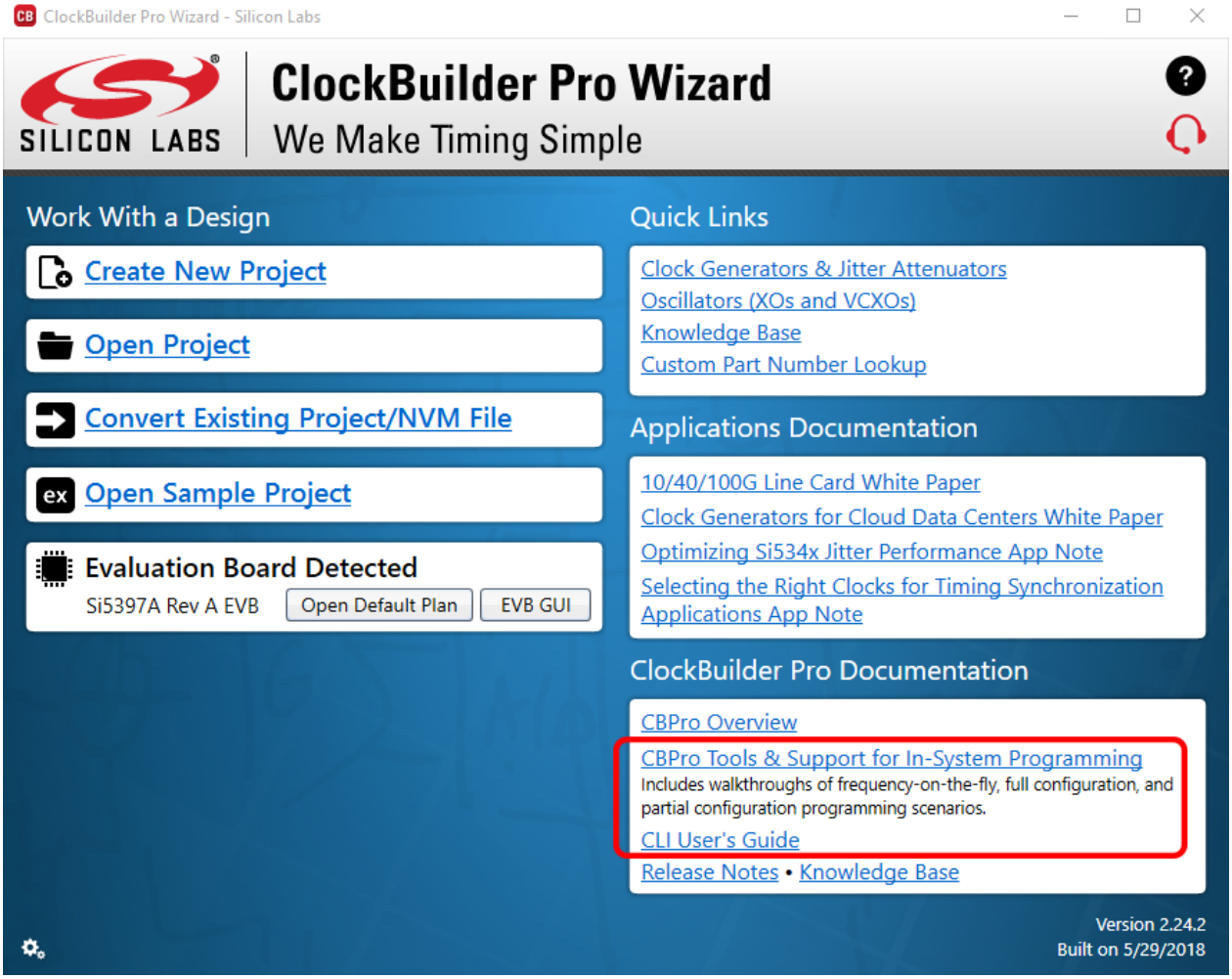


Figure 8.1. CBPro Tools & Support for In-System Programming

The following steps outline the procedure to initiate Frequency-On-The-Fly:

1. Create CBPro project as base frequency plan.

2. Create text files detailing the input/output frequency, bandwidth, and/or LOL/OOF thresholds of new plans. Plans are defined independently for each PLL.

3. Use CLI FOTF tool (create a batch script) to auto generate register files for switching among different plans.

The CLI FOTF tool optimizes the VCO frequency for all of the plans “CLI User’s Guide” includes more in-depth and detailed syntax explanation and function definition. Example files are bundled in CBPro at C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro \CLI\Samples\FOTF-For-Multi-PLL-Device.

For a more detailed information on this procedure, refer to “CBPro Tools & Support for In-System Programming” on the CBPro main page. Note that the frequency plan cannot allow an input to be shared with multiple PLLs. If an input is shared across multiple PLLs an error will be raised. The tool enforces this restriction.

FOTF can technically mean not changing input or output frequencies and instead only reconfiguring one of OOF, LOS or bandwidth. A plan file only has to reconfigure *at least one* of the following:

Clock output frequency

Clock input frequency

DSPLL bandwidth

LOL thresholds

OOF thresholds

On multi-DSPLL devices, frequency-on -the-fly can only be performed on a PLL that has exclusive clock inputs. That is, an input to the FOTF PLL cannot also be MUXed to another DSPLL. For example, given the following configuration:
Refer to AN1178: Frequency-On-the-Fly for Silicon Labs Jitter Attenuators and Clock Generators.

9. Serial Interface

Configuration and operation of the Si5397/96 is controlled by reading and writing registers using the I²C or SPI serial interface. The I2C_SEL pin selects between I²C or SPI operation. The Si5397/96 supports communication with either a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire (default) or 3-wire by setting the SPI_3WIRE configuration bit. See the figure below for supported modes of operation and settings. The I²C pins are open drain and are ESD clamped to 3.3 V, regardless of the host supply level. The I²C pins are clamped to 3.3 V so that they may be externally pulled up to 3.3 V regardless of IO_VDD_SEL (in register 0x0943).

The table below lists register settings of interest for the I²C/SPI.

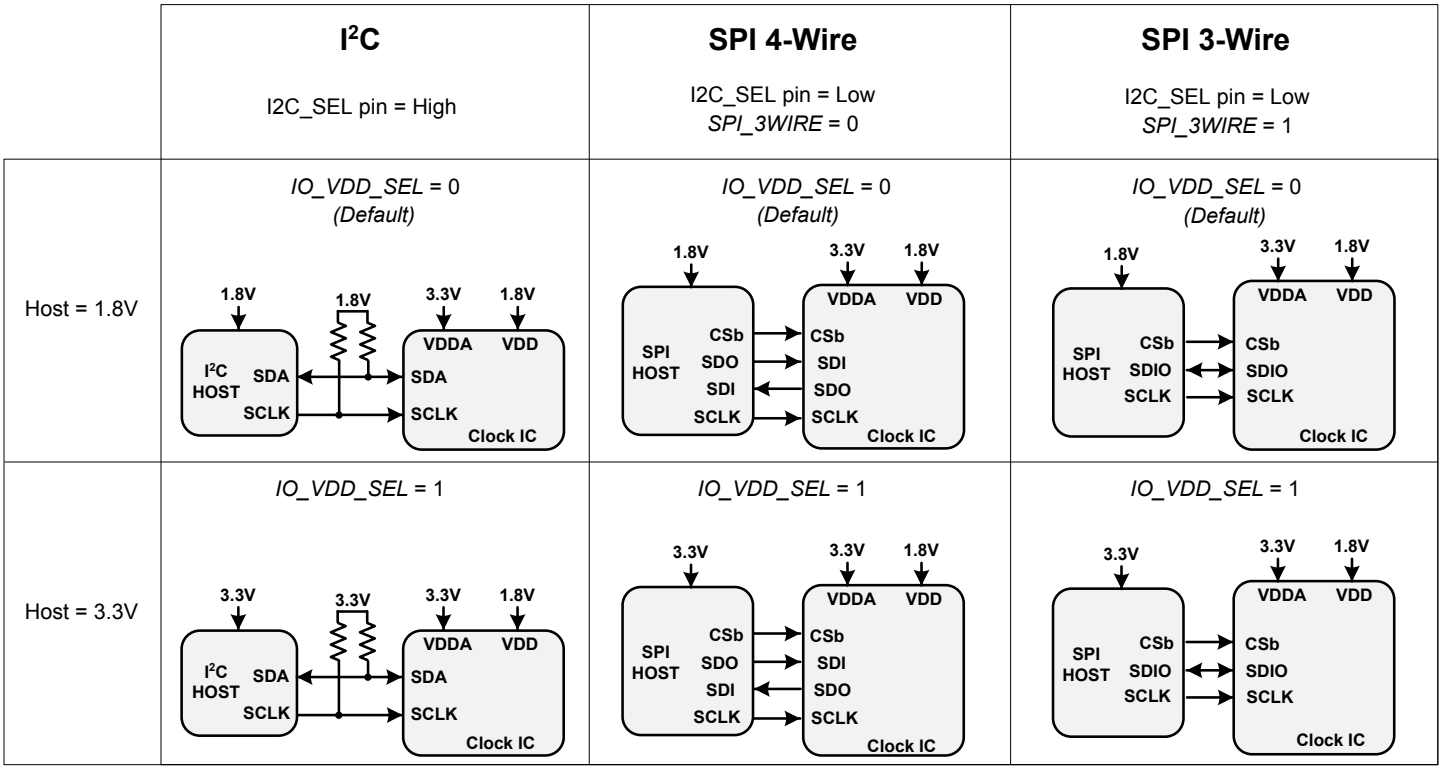


Figure 9.1. I²C/SPI Device Connectivity Configurations

If neither serial interface is used, leave I2C_SEL unconnected. Pull pins SDA/SDIO, SCLK, A1/SDO, and A0/CS all low.

Note that the Si5397/96 is not I²C fail-safe upon loss of power. Applications that require fail-safe operation should isolate the device from a shared I²C bus.

Table 9.1. I²C/SPI Register Settings

Setting Name	Hex Address [Bit Field]	Function
	Si5397/96	
IO_VDD_SEL	0x0943[0]	The IO_VDD_SEL configuration bit optimizes the V_{IL}, V_{IH}, V_{OL}, and V_{OH} thresholds to match the VDDS voltage. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I²C or SPI host is operating at 3.3 V and the Si5397/96 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.
SPI_3WIRE	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default, this configuration bit is set to the 4-wire option. In this mode the Si5397/96 will accept write commands from a 4-wire or 3- wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to “1”.

9.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure below. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I²C specification as shown in the figure below. Two address select bits (A0, A1) are provided allowing up to four Si5397/96 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

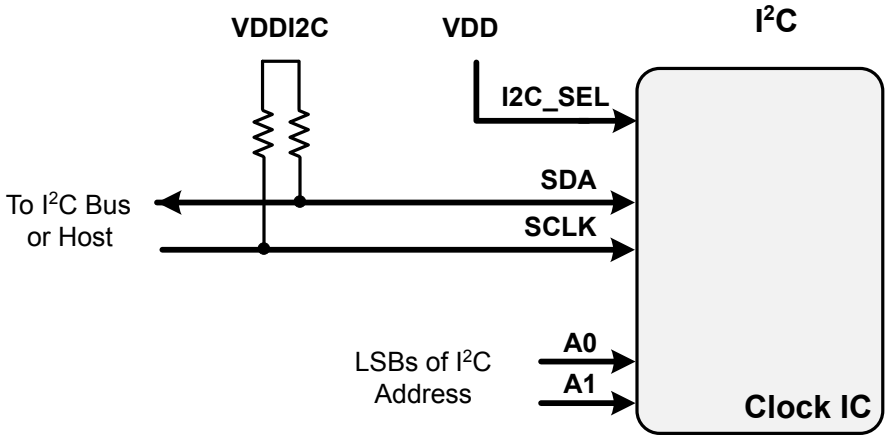


Figure 9.2. I²C Configuration

The 7-bit slave device address of the Si5397/96 consists of a 5-bit fixed address plus 2 pins which are selectable for the last two bits, as shown in the following figure.

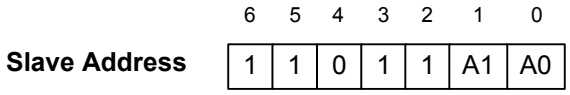


Figure 9.3. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 9.6 SPI Interface Connections on page 66. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

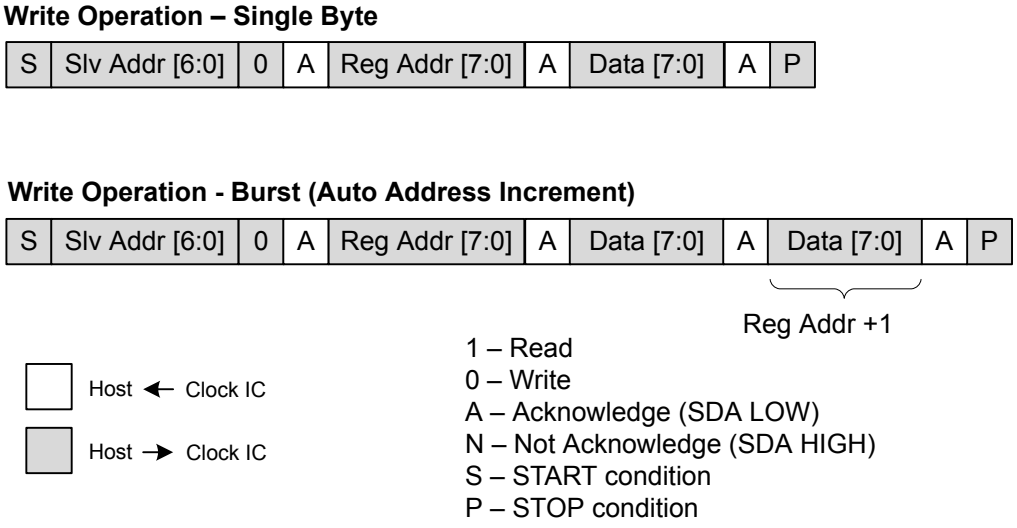


Figure 9.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the following figure.

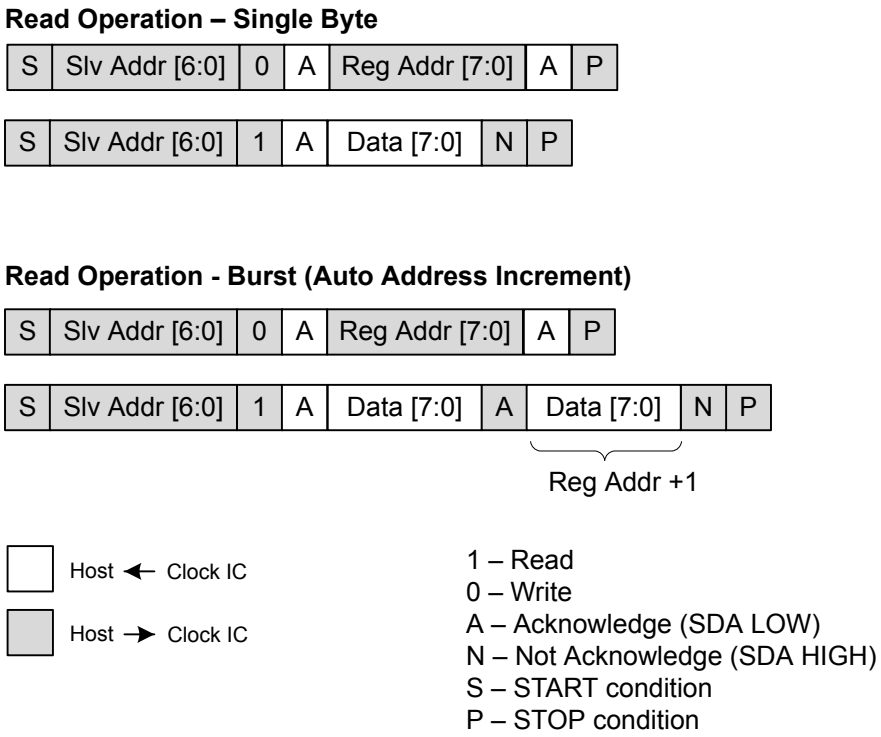


Figure 9.5. I²C Read Operation

The SMBUS interface requires a timeout. The error flags are found in the registers listed below.

Table 9.2. SMBus Timeout Error Bit Indicators

Register Name	Hex Address [Bit Field]	Function
SMBUS_TIMEOUT	0x000C[5]	1 if there is a SMBus timeout error.
SMBUS_TIME-OUT_FLG	0x0011[5]	1 if there is a SMBus timeout error.

9.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CS), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the following figure.

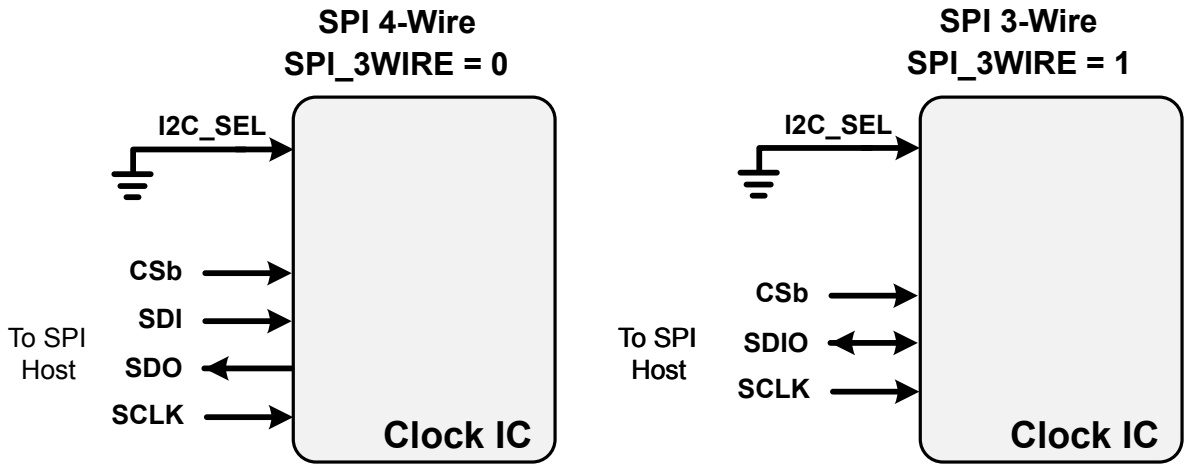


Figure 9.6. SPI Interface Connections

Table 9.3. SPI Command Format

Instruction	1st Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Note:

1. X = don't care (1 or 0).
2. The Burst Write Command is terminated by de-asserting CSb (CSb = high).
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a "Set Address" command followed by a "Write Data" or "Read Data" command. The 'Write Data + Address Increment' or "Read Data + Address Increment" commands are available for cases where multiple byte operations in sequential address locations is necessary. The "Burst Write Data" instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. Figure 9.7 Example Writing Three Data Bytes using the SPI Write Commands on page 67 shows an example of writing three bytes of data using the write commands. As can be seen, the "Write Burst Data" command is the most efficient method for writing data to sequential address locations. Figure 9.8 Example of Reading Three Data Bytes Using the SPI Read Commands on page 67 provides a similar comparison for reading data with the read commands. Note that there is no equivalent burst read; the read increment function is used in this case.

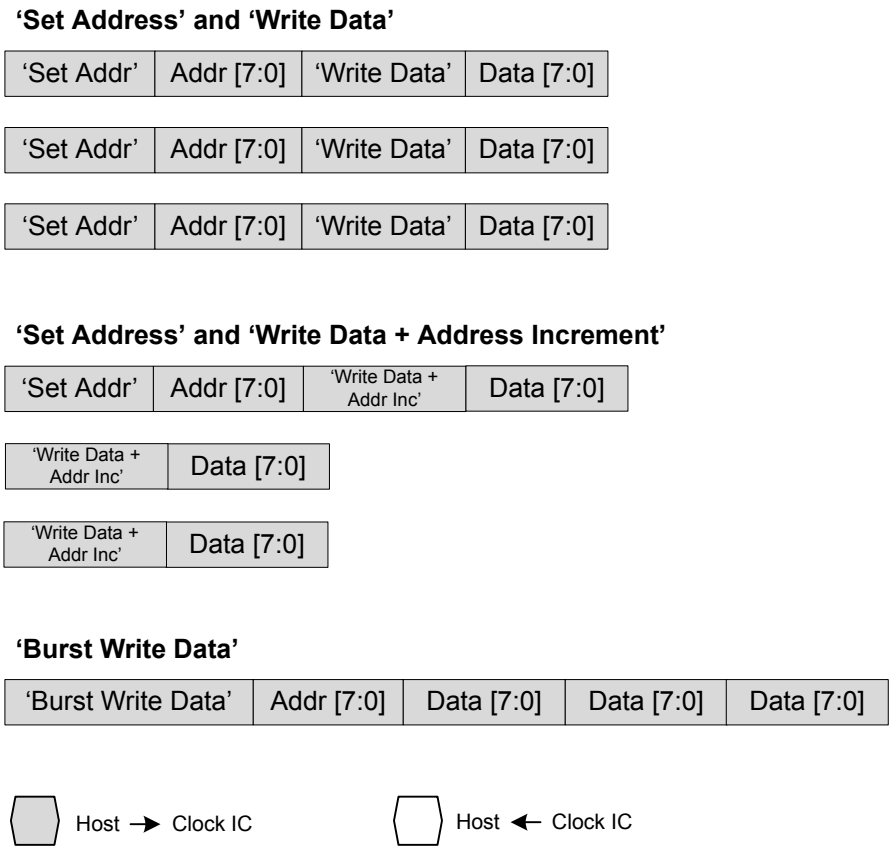


Figure 9.7. Example Writing Three Data Bytes using the SPI Write Commands

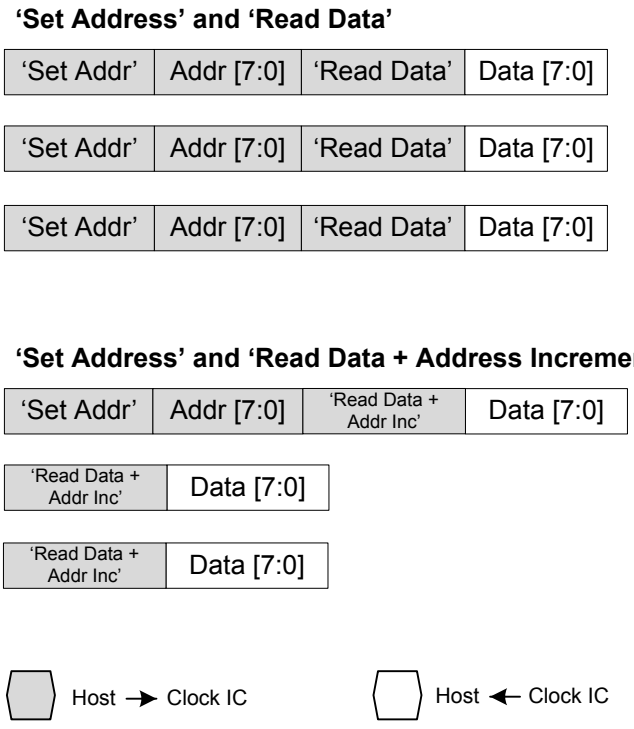


Figure 9.8. Example of Reading Three Data Bytes Using the SPI Read Commands

The timing diagrams for the SPI commands are shown in Figures Figure 9.9 SPI “Set Address” Command Timing on page 68, Figure 9.10 SPI “Write Data” and “Write Data+ Address Increment” Instruction Timing on page 69, Figure 9.11 SPI “Read Data” and “Read Data + Address Increment” Instruction Timing on page 70, and Figure 9.12 SPI “Burst Data Write” Instruction Timing on page 70.

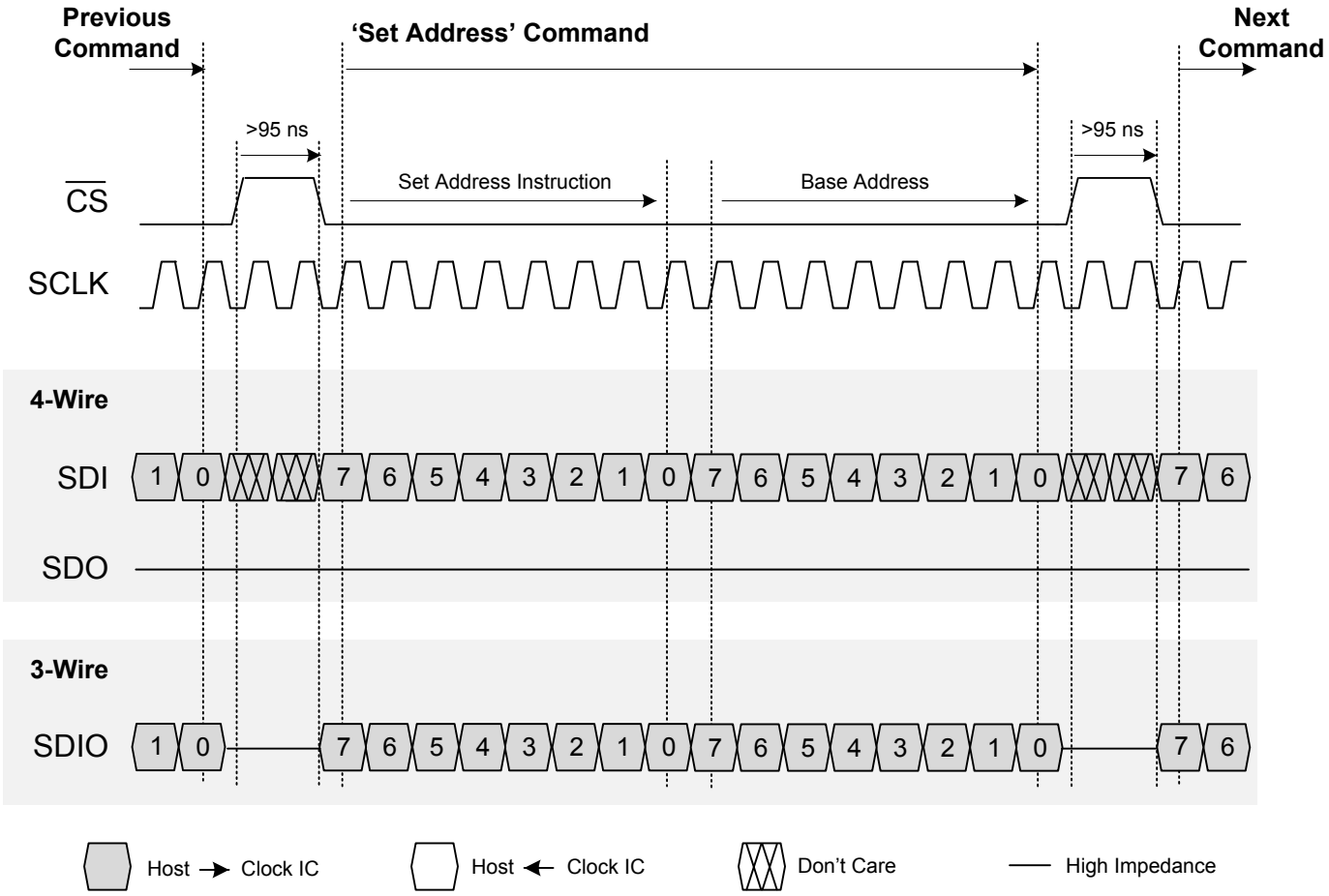


Figure 9.9. SPI “Set Address” Command Timing

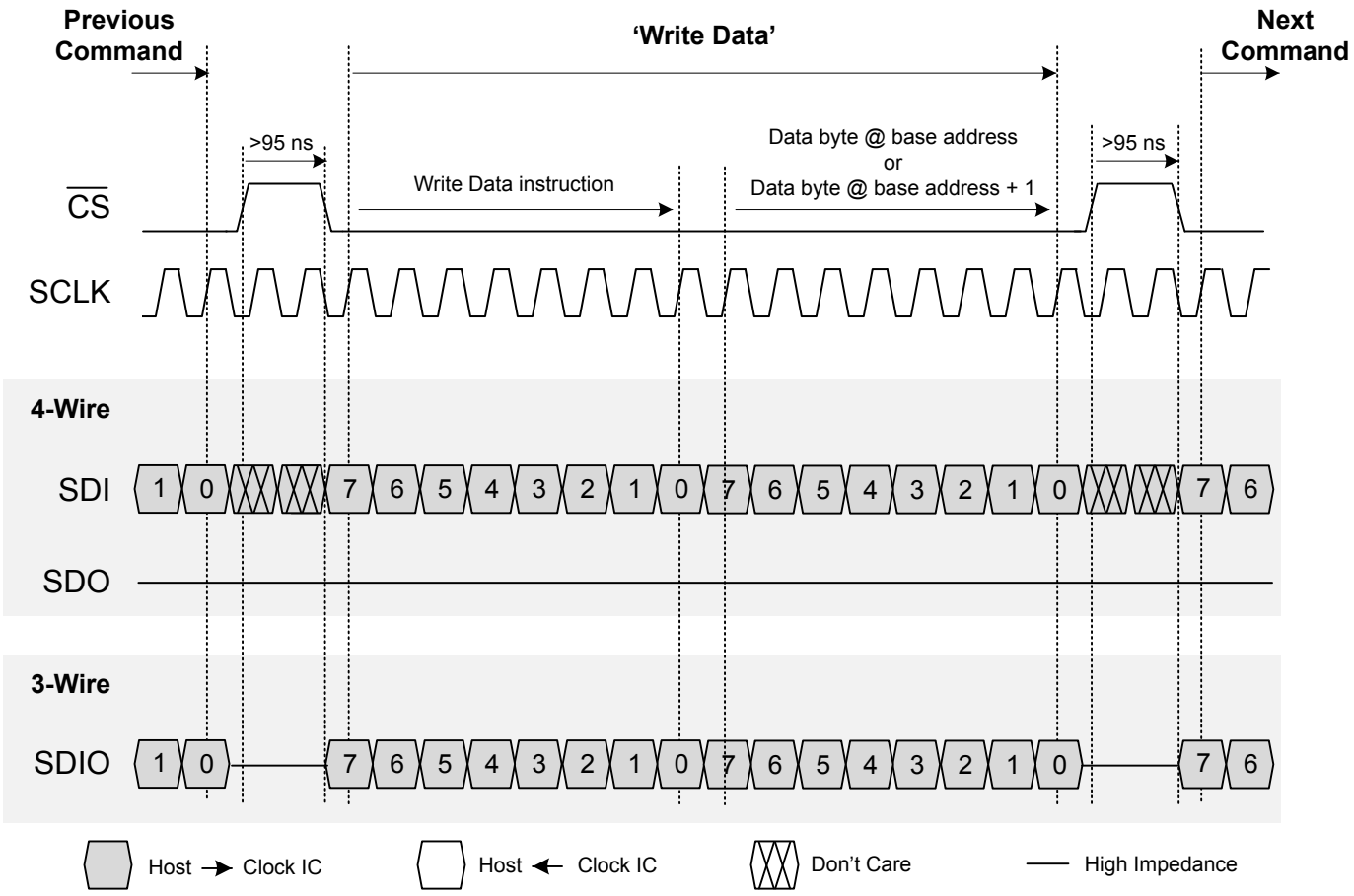


Figure 9.10. SPI "Write Data" and "Write Data+ Address Increment" Instruction Timing

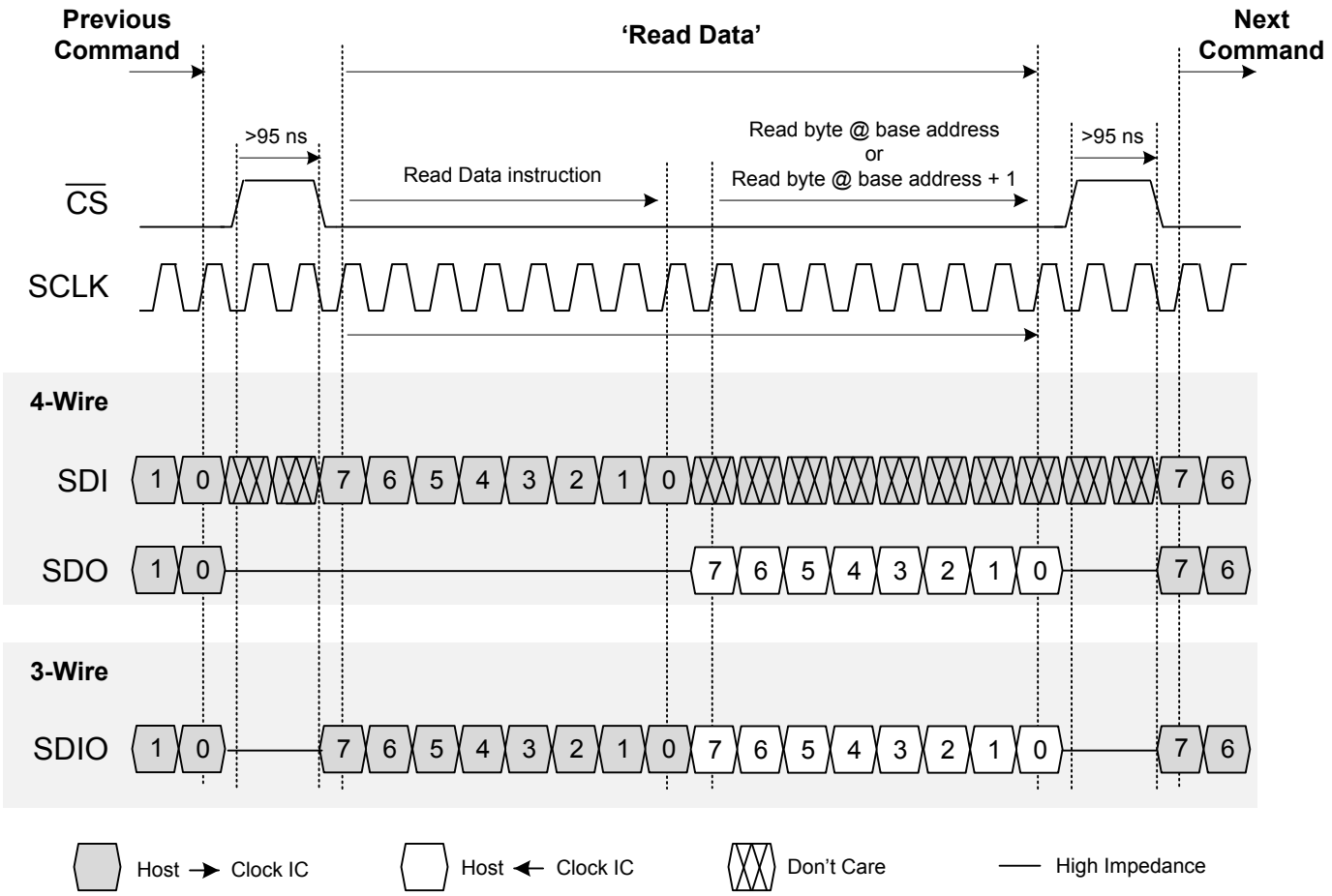


Figure 9.11. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

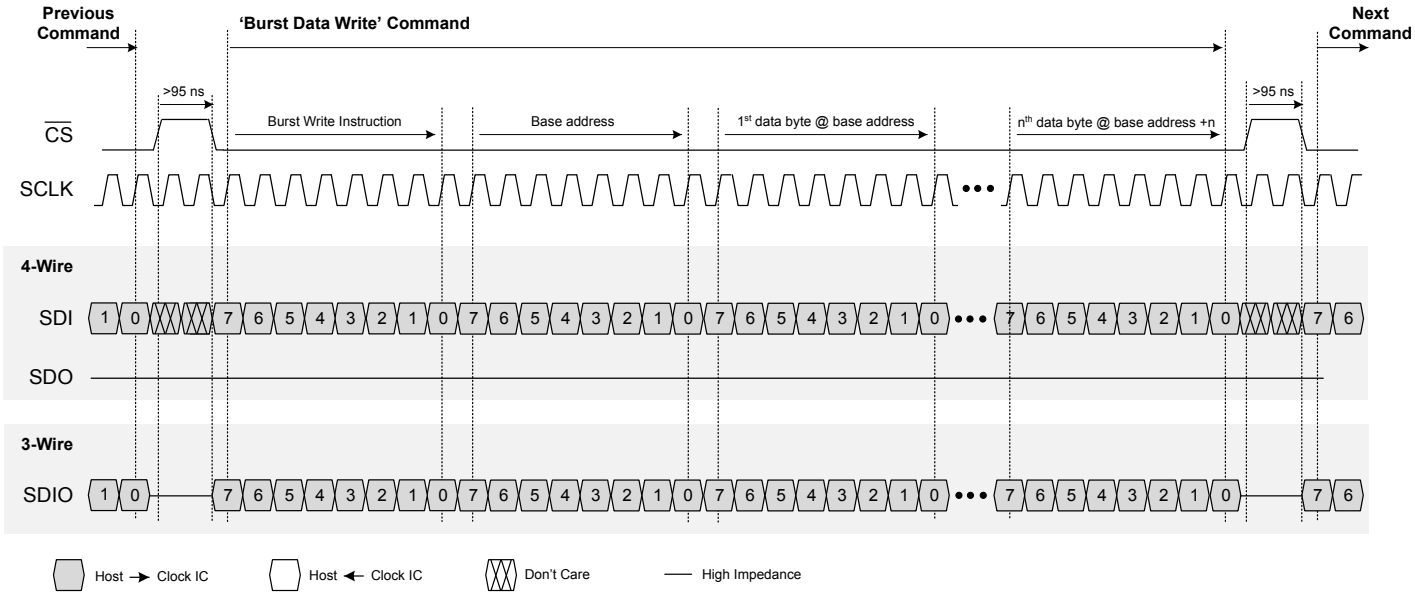


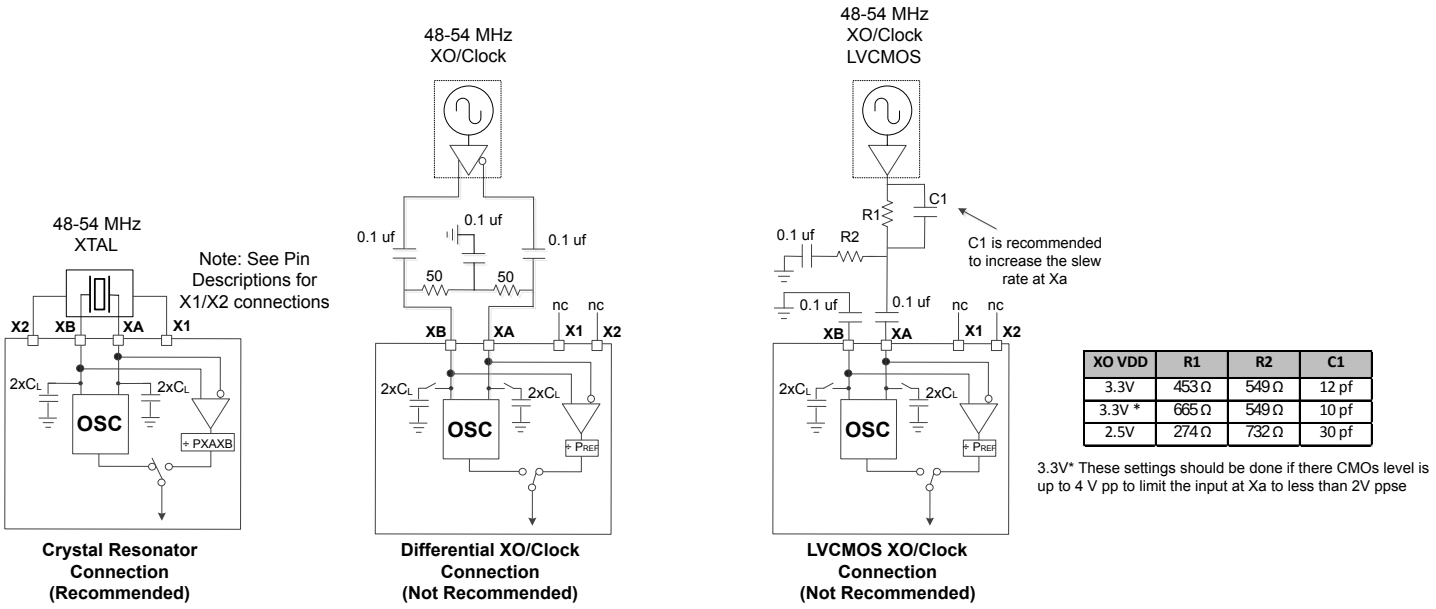
Figure 9.12. SPI "Burst Data Write" Instruction Timing

Note that for all SPI communication the chip select (CS) must be high for the minimum time period between commands. When chip select goes high it indicates the termination of the command. The SCLK can be turned off between commands, particularly if there are very long delays between commands.

10. XAXB References

10.1 External References

An external standard low-pullability crystal (XTAL) is recommended in combination with the internal oscillator (OSC) to produce an ultra low phase noise reference clock for the DSPLL, as well as providing a stable reference for the Freerun and Holdover modes. Simplified connection diagrams are shown below. The device includes internal 8 pF crystal loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. In most applications, using the internal OSC with an external crystal provides the best phase noise performance. See AN905: External References; Optimizing Performance for more information on the performance of various XO's with these devices. The recommended crystal suppliers are listed in the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.



XO VDD	R1	R2	C1
3.3V	453 Ω	549 Ω	12 pf
3.3V *	665 Ω	549 Ω	10 pf
2.5V	274 Ω	732 Ω	30 pf

3.3V* These settings should be done if there CMOs level is up to 4 V pp to limit the input at Xa to less than 2V ppse

Note: XA and XB must not exceed the maximum input voltage listed in Si5372-71 Datasheet Table 5.3 Input Clock Specifications.

Figure 10.1. XAXB Crystal Resonator and External Reference Clock Connection Options

In addition to crystal operations, the Si5397/96 accepts a clipped sine wave, CMOS, or differential reference clock on the XA/XB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 100 Ω or 50 Ω load. For this reason, place the TCXO as close to the Si5397/96 as possible to minimize PCB trace length. In addition, ensure that both the Si5397/96 and the TCXO are both connected directly to the ground plane. Figure 10.1 XAXB Crystal Resonator and External Reference Clock Connection Options on page 71 shows the recommended method of connecting a clipped sine wave TCXO to the Si5397/96. Because the Si5397/96 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into the XA interface of the Si5397/96 once it has been ac-coupled. Because the signal is single-ended, the XB input is ac-coupled to ground. Figure 10.1 XAXB Crystal Resonator and External Reference Clock Connection Options on page 71 illustrates the recommended method of connecting a CMOS rail-to-rail output to the XA/XB inputs of the Si5397/96. The resistor network attenuates the rail-to-rail output swing to ensure that the maximum input voltage swing at the XA pin is less than the data sheet specification. The signal is ac-coupled before connecting it to the Si5397/96 XA input. Again, since the signal is single-ended, the XB input should be ac-coupled to ground. For applications with loop BW values less than 10 Hz that require low wander output clocks, using a TCXO as the XAXB reference source should be considered to avoid the wander of a crystal.

If an external oscillator is used as the XAXB reference, it is important to use a low jitter source because there is effectively no jitter attenuation from the XAXB pins to the outputs. To minimize jitter at the XA/XB pins, the rise time of the XA/XB signals should be as fast as possible.

For best jitter performance, use a XAXB frequency above 40 MHz. Also, for XAXB frequencies higher than 125 MHz, the PXAXB control must be used to divide the input frequency down below 125 MHz.

10.2 Recommended Crystals and Oscillators

Refer to the Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators for more information.

10.3 Register Settings to Configure for External XTAL Reference

The following registers can be used to control and make adjustments for the external reference source used.

10.3.1 XAXB_EXTCLK_EN Reference Clock Selection Register

Table 10.1. XAXB External Clock Selection Register

Setting Name	Hex Address [Bit Field]	Function
	Si5397/96	
XAXB_EXTCLK_EN	090E[0]	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

The internal crystal loading capacitors (CL) are disabled when an external clock source is selected.

10.3.2 PXAXB Pre-scale Divide Ratio for Reference Clock Register

Table 10.2. XAXB Pre-Scale Divide Ratio Register

Setting Name	Hex Address [Bit Field]	Function
	Si5397/96	
PXAXB	0x0206[1:0]	Sets the XAXB input divider value according to the table below.

The following table lists the values, along with the corresponding divider ratio.

Table 10.3. XAXB Pre-Scale Divide Values

Value (Decimal)	PXAXB Divider Value
0	1
1	2
2	4
3	8

11. Internal Reference

Devices with internal reference (J/K/L/M) have a 48MHz crystal integrated in the package, to deliver a smaller layout footprint and more immunity to acoustic emissions. This crystal is manufactured by a reliable Japanese crystal manufacturer and has been pre-screened for activity dips before being assembled. It is important to note that connecting an external reference to XA/XB of a device that already has an integrated reference is not allowed. Doing so could lead to internal damage to the circuits. When using this integrated crystal option in a design that has been laid out for an external crystal, simply depopulate the crystal and replace the external crystal device with the internal crystal version. It is important to note that a new CBPro plan is required for the integrated crystal variant. For more information, please contact Silicon Labs support. For specifications of the internal crystal, please refer to the data sheet. During the initial power up, the integrated crystal quickly settles down to a temperature that is slightly higher than ambient temperature due to proximity to the die. If the PLL is locked to an input, the frequency accuracy of the crystal has no impact on the output frequency accuracy; if the PLL is free-running, then the output frequency tracks the crystal frequency which is still well within the spec.

The internal reference devices have a crystal inside which can take a little longer (~ 40-45 sec) to settle, which is longer than the external crystal devices. The settling time is the time required for the crystal to reach a stable operating frequency. This will not affect the start-up time of the device or the lock time. The device will pull in the output frequency at the rate set by the PLL bandwidth which will be faster, and the device will produce valid clock outputs within the start-up time mentioned in the device data sheet.

12. Crystal, XO and Device Circuit Layout Recommendations

The following are recommendations for crystal layout (for devices that require an external reference), as well as device layout for all variants. The main layout issues that should be carefully considered include the following:

- Number and size of the ground vias for the Epad
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace coupling
- Xtal signal coupling (external reference devices)
- Xtal layout (external reference devices)

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins to provide the best possible performance. The shield should not be connected to the ground plane(s), and the layers underneath should have as little area under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

Go to the Silicon Labs Clock Development Tool webpage to obtain Si5397, Si5396 evaluation board schematics, layouts, and component BOM files.

12.1 64-Pin QFN Si5397/96 Layout Recommendations

This section details the recommended guidelines for the external reference layout of the 64-pin Si5397/96 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals
- Layer 2: crystal shield (applies to external reference devices only)
- Layer 3: ground plane
- Layer 4: power distribution
- Layer 5: power routing layer
- Layer 6: input clocks
- Layer 7: output clocks layer
- Layer 8: ground layer

The 64 pin QFN crystal guidelines show the top layer layout of the Si5397/96 device mounted on the top PCB layer. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. Note this applies only to external reference devices. The crystal/ oscillator area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

12.1.1 Si5397/96 XO Guidelines

For devices that use an external reference like an XO, pins X1 and X2 should not be connected to "ground" and should be left as "no-connects". An external reference does not need a crystal shield or the voids underneath the shield. The XA/XB connection should be treated as a high speed critical path that is ac-coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA pin to the XB pin. Jitter is very critical at the XA/XB pins and therefore split termination and differential signaling should be used whenever possible.

12.1.2 Si5397/96 Crystal Guidelines

The following are five recommended crystal guidelines used with external reference devices:

1. Place the crystal as close as possible to the XA/XB pins.

2. DO NOT connect the crystal's GND pins to PCB gnd.

3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal GND shield placed around and under the crystal. See Figure 12.1 64-pin Si5397/96 Crystal Layout Recommendations Top Layer (Layer 1) on page 75 at the bottom left for an illustration of how to create a crystal GND shield by placing vias connecting the top layer traces to the shield layer underneath. Note that a zoom view of the crystal shield layer on the next layer down is shown in Figure 12.2 Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2) on page 76.

4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.

5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5397/96 should have all layers underneath the ground shield removed if possible.

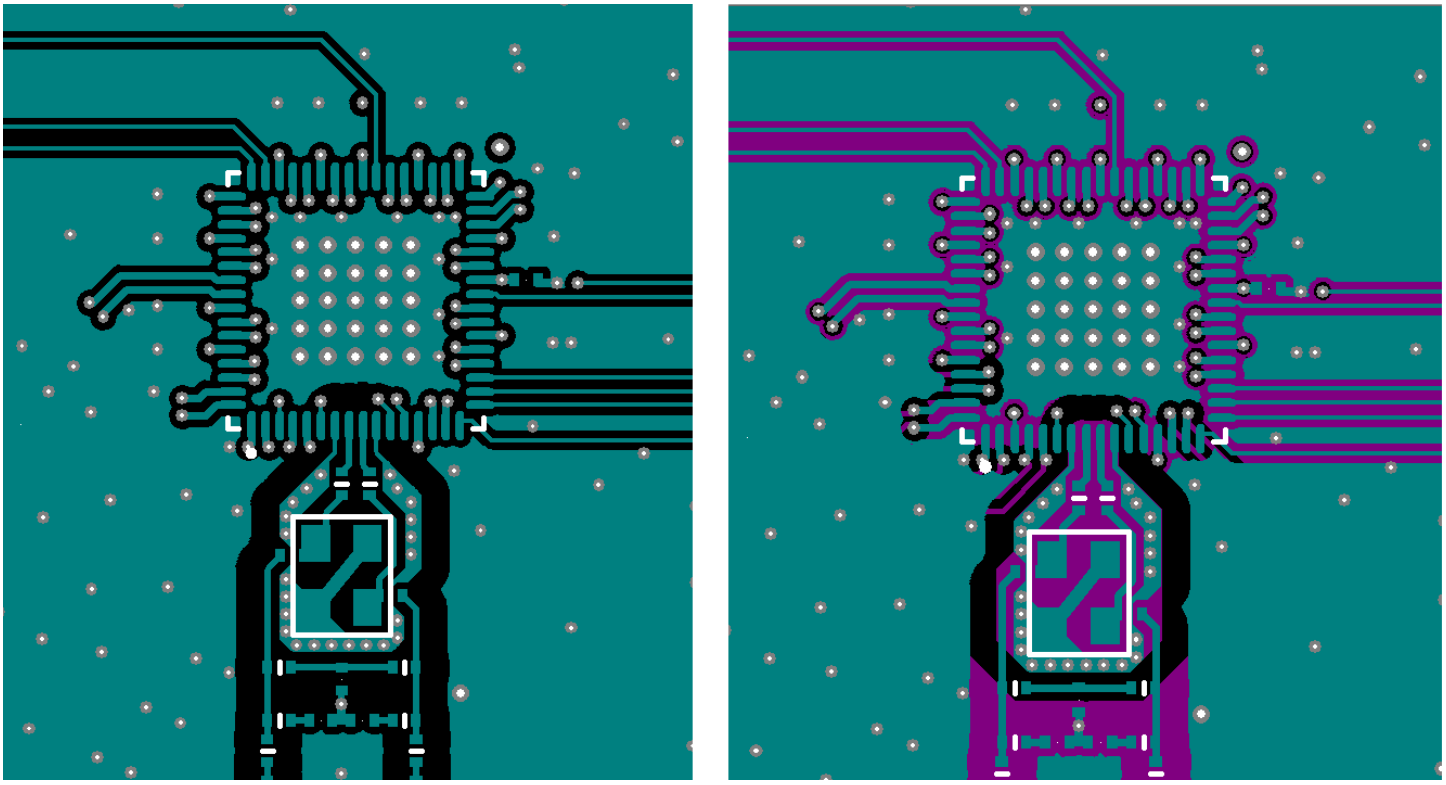


Figure 12.1. 64-pin Si5397/96 Crystal Layout Recommendations Top Layer (Layer 1)

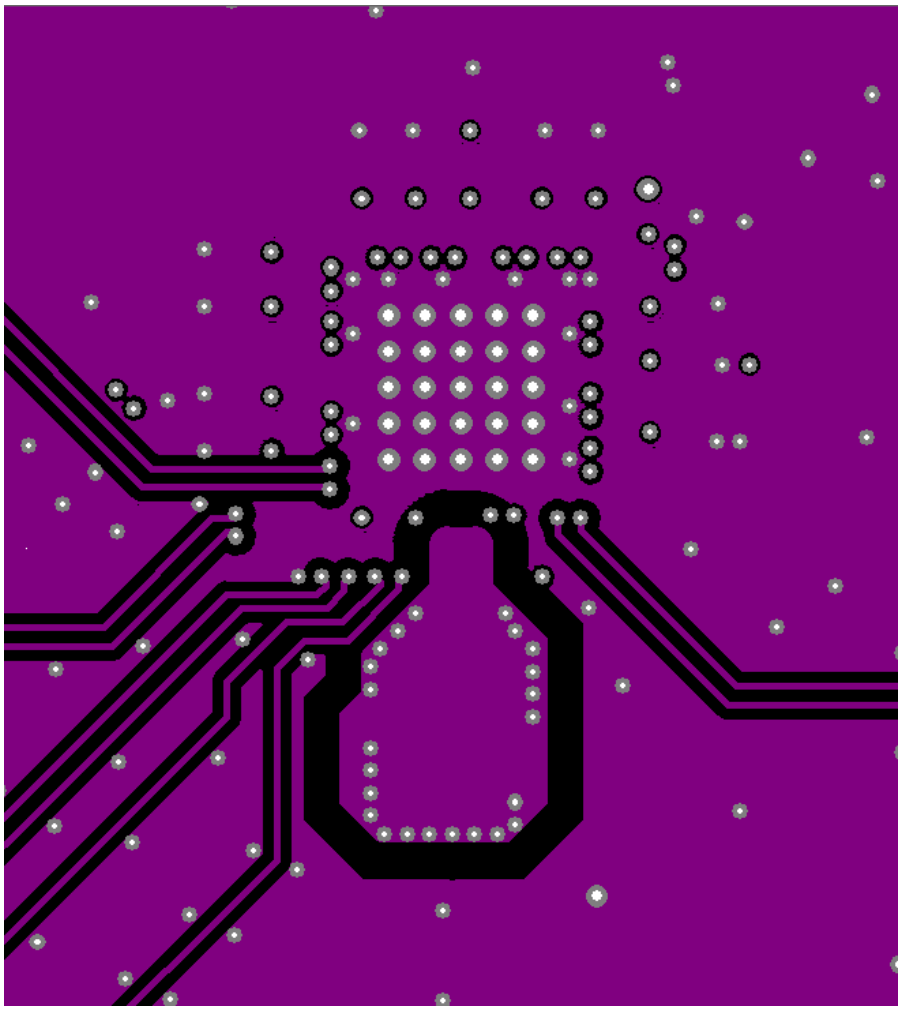


Figure 12.2. Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2)

Figure 12.2 Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2) on page 76 shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2, they have a ground shield above, below, and on the sides for protection.

Figure 12.3 Crystal Ground Plane (Layer 3) on page 77 is the ground plane and shows a void underneath the crystal shield. Figure 12.4 Power Plane (Layer 4) on page 78 is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

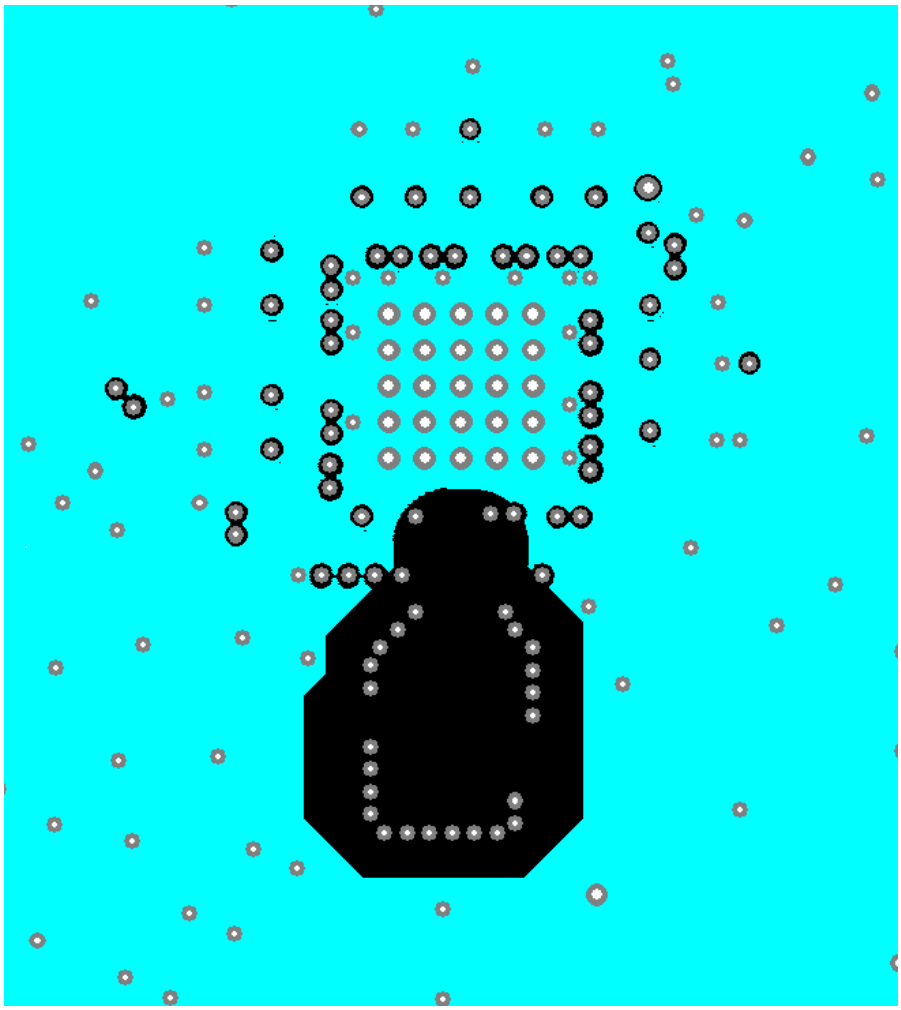


Figure 12.3. Crystal Ground Plane (Layer 3)

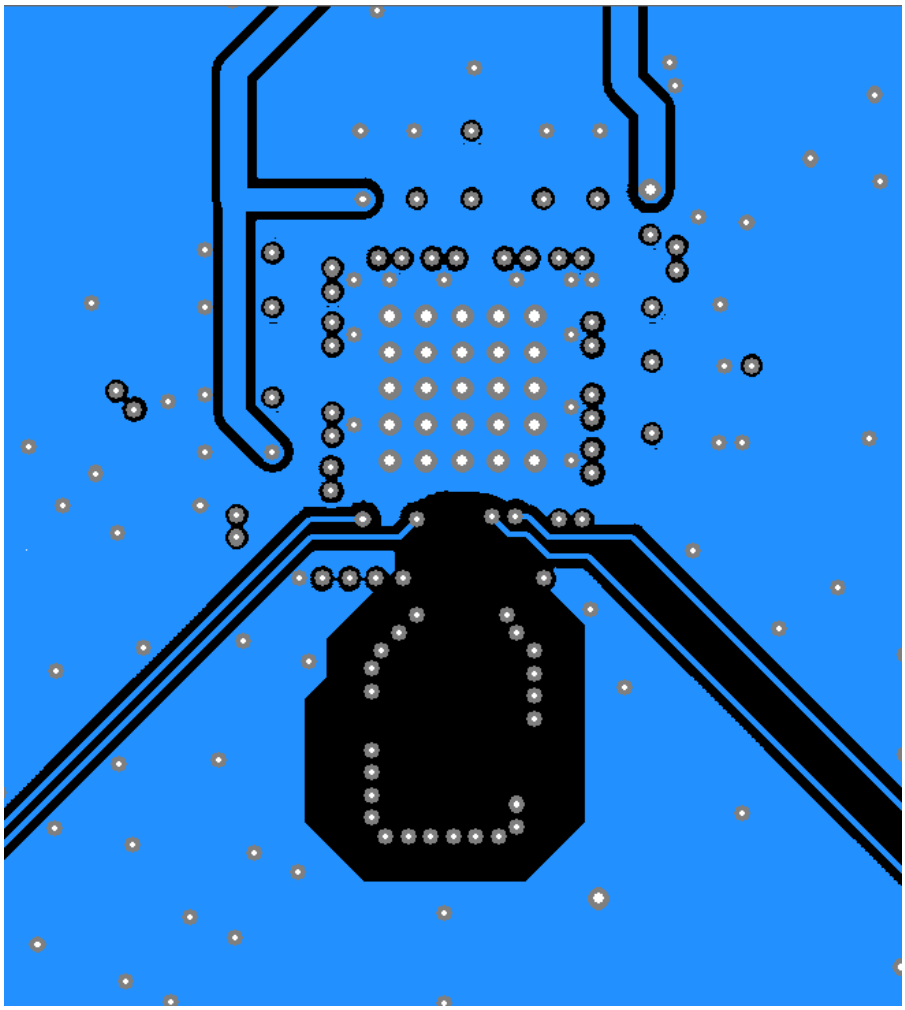


Figure 12.4. Power Plane (Layer 4)

Figure 12.5 Layer 5 Power Routing on Power Plane (Layer 5) on page 79 shows layer 5, which is the power plane with the power routed to the clock output power pins.

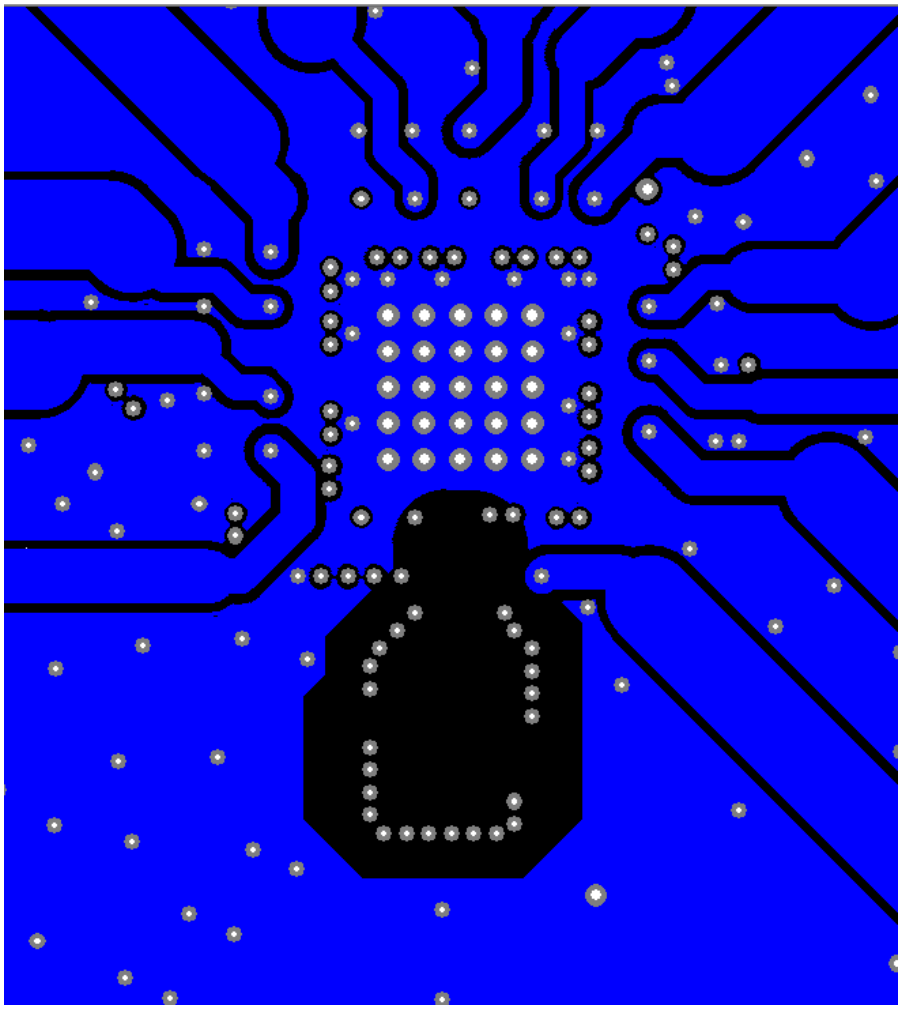


Figure 12.5. Layer 5 Power Routing on Power Plane (Layer 5)

Figure 12.6 Ground Plane (Layer 6) on page 80 is another ground plane similar to layer 3.

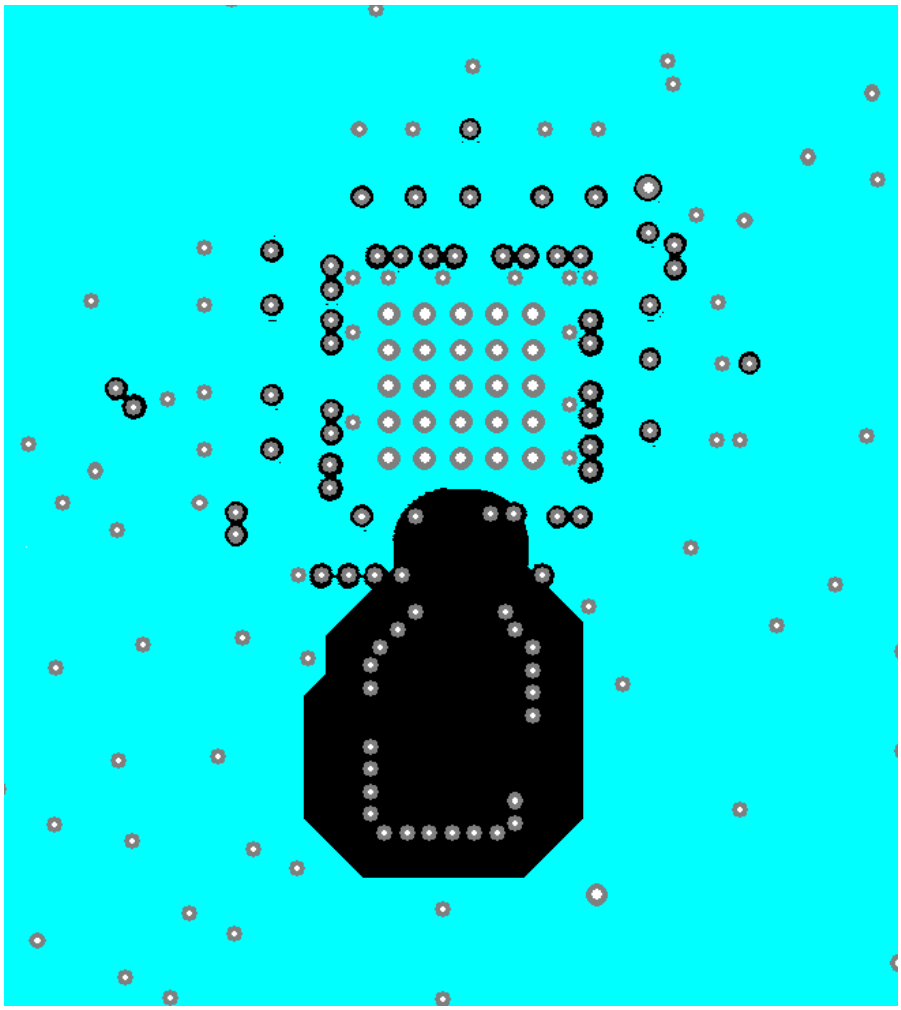


Figure 12.6. Ground Plane (Layer 6)

12.1.3 Si5397/96 Output Clocks

Figure 12.7 Output Clock Layer (Layer 7) on page 81 shows the output clocks. Similar to the input clocks the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

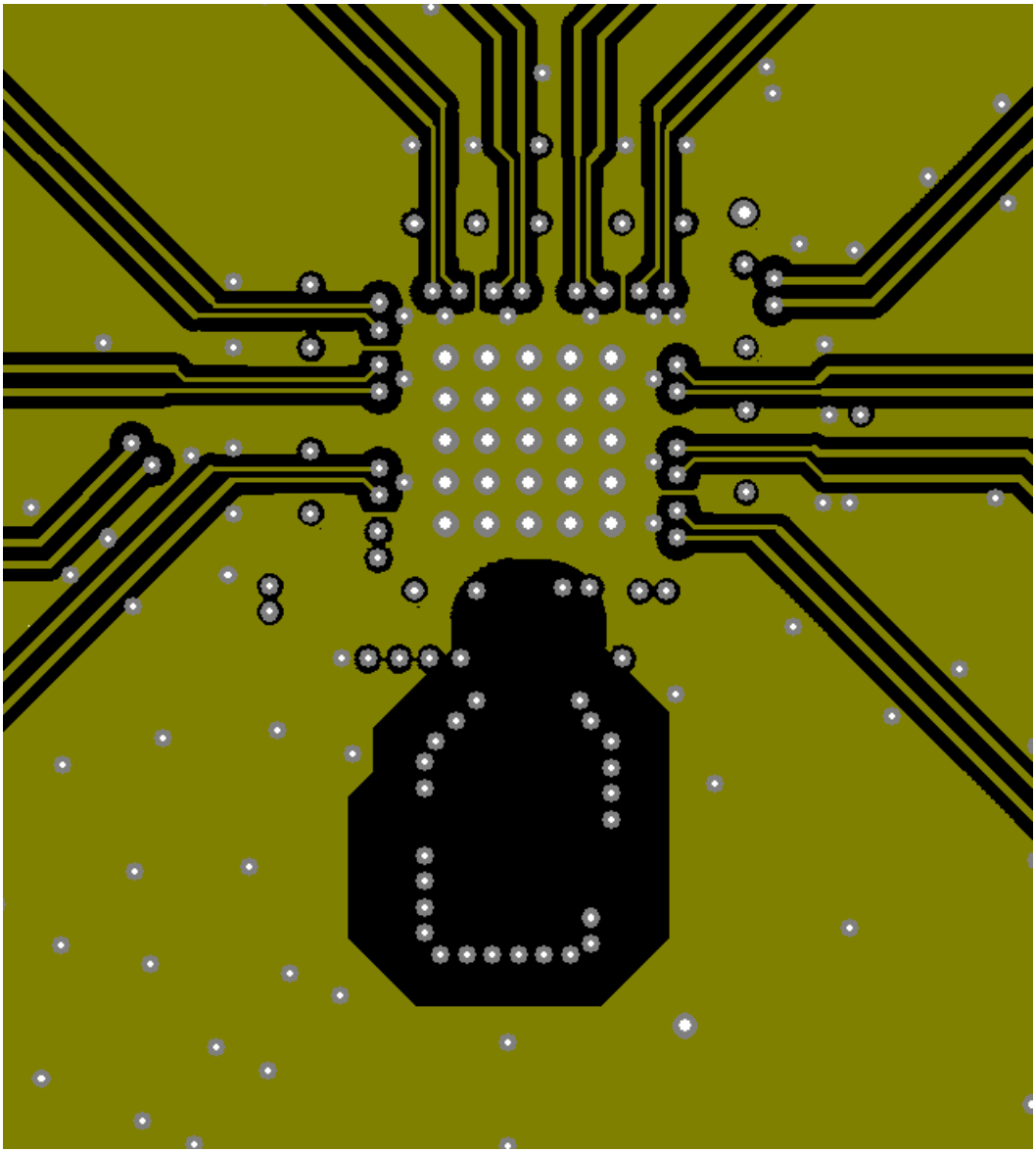


Figure 12.7. Output Clock Layer (Layer 7)

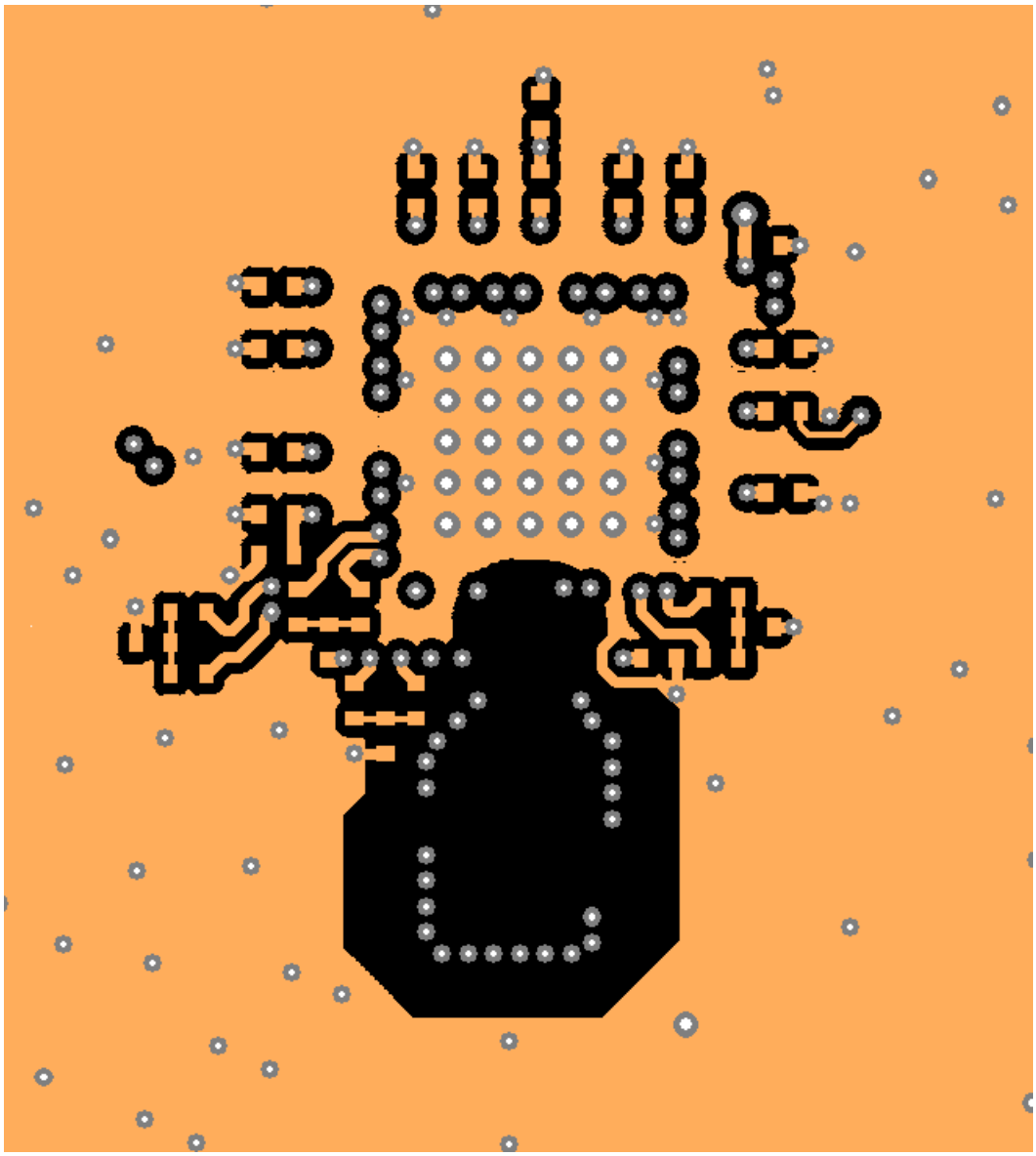


Figure 12.8. Bottom Layer Ground Flooded (Layer 8)

12.2 64-Pin LGA Si5397/96 Layout Recommendations

This section details the recommended guidelines for the internal reference layout. The crystal is integrated inside the package so leave XA, XB, X1, and X2 unconnected. An additional benefit of the internal crystal is that is does NOT need a crystal shield or voids on the PCB layers beneath the crystal. It is recommended to minimize traces adjacent to the chip especially if there are clocks or frequently toggling digital signals to avoid coupling of these signals into the device.

12.3 44-Pin QFN Si5396 Layout Recommendations

This section details the layout recommendations for the 44-pin external reference devices using an example 6-layer PCB.

The following guidelines details images of a six layer board with the following stack:

Layer 1: device layer, with low speed CMOS control/status signals, ground flooded

Layer 2: crystal shield, output clocks, ground flooded

Layer 3: ground plane

Layer 4: power distribution, ground flooded

Layer 5: input clocks, ground flooded

Layer 6: low-speed CMOS control/status signals, ground flooded

This layout was designed to implement either a crystal or an external oscillator as the XAXB reference (used with external reference devices). The top layer is flooded with ground. The clock output pins go to layer 2 using vias to avoid crosstalk during transit. When the clock output signals are on layer 2 there is a ground shield above, below and on all sides for protection. Output clocks should always be routed on an internal layer with ground reference planes directly above and below. The plane that has the routing for the output clocks should have ground flooded near the clock traces to further isolate the clocks from noise and other signals.

12.3.1 Si5396 XO Guidelines

For devices that use an external reference like an XO, pins X1 and X2 should not be connected to "ground" and should be left as "no-connects". An external reference does not need a crystal shield or the voids underneath the shield. The XA/XB connection should be treated as a high speed critical path that is ac-coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA pin to the XB pin. Jitter is very critical at the XA/XB pins and therefore split termination and differential signaling should be used whenever possible. See Recommended Crystal, TCXO and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators for a suggested list of XOs.

12.3.2 Si5396 Crystal Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. DO NOT connect the crystal's GND pins to PCB gnd.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal GND shield placed around and under the crystal. See Figure 12.9 Device Layer (Layer 1) on page 84 at the bottom left for an illustration of how to create a crystal GND shield by placing vias connecting the top layer traces to the shield layer underneath. Note that a zoom view of the crystal shield layer on the next layer down is shown in Figure 12.10 Crystal Shield Layer 2 on page 85.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.
5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5396 should have all layers underneath the ground shield removed if possible.

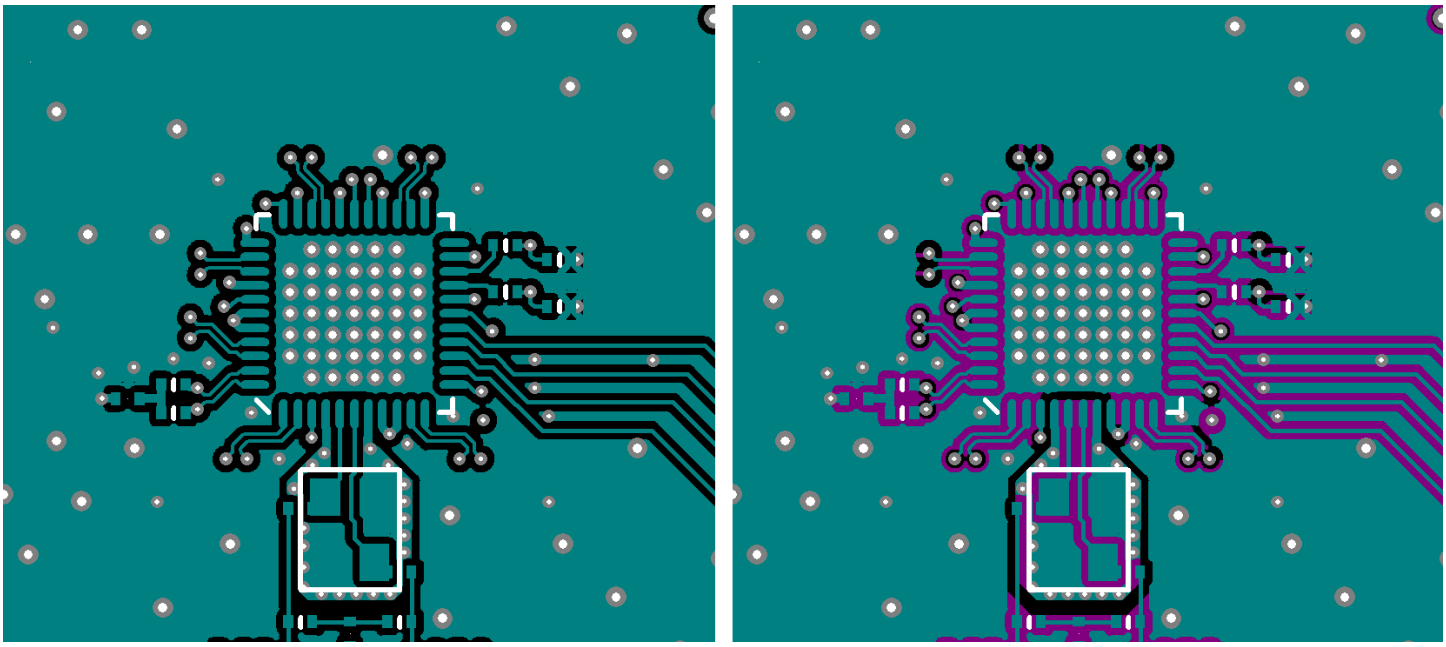


Figure 12.9. Device Layer (Layer 1)

Figure 12.10 Crystal Shield Layer 2 on page 85 is the second layer. The second layer implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. There should be no less than 12 vias to connect the X1 and X2 planes on layers 1 and 2. These vias are not shown in any other figures. All traces with signals that are not static must be kept well away from the crystal and the X1 and X2 plane.

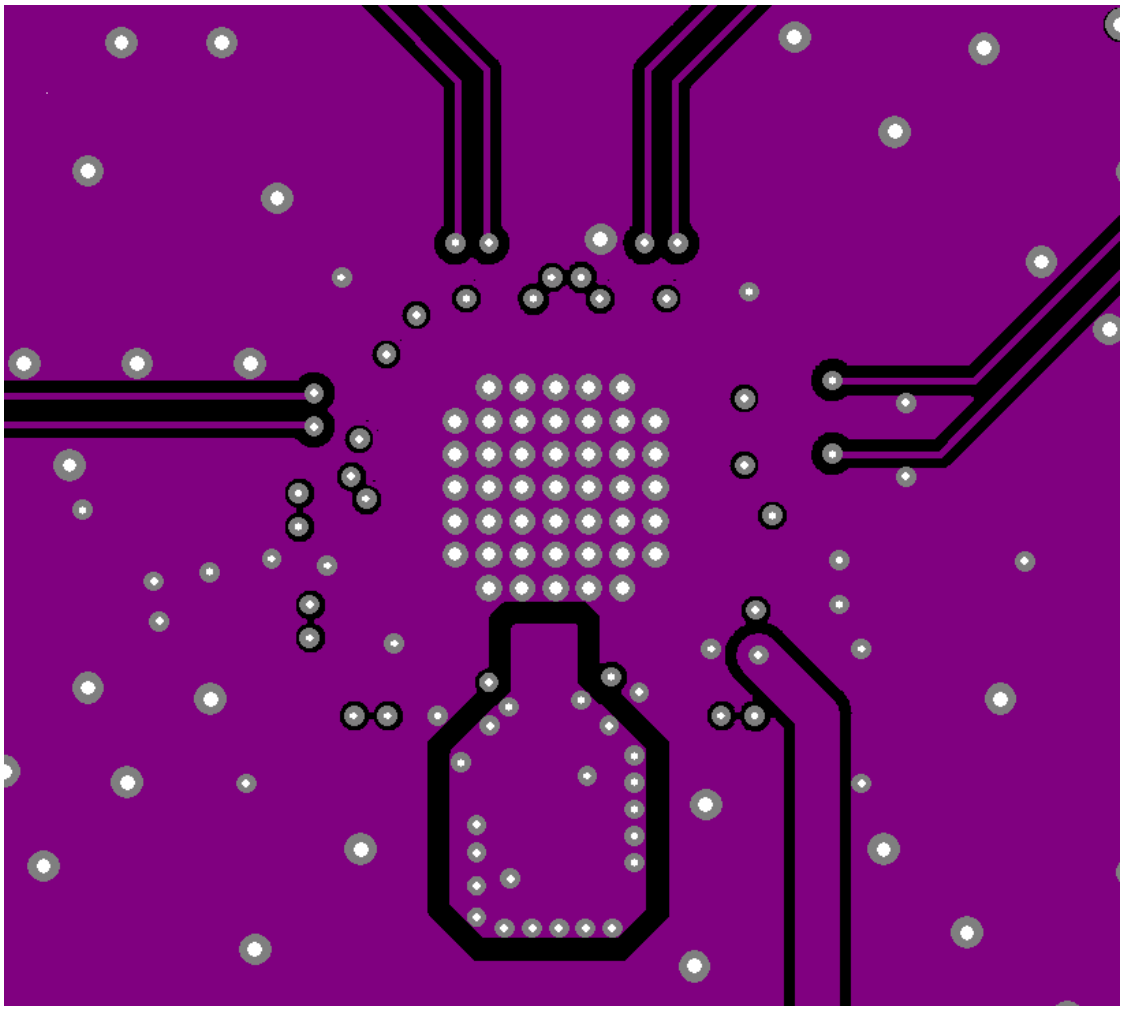


Figure 12.10. Crystal Shield Layer 2

Figure 12.11 Ground Plane (Layer 3) on page 86 is the ground plane and shows a void underneath the crystal shield.

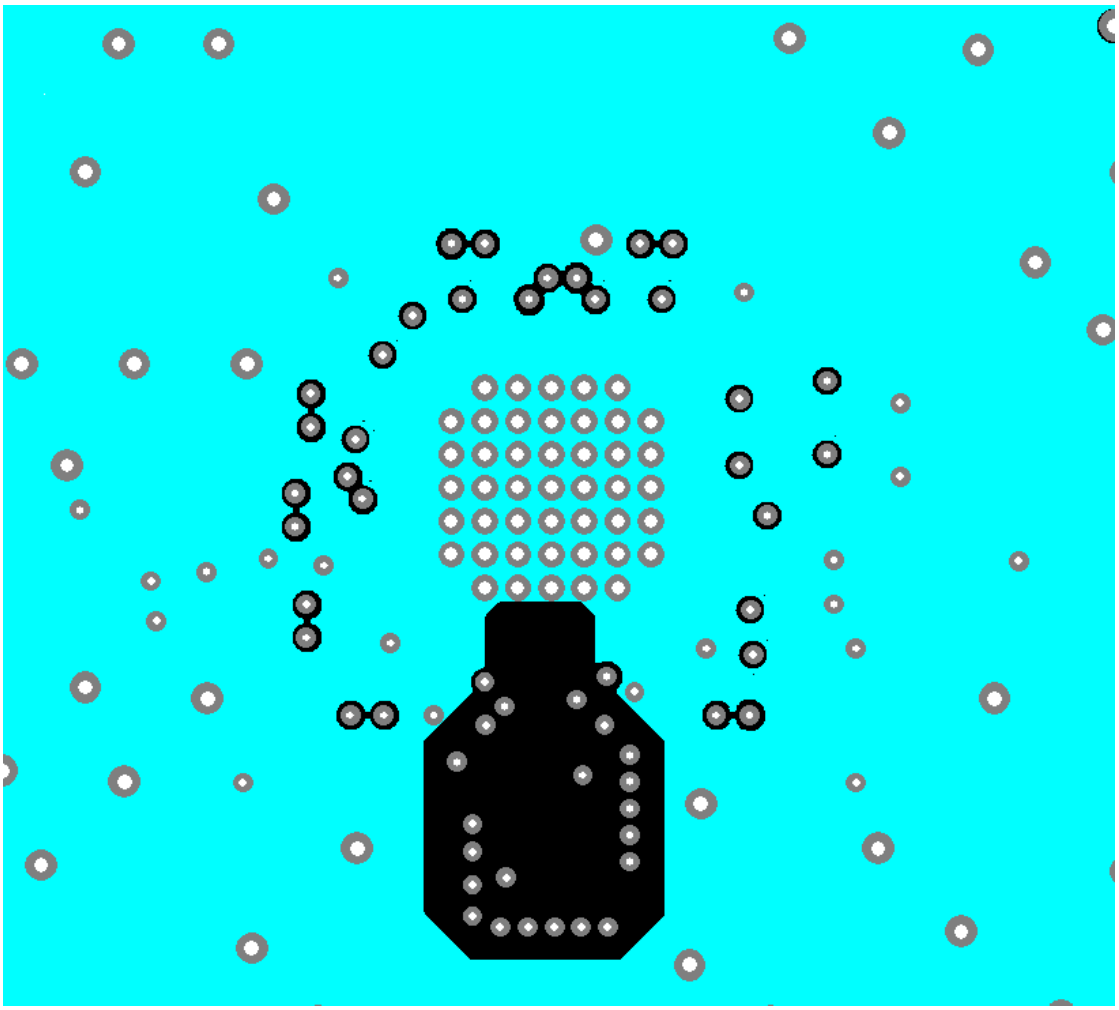


Figure 12.11. Ground Plane (Layer 3)

Figure 12.12 Power Plane and Clock Output Power Supply Traces (Layer 4) on page 87 is a power plane showing the clock output power supply traces. The void underneath the crystal shield is continued.

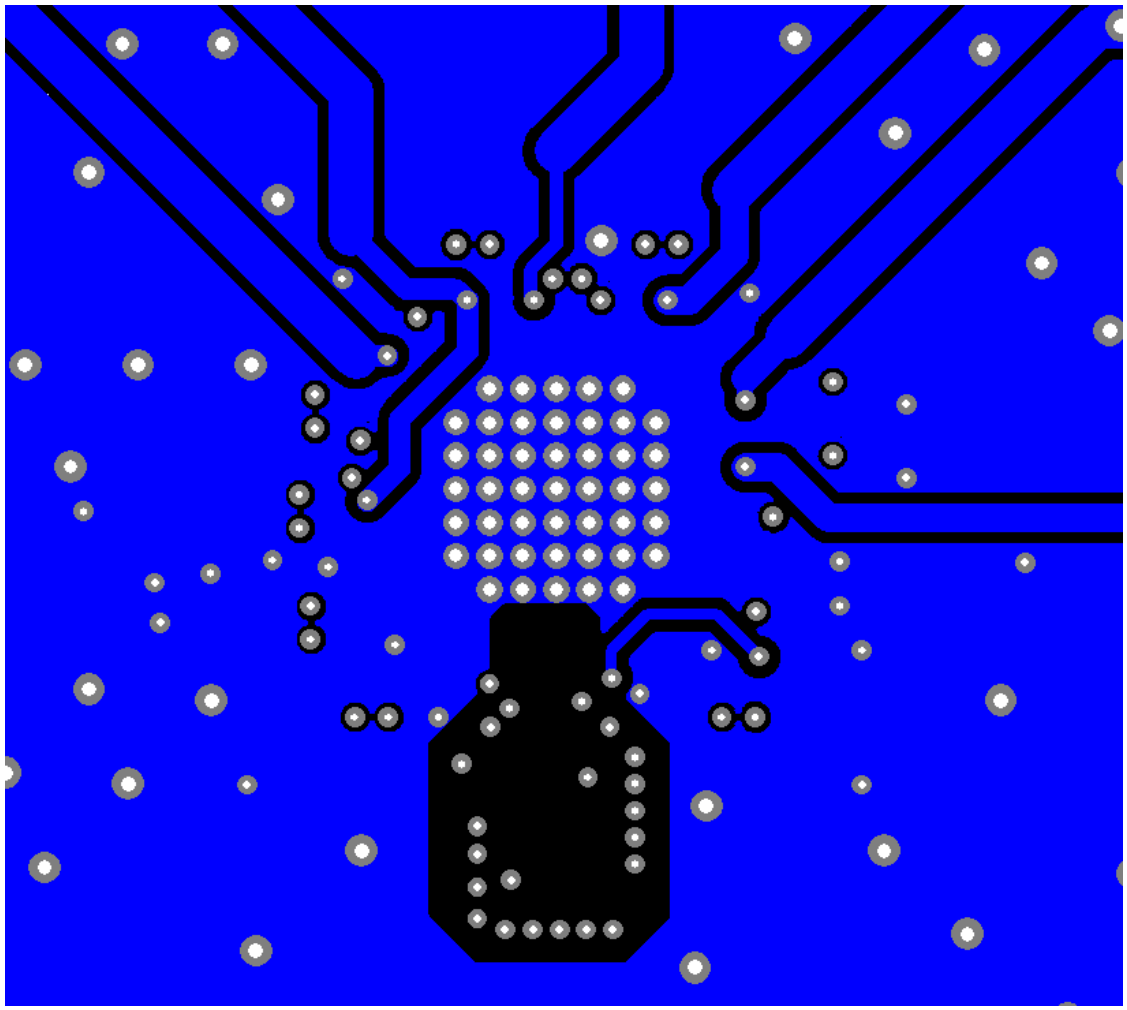


Figure 12.12. Power Plane and Clock Output Power Supply Traces (Layer 4)

Figure 12.13 Clock Input Traces (Layer 5) on page 88 shows layer 5 and the clock input traces. Similar to the clock output traces, they are routed to an inner layer and surrounded by ground to avoid crosstalk.

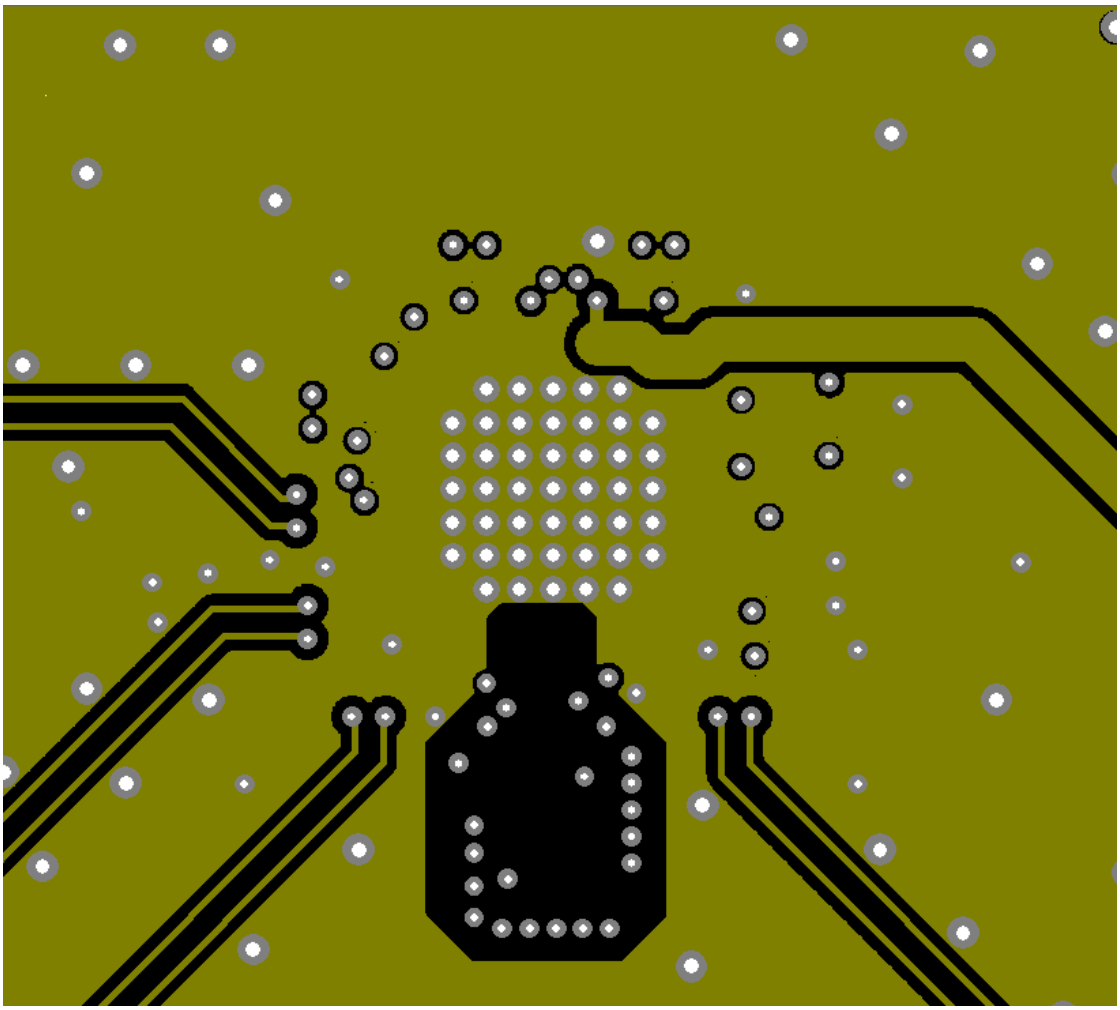


Figure 12.13. Clock Input Traces (Layer 5)

Figure 12.14 Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer) on page 89 shows the bottom layer, which continues the void underneath the shield. Layer 6 and layer 1 are mainly used for low speed CMOS control and status signals for which crosstalk is not a significant issue. PCB ground can be placed under the XTAL Ground shield (X1/X2) as long as the PCB ground is at least 0.05 inches below it.

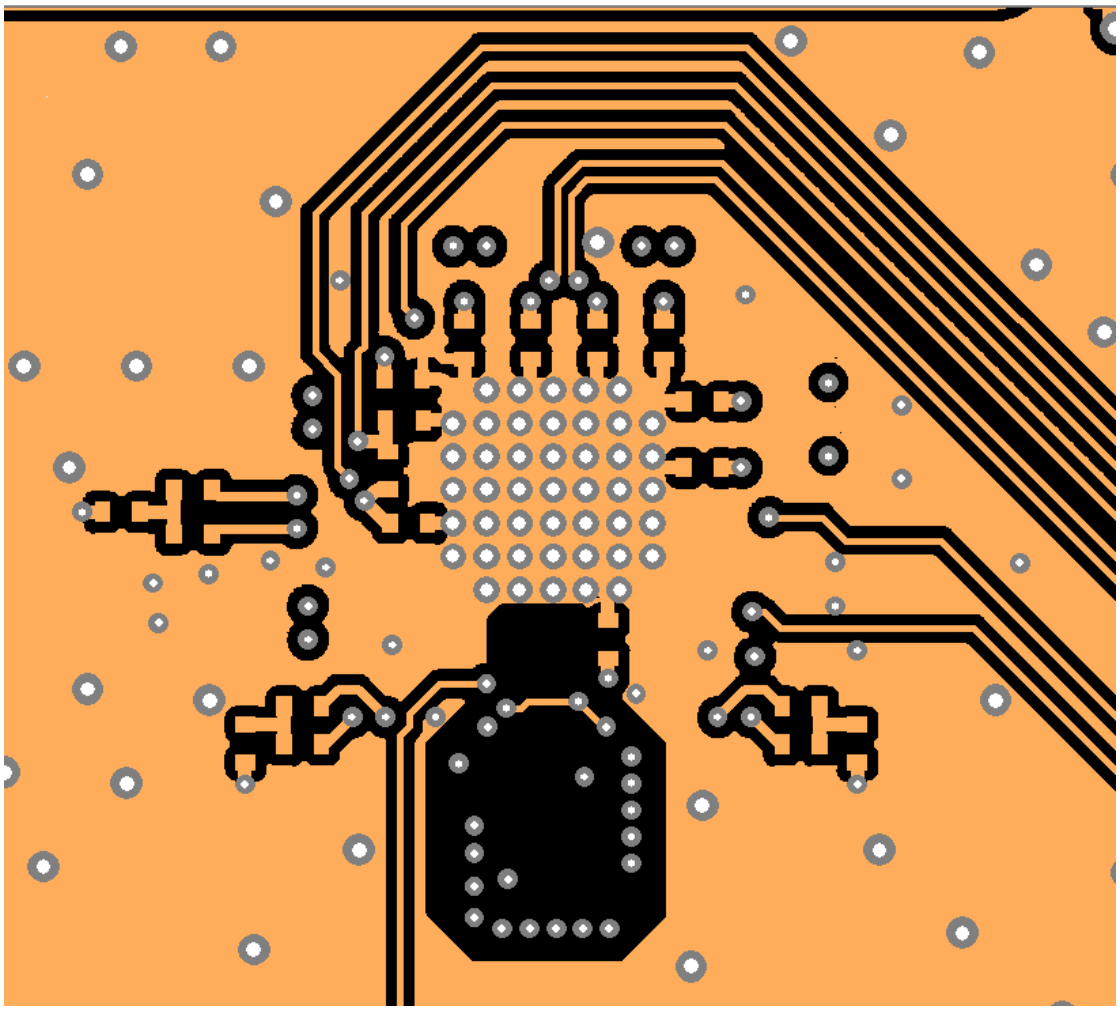


Figure 12.14. Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer)

For any high-speed, low-jitter application, the clock signal runs should be impedance-controlled to 100 Ω differential or 50 Ω single-ended. Differential signaling is preferred because of its increased immunity to common-mode noise. All clock I/O runs should be properly terminated.

12.4 44-Pin LGA Si5396 Layout Recommendations

The crystal is integrated inside the package so leave XA, XB, X1, and X2 unconnected. An additional benefit of the internal crystal is that is does NOT need a crystal shield or voids on the PCB layers beneath the crystal. It is recommended to minimize traces adjacent to the chip especially if there are clocks or frequently toggling digital signals to avoid coupling of these signals into the device.

13. Power Management

13.1 Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed below are used for powering down different features.

Table 13.1. Power-Down Registers

Setting Name	Hex Address [Bit Field]				Function
	Si5397A/B	Si5397C/D	Si5396A/B	Si5396C/D	
PDN	001E[0]				This bit allows powering down the device. The serial interface remains powered during power down mode and the registers are available to be read and written.
OUT0A_PDN	—	—	—	0103[0]	Powers down unused clock outputs. When powered down, output pins will be high-impedance with a light pull-down effect.
OUT0_PDN	0108[0]	0108[0]	0112[0]	0108[0]	
OUT1_PDN	0112[0]	011C[0]	0117[0]	010D[0]	
OUT2_PDN	0117[0]	0126[0]	0126[0]	0112[0]	
OUT3_PDN	011C[0]	012B[0]	012B[0]	0117[0]	
OUT4_PDN	0126[0]	—	—	011C[0]	
OUT5_PDN	012B[0]	—	—	0121[0]	
OUT6_PDN	0130[0]	—	—	0126[0]	
OUT7_PDN	0x013A[0]	—	—	012B[0]	
OUT8_PDN	—	—	—	0130[0]	
OUT9_PDN	—	—	—	0135[0]	
OUT9A_PDN	—	—	—	013A[0]	
OUT_PDN_ALL	0145[0]				Power down all output drivers

13.2 Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5397/96 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 1 µF 0402 ceramic capacitor on each VDD for optimal performance. It is also suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed.

13.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5397/96:

1. VDD = 1.8 V (Core digital supply)
2. VDDA = 3.3 V (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTB pin. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

One may observe that when powering up the VDD = 1.8 V rail first, that the VDDA = 3.3 V rail will initially follow the 1.8 V rail. Likewise, if the VDDA rail is powered down first then it will not drop far below VDD until VDD itself is powered down. This is due to the pad I/O circuits which have large MOSFET switches to select the local supply from either the VDD or VDDA rails. These devices are relatively large and yield a parasitic diode between VDD and VDDA. Please allow for both VDD and VDDA to power-up and power-down before measuring their respective voltages.

13.4 Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground and primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

14. Register Map

14.1 Base vs. Factory Preprogrammed Devices

The Si5397/96 devices can be ordered as “base” or “factory-preprogrammed” (also known as “custom OPN”) versions.

14.2 “Base” Devices (a.k.a. “Blank” Devices)

Example “base” orderable part numbers (OPNs) are of the form “Si5397A-E-GM” or “Si5396B-E-GM”.

Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.

Base devices do not power up in a usable state (all output clocks are disabled).

Base devices are, however, configured by default to use a 48 MHz crystal on the XA/XB reference and a 1.8 V compatible I/O voltage setting for the host I^2C/SPI interface.

Additional programming of a base device is mandatory to achieve a usable configuration.

See the on-line lookup utility at: https://www.silabs.com/timing/lookup-customize to access the default configuration plan and register settings for any base OPN.

14.3 “Factory Preprogrammed” (Custom OPN) Devices

Factory preprogammed devices use a “custom OPN”, such as Si5397A-E-xxxxx-GM, where xxxxx is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.

Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XA/XB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).

Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.

Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: https://www.silabs.com/timing/lookup-customize.

Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both “base” and “factory preprogrammed” devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see Section 4.3 NVM Programming.)

14.4 Register Map Overview and Default Settings Values

The Si5397/96 family parts have large register maps that are divided into separate “Pages” of register banks. This allows more register addresses than either the I^2C or SPI serial interface standards 8-bit addressing provide. Each page has a maximum of 256 addresses, however not all addresses are used on every page. Every register has a maximum data size of 8-bits, or 1 byte. Writing the page number to the 8-bit serial interface address of 0x01 on any page (0x0001, 0x0101, 0x0201, etc.) updates the page selection for subsequent register reads and writes. For example, to access the value in register 0x040E, it is first necessary to write the page value 0x04 to serial interface register address 0x01. At this point, the value of serial interface address 0x0E (0x040E) may be read or written. Note that is it not necessary to write the page select register again when accessing other registers on the same page. Similarly, the read-only DEVICE_READY status is available from every page at serial interface address 0xFE (0x00FE, 0x01FE, 0x02FE, etc.).

It is recommended to use dynamic Read-Modify-Write methods when writing to registers which contain multiple settings, such as register 0x0011. To do this, first read the current contents of the register. Next, update only the select bit or bits that are being modified. This may involve using both logical AND and logical OR operations. Finally, write the updated contents back to the register. Writing to pages, registers, or bits not documented below may cause undesired behavior in the device.

Details of the register and settings information are organized hierarchically below. To find the relevant information for your application, first choose the section corresponding to the base part number, Si5397, Si5396 for your design. Then, choose the section under that for the page containing the desired register(s).

Default register contents and settings differ for each device part number, or OPN. This information may be found by searching for the Custom OPN for your device using the link below. Both Base/Blank and Custom OPNs are available there. See the previous section on “Base vs. Factory Preprogrammed Devices" for more information on part numbers. The Private Addendum to the data sheet lists the default settings and frequency plan information. You must be logged into the Silicon Labs website to access this information. The Public addendum gives only the general frequency plan information (https://www.silabs.com/timing/lookup-customize).

Table 14.1. Register Map Paging Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, and other configuration
Page 1	0100h	256	Output clock configuration
Page 2	0200h	512	P and R dividers, user scratch area
Page 3	0300h	768	Internal divider value updates
Page 4	0400h	1024	DSPLLA
Page 5	0500h	1280	DSPLLB
Page 6	0600h	1536	DSPLLC, Si5397 only
Page 7	0700h	1792	DSPLLD, Si5397 only
Page 9	0900h	2304	Control IO configuration
Page A	0A00h	2560	Internal divider enables
Page B	0B00h	2816	Internal clock disables and control

R = Read Only

R/W = Read Write

S = Self Clearing

A self-clearing bit will be cleared by the device once the operation initiated by this bit is complete. Registers with “sticky” flag bits, such as LOS0_FLG, are cleared by writing “0” to the bit that has been automatically set high by the device.

15. Si5397A/B Register Map

15.1 Page 0 Registers Si5397A/B

Table 15.1. 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 15.2. 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 15.3. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x97	Four-digit “base” part number, one nibble per digit Example: Si5397A-A-GM. The base part number (OPN) is 5397, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Table 15.4. 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode. 0 = A 1 = B 2 = C 3 = D 9=J, 10=K,11=L,12=M

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 15.5. 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5397C-A12345-GM, the device revision is “A” and stored as 0

Table 15.6. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

Table 15.7. 0x0009–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5397C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5397C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5397 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 15.8. 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address. Note: This register is not bank burnable.

Table 15.9. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if there is no signal detected on the XAXB input signal.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Table 15.10. 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [3 2 1 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [3 2 1 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 15.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Table 15.12. 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4

DSPLL_B corresponds to bit 5

DSPLL_C corresponds to bit 6

DSPLL_D corresponds to bit 7

Table 15.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R/W	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to clear the flag.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Table 15.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]
- Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Table 15.15. 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Table 15.16. 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Table 15.17. 0x0016

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	3:0	R/W	LOL_ON_HOLD_PLL[D:A]	Set by CBPro.

Table 15.18. 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOS-XAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOS-REF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	XAXB_ERR_INTR_MSK	
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt
0x0017	6	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this register is 0x035.

Table 15.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1: To mask the clock input OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]
- Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 15.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]
- DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019 [2], HOLD_INTR_MSK_PLL 0x0019 [6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019 [3], HOLD_INTR_MSK_PLL 0x0019 [7]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 15.21. 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Table 15.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: Initialize and calibrate the entire device.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB
0x001C	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715.

Table 15.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

Table 15.24. 0x001E Sync, Power Down, and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1: To put the device into low power mode
0x001E	1	R/W	HARD_RST	Perform hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	1 to reset all the R dividers to the same state.

Table 15.25. 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	FSTEP_PLL_SINGLE	0: DSPLL_SEL[1:0] pins and bits are disabled. 1: DSPLL_SEL[1:0] pins or FSTEP_PLL bits are enabled. See FSTEP_PLL_REGCTRL
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only functions when FSTEP_PLL_SINGLE = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	3:2	R/W	FSTEP_PLL	Register version of the DSPLL_SEL[1:0] pins. Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: DSPLL B M-divider 2: DSPLL C M-divider 3: DSPLL D M-divider

By default ClockBuilder Pro sets OE0 controlling all outputs. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0. Note that the OE0 register bits (active high) have inverted logic sense from the pins (active low).

Table 15.26. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI.

Table 15.27. 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Input 3 (IN3): LOS_EN[3]

Table 15.28. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 15.29. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 15.30. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 15.31. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 15.32. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 15.33. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 15.34. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 15.35. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 15.36. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 15.37. 0x003E

Reg Address	Bit Field	Type	Setting Name	Description
0x003E	7:4	R/W	LOS_MIN_PERIOD_EN	Set by CBPro.

Table 15.38. 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable
0x003F	7:4	R/W	FAST_OOF_EN	1: To enable

Table 15.39. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 15.40. 0x0041-0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 15.41. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 15.42. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 15.43. 0x004E-0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DET-WIN_SEL	Values calculated by CBPro.
0x004E	6:4	R/W	OOF1_DET-WIN_SEL	
0x004F	2:0	R/W	OOF2_DET-WIN_SEL	
0x004F	6:4	R/W	OOF3_DET-WIN_SEL	

Table 15.44. 0x0050

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro.

Table 15.45. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 15.46. 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 15.47. 0x0059 Fast OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	1:0	R/W	FAST_OOF0_DET-WIN_SEL	Values calculated by CBPro.
0x0059	3:2	R/W	FAST_OOF1_DET-WIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DET-WIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DET-WIN_SEL	

Table 15.48. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 15.49. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 15.50. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 15.51. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 15.52. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Enables fast detection of LOL for PLLx. A large input frequency error will quickly assert LOL when this is enabled.
0x0092	1	R/W	LOL_FST_EN_PLLB	
0x0092	2	R/W	LOL_FST_EN_PLLC	
0x0092	3	R/W	LOL_FST_EN_PLLD	

Table 15.53. 0x0093-0x0094 Fast LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DETWIN_SEL_PLLA	Values calculated by CBPro
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL_PLLB	
0x0094	3:0	R/W	LOL_FST_DETWIN_SEL_PLLC	
0x0094	7:4	R/W	LOL_FST_DETWIN_SEL_PLLD	

Table 15.54. 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x0095	1:0	R/W	LOL_FST_VALWIN_SEL_PLLA	Values calculated by CBPro
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL_PLLB	
0x0095	5:4	R/W	LOL_FST_VALWIN_SEL_PLLC	
0x0095	7:6	R/W	LOL_FST_VALWIN_SEL_PLLD	

Table 15.55. 0x0096-0x0097 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	
0x0097	3:0	R/W	LOL_FST_SET_THR_SEL_PLLC	
0x0097	7:4	R/W	LOL_FST_SET_THR_SEL_PLLD	

Table 15.56. 0x0098-0x0099 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	
0x0099	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLC	
0x0099	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLD	

Table 15.57. 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	0	R/W	LOL_SLOW_EN_PLLA	0: To disable LOL. 1: To enable LOL.
0x009A	1		LOL_SLOW_EN_PLLB	0: To disable LOL. 1: To enable LOL.
0x009A	2		LOL_SLOW_EN_PLLC	0: To disable LOL. 1: To enable LOL.
0x009A	3		LOL_SLOW_EN_PLLD	0: To disable LOL. 1: To enable LOL.

Table 15.58. 0x009B-0x009C Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Values calculated by CBPro
0x009B	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLB	
0x009C	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLC	
0x009C	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLD	

Table 15.59. 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Values calculated by CBPro
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	
0x009D	5:4	R/W	LOL_SLW_VAL-WIN_SEL_PLLC	
0x009D	7:6	R/W	LOL_SLW_VAL-WIN_SEL_PLLD	

Table 15.60. 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. See list below for selectable values.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. See list below for selectable values.

Table 15.61. 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. See list below for selectable values.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	Configures the loss of lock set thresholds. See list below for selectable values.

The following are the LOL_SLW_SET_THR_PLLx thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm
- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 15.62. 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. See list below for selectable values.

Table 15.63. 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	Configures the loss of lock clear thresholds. See list below for selectable values.

The following are the LOL_SLW_CLR_THR_PLLx thresholds for the value that is placed in the four bits of the DSPLLs. ClockBuilder Pro sets these values.

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm
- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 15.64. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	0 1 2 3	R/W	LOL_TIMER_EN_PLLA LOL_TIMER_EN_PLLB LOL_TIMER_EN_PLLC LOL_TIMER_EN_PLLD	Enable Delay for LOL Clear. 0: Disable Delay for LOL Clear 1: Enable Delay for LOL Clear

Table 15.65. 0x00A4-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00A5	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLA	

Table 15.66. 0x00A9-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AA	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	

Table 15.67. 0x00AE-0x00B1 LOL Clear Delay DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x00AE	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AF	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	
0x00B0	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	
0x00B1	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	

Table 15.68. 0x00B3-0x00B6 LOL Clear Delay DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x00B3	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00B4	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	
0x00B5	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	
0x00B6	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	

Table 15.69. 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	7:0	R	AC-TIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See for a detailed description of how to program the NVM.

Table 15.70. 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

Table 15.71. 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	When set, this bit will read the NVM down into the volatile memory.

Table 15.72. 0x00E5

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	
0x00E5	6	R/W	FASTLOCK_EXTEND_EN_PLLC	
0x00E5	7	R/W	FASTLOCK_EXTEND_EN_PLLD	

Table 15.73. 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 15.74. 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x00EA	7:0	R/W	FASTLOCK_EXTEND_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FASTLOCK_EXTEND_PLLB	
0x00EC	23:16	R/W	FASTLOCK_EXTEND_PLLB	
0x00ED	28:24	R/W	FASTLOCK_EXTEND_PLLB	

Table 15.75. 0x00EE-0x00F1 FASTLOCK_EXTEND_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x00EE	7:0	R/W	FASTLOCK_EXTEND_PLLC	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EF	15:8	R/W	FASTLOCK_EXTEND_PLLC	
0x00F0	23:16	R/W	FASTLOCK_EXTEND_PLLC	
0x00F1	28:24	R/W	FASTLOCK_EXTEND_PLLC	

Table 15.76. 0x00F2-0x00F5 FASTLOCK_EXTEND_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x00F2	7:0	R/W	FASTLOCK_EXTEND_PLLD	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00F3	15:8	R/W	FASTLOCK_EXTEND_PLLD	
0x00F4	23:16	R/W	FASTLOCK_EXTEND_PLLD	
0x00F5	28:24	R/W	FASTLOCK_EXTEND_PLLD	

Table 15.77. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 15.78. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 15.79. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 15.80. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	0:3	R	LOL_INTR_PLL[D:A]	Set by CBPro.
0x00F9	7:4	R	HOLD_INTR_PLL[D:A]	Set by CBPro.

Table 15.81. 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page so that a page write is not ever required to read the DEVICE_READY status.

WARNING: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note this includes writes to the PAGE register.

15.2 Page 1 Registers Si5397A/B

Table 15.82. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers 1: Pass through the output enables.

Table 15.83. 0x0108, 0x0112, 0x0117, 0x011C, 0x0126, 0x012B, 0x0130, 0x013AClock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0108	0	R/W	OUT0_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pull-down effect.
0x0112			OUT1_PDN	
0x0117			OUT2_PDN	
0x011C			OUT3_PDN	
0x0126			OUT4_PDN	
0x012B			OUT5_PDN	
0x0130			OUT6_PDN	
0x013A			OUT7_PDN	
0x0108	1	R/W	OUT0_OE	0: To disable the output 1: To enable the output
0x0112			OUT1_OE	
0x0117			OUT2_OE	
0x011C			OUT3_OE	
0x0126			OUT4_OE	
0x012B			OUT5_OE	
0x0130			OUT6_OE	
0x013A			OUT7_OE	

Reg Address	Bit Field	Type	Setting Name	Description
0x0108 0x0112 0x0117 0x011C 0x0126 0x012B 0x0130 0x013A	2	R/W	OUT0_RDIV_FORCE2 OUT1_RDIV_FORCE2 OUT2_RDIV_FORCE2 OUT3_RDIV_FORCE2 OUT4_RDIV_FORCE2 OUT5_RDIV_FORCE2 OUT6_RDIV_FORCE2 OUT7_RDIV_FORCE2	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2

The output drivers are all identical. See .

Table 15.84. 0x0109, 0x0113, 0x0118, 0x011D, 0x0127, 0x012C, 0x0131, 0x013B Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT OUT4_FORMAT OUT5_FORMAT OUT6_FORMAT OUT7_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5: LVCMOS (+pin only) 6: LVCMOS (-pin only) 7: Reserved
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN OUT4_SYNC_EN OUT5_SYNC_EN OUT6_SYNC_EN OUT7_SYNC_EN	0: Disable 1: Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0109	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high 2-3: Reserved
0x0113			OUT1_DIS_STATE	
0x0118			OUT2_DIS_STATE	
0x011D			OUT3_DIS_STATE	
0x0127			OUT4_DIS_STATE	
0x012C			OUT5_DIS_STATE	
0x0131			OUT6_DIS_STATE	
0x013B			OUT7_DIS_STATE	
0x0109	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance drive strength see .
0x0113			OUT1_CMOS_DRV	
0x0118			OUT2_CMOS_DRV	
0x011D			OUT3_CMOS_DRV	
0x0127			OUT4_CMOS_DRV	
0x012C			OUT5_CMOS_DRV	
0x0131			OUT6_CMOS_DRV	
0x013B			OUT7_CMOS_DRV	

The output drivers are all identical.

Table 15.85. 0x010A, 0x0114, 0x0119, 0x011E, 0x0128, 0x012D, 0x0132, 0x0137 Output Amplitude and Common Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x010A	3:0	R/W	OUT0_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .
0x0114			OUT1_CM	
0x0119			OUT2_CM	
0x011E			OUT3_CM	
0x0128			OUT4_CM	
0x012D			OUT5_CM	
0x0132			OUT6_CM	
0x0137			OUT7_CM	
0x010A	6:4	R/W	OUT0_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .
0x0114			OUT1_AMPL	
0x0119			OUT2_AMPL	
0x011E			OUT3_AMPL	
0x0128			OUT4_AMPL	
0x012D			OUT5_AMPL	
0x0132			OUT6_AMPL	
0x0137			OUT7_AMPL	

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Table 15.86. 0x010B, 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133, 0x013D Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x010B 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x013D	2:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL OUT4_MUX_SEL OUT5_MUX_SEL OUT6_MUX_SEL OUT7_MUX_SEL	Output driver input mux select.This selects the source of the output clock. 0: DSPLL A 1: DSPLL B 2: DSPLL C 3: DSPLL D 5-7: Reserved
0x010B 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x013D	3	R/W	OUT0_VDD_SEL_EN OUT1_VDD_SEL_EN OUT2_VDD_SEL_EN OUT3_VDD_SEL_EN OUT4_VDD_SEL_EN OUT5_VDD_SEL_EN OUT6_VDD_SEL_EN OUT7_VDD_SEL_EN	0: Reserved 1: Enable manual OUTx_VDD_SEL
0x010B 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x013D	5:4	R/W	OUT0_VDD_SEL OUT1_VDD_SEL OUT2_VDD_SEL OUT3_VDD_SEL OUT4_VDD_SEL OUT5_VDD_SEL OUT6_VDD_SEL OUT7_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x010B	7:6	R/W	OUT0_INV	LVCMOS output inversion. Only applies when OUT0A_FORMAT = 4. See for more information.
0x0115			OUT1_INV	
0x011A			OUT2_INV	
0x011F			OUT3_INV	
0x0129			OUT4_INV	
0x012E			OUT5_INV	
0x0133			OUT6_INV	
0x013D			OUT7_INV	

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical. The OUTx_MUX_SEL settings should match the corresponding OUTx_DIS_SRC selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 15.87. 0x010C, 0x0116, 0x011B, 0x0120, 0x012A, 0x012F, 0x0134, 0x0139 Output Disable Source DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x010C	2:0	R/W	OUT0_DIS_SRC	Output driver 0 input mux select. This selects the source of the output clock. 0: DSPLL A squelches output 1: DSPLL B squelches output 2: DSPLL C squelches output 3: DSPLL D squelches output 5-7: Reserved
0x0116			OUT1_DIS_SRC	
0x011B			OUT2_DIS_SRC	
0x0120			OUT3_DIS_SRC	
0x012A			OUT4_DIS_SRC	
0x012F			OUT5_DIS_SRC	
0x0134			OUT6_DIS_SRC	
0x013E			OUT7_DIS_SRC	

These CLKx_DIS_SRC settings should match the corresponding OUTx_MUX_SEL selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 15.88. 0x013F

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	11:0	R/W	OUTX_AL-WAYS_ON	Set by CBPro

Table 15.89. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	0	R/W	OUT_DIS_MSK_PLLA	Set by CBPro
0x0141	1	R/W	OUT_DIS_MSK_PLLB	
0x0141	2	R/W	OUT_DIS_MSK_PLLC	
0x0141	3	R/W	OUT_DIS_MSK_PLLD	
0x0141	5	R/W	OUT_DIS_LOL_MSK	
0x0141	6	R/W	OUT_DIS_LOS-XAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	Set by CBPro

Table 15.90. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MSK_LOL_PLL[D:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	7:4	R/W	OUT_DIS_MSK_HOLD_PLL[D:A]	Set by CBPro.

Bit 0 LOL_DSPLL_A mask

Bit 1 LOL_DSPLL_B mask

Bit 2 LOL_DSPLL_C mask

Bit 3 LOL_DSPLL_D mask

15.3 Page 2 Registers Si5397A/B

Table 15.91. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This valid with external clock sources, not crystals.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 3 = pre-scale value 8

Note that changing this register furing operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.92. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.93. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.94. Si5397A/B P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211

Register Address	Description	Size	Same as Address
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.95. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in . Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values.

Table 15.96. 0x0231 P0 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 15.97. 0x0232 P1 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 15.98. 0x0233 P2 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 15.99. 0x0234 P3 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 15.100. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.101. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 15.102. 0x023F

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	R/W	MXAXB_UPDATE	The divider value for the XAXB input

Table 15.103. 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x024A	7:0	R/W	R0_REG	24-bit Integer output divider divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 15.104. Si5397A/B R1–R7 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0250-0x0252	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0253-0x0255	R2_REG	24-bit Integer Number	0x024A-0x024C
0x0256-0x0258	R3_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R4_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R5_REG	24-bit Integer Number	0x024A-0x024C
0x0262-0x0264	R6_REG	24-bit Integer Number	0x024A-0x024C
0x0268-0x026A	R7_REG	24-bit Integer Number	0x024A-0x024C

Table 15.105. 0x026B–0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 15.106. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5397A-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5397A-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5397A-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5397 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 15.107. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 15.108. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 15.109. 0x028A-0x028D

Reg Address	Bit Field	Type	Setting Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	The OOF0 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	The OOF1 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	The OOF2 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	The OOF3 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 15.110. 0x028E-0x0291

Reg Address	Bit Field	Type	Setting Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	The OOF0 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	The OOF1 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	The OOF2 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	The OOF3 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 15.111. 0x0292-0x0293

Reg Address	Bit Field	Type	Setting Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro.
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro.

Table 15.112. 0x0294-0x0295 FASTLOCK EXTEND SCL PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro.
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	
0x0295	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLC	
0x0295	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLD	

Table 15.113. 0x0296 LOL SLW VALWIN SELX PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	
0x0296	2	R/W	LOL_SLW_VALWIN_SELX_PLLC	
0x0296	3	R/W	LOL_SLW_VALWIN_SELX_PLLD	

Table 15.114. 0x0297 FASTLOCK_DLY_ONSW_EN_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0297	0	R/W	FAST-LOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FAST-LOCK_DLY_ONSW_EN_PLLB	
0x0297	2	R/W	FAST-LOCK_DLY_ONSW_EN_PLLC	
0x0297	3	R/W	FAST-LOCK_DLY_ONSW_EN_PLLD	

Table 15.115. 0x0299 FASTLOCK_DLY_ONLOL_EN_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0299	0	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLB	
0x0299	2	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLC	
0x0299	3	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLD	

Table 15.116. 0x029A-0x029C FASTLOCK_DLY_ONLOL_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x029A	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	
0x029C	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	

Table 15.117. 0x029D-0x029F FASTLOCK_DLY_ONLOL_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x029D	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	

Table 15.118. 0x02A0-0x02A2 FASTLOCK_DLY_ONLOL_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x02A0	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	Set by CBPro.
0x02A1	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	
0x02A2	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	

Table 15.119. 0x02A3-0x02A5 FASTLOCK_DLY_ONLOL_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x02A3	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	Set by CBPro.
0x02A4	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	
0x02A5	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	

Table 15.120. 0x02A6-0x02A8 FASTLOCK DLY ONSW PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	20-bit value. Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 15.121. 0x02A9-0x02AB FASTLOCK DLY ONSW PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 15.122. 0x02AC-0x02AE FASTLOCK_DLY_ONSW_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x02AC	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLC	20-bit value. Set by CBPro.
0x02AD	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLC	
0x02AE	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLC	

Table 15.123. 0x02AF-0x02B1 FASTLOCK_DLY_ONSW_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x02AF	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLD	20-bit value. Set by CBPro.
0x02B0	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLD	
0x02B1	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLD	

Table 15.124. 0x02B7 LOL_NOSIG_TIME_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	
0x02B7	5:4	R/W	LOL_NO-SIG_TIME_PLLC	
0x02B7	7:6	R/W	LOL_NO-SIG_TIME_PLLD	

Table 15.125. 0x02B8 LOL LOS REFCLK PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8	0	R/W	LOL_LOS_REFCLK_PLLA	Set by CBPro.
0x02B8	1	R/W	LOL_LOS_REFCLK_PLLB	Set by CBPro.
0x02B8	2	R/W	LOL_LOS_REFCLK_PLLC	Set by CBPro.
0x02B8	3	R/W	LOL_LOS_REFCLK_PLLD	Set by CBPro.

Table 15.126. 0x02B9 LOL NOSIG TIME PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	0	R/W	LOL_LOS_REFCLK_PLLA_FLG	Set by CBPro.
0x02B9	1	R/W	LOL_LOS_REFCLK_PLLB_FLG	Set by CBPro.
0x02B9	2	R/W	LOL_LOS_REFCLK_PLLC_FLG	Set by CBPro.
0x02B9	3	R/W	LOL_LOS_REFCLK_PLLD_FLG	Set by CBPro.

Table 15.127. 0x02BC

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

15.4 Page 3 Registers Si5397A/B

Table 15.128. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 15.129. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer.
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.130. 0x030C N0 Update

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. A Soft Reset will have the same effect.

Table 15.131. N0_NUM and N0_DEN Definitions

Reg Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 15.132. 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

15.5 Page 4 Registers Si5397A/B

Table 15.133. 0x0407 DSPLL A Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 15.134. 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Parameters that create the normal PLL bandwidth
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 15.135. 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST-LOCK_BW0_PLLA	Parameters that create the fast lock PLL bandwidth
0x040F	5:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	5:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	5:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	5:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	5:0	R/W	FAST-LOCK_BW5_PLLA	
0x0414	0	S	BW_UP-DATE_PLLA	0: No effect 1: Update both the Normal and Fastlock BWs for PLL A.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the

BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 15.136. 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56-bit number.
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.137. 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.138. 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 15.139. 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 15.140. 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0422	1	R/W	M_FSTEP_DEN_PLLA	Set by CBPro.

Table 15.141. 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Table 15.142. 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register-based clock selection.

Table 15.143. 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 15.144. 0x042C Holdover Exit Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042C	0	R/W	HOLD_EN_PLLA	Holdover Enable 0: Holdover Disabled 1: Holdover Enabled
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Set by CBPro.
0x042C	4	R/W	HOLDEXIT_BW_SEL1_PLLA	Holdover Exit Bandwidth select. Selects the exit bandwidth from Holdover when ramped exit is disabled (HOLD_RAMP_BYP_PLLA = 1). 0: Exit Holdover using Holdover Exit or Fastlock bandwidths (default). See HOLDEXIT_BW_SEL0_PLLA (0x049B[6]) for additional information. 1: Exit Holdover using the Normal loop bandwidth
0x042C	5:7	R/W	RAMP_STEP_INTERVAL_PLLA	Time Interval of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.

Table 15.145. 0x042D

Reg Address	Bit Field	Type	Setting Name	Description
0x042D	1	R/W	HOLD_RAMP_BYP_NOHIST_PLLA	Set by CBPro.

Table 15.146. 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 15.147. 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the window length from the register value. time = (2^{DELAY})*268nsec

Table 15.148. 0x0431

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	5- bit value

Table 15.149. 0x0432

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Value calculated by CBPro
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 15.150. 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Table 15.151. 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 15.152. 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Table 15.153. 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.154. 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.155. 0x043A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0,2,3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 1,2,3: Reserved

Table 15.156. 0x043B-0x043C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Set by CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 15.157. 0x043D

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Set by CBPro

Table 15.158. 0x043E

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Set by CBPro

Table 15.159. 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 15.160. 0x0442-0x0444

Reg Address	Bit Field	Type	Setting Name	Description
0x0442	7:0	R/W	FINE_ADJ_OVR_PLLA	Set by CBPro
0x0443	15:8	R/W	FINE_ADJ_OVR_PLLA	
0x0444	17:16	R/W	FINE_ADJ_OVR_PLLA	

Table 15.161. 0x0445

Reg Address	Bit Field	Type	Setting Name	Description
0x0445	1	R/W	FORCE_FINE_ADJ_PLLA	Set by CBPro

Table 15.162. 0x0488 HSW_FINE_PM_LEN_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Set by CBPro.

Table 15.163. 0x0489 PFD_EN_DELAY_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	7:0	R/W	PFD_EN_DELAY_PLLA	Set by CBPro.
0x048A	12:8	R/W	PFD_EN_DELAY_PLLA	

Table 15.164. 0x048B

Reg Address	Bit Field	Type	Setting Name	Description
0x048B	19:0	R/W	HSW_MEAS_SETTLE_PLLA	Set by CBPro.

Table 15.165. 0x049B HOLDEXIT_BW_SEL0_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	Set by CBPro.
0x049B	2	R/W	HO_SKIP_PHASE_PLLA	Set by CBPro.
0x049B	4	R/W	HOLD_PRESERVE_HIST_PLLA	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLA	Set by CBPro.
0x049B	6	R/W	HOLDEX-IT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEX-IT_STD_BO_PLLA	Set by CBPro.

Table 15.166. 0x049C

Reg Address	Bit Field	Type	Setting Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NOHIST_PLLA	Set by CBPro.

Table 15.167. 0x049D-0x04A2 DSPLL Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	5:0	R/W	BW0_HO_PLLA	DSPLL A Holdover Bandwidth parameters.
0x049E	5:0	R/W	BW1_HO_PLLA	
0x049F	5:0	R/W	BW2_HO_PLLA	
0x04A0	5:0	R/W	BW3_HO_PLLA	
0x04A1	5:0	R/W	BW4_HO_PLLA	
0x04A2	5:0	R/W	BW5_HO_PLLA	

This group of registers determines the DSPLL A bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that the individual SOFT_RST_PLLA (0x001C[1]) does not update these bandwidth parameters.

Table 15.168. 0x04A4-0x04A5

Reg Address	Bit Field	Type	Setting Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Set by CBPro.
0x04A5	0	R/W	HSW_LIMIT_ACTION_PLLA	Set by CBPro.

Table 15.169. 0x04A6

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	Set by CBPro.
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	Set by CBPro.

Table 15.170. 0x04AC-0x04B2

Reg Address	Bit Field	Type	Setting Name	Description
0x04AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLA	Set by CBPro.
0x04AD	15:0	R/W	OUT_MAX_LIM-IT_LMT_PLLA	Set by CBPro.
0x04B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLA	Set by CBPro.

15.6 Page 5 Registers Si5397A/B

Table 15.171. 0x0507 DSPLL B Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 15.172. 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Parameters that create the normal PLL bandwidth
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 15.173. 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLLB	Parameters that create the fast lock PLL bandwidth
0x050F	5:0	R/W	FAST-LOCK_BW1_PLLB	
0x0510	5:0	R/W	FAST-LOCK_BW2_PLLB	
0x0511	5:0	R/W	FAST-LOCK_BW3_PLLB	
0x0512	5:0	R/W	FAST-LOCK_BW4_PLLB	
0x0513	5:0	R/W	FAST-LOCK_BW5_PLLB	
0x0514	0	S	BW_UP-DATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of

the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 15.174. 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.175. 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MB divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.176. 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 15.177. 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.

Table 15.178. 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0522	1	R/W	M_FSTEPW_DEN_PLLB	0: Modify numerator 1: Modify denominator

Table 15.179. 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEPW_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEPW_PLLB	
0x0525	23:16	R/W	M_FSTEPW_PLLB	
0x0526	31:24	R/W	M_FSTEPW_PLLB	
0x0527	39:32	R/W	M_FSTEPW_PLLB	
0x0528	47:40	R/W	M_FSTEPW_PLLB	
0x0529	55:48	R/W	M_FSTEPW_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0515–0x051F.

Table 15.180. 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	0: Pin Control 1: Register Control
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 15.181. 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FASTLOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	1	R/W	FAST-LOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Table 15.182. 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	0: Holdover Disabled 1: Holdover Enabled
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EX-IT_BW_SEL1_PLLB	0: To use the fastlock loop BW when exiting from hold-over 1: To use the normal loop BW when exiting from hold-over
0x52C	7:5	R/W	RAMP_STEP_IN-TERVAL_PLLB	Controls the frequency ramp rate when exiting from holdover. Set by CBPro.

Table 15.183. 0x052D

Reg Address	Bit Field	Type	Setting Name	Description
0x052D	1	R/W	HOLD_RAMP-BYP_NOH-IST_PLLB	Set by CBPro.

Table 15.184. 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 15.185. 0x052F DSPLLB Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R/W	HOLD_HIST_DE-LAY_PLLB	5-bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 15.186. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC_PLLB	5- bit value

Table 15.187. 0x0532

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Set by CBPro.
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 15.188. 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Table 15.189. 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 15.190. 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]

IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]

IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]

IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Table 15.191. 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.192. 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.193. 0x053A DSPLL B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1:Default setting, do not modify 0,2,3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1,2,3: Reserved

Table 15.194. 0x053B-0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 15.195. 0x053D

Reg Address	Bit Field	Type	Setting Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Set by CBPro.

Table 15.196. 0x053E

Reg Address	Bit Field	Type	Setting Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Set by CBPro.

Table 15.197. 0x053F DSPLL B Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 15.198. 0x0542-0x0544 FINE_ADJ_OVR_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0542	7:0	R/W	FINE_ADJ_OVR_PLLB	Set by CBPro.
0x0543	15:8	R/W	FINE_ADJ_OVR_PLLB	
0x0544	17:16	R/W	FINE_ADJ_OVR_PLLB	

Table 15.199. 0x0545 FORCE_FINE_ADJ_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0545	1	R/W	FORCE_FINE_ADJ_PLLB	Set by CBPro.

Table 15.200. 0x0588 HSW_FINE_PM_LEN_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	Set by CBPro.

Table 15.201. 0x0589 PFD_EN_DELAY_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	Set by CBPro.
0x0589	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 15.202. 0x058B

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	19:0	R/W	HSW_MEAS_SETTLE_PLLB	Set by CBPro.

Table 15.203. 0x059B HOLDEXIT_BW_SEL0_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	IN-IT_LP_CLOSE_HO_PLLB	Set by CBPro.
0x059B	2	R/W	HO_SKIP_PHASE_PLLB	
0x059B	4	R/W	HOLD_PRE-SERVE_HIST_PLLB	
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	
0x059B	6	R/W	HOLDEX-IT_BW_SEL0_PLLB	
0x059B	7	R/W	HOLDEX-IT_STD_BO_PLLB	

Table 15.204. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NOHIST_PLLB	Set by CBPro.

Table 15.205. 0x059D-0x05A2 DSPLL Holdover Exit Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEX-IT_BW0_PLLB	DSPLL B Fastlock Bandwidth parameters.
0x059E	5:0	R/W	HOLDEX-IT_BW1_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1.
0x059F	5:0	R/W	HOLDEX-IT_BW2_PLLB	
0x05A0	5:0	R/W	HOLDEX-IT_BW3_PLLB	
0x05A1	5:0	R/W	HOLDEX-IT_BW4_PLLB	
0x05A2	5:0	R/W	HOLDEX-IT_BW5_PLLB	

This group of registers determines the DSPLL B bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that the individual SOFT_RST_PLLB (0x001C[2]) does not update these bandwidth parameters.

Table 15.206. 0x05A4-0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Set by CBPro.
0x05A5	0	R/W	HSW_LIMIT_AC-TION_PLLB	Set by CBPro.

Table 15.207. 0x05A6

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE_PLLB	Sets the size of the frequency step when frequency ramping is used for holdover exit. Set by CBPro.
0x05A6	3	R/W	RAMP_SWITCH_EN_PLLB	1 = enable frequency ramping on holdover exit.

Table 15.208. 0x05AC-0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLB	Set by CBPro.
0x05AD	15:0	R/W	OUT_MAX_LIM-IT_LMT_PLLB	Set by CBPro.
0x05B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLB	Set by CBPro.

15.7 Page 6 Registers Si5397A/B

Table 15.209. 0x0607 DSPLL C Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 15.210. 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	5:0	R/W	BW0_PLLC	Parameters that create the normal PLL bandwidth
0x0609	5:0	R/W	BW1_PLLC	
0x060A	5:0	R/W	BW2_PLLC	
0x060B	5:0	R/W	BW3_PLLC	
0x060C	5:0	R/W	BW4_PLLC	
0x060D	5:0	R/W	BW5_PLLC	

This group of registers determines the DSPLL C loop bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 15.211. 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	5:0	R/W	FAST-LOCK_BW0_PLLC	Parameters that create the fast lock PLL bandwidth
0x060F	5:0	R/W	FAST-LOCK_BW1_PLLC	
0x0610	5:0	R/W	FAST-LOCK_BW2_PLLC	
0x0611	5:0	R/W	FAST-LOCK_BW3_PLLC	
0x0612	5:0	R/W	FAST-LOCK_BW4_PLLC	
0x0613	5:0	R/W	FAST-LOCK_BW5_PLLC	
0x0614	0	S	BW_UP-DATE_PLLC	0: No effect. 1: Update both the Normal and Fastback BWs for PLL C.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of

the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 15.212. 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	56-bit number
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

The MC divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.213. 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	32-bit number
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

The loop MC divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.214. 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UPDATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 15.215. 0x0621 DSPLL C M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	3:0	R/W	M_FRAC_MODE_PLLC	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0621	4	R/W	M_FRAC_EN_PLLC	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0621	5	R/W	Reserved	Must be set to 1 for DSPLL C

Table 15.216. 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0622	1	R/W	M_FSTEPW_DEN_PLLC	0: Modify numerator 1: Modify denominator

Table 15.217. 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	56-bit number
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F.

Table 15.218. 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 15.219. 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLC is out of lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Table 15.220. 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062C	0	R/W	HOLD_EN_PLLC	0: Holdover disabled 1: Holdover enabled
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	Must be set to 1 for normal operation.
0x062C	4	R/W	HOLD_EXIT_BW_SEL1_PLLC	0: Use Fastlock bandwidth for Holdover Entry/Exit (default) 1: Use the normal loop BW when exiting from holdover
0x062C	7:5	R/W	RAMP_STEP_INTERVAL_PLLC	Set by CBPro.

Table 15.221. 0x062D

Reg Address	Bit Field	Type	Setting Name	Description
0x062D	1	R/W	HOLD_RAMPBYP_NOHIST_PLLC	Set by CBPro.

Table 15.222. 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 15.223. 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 15.224. 0x0631

Reg Address	Bit Field	Type	Setting Name	Description
0x0631	4:0	R/W	HOLD_REF_COUNT_FRC_PLLC	Set by CBPro.

Table 15.225. 0x0632-0x0634

Reg Address	Bit Field	Type	Setting Name	Description
0x0632	7:0	R/W	HOLD_15M_CYC_COUNT_PLLC	Set by CBPro.
0x0633	15:8	R/W	HOLD_15M_CYC_COUNT_PLLC	
0x0634	23:16	R/W	HOLD_15M_CYC_COUNT_PLLC	

Table 15.226. 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Table 15.227. 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 15.228. 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN2 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

IN3 Input 3 applies to LOS alarm 0x0637[3], OOF alarm 0x0637[7]

Table 15.229. 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.230. 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0639	6:4	R/W	IN3_PRIORITY_PLLC	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.231. 0x063A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x063A	1:0	R/W	HSW_MODE_PLLC	1:Default setting, do not modify 0,2,3: Reserved
0x063A	3:2	R/W	HSW_PHMEAS_CTRL_PLLC	0: Default setting, do not modify 1,2,3: Reserved

Table 15.232. 0x063B-0x063C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x063B	7:0	R/W	HSW_PHMEAS_THR_PLLC	10-bit value. Set by CBPro.
0x063C	9:8	R/W	HSW_PHMEAS_THR_PLLC	

Table 15.233. 0x063D

Reg Address	Bit Field	Type	Setting Name	Description
0x063D	4:0	R/W	HSW_COARSE_PM_LEN_PLLC	Set by CBPro.

Table 15.234. 0x063E

Reg Address	Bit Field	Type	Setting Name	Description
0x063E	4:0	R/W	HSW_COARSE_PM_DLY_PLLC	Set by CBPro.

Table 15.235. 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x063F	2	R	FASTLOCK_STATUS_PLLC	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLC accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 15.236. 0x0642-0x0644

Reg Address	Bit Field	Type	Setting Name	Description
0x0642	7:0	R/W	FINE_ADJ_OVR_PLLC	Set by CBPro.
0x0643	15:8	R/W	FINE_ADJ_OVR_PLLC	
0x0644	17:16	R/W	FINE_ADJ_OVR_PLLC	

Table 15.237. 0x0645

Reg Address	Bit Field	Type	Setting Name	Description
0x0645	1	R/W	FORCE_FINE_ADJ_PLLC	Set by CBPro.

Table 15.238. 0x0688 HSW_FINE_PM_LEN_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0688	3:0	R/W	HSW_FINE_PM_LEN_PLLC	Set by CBPro.

Table 15.239. 0x0689 PFD_EN_DELAY_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0689	7:0	R/W	PFD_EN_DELAY_PLLC	Set byCBPro.
0x0689	12:8	R/W	PFD_EN_DELAY_PLLC	

Table 15.240. 0x068B

Reg Address	Bit Field	Type	Setting Name	Description
0x068B	19:0	R/W	HSW_MEAS_SETTLE_PLLC	Set by CBPro.

Table 15.241. 0x069B HOLDEXIT_BW_SEL0_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	1	R/W	INIT_LP_CLOSE_HO_PLLB	
0x069B	2	R/W	HO_SKIP_PHASE_PLLC	Set by CBPro.
0x069B	4	R/W	HOLD_PRESERVE_HIST_PLLC	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLC	Set by CBPro.
0x069B	6	R/W	HOLDEX-IT_BW_SEL0_PLLC	Set by CBPro.
0x069B	7	R/W	HOLDEX-IT_STD_BO_PLLC	Set by CBPro.

Table 15.242. 0x069C

Reg Address	Bit Field	Type	Setting Name	Description
0x069C	6	R/W	HOLDEX-IT_ST_BO_PLLC	Set by CBPro.
0x069C	7	R/W	HOLD_RAMPBP_NOHIST_PLLC	Set by CBPro.

Table 15.243. 0x069D-0x06A2 DSPLL Holdover Exit Bandwidth for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x069D	5:0	R/W	HOLDEX-IT_BW0_PLLC	DSPLL C Fastlock Bandwidth parameters.
0x069E	5:0	R/W	HOLDEX-IT_BW1_PLLC	
0x069F	5:0	R/W	HOLDEX-IT_BW2_PLLC	
0x06A0	5:0	R/W	HOLDEX-IT_BW3_PLLC	
0x06A1	5:0	R/W	HOLDEX-IT_BW4_PLLC	
0x06A2	5:0	R/W	HOLDEX-IT_BW5_PLLC	

This group of registers determines the DSPLL C bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that the individual SOFT_RST_PLLC (0x001C[3]) does not update these bandwidth parameters.

Table 15.244. 0x06A4-0x06A5

Reg Address	Bit Field	Type	Setting Name	Description
0x06A4	7:0	R/W	HSW_LIMIT_PLLC	Set by CBPro.
0x06A5	0	R/W	HSW_LIMIT_ACTION_PLLC	Set by CBPro.

Table 15.245. 0x06A6

Reg Address	Bit Field	Type	Setting Name	Description
0x06A6	2:0	R/W	RAMP_STEP_SIZE_PLLC	Set by CBPro.
0x06A6	3	R/W	RAMP_SWITCH_EN_PLLC	

Table 15.246. 0x06AC-0x06B2

Reg Address	Bit Field	Type	Setting Name	Description
0x06AC	0	R/W	OUT_MAX_LIMIT_EN_PLLC	Set by CBPro.
0x06AC	3	R/W	HOLD_SETTLE_DET_EN_PLLC	Set by CBPro.
0x06AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLC	Set by CBPro.
0x06B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLC	Set by CBPro.

15.8 Page 7 Registers Si5397A/B

Note that register addresses for Page 7 DSPLL D Registers 0x0709–0x074D are incremented relative to similar DSPLL A/B/C addresses on Pages 4, 5, and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0508/0x0608.

Table 15.247. 0x0708 DSPLL D Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	2:0	R	IN_PLLD_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3 4: Reserved

Table 15.248. 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	5:0	R/W	BW0_PLLD	Parameters that create the normal PLL bandwidth
0x070A	5:0	R/W	BW1_PLLD	
0x070B	5:0	R/W	BW2_PLLD	
0x070C	5:0	R/W	BW3_PLLD	
0x070D	5:0	R/W	BW4_PLLD	
0x070E	5:0	R/W	BW5_PLLD	

This group of registers determines the DSPLL D loop bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 15.249. 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	5:0	R/W	FAST-LOCK_BW0_PLLD	Parameters that create the fast lock PLL bandwidth
0x0710	5:0	R/W	FAST-LOCK_BW_1PLLD	
0x0711	5:0	R/W	FAST-LOCK_BW2_PLLD	
0x0712	5:0	R/W	FAST-LOCK_BW3_PLLD	
0x0713	5:0	R/W	FAST-LOCK_BW_4PLLD	
0x0714	5:0	R/W	FAST-LOCK_BW5_PLLD	

Reg Address	Bit Field	Type	Setting Name	Description
0x0715	0	S	BW_UP-DATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 15.250. 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	56- bit number
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MD divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.251. 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	32-bit number
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MD divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 15.252. 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 15.253. 0x0722 DSPLL D M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	3:0	R/W	M_FRAC_MODE_PLLD	M feedback divider fractional mode. Must be set to 0xB for proper operation.

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	4	R/W	M_FRAC_EN_PLL D	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0722	5	R/W	Reserved	Must be set to 1 for DSPLL D

Table 15.254. 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_P LLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0723	1	R/W	M_FSTEPW_DEN_ PLLD	0: Modify numerator 1: Modify denominator

Table 15.255. 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	56-bit number
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716–0x0720.

Table 15.256. 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 15.257. 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLD is out of lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Table 15.258. 0x072D DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	0	R/W	HOLD_EN_PLLD	0: Holdover disabled 1: Holdover enabled
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	Must be set to 1 for normal operation.
0x072D	4	R/W	HOLDEXIT_BW_SEL1_PLLD	0: Use Fastlock bandwidth for Holdover Entry/Exit (default) 1: Use the normal loop BW when exiting from holdover
0x072D	7:5	R/W	RAMP_STEP_INTERVAL_PLLD	Set by CBPro.

Table 15.259. 0x072E

Reg Address	Bit Field	Type	Setting Name	Description
0x072E	1	R/W	HOLD_RAMPBYP_NOHIST_PLLD	Set by CBPro.

Table 15.260. 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 15.261. 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 15.262. 0x0732

Reg Address	Bit Field	Type	Setting Name	Description
0x0732	4:0	R/W	HOLD_REF_COUNT_FRC_PLLD	5- bit value

Table 15.263. 0x0733-0x0735

Reg Address	Bit Field	Type	Setting Name	Description
0x0733	7:0	R/W	HOLD_15M_CYC_COUNT_PLLD	Set by CBPro.
0x0734	15:8	R/W	HOLD_15M_CYC_COUNT_PLLD	
0x0735	23:16	R/W	HOLD_15M_CYC_COUNT_PLLD	

Table 15.264. 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover

Table 15.265. 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 15.266. 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applies to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

IN3 Input 3 applies to LOS alarm 0x0738[3], OOF alarm 0x0738[7]

Table 15.267. 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.268. 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	6:4	R/W	IN3_PRIORI-TY_PLLD	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 15.269. 0x073B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x073B	1:0	R/W	HSW_MODE_PLLD	1:Default setting, do not modify 0,2,3: Reserved
0x073B	3:2	R/W	HSW_PHMEAS_CT RL_PLLD	0: Default setting, do not modify 1,2,3: Reserved

Table 15.270. 0x073C-0x073D Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x073C	7:0	R/W	HSW_PHMEAS_TH R_PLLD	10-bit value. Set by CBPro.
0x073D	9:8	R/W	HSW_PHMEAS_TH R_PLLD	

Table 15.271. 0x073E

Reg Address	Bit Field	Type	Setting Name	Description
0x073E	4:0	R/W	HSW_COARSE_P M_LEN_PLLD	Set by CBPro.

Table 15.272. 0x073F

Reg Address	Bit Field	Type	Setting Name	Description
0x073F	4:0	R/W	HSW_COARSE_P M_DLY_PLLD	Set by CBPro.

Table 15.273. 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VAL-ID_PLLD	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	2	R	FASTLOCK_STATUS_PLLD	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLD accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 15.274. 0x0743-0x0745

Reg Address	Bit Field	Type	Setting Name	Description
0x0743	7:0	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.
0x0744	15:8	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.
0x0745	17:16	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.

Table 15.275. 0x0746

Reg Address	Bit Field	Type	Setting Name	Description
0x0746	1	R/W	FORCE_FINE_ADJ_PLLD	Set by CBPro.

Table 15.276. 0x0789-0x078A

Reg Address	Bit Field	Type	Setting Name	Description
0x0789	7:0	R/W	PFD_EN_DELAY_PLLD	Set by CBPro.
0x078A	12:8	R/W	PFD_EN_DELAY_PLLD	Set by CBPro.

Table 15.277. 0x078B

Reg Address	Bit Field	Type	Setting Name	Description
0x078B	19:0	R/W	HSW_MEAS_SETTLE_PLLD	Set by CBPro.

Table 15.278. 0x079B

Reg Address	Bit Field	Type	Setting Name	Description
0x079B	1	R/W	INIT_LP_CLOSE_HO_PLLD	
0x079B	2	R/W	HO_SKIP_PHASE_PLLD	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x079B	4	R/W	HOLD_PRE-SERVE_HIST_PLL D	Set by CBPro.
0x079B	5	R/W	HOLD_FRZ_WITH_ INTONLY_PLLD	Set by CBPro.
0x079B	6	R/W	HOLDEX-IT_BW_SEL0_PLL D	Set by CBPro.
0x079B	7	R/W	HOLDEX-IT_STD_BO_PLLD	Set by CBPro.

Table 15.279. 0x079C

Reg Address	Bit Field	Type	Setting Name	Description
0x079C	6	R/W	HOLDEX-IT_ST_BO_PLLD	Set by CBPro.
0x079C	7	R/W	HOLD_RAMPBP_N OHIST_PLLD	Set by CBPro.

Table 15.280. 0x079D-0x07A2 DSPLL Holdover Exit Bandwidth for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x079D	5:0	R/W	HOLDEX-IT_BW0_PLLD	DSPLL D Fastlock Bandwidth parameters.
0x079E	5:0	R/W	HOLDEX-IT_BW1_PLLD	
0x079F	5:0	R/W	HOLDEX-IT_BW2_PLLD	
0x07A0	5:0	R/W	HOLDEX-IT_BW3_PLLD	
0x07A1	5:0	R/W	HOLDEX-IT_BW4_PLLD	
0x07A2	5:0	R/W	HOLDEX-IT_BW5_PLLD	

This group of registers determines the DSPLL D bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that the individual SOFT_RST_PLLD (0x001C[4]) does not update these bandwidth parameters.

Table 15.281. 0x07A4-0x07A5

Reg Address	Bit Field	Type	Setting Name	Description
0x07A4	7:0	R/W	HSW_LIMIT_PLLD	Set by CBPro.
0x07A5	0	R/W	HSW_LIMIT_AC-TION_PLLD	Set by CBPro.

Table 15.282. 0x07A6

Reg Address	Bit Field	Type	Setting Name	Description
0x07A6	2:0	R/W	RAMP_STEP_SIZE_PLLD	Set by CBPro.
0x07A6	3	R/W	RAMP_SWITCH_EN_PLLD	

Table 15.283. 0x07AC-0x07B2

Reg Address	Bit Field	Type	Setting Name	Description
0x07AC	0	R/W	OUT_MAX_LIMIT_EN_PLLD	Set by CBPro.
0x07AC	3	R/W	HOLD_SETTLE_DET_EN_PLLD	Set by CBPro.
0x07AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLD	Set by CBPro.
0x07B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLD	Set by CBPro.

15.9 Page 9 Registers Si5397A/B

Table 15.284. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Table 15.285. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit selects between 1.8 V and 3.3 V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3 V-tolerant. Setting this to the default 1.8 V is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I2C or SPI host is operating at 3.3 V and the Si5397/96 at VDD=1.8 V, the host must write IO_VDD_SEL=1. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 15.286. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See for more information.

When a clock is disabled, it is powered down.

Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 15.287. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 15.288. 0x094E-0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	
0x094F	7:4	R/W	IN_CMOS_USE1P8	

Table 15.289. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTEGER	0: Integer MXAXB 1: Fractional MXAXB

15.10 Page A Registers Si5397A/B

Table 15.290. 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 15.291. 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	4:0	R/W	N_PIBYP	Bypass fractional divider for N[3:0]. 0: Fractional (or Integer) division - Recommended if changing settings during operation 1: Integer-only division - best phase noise - Recommended for Integer N values Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 15.292. 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

15.11 Page B Registers Si5397A/B

Table 15.293. 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 15.294. 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 15.295. 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Reg Address	Bit Field	Type	Name	Description
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 15.296. 0x0B45 LOL Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	1: Clock disabled.
0x0B45	1	R/W	CLK_DIS_PLLB	1: Clock disabled.
0x0B45	2	R/W	CLK_DIS_PLLC	1: Clock disabled.
0x0B45	3	R/W	CLK_DIS_PLLD	1: Clock disabled.

Table 15.297. 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (IN3 IN2 IN1 IN0). Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 15.298. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set by CBPro.

Table 15.299. 0x0B48

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set by CBPro.

Table 15.300. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (D C B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 15.301. 0x0B4E Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B4E	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 15.302. 0x0B57 VCO_RESET_CALCODE

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CAL-CODE	
0x0B58	11:8	R/W	VCO_RESET_CAL-CODE	

15.12 Page C Registers Si5397A/B

Table 15.303. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 15.304. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 15.305. 0x0C05

Reg Address	Bit Field	Type	Name	Description
0x0C05	0	R/W	IN_CLK_VAL_EN_PLLA	Set by CBPro

Table 15.306. 0x0C06

Reg Address	Bit Field	Type	Name	Description
0x0C06	7:0	R/W	IN_CLK_VAL_TIME_PLLA	Set by CBPro

Table 15.307. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN_PLLB	Set by CBPro

Table 15.308. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME_PLLB	Set by CBPro

Table 15.309. 0x0C09

Reg Address	Bit Field	Type	Name	Description
0x0C09	0	R/W	IN_CLK_VAL_EN_PLLC	Set by CBPro

Table 15.310. 0x0C0A

Reg Address	Bit Field	Type	Name	Description
0x0C0A	7:0	R/W	IN_CLK_VAL_TIME_PLLC	Set by CBPro

Table 15.311. 0x0C0B

Reg Address	Bit Field	Type	Name	Description
0x0C0B	0	R/W	IN_CLK_VAL_EN_PLLD	Set by CBPro

Table 15.312. 0x0C0C

Reg Address	Bit Field	Type	Name	Description
0x0C0C	7:0	R/W	IN_CLK_VAL_TIME_PLLD	Set by CBPro

16. Si5397C/D Register Map

16.1 Page 0 Registers Si5397C/D

Table 16.1. 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 16.2. 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 16.3. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x97	Four-digit “base” part number, one nibble per digit Example: Si5397A-A-GM. The base part number (OPN) is 5397, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Table 16.4. 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode. 0 = A 1 = B 2 = C 3 = D 9=J, 10=K,11=L,12=M

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 16.5. 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5397C-A12345-GM, the device revision is “A” and stored as 0

Table 16.6. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

Table 16.7. 0x0009–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5397C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5397C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5397 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 16.8. 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address. Note: This register is not bank burnable.

Table 16.9. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if there is no signal detected on the XAXB input signal.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Table 16.10. 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [3 2 1 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [3 2 1 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 16.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Table 16.12. 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4

DSPLL_B corresponds to bit 5

DSPLL_C corresponds to bit 6

DSPLL_D corresponds to bit 7

Table 16.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R/W	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to clear the flag.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Table 16.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]
- Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Table 16.15. 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Table 16.16. 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Table 16.17. 0x0016

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	3:0	R/W	LOL_ON_HOLD_PLL[D:A]	

Table 16.18. 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOS-XAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOS-REF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	XAXB_ERR_INTR_MSK	
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt
0x0017	6	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this register is 0x035.

Table 16.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1: To mask the clock input OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]
- Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 16.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]
- DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019 [2], HOLD_INTR_MSK_PLL 0x0019 [6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019 [3], HOLD_INTR_MSK_PLL 0x0019 [7]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 16.21. 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Table 16.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: Initialize and calibrate the entire device.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB
0x001C	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715.

Table 16.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

Table 16.24. 0x001E Sync, Power Down, and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1: To put the device into low power mode
0x001E	1	R/W	HARD_RST	Perform hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	1 to reset all the R dividers to the same state.

Table 16.25. 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	FSTEP_PLL_SINGLE	0: DSPLL_SEL[1:0] pins and bits are disabled. 1: DSPLL_SEL[1:0] pins or FSTEP_PLL bits are enabled. See FSTEP_PLL_REGCTRL
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only functions when FSTEP_PLL_SINGLE = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	3:2	R/W	FSTEP_PLL	Register version of the DSPLL_SEL[1:0] pins. Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: DSPLL B M-divider 2: DSPLL C M-divider 3: DSPLL D M-divider

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Table 16.26. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI.

Table 16.27. 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Input 3 (IN3): LOS_EN[3]

Table 16.28. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 16.29. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 16.30. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 16.31. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 16.32. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 16.33. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 16.34. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 16.35. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 16.36. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 16.37. 0x003E

Reg Address	Bit Field	Type	Setting Name	Description
0x003E	7:4	R/W	LOS_MIN_PERIOD_EN	Set by CBPro.

Table 16.38. 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable
0x003F	7:4	R/W	FAST_OOF_EN	1: To enable

Table 16.39. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 16.40. 0x0041-0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 16.41. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 16.42. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear Threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 16.43. 0x004E-0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DET-WIN_SEL	Values calculated by CBPro.
0x004E	6:4	R/W	OOF1_DET-WIN_SEL	
0x004F	2:0	R/W	OOF2_DET-WIN_SEL	
0x004F	6:4	R/W	OOF3_DET-WIN_SEL	

Table 16.44. 0x0050

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro.

Table 16.45. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 16.46. 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 16.47. 0x0059 Fast OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	1:0	R/W	FAST_OOF0_DET-WIN_SEL	Values calculated by CBPro.
0x0059	3:2	R/W	FAST_OOF1_DET-WIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DET-WIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DET-WIN_SEL	

Table 16.48. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 16.49. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 16.50. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 16.51. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 16.52. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Enables fast detection of LOL for PLLx. A large input frequency error will quickly assert LOL when this is enabled.
0x0092	1	R/W	LOL_FST_EN_PLLB	
0x0092	2	R/W	LOL_FST_EN_PLLC	
0x0092	3	R/W	LOL_FST_EN_PLLD	

Table 16.53. 0x0093-0x0094 Fast LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DETWIN_SEL_PLLA	Values calculated by CBPro
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL_PLLB	
0x0094	3:0	R/W	LOL_FST_DETWIN_SEL_PLLC	
0x0094	7:4	R/W	LOL_FST_DETWIN_SEL_PLLD	

Table 16.54. 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x0095	1:0	R/W	LOL_FST_VALWIN_SEL_PLLA	Values calculated by CBPro
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL_PLLB	
0x0095	5:4	R/W	LOL_FST_VALWIN_SEL_PLLC	
0x0095	7:6	R/W	LOL_FST_VALWIN_SEL_PLLD	

Table 16.55. 0x0096-0x0097 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	
0x0097	3:0	R/W	LOL_FST_SET_THR_SEL_PLLC	
0x0097	7:4	R/W	LOL_FST_SET_THR_SEL_PLLD	

Table 16.56. 0x0098-0x0099 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	
0x0099	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLC	
0x0099	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLD	

Table 16.57. 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	0	R/W	LOL_SLOW_EN_PLLA	0: To disable LOL. 1: To enable LOL.
0x009A	1		LOL_SLOW_EN_PLLB	0: To disable LOL. 1: To enable LOL.
0x009A	2		LOL_SLOW_EN_PLLC	0: To disable LOL. 1: To enable LOL.
0x009A	3		LOL_SLOW_EN_PLLD	0: To disable LOL. 1: To enable LOL.

Table 16.58. 0x009B-0x009C Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Values calculated by CBPro
0x009B	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLB	
0x009C	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLC	
0x009C	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLD	

Table 16.59. 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Values calculated by CBPro
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	
0x009D	5:4	R/W	LOL_SLW_VAL-WIN_SEL_PLLC	
0x009D	7:6	R/W	LOL_SLW_VAL-WIN_SEL_PLLD	

Table 16.60. 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. See list below for selectable values.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. See list below for selectable values.

Table 16.61. 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. See list below for selectable values.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	Configures the loss of lock set thresholds. See list below for selectable values.

The following are the LOL_SLW_SET_THR_PLLx thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm
- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 16.62. 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. See list below for selectable values.

Table 16.63. 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	Configures the loss of lock clear thresholds. See list below for selectable values.

The following are the LOL_SLW_CLR_THR_PLLx thresholds for the value that is placed in the four bits of the DSPLLs. ClockBuilder Pro sets these values.

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm
- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 16.64. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	0 1 2 3	R/W	LOL_TIMER_EN_PLLA LOL_TIMER_EN_PLLB LOL_TIMER_EN_PLLC LOL_TIMER_EN_PLLD	Enable Delay for LOL Clear. 0: Disable Delay for LOL Clear 1: Enable Delay for LOL Clear

Table 16.65. 0x00A4-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00A5	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLA	

Table 16.66. 0x00A9-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AA	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	

Table 16.67. 0x00AE-0x00B1 LOL Clear Delay DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x00AE	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AF	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	
0x00B0	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	
0x00B1	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLC	

Table 16.68. 0x00B3-0x00B6 LOL Clear Delay DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x00B3	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00B4	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	
0x00B5	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	
0x00B6	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLD	

Table 16.69. 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	7:0	R	AC-TIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See for a detailed description of how to program the NVM.

Table 16.70. 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

Table 16.71. 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	When set, this bit will read the NVM down into the volatile memory.

Table 16.72. 0x00E5

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	
0x00E5	6	R/W	FASTLOCK_EXTEND_EN_PLLC	
0x00E5	7	R/W	FASTLOCK_EXTEND_EN_PLLD	

Table 16.73. 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 16.74. 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x00EA	7:0	R/W	FASTLOCK_EXTEND_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FASTLOCK_EXTEND_PLLB	
0x00EC	23:16	R/W	FASTLOCK_EXTEND_PLLB	
0x00ED	28:24	R/W	FASTLOCK_EXTEND_PLLB	

Table 16.75. 0x00EE-0x00F1 FASTLOCK_EXTEND_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x00EE	7:0	R/W	FASTLOCK_EXTEND_PLLC	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EF	15:8	R/W	FASTLOCK_EXTEND_PLLC	
0x00F0	23:16	R/W	FASTLOCK_EXTEND_PLLC	
0x00F1	28:24	R/W	FASTLOCK_EXTEND_PLLC	

Table 16.76. 0x00F2-0x00F5 FASTLOCK_EXTEND_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x00F2	7:0	R/W	FASTLOCK_EXTEND_PLLD	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00F3	15:8	R/W	FASTLOCK_EXTEND_PLLD	
0x00F4	23:16	R/W	FASTLOCK_EXTEND_PLLD	
0x00F5	28:24	R/W	FASTLOCK_EXTEND_PLLD	

Table 16.77. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 16.78. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 16.79. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 16.80. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	0:3	R	LOL_INTR_PLL[D:A]	Set by CBPro.
0x00F9	7:4	R	HOLD_INTR_PLL[D:A]	Set by CBPro.

Table 16.81. 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page so that a page write is not ever required to read the DEVICE_READY status.

WARNING: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note this includes writes to the PAGE register.

16.2 Page 1 Registers Si5397C/D

Table 16.82. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISA-BLE_LOW	0: Disables all output drivers 1: Pass through the output enables.

Table 16.83. 0x0108, 0x011C, 0x0126, 0x012B Clock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0108 0x011C 0x0126 0x012B	0	R/W	OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pull-down effect.
0x0108 0x011C 0x0126 0x012B	1	R/W	OUT0_OE OUT1_OE OUT2_OE OUT3_OE	0: To disable the output 1: To enable the output
0x0108 0x011C 0x0126 0x012B	2	R/W	OUT0_RDIV_-FORCE2 OUT1_RDIV_-FORCE2 OUT2_RDIV_-FORCE2 OUT3_RDIV_-FORCE2	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2

The output drivers are all identical. See .

Table 16.84. 0x0109, 0x011D, 0x0127, 0x012C Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0109 0x011D 0x0127 0x012C	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5: LVCMOS (+pin only) 6: LVCMOS (-pin only) 7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0109 0x011D 0x0127 0x012C	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN	0: Disable 1: Enable
0x0109 0x011D 0x0127 0x012C	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high 2-3: Reserved
0x0109 0x011D 0x0127 0x012C	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV	LVCMOS output impedance drive strength see .

The output drivers are all identical.

Table 16.85. 0x010A, 0x011E, 0x0128, 0x012D Output Amplitude and Common Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x010A 0x011E 0x0128 0x012D	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .
0x010A 0x011E 0x0128 0x012D	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Table 16.86. 0x010B, 0x011F, 0x0129, 0x012E Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x010B 0x011F 0x0129 0x012E	2:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL	Output driver input mux select.This selects the source of the output clock. 0: DSPLL A 1: DSPLL B 2: DSPLL C 3: DSPLL D 5-7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x010B 0x011F 0x0129 0x012E	3	R/W	OUT0_VDD_SEL_EN OUT1_VDD_SEL_EN OUT2_VDD_SEL_EN OUT3_VDD_SEL_EN	1: Enable OUTx_VDD_SEL
0x010B 0x011F 0x0129 0x012E	5:4	R/W	OUT0_VDD_SEL OUT1_VDD_SEL OUT2_VDD_SEL OUT3_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x010B 0x011F 0x0129 0x012E	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV	LVCMOS output inversion. Only applies when OUT0A_FORMAT = 4. See for more information.

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical. The OUTx_MUX_SEL settings should match the corresponding OUTx_DIS_SRC selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 16.87. 0x010C, 0x0116, 0x011B, 0x0120, 0x012A, 0x012F, 0x0134, 0x0139 Output Disable Source DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x010C 0x0120 0x012A 0x012F	2:0	R/W	OUT0_DIS_SRC OUT1_DIS_SRC OUT2_DIS_SRC OUT3_DIS_SRC	Output driver 0 input mux select. This selects the source of the output clock. 0: DSPLL A squelches output 1: DSPLL B squelches output 2: DSPLL C squelches output 3: DSPLL D squelches output 5-7: Reserved

These CLKx_DIS_SRC settings should match the corresponding OUTx_MUX_SEL selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 16.88. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	0	R/W	OUT_DIS_MSK_PLLA	Set by CBPro.
0x0141	1	R/W	OUT_DIS_MSK_PLLB	
0x0141	2	R/W	OUT_DIS_MSK_PLLC	
0x0141	3	R/W	OUT_DIS_MSK_PLLD	
0x0141	5	R/W	OUT_DIS_LOL_MSK	

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	6	R/W	OUT_DIS_LOS-XAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	Set by CBPro.

Table 16.89. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MSK_LOL_PLL[D:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	7:4	R/W	OUT_DIS_MSK_HOLD_PLL[D:A]	Set by CBPro.

Bit 0 LOL_DSPLL_A mask

Bit 1 LOL_DSPLL_B mask

Bit 2 LOL_DSPLL_C mask

Bit 3 LOL_DSPLL_D mask

16.3 Page 2 Registers Si5397C/D

Table 16.90. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This valid with external clock sources, not crystals.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 3 = pre-scale value 8

Note that changing this register furing operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.91. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.92. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.93. Si5397C/D P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211

Register Address	Description	Size	Same as Address
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.94. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in . Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values.

Table 16.95. 0x0231 P0 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.96. 0x0232 P1 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.97. 0x0233 P2 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.98. 0x0234 P3 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.99. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.100. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 16.101. 0x023F

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	R/W	MXAXB_UPDATE	The divider value for the XAXB input

Table 16.102. 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x024A	7:0	R/W	R0_REG	24-bit Integer output divider divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 16.103. Si5397C/D R1–R3 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0256-0x0258	R1_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R2_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R3_REG	24-bit Integer Number	0x024A-0x024C

Table 16.104. 0x026B–0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 16.105. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5397C-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5397C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5397C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5397 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 16.106. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 16.107. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 16.108. 0x028A-0x028D

Reg Address	Bit Field	Type	Setting Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	The OOF0 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	The OOF1 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	The OOF2 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	The OOF3 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 16.109. 0x028E-0x0291

Reg Address	Bit Field	Type	Setting Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	The OOF0 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	The OOF1 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	The OOF2 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	The OOF3 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 16.110. 0x0292-0x0293

Reg Address	Bit Field	Type	Setting Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro.
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro.

Table 16.111. 0x0294-0x0295 FASTLOCK EXTEND SCL PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro.
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	
0x0295	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLC	
0x0295	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLD	

Table 16.112. 0x0296 LOL SLW VALWIN SELX PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	
0x0296	2	R/W	LOL_SLW_VALWIN_SELX_PLLC	
0x0296	3	R/W	LOL_SLW_VALWIN_SELX_PLLD	

Table 16.113. 0x0297 FASTLOCK_DLY_ONSW_EN_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0297	0	R/W	FAST-LOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FAST-LOCK_DLY_ONSW_EN_PLLB	
0x0297	2	R/W	FAST-LOCK_DLY_ONSW_EN_PLLC	
0x0297	3	R/W	FAST-LOCK_DLY_ONSW_EN_PLLD	

Table 16.114. 0x0299 FASTLOCK_DLY_ONLOL_EN_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0299	0	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLB	
0x0299	2	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLC	
0x0299	3	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLD	

Table 16.115. 0x029A-0x29C FASTLOCK_DLY_ONLOL_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x029A	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	
0x029C	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	

Table 16.116. 0x029D-0x29F FASTLOCK_DLY_ONLOL_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x029D	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	

Table 16.117. 0x02A0-0x2A2 FASTLOCK_DLY_ONLOL_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x02A0	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	Set by CBPro.
0x02A1	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	
0x02A2	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLC	

Table 16.118. 0x02A3-0x02A5 FASTLOCK_DLY_ONLOL_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x02A3	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	Set by CBPro.
0x02A4	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	
0x02A5	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLD	

Table 16.119. 0x02A6-0x02A8 FASTLOCK DLY ONSW PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	20-bit value. Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 16.120. 0x02A9-0x02AB FASTLOCK DLY ONSW PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 16.121. 0x02AC-0x02AE FASTLOCK_DLY_ONSW_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x02AC	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLC	20-bit value. Set by CBPro.
0x02AD	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLC	
0x02AE	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLC	

Table 16.122. 0x02AF-0x02B1 FASTLOCK_DLY_ONSW_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x02AF	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLD	20-bit value. Set by CBPro.
0x02B0	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLD	
0x02B1	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLD	

Table 16.123. 0x02B7 LOL_NOSIG_TIME_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	
0x02B7	5:4	R/W	LOL_NO-SIG_TIME_PLLC	
0x02B7	7:6	R/W	LOL_NO-SIG_TIME_PLLD	

Table 16.124. 0x02B8 LOL LOS REFCLK PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8	0	R/W	LOL_LOS_REFCLK_PLLA	Set by CBPro.
0x02B8	1	R/W	LOL_LOS_REFCLK_PLLB	Set by CBPro.
0x02B8	2	R/W	LOL_LOS_REFCLK_PLLC	Set by CBPro.
0x02B8	3	R/W	LOL_LOS_REFCLK_PLLD	Set by CBPro.

Table 16.125. 0x02B9 LOL NOSIG TIME PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	0	R/W	LOL_LOS_REFCLK_PLLA_FLG	Set by CBPro.
0x02B9	1	R/W	LOL_LOS_REFCLK_PLLB_FLG	Set by CBPro.
0x02B9	2	R/W	LOL_LOS_REFCLK_PLLC_FLG	Set by CBPro.
0x02B9	3	R/W	LOL_LOS_REFCLK_PLLD_FLG	Set by CBPro.

Table 16.126. 0x02BC

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

16.4 Page 3 Registers Si5397C/D

Table 16.127. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 16.128. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer.
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.129. 0x030C N0 Update

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. A Soft Reset will have the same effect.

Table 16.130. N0_NUM and N0_DEN Definitions

Reg Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 16.131. 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

16.5 Page 4 Registers Si5397C/D

Table 16.132. 0x0407 DSPLL A Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 16.133. 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Parameters that create the normal PLL bandwidth
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 16.134. 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST-LOCK_BW0_PLLA	Parameters that create the fast lock PLL bandwidth
0x040F	5:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	5:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	5:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	5:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	5:0	R/W	FAST-LOCK_BW5_PLLA	
0x0414	0	S	BW_UP-DATE_PLLA	0: No effect 1: Update both the Normal and Fastlock BWs for PLL A.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the

BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 16.135. 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56-bit number.
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.136. 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.137. 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 16.138. 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 16.139. 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0422	1	R/W	M_FSTEP_DEN_PLLA	Set by CBPro.

Table 16.140. 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Table 16.141. 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register-based clock selection.

Table 16.142. 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 16.143. 0x042C Holdover Exit Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042C	0	R/W	HOLD_EN_PLLA	Holdover Enable 0: Holdover Disabled 1: Holdover Enabled
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Set by CBPro.
0x042C	4	R/W	HOLDEXIT_BW_SEL1_PLLA	Holdover Exit Bandwidth select. Selects the exit bandwidth from Holdover when ramped exit is disabled (HOLD_RAMP_BYP_PLLA = 1). 0: Exit Holdover using Holdover Exit or Fastlock bandwidths (default). See HOLDEXIT_BW_SEL0_PLLA (0x049B[6]) for additional information. 1: Exit Holdover using the Normal loop bandwidth
0x042C	5:7	R/W	RAMP_STEP_INTERVAL_PLLA	Time Interval of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.

Table 16.144. 0x042D

Reg Address	Bit Field	Type	Setting Name	Description
0x042D	1	R/W	HOLD_RAMP_BYP_NOHIST_PLLA	Set by CBPro.

Table 16.145. 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 16.146. 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the window length from the register value. time = (2^{DELAY})*268nsec

Table 16.147. 0x0431

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	5- bit value

Table 16.148. 0x0432

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Value calculated by CBPro
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 16.149. 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Table 16.150. 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 16.151. 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Table 16.152. 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.153. 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.154. 0x043A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0,2,3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 1,2,3: Reserved

Table 16.155. 0x043B-0x043C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Set by CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 16.156. 0x043D

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Set by CBPro

Table 16.157. 0x043E

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Set by CBPro

Table 16.158. 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 16.159. 0x0442-0x0444

Reg Address	Bit Field	Type	Setting Name	Description
0x0442	7:0	R/W	FINE_ADJ_OVR_PLLA	Set by CBPro
0x0443	15:8	R/W	FINE_ADJ_OVR_PLLA	
0x0444	17:16	R/W	FINE_ADJ_OVR_PLLA	

Table 16.160. 0x0445

Reg Address	Bit Field	Type	Setting Name	Description
0x0445	1	R/W	FORCE_FINE_ADJ_PLLA	Set by CBPro

Table 16.161. 0x0488 HSW_FINE_PM_LEN_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Set by CBPro.

Table 16.162. 0x0489 PFD_EN_DELAY_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	7:0	R/W	PFD_EN_DELAY_PLLA	Set by CBPro.
0x048A	12:8	R/W	PFD_EN_DELAY_PLLA	

Table 16.163. 0x048B

Reg Address	Bit Field	Type	Setting Name	Description
0x048B	19:0	R/W	HSW_MEAS_SETTLE_PLLA	Set by CBPro.

Table 16.164. 0x049B HOLDEXIT_BW_SEL0_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	Set by CBPro.
0x049B	2	R/W	HO_SKIP_PHASE_PLLA	Set by CBPro.
0x049B	4	R/W	HOLD_PRESERVE_HIST_PLLA	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLA	Set by CBPro.
0x049B	6	R/W	HOLDEX-IT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEX-IT_STD_BO_PLLA	Set by CBPro.

Table 16.165. 0x049C

Reg Address	Bit Field	Type	Setting Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NOHIST_PLLA	Set by CBPro.

Table 16.166. 0x049D-0x04A2 DSPLL Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	7:0	R/W	BW0_HO_PLLA	DSPLL A Holdover Bandwidth parameters.
0x049E	7:0	R/W	BW1_HO_PLLA	
0x049F	7:0	R/W	BW2_HO_PLLA	
0x04A0	7:0	R/W	BW3_HO_PLLA	
0x04A1	7:0	R/W	BW4_HO_PLLA	
0x04A2	7:0	R/W	BW5_HO_PLLA	

This group of registers determines the DSPLL A bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that the individual SOFT_RST_PLLA (0x001C[1]) does not update these bandwidth parameters.

Table 16.167. 0x04A4-0x04A5

Reg Address	Bit Field	Type	Setting Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Set by CBPro.
0x04A5	0	R/W	HSW_LIMIT_ACTION_PLLA	Set by CBPro.

Table 16.168. 0x04A6

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	Set by CBPro.
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	Set by CBPro.

Table 16.169. 0x04AC-0x04B2

Reg Address	Bit Field	Type	Setting Name	Description
0x04AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLA	Set by CBPro.
0x04AD	15:0	R/W	OUT_MAX_LIM-IT_LMT_PLLA	Set by CBPro.
0x04B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLA	Set by CBPro.

16.6 Page 5 Registers Si5397C/D

Table 16.170. 0x0507 DSPLL B Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 16.171. 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Parameters that create the normal PLL bandwidth
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 16.172. 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLLB	Parameters that create the fast lock PLL bandwidth
0x050F	5:0	R/W	FAST-LOCK_BW1_PLLB	
0x0510	5:0	R/W	FAST-LOCK_BW2_PLLB	
0x0511	5:0	R/W	FAST-LOCK_BW3_PLLB	
0x0512	5:0	R/W	FAST-LOCK_BW4_PLLB	
0x0513	5:0	R/W	FAST-LOCK_BW5_PLLB	
0x0514	0	S	BW_UP-DATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

This group of registers determines the DSPLL Fastlock bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of

the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 16.173. 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.174. 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.175. 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 16.176. 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.

Table 16.177. 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0522	1	R/W	M_FSTEPW_DEN_PLLB	0: Modify numerator 1: Modify denominator

Table 16.178. 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEPW_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEPW_PLLB	
0x0525	23:16	R/W	M_FSTEPW_PLLB	
0x0526	31:24	R/W	M_FSTEPW_PLLB	
0x0527	39:32	R/W	M_FSTEPW_PLLB	
0x0528	47:40	R/W	M_FSTEPW_PLLB	
0x0529	55:48	R/W	M_FSTEPW_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0515–0x051F.

Table 16.179. 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	0: Pin Control 1: Register Control
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 16.180. 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FASTLOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	1	R/W	FAST-LOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Table 16.181. 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	0: Holdover Disabled 1: Holdover Enabled
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EX-IT_BW_SEL1_PLLB	0: To use the fastlock loop BW when exiting from hold-over 1: To use the normal loop BW when exiting from hold-over
0x052C	7:5	R/W	RAMP_STEP_IN-TERVAL_PLLB	

Table 16.182. 0x052D

Reg Address	Bit Field	Type	Setting Name	Description
0x052D	1	R/W	HOLD_RAMP-BYP_NOH-IST_PLLB	Set by CBPro.

Table 16.183. 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 16.184. 0x052F DSPLLB Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R/W	HOLD_HIST_DE-LAY_PLLB	5-bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 16.185. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUN T_FRC_PLLB	5- bit value

Table 16.186. 0x0532

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Set by CBPro.
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 16.187. 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Table 16.188. 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 16.189. 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]

IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]

IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]

IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Table 16.190. 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.191. 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.192. 0x053A DSPLL B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1:Default setting, do not modify 0,2,3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1,2,3: Reserved

Table 16.193. 0x053B-0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 16.194. 0x053D

Reg Address	Bit Field	Type	Setting Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Set by CBPro.

Table 16.195. 0x053E

Reg Address	Bit Field	Type	Setting Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Set by CBPro.

Table 16.196. 0x053F DSPLL B Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 16.197. 0x0542-0x0544 FINE_ADJ_OVR_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0542	7:0	R/W	FINE_ADJ_OVR_PLLB	Set by CBPro.
0x0543	15:8	R/W	FINE_ADJ_OVR_PLLB	
0x0544	17:16	R/W	FINE_ADJ_OVR_PLLB	

Table 16.198. 0x0545 FORCE_FINE_ADJ_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0545	1	R/W	FORCE_FINE_ADJ_PLLB	Set by CBPro.

Table 16.199. 0x0588 HSW_FINE_PM_LEN_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	

Table 16.200. 0x0589 PFD_EN_DELAY_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	Set by CBPro.
0x0589	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 16.201. 0x058B

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	19:0	R/W	HSW_MEAS_SETTLE_PLLB	Set by CBPro.

Table 16.202. 0x059B HOLDEXIT_BW_SEL0_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	IN-IT_LP_CLOSE_HO_PLLB	Set by CBPro.
0x059B	2	R/W	HO_SKIP_PHASE_PLLB	
0x059B	4	R/W	HOLD_PRE-SERVE_HIST_PLLB	
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	
0x059B	6	R/W	HOLDEX-IT_BW_SEL0_PLLB	
0x059B	7	R/W	HOLDEX-IT_STD_BO_PLLB	

Table 16.203. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NOHIST_PLLB	Set by CBPro.

Table 16.204. 0x059D-0x05A2 DSPLL Holdover Exit Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEX-IT_BW0_PLLB	DSPLL B Fastlock Bandwidth parameters.
0x059E	5:0	R/W	HOLDEX-IT_BW1_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1.
0x059F	5:0	R/W	HOLDEX-IT_BW2_PLLB	
0x05A0	5:0	R/W	HOLDEX-IT_BW3_PLLB	
0x05A1	5:0	R/W	HOLDEX-IT_BW4_PLLB	
0x05A2	5:0	R/W	HOLDEX-IT_BW5_PLLB	

This group of registers determines the DSPLL B bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that the individual SOFT_RST_PLLB (0x001C[2]) does not update these bandwidth parameters.

Table 16.205. 0x05A4-0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Set by CBPro.
0x05A5	0	R/W	HSW_LIMIT_ACTION_PLLB	Set by CBPro.

Table 16.206. 0x05A6

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE_PLLB	
0x05A6	3		RAMP_SWITCH_EN_PLLB	

Table 16.207. 0x05AC-0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SETTLE_DET_EN_PLLB	Set by CBPro.
0x05AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLB	Set by CBPro.
0x05B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLB	Set by CBPro.

16.7 Page 6 Registers Si5397C/D

Table 16.208. 0x0607 DSPLL C Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 16.209. 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	5:0	R/W	BW0_PLLC	Parameters that create the normal PLL bandwidth
0x0609	5:0	R/W	BW1_PLLC	
0x060A	5:0	R/W	BW2_PLLC	
0x060B	5:0	R/W	BW3_PLLC	
0x060C	5:0	R/W	BW4_PLLC	
0x060D	5:0	R/W	BW5_PLLC	

This group of registers determines the DSPLL C loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 16.210. 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	5:0	R/W	FAST-LOCK_BW0_PLLC	Parameters that create the fast lock PLL bandwidth
0x060F	5:0	R/W	FAST-LOCK_BW1_PLLC	
0x0610	5:0	R/W	FAST-LOCK_BW2_PLLC	
0x0611	5:0	R/W	FAST-LOCK_BW3_PLLC	
0x0612	5:0	R/W	FAST-LOCK_BW4_PLLC	
0x0613	5:0	R/W	FAST-LOCK_BW5_PLLC	
0x0614	0	S	BW_UP-DATE_PLLC	0: No effect. 1: Update both the Normal and Fastback BWs for PLL C.

This group of registers determines the DSPLL Fastlock bandwidth. In Clock Builder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 16.211. 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	56-bit number
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.212. 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	32-bit number
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.213. 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UPDATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 16.214. 0x0621 DSPLL C M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	3:0	R/W	M_FRAC_MODE_PLLC	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0621	4	R/W	M_FRAC_EN_PLLC	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0621	5	R/W	Reserved	Must be set to 1 for DSPLL C

Table 16.215. 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0622	1	R/W	M_FSTEPW_DEN_PLLC	0: Modify numerator 1: Modify denominator

Table 16.216. 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	56-bit number
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F.

Table 16.217. 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 16.218. 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLC is out of lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Table 16.219. 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062C	0	R/W	HOLD_EN_PLLC	0: Holdover disabled 1: Holdover enabled
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	Must be set to 1 for normal operation.
0x062C	4	R/W	HOLDEXIT_BW_SEL1_PLLC	0: Use Fastlock bandwidth for Holdover Entry/Exit (default) 1: Use the normal loop BW when exiting from holdover
0x062C	7:5	R/W	RAMP_STEP_INTERVAL_PLLC	Set by CBPro.

Table 16.220. 0x062D

Reg Address	Bit Field	Type	Setting Name	Description
0x062D	1	R/W	HOLD_RAMPBYP_NOHIST_PLLC	Set by CBPro.

Table 16.221. 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 16.222. 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 16.223. 0x0631

Reg Address	Bit Field	Type	Setting Name	Description
0x0631	4:0	R/W	HOLD_REF_COUNT_FRC_PLLC	Set by CBPro.

Table 16.224. 0x0632-0x0634

Reg Address	Bit Field	Type	Setting Name	Description
0x0632	7:0	R/W	HOLD_15M_CYC_COUNT_PLLC	Set by CBPro.
0x0633	15:8	R/W	HOLD_15M_CYC_COUNT_PLLC	
0x0634	23:16	R/W	HOLD_15M_CYC_COUNT_PLLC	

Table 16.225. 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Table 16.226. 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 16.227. 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN2 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

IN3 Input 3 applies to LOS alarm 0x0637[3], OOF alarm 0x0637[7]

Table 16.228. 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.229. 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0639	6:4	R/W	IN3_PRIORITY_PLLC	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.230. 0x063A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x063A	1:0	R/W	HSW_MODE_PLLC	1:Default setting, do not modify 0,2,3: Reserved
0x063A	3:2	R/W	HSW_PHMEAS_CTRL_PLLC	0: Default setting, do not modify 1,2,3: Reserved

Table 16.231. 0x063B-0x063C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x063B	7:0	R/W	HSW_PHMEAS_THR_PLLC	10-bit value. Set by CBPro.
0x063C	9:8	R/W	HSW_PHMEAS_THR_PLLC	

Table 16.232. 0x063D

Reg Address	Bit Field	Type	Setting Name	Description
0x063D	4:0	R/W	HSW_COARSE_PM_LEN_PLLC	Set by CBPro.

Table 16.233. 0x063E

Reg Address	Bit Field	Type	Setting Name	Description
0x063E	4:0	R/W	HSW_COARSE_PM_DLY_PLLC	Set by CBPro.

Table 16.234. 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x063F	2	R	FASTLOCK_STATUS_PLLC	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLC accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 16.235. 0x0642-0x0644

Reg Address	Bit Field	Type	Setting Name	Description
0x0642	7:0	R/W	FINE_ADJ_OVR_PLLC	Set by CBPro.
0x0643	15:8	R/W	FINE_ADJ_OVR_PLLC	
0x0644	17:16	R/W	FINE_ADJ_OVR_PLLC	

Table 16.236. 0x0645

Reg Address	Bit Field	Type	Setting Name	Description
0x0645	1	R/W	FORCE_FINE_ADJ_PLLC	Set by CBPro.

Table 16.237. 0x0688 HSW_FINE_PM_LEN_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0688	3:0	R/W	HSW_FINE_PM_LEN_PLLC	

Table 16.238. 0x0689 PFD_EN_DELAY_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0689	7:0	R/W	PFD_EN_DELAY_PLLC	
0x068A	12:8	R/W	PFD_EN_DELAY_PLLC	

Table 16.239. 0x068B

Reg Address	Bit Field	Type	Setting Name	Description
0x068B	19:0	R/W	HSW_MEAS_SETTLE_PLLC	Set by CBPro.

Table 16.240. 0x069B HOLDEXIT_BW_SEL0_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	1	R/W	INIT_LP_CLOSE_HO_PLLC	
0x069B	2	R/W	HO_SKIP_PHASE_PLLC	Set by CBPro.
0x069B	4	R/W	HOLD_PRESERVE_HIST_PLLC	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLC	Set by CBPro.
0x069B	6	R/W	HOLDEX-IT_BW_SEL0_PLL	Set by CBPro.
0x069B	7	R/W	HOLDEX-IT_STD_BO_PLLC	Set by CBPro.

Table 16.241. 0x069C

Reg Address	Bit Field	Type	Setting Name	Description
0x069C	6	R/W	HOLDEX-IT_ST_BO_PLLC	Set by CBPro.
0x069C	7	R/W	HOLD_RAMPBP_NOHIST_PLLC	Set by CBPro.

Table 16.242. 0x069D-0x06A2 DSPLL Holdover Exit Bandwidth for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x069D	5:0	R/W	HOLDEX-IT_BW0_PLLC	DSPLL C Fastlock Bandwidth parameters.
0x069E	5:0	R/W	HOLDEX-IT_BW1_PLLC	
0x069F	5:0	R/W	HOLDEX-IT_BW2_PLLC	
0x06A0	5:0	R/W	HOLDEX-IT_BW3_PLLC	
0x06A1	5:0	R/W	HOLDEX-IT_BW4_PLLC	
0x06A2	5:0	R/W	HOLDEX-IT_BW5_PLLC	

This group of registers determines the DSPLL C bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that the individual SOFT_RST_PLLC (0x001C[3]) does not update these bandwidth parameters.

Table 16.243. 0x06A4-0x06A5

Reg Address	Bit Field	Type	Setting Name	Description
0x06A4	7:0	R/W	HSW_LIMIT_PLLC	Set by CBPro.
0x06A5	0	R/W	HSW_LIMIT_ACTION_PLLC	Set by CBPro.

Table 16.244. 0x06A6

Reg Address	Bit Field	Type	Setting Name	Description
0x06A6	2:0	R/W	RAMP_STEP_SIZE_PLLC	Set by CBPro.
0x06A6	3	R/W	RAMP_SWITCH_EN_PLLC	

Table 16.245. 0x06AC-0x06B2

Reg Address	Bit Field	Type	Setting Name	Description
0x06AC	0	R/W	OUT_MAX_LIMIT_EN_PLLC	Set by CBPro.
0x06AC	3	R/W	HOLD_SETTLE_DET_EN_PLLC	Set by CBPro.
0x06AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLC	Set by CBPro.
0x06B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLC	Set by CBPro.

16.8 Page 7 Registers Si5397C/D

Note that register addresses for Page 7 DSPLL D Registers 0x0709–0x074D are incremented relative to similar DSPLL A/B/C addresses on Pages 4, 5, and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0508/0x0608.

Table 16.246. 0x0708 DSPLL D Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	2:0	R	IN_PLLD_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3 4: Reserved

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the voltages on the IN_SEL1 and INSEL0 pins or the register value. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 16.247. 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	5:0	R/W	BW0_PLLD	Parameters that create the normal PLL bandwidth
0x070A	5:0	R/W	BW1_PLLD	
0x070B	5:0	R/W	BW2_PLLD	
0x070C	5:0	R/W	BW3_PLLD	
0x070D	5:0	R/W	BW4_PLLD	
0x070E	5:0	R/W	BW5_PLLD	

This group of registers determines the DSPLL D loop bandwidth. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 16.248. 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	5:0	R/W	FAST-LOCK_BW0_PLLD	Parameters that create the fast lock PLL bandwidth
0x0710	5:0	R/W	FAST-LOCK_BW_1PLLD	
0x0711	5:0	R/W	FAST-LOCK_BW2_PLLD	
0x0712	5:0	R/W	FAST-LOCK_BW3_PLLD	
0x0713	5:0	R/W	FAST-LOCK_BW_4PLLD	
0x0714	5:0	R/W	FAST-LOCK_BW5_PLLD	
0x0715	0	S	BW_UP-DATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D.

This group of registers determines the DSPLL Fastlock bandwidth. In Clock Builder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 16.249. 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	56- bit number
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.250. 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	32-bit number
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 16.251. 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 16.252. 0x0722 DSPLL D M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	3:0	R/W	M_FRAC_MODE_PLLD	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0722	4	R/W	M_FRAC_EN_PLLD	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0722	5	R/W	Reserved	Must be set to 1 for DSPLL D

Table 16.253. 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_PLLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0723	1	R/W	M_FSTEPW_DEN_PLLD	0: Modify numerator 1: Modify denominator

Table 16.254. 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	56-bit number
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716–0x0720

Table 16.255. 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 16.256. 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLD is out of lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Table 16.257. 0x072D DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	0	R/W	HOLD_EN_PLLD	0: Holdover disabled 1: Holdover enabled
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	Must be set to 1 for normal operation.
0x072D	4	R/W	HOLD_EXIT_BW_SEL1_PLLD	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover
0x072D	7:5	R/W	RAMP_STEP_INTERVAL_PLLD	

Table 16.258. 0x072E

Reg Address	Bit Field	Type	Setting Name	Description
0x072E	1	R/W	HOLD_RAMPBYP_NOHIST_PLLD	Set by CBPro.

Table 16.259. 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 16.260. 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DE-LAY_PLLD	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 16.261. 0x0732

Reg Address	Bit Field	Type	Setting Name	Description
0x0732	4:0	R/W	HOLD_REF_COUNT_FRC_PLLD	5- bit value

Table 16.262. 0x0733-0x0735

Reg Address	Bit Field	Type	Setting Name	Description
0x0733	7:0	R/W	HOLD_15M_CYC_COUNT_PLLD	Set by CBPro.
0x0734	15:8	R/W	HOLD_15M_CYC_COUNT_PLLD	
0x0735	23:16	R/W	HOLD_15M_CYC_COUNT_PLLD	

Table 16.263. 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover

Table 16.264. 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 16.265. 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applies to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

IN3 Input 3 applies to LOS alarm 0x0738[3], OOF alarm 0x0738[7]

Table 16.266. 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	6:4	R/W	IN1_PRIORI-TY_PLLD	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.267. 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORI-TY_PLLD	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x073A	6:4	R/W	IN3_PRIORI-TY_PLLD	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 16.268. 0x073B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x073B	1:0	R/W	HSW_MODE_PLLD	1:Default setting, do not modify 0,2,3: Reserved
0x073B	3:2	R/W	HSW_PHMEAS_CT RL_PLLD	0: Default setting, do not modify 1,2,3: Reserved

Table 16.269. 0x073C-0x073D Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x073C	7:0	R/W	HSW_PHMEAS_THR_PLLD	10-bit value. Set by CBPro.
0x073D	9:8	R/W	HSW_PHMEAS_THR_PLLD	

Table 16.270. 0x073E

Reg Address	Bit Field	Type	Setting Name	Description
0x073E	4:0	R/W	HSW_COARSE_PM_LEN_PLLD	Set by CBPro.

Table 16.271. 0x073F

Reg Address	Bit Field	Type	Setting Name	Description
0x073F	4:0	R/W	HSW_COARSE_PM_DLY_PLLD	Set by CBPro.

Table 16.272. 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x0740	2	R	FASTLOCK_STATUS_PLLD	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

Table 16.273. 0x0743-0x0745

Reg Address	Bit Field	Type	Setting Name	Description
0x0743	7:0	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.
0x0744	15:8	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.
0x0745	17:16	R/W	FINE_ADJ_OVR_PLLD	Set by CBPro.

Table 16.274. 0x0746

Reg Address	Bit Field	Type	Setting Name	Description
0x0746	1	R/W	FORCE_FINE_ADJ_PLLD	Set by CBPro.

Table 16.275. 0x0789-0x078A

Reg Address	Bit Field	Type	Setting Name	Description
0x0789	7:0	R/W	PFD_EN_DELAY_PLLD	Set by CBPro.
0x078A	12:8	R/W	PFD_EN_DELAY_PLLD	Set by CBPro.

Table 16.276. 0x078B

Reg Address	Bit Field	Type	Setting Name	Description
0x078B	19:0	R/W	HSW_MEAS_SETTLE_PLLD	Set by CBPro.

Table 16.277. 0x079B

Reg Address	Bit Field	Type	Setting Name	Description
0x079B	1	R/W	INIT_LP_CLOSE_HO_PLLB	
0x079B	2	R/W	HO_SKIP_PHASE_PLLD	Set by CBPro.
0x079B	4	R/W	HOLD_PRESERVE_HIST_PLLD	Set by CBPro.
0x079B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLD	Set by CBPro.
0x079B	6	R/W	HOLDEXIT_BW_SEL0_PLLD	Set by CBPro.
0x079B	7	R/W	HOLDEXIT_STD_BO_PLLD	Set by CBPro.

Table 16.278. 0x079C

Reg Address	Bit Field	Type	Setting Name	Description
0x079C	6	R/W	HOLDEXIT_ST_BO_PLLD	Set by CBPro.
0x079C	7	R/W	HOLD_RAMPBP_NOHIST_PLLD	Set by CBPro.

Table 16.279. 0x079D-0x07A2 DSPLL Holdover Exit Bandwidth for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x079D	5:0	R/W	HOLDEX-IT_BW0_PLLD	DSPLL D Fastlock Bandwidth parameters.
0x079E	5:0	R/W	HOLDEX-IT_BW1_PLLD	
0x079F	5:0	R/W	HOLDEX-IT_BW2_PLLD	
0x07A0	5:0	R/W	HOLDEX-IT_BW3_PLLD	
0x07A1	5:0	R/W	HOLDEX-IT_BW4_PLLD	
0x07A2	5:0	R/W	HOLDEX-IT_BW5_PLLD	

This group of registers determines the DSPLL D bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that the individual SOFT_RST_PLLD (0x001C[4]) does not update these bandwidth parameters.

Table 16.280. 0x07A4-0x07A5

Reg Address	Bit Field	Type	Setting Name	Description
0x07A4	7:0	R/W	HSW_LIMIT_PLLD	Set by CBPro.
0x07A5	0	R/W	HSW_LIMIT_ACTION_PLLD	Set by CBPro.

Table 16.281. 0x07A6

Reg Address	Bit Field	Type	Setting Name	Description
0x07A6	2:0	R/W	RAMP_STEP_SIZE_PLLD	Set by CBPro.
0x07A6	3	R/W	RAMP_SWITCH_EN_PLLD	

Table 16.282. 0x07AC-0x07B2

Reg Address	Bit Field	Type	Setting Name	Description
0x07AC	0	R/W	OUT_MAX_LIMIT_EN_PLLD	Set by CBPro.
0x07AC	3	R/W	HOLD_SETTLE_DET_EN_PLLD	Set by CBPro.
0x07AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLD	Set by CBPro.
0x07B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLD	Set by CBPro.

16.9 Page 9 Registers Si5397C/D

Table 16.283. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Table 16.284. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit selects between 1.8 V and 3.3 V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3 V tolerant. Setting this to the default 1.8 V is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I2C or SPI host is operating at 3.3 V and the Si5397/96 at VDD=1.8 V, the host must write IO_VDD_SEL=1. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 16.285. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See for more information.

When a clock is disabled, it is powered down.

Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 16.286. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 16.287. 0x094E-0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	
0x094F	7:4	R/W	IN_CMOS_USE1P8	

Table 16.288. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTEGER	0: Integer MXAXB 1: Fractional MXAXB

16.10 Page A Registers Si5397C/D

Table 16.289. 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 16.290. 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	4:0	R/W	N_PIBYP	Bypass fractional divider for N[3:0]. 0: Fractional (or Integer) division - Recommended if changing settings during operation 1: Integer-only division - best phase noise - Recommended for Integer N values Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 16.291. 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

16.11 Page B Registers Si5397C/D

Table 16.292. 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 16.293. 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 16.294. 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Reg Address	Bit Field	Type	Name	Description
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 16.295. 0x0B45 LOL Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	1: Clock disabled.
0x0B45	1	R/W	CLK_DIS_PLLB	1: Clock disabled.
0x0B45	2	R/W	CLK_DIS_PLLC	1: Clock disabled.
0x0B45	3	R/W	CLK_DIS_PLLD	1: Clock disabled.

Table 16.296. 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (IN3 IN2 IN1 IN0). Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 16.297. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	

Table 16.298. 0x0B48

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	

Table 16.299. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (D C B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 16.300. 0x0B4E Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B4E	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 16.301. 0x0B57 VCO_RESET_CALCODE

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CAL-CODE	
0x0B58	11:8	R/W	VCO_RESET_CAL-CODE	

16.12 Page C Registers Si5397C/D

Table 16.302. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 16.303. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 16.304. 0x0C05

Reg Address	Bit Field	Type	Name	Description
0x0C05	0	R/W	IN_CLK_VAL_EN_PLLA	Set by CBPro

Table 16.305. 0x0C06

Reg Address	Bit Field	Type	Name	Description
0x0C06	7:0	R/W	IN_CLK_VAL_TIME_PLLA	Set by CBPro

Table 16.306. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN_PLLB	Set by CBPro

Table 16.307. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME_PLLB	Set by CBPro

Table 16.308. 0x0C09

Reg Address	Bit Field	Type	Name	Description
0x0C09	0	R/W	IN_CLK_VAL_EN_PLLC	Set by CBPro

Table 16.309. 0x0C0A

Reg Address	Bit Field	Type	Name	Description
0x0C0A	7:0	R/W	IN_CLK_VAL_TIME_PLLC	Set by CBPro

Table 16.310. 0x0C0B

Reg Address	Bit Field	Type	Name	Description
0x0C0B	0	R/W	IN_CLK_VAL_EN_PLLD	Set by CBPro

Table 16.311. 0x0C0C

Reg Address	Bit Field	Type	Name	Description
0x0C0C	7:0	R/W	IN_CLK_VAL_TIME_PLLD	Set by CBPro

17. Si5396A/B Register Map

17.1 Page 0 Registers Si5396A/B

Table 17.1. 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 17.2. 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Register” is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 17.3. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x96	Four-digit “base” part number, one nibble per digit Example: Si5396A-A-GM. The base part number (OPN) is 5396, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 17.4. 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A 1 = B 2 = C 3 = D 9=J, 10=K,11=L,12=M

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 17.5. 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5396C-A12345-GM, the device revision is “A” and stored as 0

Table 17.6. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

Table 17.7. 0x0009–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5396C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5396C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5396 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 17.8. 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address. Note: This register is not bank burnable.

Table 17.9. 0x000C Internal Fault Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if no signal is detected on the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Table 17.10. 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]

Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]

Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 17.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	1:0	R	LOL_PLL[B:A]	1 if the DSPLL is out of lock
0x000E	5:4	R	HOLD_PLL[B:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Table 17.12. 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	5:4	R	CAL_PLL[B:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4

DSPLL_B corresponds to bit 5

Table 17.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R/W	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C.

Table 17.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF

These are sticky flag versions of 0x000D.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]

Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]

Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Table 17.15. 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	1:0	R/W	LOL_FLG_PLL[B:A]	1 if the DSPLL was unlocked
0x0013	5:4	R/W	HOLD_FLG_PLL[B:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Table 17.16. 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	5:4	R/W	CAL_FLG_PLL[B:A]	1 if the DSPLL internal calibration was busy

These are sticky flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

Table 17.17. 0x0016 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	1:0	R/W	LOL_ON_HOLD_PLL[B:A]	Set by CBPro.

Table 17.18. 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	
0x0017	1	R/W	LOS-XAXB_INTR_MSK	1 to mask out LOSXAXB.

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	2	R/W	LOS-REF_INTR_MSK	
0x0017	3	R/W	XAXB_ERR_INTR_MSK	
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask out SMBUS_TIMEOUT.
0x0017	6	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt.

Table 17.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]

Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]

Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 17.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	1:0	R/W	LOL_INTR_MSK_PLL[B:A]	1 to mask the clock input LOL flag
0x0019	5:4	R/W	HOLD_INTR_MSK_PLL[B:A]	1 to mask the holdover flag

DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]

DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 17.21. 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	5:4	R/W	CAL_INTR_MSK_PLL[B:A]	1 to mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

Table 17.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: initialize and calibrate the entire device.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLa bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA and BW_UPDATE_PLLB at addresses 0x0414 and 0x514.

Table 17.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement

Table 17.24. 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	1 to reset all the R dividers to the same state.

Table 17.25. 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only functions when FSTEP_PLL_SINGLE = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	3:2	R/W	FSTEP_PLL	Register version of the DSPLL_SEL[1:0] pins. Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: DSPLL B M-divider 2: DSPLL C M-divider 3: DSPLL D M-divider

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Table 17.26. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI

Table 17.27. 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable 1: To enable LOS for a clock input
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection 1: Disable LOS Detection

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Input 2 (IN2): LOS_EN[2]

Input 3 (IN3): LOS_EN[3]

Table 17.28. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 17.29. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 17.30. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 17.31. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 17.32. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 17.33. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 17.34. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 17.35. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 17.36. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 17.37. 0x003E

Reg Address	Bit Field	Type	Setting Name	Description
0x003E	7:4	R/W	LOS_MIN_PERI-OD_EN	Set by CBPro.

Table 17.38. 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable
0x003F	7:4	R/W	FAST_OOF_EN	1: To enable

bit 0,4 correspond to IN0

bit 1,5 correspond to IN1

bit 2,6 correspond to IN2

bit 3,7 correspond to IN3

.

Table 17.39. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

.

Table 17.40. 0x0041-0X0045 OOF Divider Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 17.41. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 17.42. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 17.43. 0x004E-0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DET-WIN_SEL	Values calculated by CBPro
0x004E	6:4	R/W	OOF1_DET-WIN_SEL	
0x004F	2:0	R/W	OOF2_DET-WIN_SEL	
0x004F	6:4	R/W	OOF3_DET-WIN_SEL	

Table 17.44. 0x0050 OOF_ON_LOS

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro

Table 17.45. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1 + Value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	
0x0053	3:0	R/W	FAST_OOF2_SET_THR	
0x0054	3:0	R/W	FAST_OOF3_SET_THR	

Table 17.46. 0x0055-0x0058

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1 + Value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	

Table 17.47. 0x0059 Fast OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	1:0	R/W	FAST_OOF0_DET-WIN_SEL	Values calculated by CBPro
0x0059	3:2	R/W	FAST_OOF1_DET-WIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DET-WIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DET-WIN_SEL	

Table 17.48. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 17.49. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by ClockBuilder Pro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 17.50. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by ClockBuilder Pro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 17.51. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by ClockBuilder Pro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 17.52. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Enables fast detection of LOL for PLLx. A large input frequency error will quickly assert LOL when this is enabled.
0x0092	1	R/W	LOL_FST_EN_PLLB	

Table 17.53. 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLA	Values calculated by ClockBuilder Pro
0x0093	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLB	

Table 17.54. 0x0095

Reg Address	Bit Field	Type	Setting Name	Description
0x0095	1:0	R/W	LOL_FST_VAL-WIN_SEL_PLLA	Values calculated by ClockBuilder Pro
0x0095	3:2	R/W	LOL_FST_VAL-WIN_SEL_PLLB	

Table 17.55. 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	

Table 17.56. 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	

Table 17.57. 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	0	R/W	LOL_SLOW_EN_PLLA	0: to disable LOL 1: To enable LOL
0x009A	1	R/W	LOL_SLOW_EN_PLLB	0: to disable LOL 1: To enable LOL

Table 17.58. 0x009B Slow LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:00	R/W	LOL_SLW_DET-WIN_SEL_PLLB	Values calculated by CBPro
0x009B	7:04	R/W	LOL_SLW_DET-WIN_SEL_PLLA	

Table 17.59. 0x009D LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Values calculated by CBPro
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	

Table 17.60. 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. See list below for selectable values.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. See list below for selectable values.

Table 17.61. 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. See list below for selectable values.

Table 17.62. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	0 1	R/W	LOL_TIM-ER_EN_PLLA LOL_TIM-ER_EN_PLLB	0: To disable 1: To enable

Table 17.63. 0x00A4-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLA	29-bit value
0x00A5	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLA	

Table 17.64. 0x00A9-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AA	15:8	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DE-LAY_DIV256_PLLB	

ClockBuilder Pro is used to set these values.

Table 17.65. 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	7:0	R	AC-TIVE_NVM_BLANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See for a detailed description of how to program the NVM.

Table 17.66. 0x00E5

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	4	R/W	FASTLOCK_EX-TEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EX-TEND_EN_PLLB	

Table 17.67. 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 17.68. 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x00EA	7:0	R/W	FSTLK_TIMER_EXT_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FSTLK_TIMER_EXT_PLLB	
0x00EC	23:16	R/W	FSTLK_TIMER_EXT_PLLB	
0x00ED	28:24	R/W	FSTLK_TIMER_EXT_PLLB	

Table 17.69. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 17.70. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 17.71. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 17.72. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	0:1	R	LOL_INTR_PLL[B:A]	Set by CBPro.
0x00F9	5:4	R	HOLD_INTR_PLL[B:A]	Set by CBPro.

Table 17.73. 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page so that a page write is not ever required to read the DEVICE_READY status.

WARNING: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note this includes writes to the PAGE register.

17.2 Page 1 Registers Si5396A/B

Table 17.74. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISA-BLE_LOW	0: Disables all output drivers 1: Pass through the output enables

Table 17.75. 0x0112, 0x0117, 0x0126, 0x012B Clock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0112 0x0117 0x0126 0x012B	0	R/W	OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pulldown effect.
0x0112 0x0117 0x0126 0x012B	1	R/W	OUT0_OE OUT1_OE OUT2_OE OUT3_OE	0: To disable the output 1: To enable the output
0x0112 0x0117 0x0126 0x012B	2	R/W	OUT0_RDIV_-FORCE2 OUT1_RDIV_-FORCE2 OUT2_RDIV_-FORCE2 OUT3_RDIV_-FORCE2	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2.

The output drivers are all identical.

Table 17.76. 0x0113, 0x0118, 0x0127, 0x012C Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0113 0x0118 0x0127 0x012C	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5: LVCMOS (+pin only) 6: LVCMOS (-pin only) 7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0113 0x0118 0x0127 0x012C	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN	0: Disable 1: Enable
0x0113 0x0118 0x0127 0x012C	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high 2-3: Reserved
0x0113 0x0118 0x0127 0x012C	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV	LVCMOS output impedance drive strength see .

The output drivers are all identical.

Table 17.77. 0x0114, 0x0119, 0x0128, 0x012D Output Amplitude

Reg Address	Bit Field	Type	Setting Name	Description
0x0114 0x0119 0x0128 0x012D	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .
0x0114 0x0119 0x0128 0x012D	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See .

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Table 17.78. 0x0115, 0x011A, 0x00129, 0x012E R-Divider Mux Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0115 0x011A 0x0129 0x012E	2:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: DSPLL A 1: DSPLL B 2-7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0115 0x011A 0x0129 0x012E	3	R/W	OUT0_VDD_SEL_-EN OUT1_VDD_SEL_-EN OUT2_VDD_SEL_-EN OUT3_VDD_SEL_-EN	1: Enable OUTx_VDD_SEL
0x0115 0x011A 0x0129 0x012E	5:4	R/W	OUT0_VDD_SEL OUT1_VDD_SEL OUT2_VDD_SEL OUT3_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0115 0x011A 0x0129 0x012E	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV	LVCMOS output inversion. Only applies when OUT0A_FORMAT = 4. See for more information.

Each output can be connected to either of the two DSPLLs using OUTx_MUX_SEL. The output drivers are all identical. The OUTx_MUX_SEL settings should match the corresponding OUTx_DIS_SRC selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 17.79. 0x0116, 0x011B, 0x012A, 0x012F Output Disable Source DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0116 0x011B 0x012A 0x012F	2:0	R/W	OUT0_DIS_SRC OUT1_DIS_SRC OUT2_DIS_SRC OUT3_DIS_SRC	Output clock Squelched (temporary disable) on DSPLL Soft Reset: 0: Reserved 1: DSPLL A squelches output 2: DSPLL B squelches output 3: DSPLL C squelches output 4: DSPLL D squelches output 5-7: Reserved

These CLKx_DIS_SRC settings should match the corresponding OUTx_MUX_SEL selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL. OUTx_DIS_SRC = OUTx_MUX_SEL + 1

Table 17.80. 0x013F

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	11:0	R/W	OUTX_AL-WAYS_ON	Set by CBPro.

Table 17.81. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	0	R/W	OUT_DIS_MSK_PLLA	
0x0141	1	R/W	OUT_DIS_MSK_PLLB	
0x0141	5	R/W	OUT_DIS_LOL_MSK	
0x0141	6	R/W	OUT_DIS_LOS-XAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	

Table 17.82. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1:0	R/W	OUT_DIS_MSK_LOL_PLL[B:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	5:4	R/W	OUT_DIS_MSK_HOLD_PLL[B:A]	

Bit 0 LOL_DSPLL_A mask

Bit 1 LOL_DSPLL_B mask

17.3 Page 2 Registers Si5396A/B

Table 17.83. 0x0206 XAXB Clock Input Reference Divide Value

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This can be used with external clock sources, not crystals.

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 17.84. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers.

Table 17.85. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 17.86. Si5396 P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211

Register Address	Description	Size	Same as Address
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in . ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 17.87. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in . Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA and SOFT_RST_PLLB do not update the Px_NUM or Px_DEN values.

Table 17.88. 0x0231 P0 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.89. 0x0232 P1 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.90. 0x0233 P2 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.91. 0x0234 P3 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.92. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 17.93. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in are followed.

Table 17.94. 0x023F

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	The divider value for the XAXB input

Table 17.95. 0x0250-0x0252 R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x0250	7:0	R/W	R0_REG	24-bit Integer divider divider value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x0251	15:8	R/W	R0_REG	
0x0252	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 17.96. Si5396-R1–R3 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0253-0x0255	R1_REG	24-bit Integer Number	0x0250-0x0252
0x025C-0x025E	R2_REG	24-bit Integer Number	0x0250-0x0252
0x025F-0x0261	R3_REG	24-bit Integer Number	0x0250-0x0252

Table 17.97. 0x026B-0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 17.98. 0x0278- 0x027D OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5396C-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5396C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5396C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory preprogrammed to a specific base part type (e.g., Si5396 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 17.99. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 17.100. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 17.101. 0x028A-0x028D

Reg Address	Bit Field	Type	Setting Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	The OOF0 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	The OOF1 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	The OOF2 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	The OOF3 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 17.102. 0x0292-0x0293

Reg Address	Bit Field	Type	Setting Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro.
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro.

Table 17.103. 0x028E-0x0291

Reg Address	Bit Field	Type	Setting Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	The OOF0 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	The OOF1 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	The OOF2 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	The OOF3 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 17.104. 0x0294

Reg Address	Bit Field	Type	Setting Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	

Table 17.105. 0x0296

Reg Address	Bit Field	Type	Setting Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	

Table 17.106. 0x0297

Reg Address	Bit Field	Type	Setting Name	Description
0x0297	0	R/W	FASTLOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN_PLLB	

Table 17.107. 0x0299

Reg Address	Bit Field	Type	Setting Name	Description
0x0299	0	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FAST-LOCK_DLY_ON-LOL_EN_PLLB	

Table 17.108. 0x029A-0x29C

Reg Address	Bit Field	Type	Setting Name	Description
0x029A	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	
0x029C	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLA	

Table 17.109. 0x029D-0x29F

Reg Address	Bit Field	Type	Setting Name	Description
0x029D	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	

Table 17.110. 0x02A6-0x2A8

Reg Address	Bit Field	Type	Setting Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 17.111. 0x02A9-0x2AB

Reg Address	Bit Field	Type	Setting Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 17.112. 0x02B7

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	

Table 17.113. 0x02B8

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8	0	R/W	LOL_LOS_REFCLK_PLLA	Set by CBPro.
0x02B8	1	R/W	LOL_LOS_REFCLK_PLLB	Set by CBPro.

Table 17.114. 0x02B9

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	0	R/W	LOL_LOS_REFCLK_PLLA_FLG	Set by CBPro.
0x02B9	1	R/W	LOL_LOS_REFCLK_PLLB_FLG	Set by CBPro.

Table 17.115. 0x02BC

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

17.4 Page 3 Registers Si5396A/B

Table 17.116. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 17.117. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer.
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.118. 0x030C N0 Update

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. A Soft Reset will have the same effect.

Table 17.119. that Follow the N0_NUM and N0_DEN Definitions

Reg Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 17.120. 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

17.5 Page 4 Registers Si5396A/B

Table 17.121. 0x0407 DSPLL A Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 17.122. 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Parameters that create the normal PLL bandwidth
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.Appendix A—Custom Differential Amplitude Controls

The loop bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 17.123. 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST-LOCK_BW0_PLLA	Parameters that create the fast lock PLL bandwidth
0x040F	5:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	5:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	5:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	5:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	5:0	R/W	FAST-LOCK_BW5_PLLA	
0x0414	0	S	BW_UP-DATE_PLLA	0: No effect. 1: Update both the Normal and Fastlock BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 17.124. 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56-bit number
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.125. 0x041C-0x041F M Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.126. 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 17.127. 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 17.128. 0x0422 DSPLL A FINC/FDEC Masking

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Table 17.129. 0x0423-0x0429 DSPLLA M Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0415–0x041F.

Table 17.130. 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 17.131. 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 17.132. 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 17.133. 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DE-LAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 17.134. 0x0431

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	5- bit value

Table 17.135. 0x0432

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Values calculated by CBPro
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 17.136. 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Table 17.137. 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 17.138. 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Table 17.139. 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 17.140. 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 17.141. 0x043A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0,2,3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 1,2,3: Reserved

Table 17.142. 0x043B-0x043C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Set by CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 17.143. 0x043D

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Set by CBPro

Table 17.144. 0x043E

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Set by CBPro

Table 17.145. 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R/O	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R/O	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 17.146. 0x0442-0x0444

Reg Address	Bit Field	Type	Setting Name	Description
0x0442	7:0	R/W	FINE_ADJ_OVR_PLLA	Set by CBPro
0x0443	15:8	R/W	FINE_ADJ_OVR_PLLA	
0x0444	17:16	R/W	FINE_ADJ_OVR_PLLA	

Table 17.147. 0x0445

Reg Address	Bit Field	Type	Setting Name	Description
0x0445	1	R/W	FORCE_FINE_ADJ_PLLA	Set by CBPro

Table 17.148. 0x0488 HSW_FINE_PM_LEN_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	

Table 17.149. 0x0489 PFD_EN_DELAY_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	7:0	R/W	PFD_EN_DELAY_PLLA	
0x048A	12:8	R/W	PFD_EN_DELAY_PLLA	

Table 17.150. 0x048B

Reg Address	Bit Field	Type	Setting Name	Description
0x048B	19:0	R/W	HSW_MEAS_SETTLE_PLLA	Set by CBPro.

Table 17.151. 0x049B HOLDEXIT_BW_SEL0_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	Set by CBPro.
0x049B	2	R/W	HO_SKIP_PHASE_PLLA	Set by CBPro.
0x049B	4	R/W	HOLD_PRESERVE_HIST_PLLA	Set by CBPro.
0x049B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLA	Set by CBPro.
0x049B	6	R/W	HOLDEXIT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEXIT_STD_BO_PLLA	Set by CBPro.

Table 17.152. 0x049C

Reg Address	Bit Field	Type	Setting Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NOHIST_PLLA	Set by CBPro.

Table 17.153. 0x049D-0x04A2 DSPLL Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	7:0	R/W	BW0_HO_PLLA	DSPLL A Holdover Bandwidth parameters.
0x049E	7:0	R/W	BW1_HO_PLLA	
0x049F	7:0	R/W	BW2_HO_PLLA	
0x04A0	7:0	R/W	BW3_HO_PLLA	
0x04A1	7:0	R/W	BW4_HO_PLLA	
0x04A2	7:0	R/W	BW5_HO_PLLA	

Table 17.154. 0x04A4-0x04A5

Reg Address	Bit Field	Type	Setting Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Set by CBPro.
0x04A5	0	R/W	HSW_LIMIT_ACTION_PLLA	Set by CBPro.

Table 17.155. 0x04A6

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	

Table 17.156. 0x04AC-0x04B2

Reg Address	Bit Field	Type	Setting Name	Description
0x04AC	0	R/W	OUT_MAX_LIMIT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SETTLE_DET_EN_PLLA	Set by CBPro.
0x04AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLA	Set by CBPro.
0x04B1	15:0	R/W	HOLD_SETTLE_TARGET_PLLA	Set by CBPro.

17.6 Page 5 Registers Si5396A/B

Table 17.157. 0x0507 DSPLL B Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 17.158. 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Parameters that create the normal PLL bandwidth
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 17.159. 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLLB	Parameters that create the fast lock PLL bandwidth
0x050F	5:0	R/W	FAST-LOCK_BW1_PLLB	
0x0510	5:0	R/W	FAST-LOCK_BW2_PLLB	
0x0511	5:0	R/W	FAST-LOCK_BW3_PLLB	
0x0512	5:0	R/W	FAST-LOCK_BW4_PLLB	
0x0513	5:0	R/W	FAST-LOCK_BW5_PLLB	
0x0514	0	S	BW_UP-DATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

This group of registers determines the DSPLL Fastlock bandwidth. In Clock Builder Pro, it is selectable from 10 Hz to 4 kHz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL

(0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 17.160. 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB[	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB[	
0x0517	23:16	R/W	M_NUM_PLLB[	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The M divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.161. 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.162. 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 17.163. 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1 for DSPLL B

Table 17.164. 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0522	1	R/W	M_FSTEPW_DEN_PLLB	

Table 17.165. 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEP_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEP_PLLB	
0x0525	23:16	R/W	M_FSTEP_PLLB	
0x0526	31:24	R/W	M_FSTEP_PLLB	
0x0527	39:32	R/W	M_FSTEP_PLLB	
0x0528	47:40	R/W	M_FSTEP_PLLB	
0x0529	55:48	R/W	M_FSTEP_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0515–0x051F.

Table 17.166. 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	0: Pin Control 1: Register Control

This is the input clock selection for manual register based clock selection.

Table 17.167. 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FASTLOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Table 17.168. 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLDEXIT_BW_SEL1_PLLB	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover
0x52C	7:5	R/W	RAMP_STEP_INTERVAL_PLLB	

Table 17.169. 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 17.170. 0x052F DSPLLB Holdover History Delay and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R	HOLD_HIST_DELAY_PLLB	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 17.171. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC_PLLB	5- bit value

Table 17.172. 0x0532

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Values calculated by CBPro
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 17.173. 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Table 17.174. 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 17.175. 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]

IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]

IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]

IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Table 17.176. 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 17.177. 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 17.178. 0x053A DSPLL B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1:Default setting, do not modify 0,2,3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1,2,3: Reserved

Table 17.179. 0x053B-0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 17.180. 0x053D

Reg Address	Bit Field	Type	Setting Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Set by CBPro.

Table 17.181. 0x053E

Reg Address	Bit Field	Type	Setting Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Set by CBPro.

Table 17.182. 0x053F DSPLL B Hold Valid History

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R/W	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 17.183. 0x0542-0x0544 FINE_ADJ_OVR_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0542	7:0	R/W	FINE_ADJ_OVR_PLLB	Set by CBPro.
0x0543	15:8	R/W	FINE_ADJ_OVR_PLLB	
0x0544	17:16	R/W	FINE_ADJ_OVR_PLLB	

Table 17.184. 0x0545 FORCE_FINE_ADJ_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0545	1	R/W	FORCE_FINE_ADJ_PLLB	Set by CBPro.

Table 17.185. 0x0588

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	

Table 17.186. 0x0589

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	
0x0589	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 17.187. 0x058B

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	19:0	R/W	HSW_MEAS_SETTLE_PLLB	Set by CBPro.

Table 17.188. 0x059B HOLDEXIT_BW_SEL0_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	IN-IT_LP_CLOSE_HO_PLLB	Set by CBPro.
0x059B	2	R/W	HO_SKIP_PHASE_PLLB	
0x059B	4	R/W	HOLD_PRE-SERVE_HIST_PLLB	
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	
0x059B	6	R/W	HOLDEX-IT_BW_SEL0_PLLB	
0x059B	7	R/W	HOLDEX-IT_STD_BO_PLLB	

Table 17.189. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NOHIST_PLLB	Set by CBPro.

Table 17.190. 0x059D

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEX-IT_BW0_PLLB	

Table 17.191. 0x059E

Reg Address	Bit Field	Type	Setting Name	Description
0x059E	5:0	R/W	HOLDEX-IT_BW1_PLLB	

Table 17.192. 0x059F

Reg Address	Bit Field	Type	Setting Name	Description
0x059F	5:0	R/W	HOLDEX-IT_BW2_PLLB	

Table 17.193. 0x05A0

Reg Address	Bit Field	Type	Setting Name	Description
0x05A0	5:0	R/W	HOLDEX-IT_BW3_PLLB	

Table 17.194. 0x05A1

Reg Address	Bit Field	Type	Setting Name	Description
0x05A1	5:0	R/W	HOLDEX-IT_BW4_PLLB	

Table 17.195. 0x059A2

Reg Address	Bit Field	Type	Setting Name	Description
0x05A2	5:0	R/W	HOLDEX-IT_BW5_PLLB	

Table 17.196. 0x05A4-0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Set by CBPro.
0x05A5	0	R/W	HSW_LIMIT_AC-TION_PLLB	Set by CBPro.

Table 17.197. 0x05A6

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE_PLLB	
0x05A6	3	R/W	RAMP_SWITCH_EN_PLLB	

Table 17.198. 0x05AC-0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLB	Set by CBPro.
0x05AD	15:0	R/W	OUT_MAX_LIM-IT_LMT_PLLB	Set by CBPro.
0x05B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLB	Set by CBPro.

17.7 Page 9 Registers Si5396A/B

Table 17.199. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Table 17.200. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit selects between 1.8 V and 3.3 V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3 V-tolerant. Setting this to the default 1.8 V is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I2C or SPI host is operating at 3.3 V and the Si5397/96 at VDD=1.8 V, the host must write IO_VDD_SEL=1. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 17.201. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See for more information.

When a clock is disabled, it is powered down.

Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 17.202. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 17.203. 0x094E-0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	
0x094F	7:4	R/W	IN_CMOS_USE1P8	

Table 17.204. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTEGER	Set by CBPro

17.8 Page A Registers Si5396A/B

Table 17.205. 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Name	Description
0x0A03	1:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 17.206. 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Name	Description
0x0A04	1:0	R/W	N_PIBYP	Bypass fractional divider for N[1:0]. 0: Fractional (or Integer) division - Recommended if changing settings during operation 1: Integer-only division - best phase noise - Recommended for Integer N values Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 17.207. 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	1:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0]

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

17.9 Page B Registers Si5396A/B

Table 17.208. 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 17.209. 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 17.210. 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 17.211. 0x0B45

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	Set by CBPro.
0x0B45	1	R/W	CLK_DIS_PLLB	Set by CBPro.

Table 17.212. 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Controls the clock to the digital LOS circuitry. Must be set to 0 to enable the LOS function of the respective Inputs (IN3 IN2 IN1 IN0).

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 17.213. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set by CBPro.

Table 17.214. 0x0B48

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set by CBPro.

Table 17.215. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 17.216. 0x0B4E Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B4E	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 17.217. 0x0B57 VCO_RESET_CALCODE

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CALCODE	
0x0B58	11:8	R/W	VCO_RESET_CALCODE	

17.10 Page C Registers Si5396A/B

Table 17.218. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 17.219. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 17.220. 0x0C05

Reg Address	Bit Field	Type	Name	Description
0x0C05	0	R/W	IN_CLK_VAL_EN_PLLA	Set by CBPro

Table 17.221. 0x0C06

Reg Address	Bit Field	Type	Name	Description
0x0C06	7:0	R/W	IN_CLK_VAL_TIME_PLLA	Set by CBPro

Table 17.222. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN_PLLB	Set by CBPro

Table 17.223. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME_PLLB	Set by CBPro

18. Si5396C/D Register Map

18.1 Page 0 Registers Si5396C/D

Table 18.1. 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 18.2. 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Register” is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 18.3. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x96	Four-digit “base” part number, one nibble per digit Example: Si5396C-A-GM. The base part number (OPN) is 5396, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 18.4. 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A 1 = B 2 = C 3 = D 9=J, 10=K,11=L,12=M

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 18.5. 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5396C-A12345-GM, the device revision is “A” and stored as 0

Table 18.6. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

Table 18.7. 0x0009–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5396C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5396C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5396 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 18.8. 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address. Note: This register is not bank burnable.

Table 18.9. 0x000C Internal Fault Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if no signal is detected on the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Table 18.10. 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]

Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]

Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 18.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	1:0	R	LOL_PLL[B:A]	1 if the DSPLL is out of lock
0x000E	5:4	R	HOLD_PLL[B:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Table 18.12. 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	5:4	R	CAL_PLL[B:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4

DSPLL_B corresponds to bit 5

Table 18.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R/W	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C.

Table 18.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF

These are sticky flag versions of 0x000D.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]

Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]

Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Table 18.15. 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	1:0	R/W	LOL_FLG_PLL[B:A]	1 if the DSPLL was unlocked
0x0013	5:4	R/W	HOLD_FLG_PLL[B:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Table 18.16. 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	5:4	R/W	CAL_FLG_PLL[B:A]	1 if the DSPLL internal calibration was busy

These are sticky flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

Table 18.17. 0x0016 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	1:0	R/W	LOL_ON_HOLD_PLL[B:A]	Set by CBPro.

Table 18.18. 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOS-XAXB_INTR_MSK	1 to mask out LOSXAXB.

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	2	R/W	LOS-REF_INTR_MSK	
0x0017	3	R/W	XAXB_ERR_INTR_MSK	
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask out SMBUS_TIMEOUT.
0x0017	6	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	Reserved	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt.

Table 18.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]

Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]

Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 18.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	1:0	R/W	LOL_INTR_MSK_PLL[B:A]	1 to mask the clock input LOL flag
0x0019	5:4	R/W	HOLD_INTR_MSK_PLL[B:A]	1 to mask the holdover flag

DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]

DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 18.21. 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	5:4	R/W	CAL_INTR_MSK_PLL[B:A]	1 to mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

Table 18.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: initialize and calibrate the entire device.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLa bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA and BW_UPDATE_PLLB at addresses 0x0414 and 0x514.

Table 18.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement

Table 18.24. 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	1 to reset all the R dividers to the same state.

Table 18.25. 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only functions when FSTEP_PLL_SINGLE = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	3:2	R/W	FSTEP_PLL	Register version of the DSPLL_SEL[1:0] pins. Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: DSPLL B M-divider 2: DSPLL C M-divider 3: DSPLL D M-divider

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Table 18.26. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI

Table 18.27. 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable 1: To enable LOS for a clock input
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection 1: Disable LOS Detection

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Input 2 (IN2): LOS_EN[2]

Input 3 (IN3): LOS_EN[3]

Table 18.28. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 18.29. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 18.30. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 18.31. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 18.32. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 18.33. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 18.34. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 18.35. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 18.36. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 18.37. 0x003E

Reg Address	Bit Field	Type	Setting Name	Description
0x003E	7:4	R/W	LOS_MIN_PERI-OD_EN	Set by CBPro.

Table 18.38. 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable
0x003F	7:4	R/W	FAST_OOF_EN	1: To enable

bit 0,4 correspond to IN0

bit 1,5 correspond to IN1

bit 2,6 correspond to IN2

bit 3,7 correspond to IN3

.

Table 18.39. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

.

Table 18.40. 0x0041-0X0045 OOF Divider Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 18.41. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 18.42. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear threshold. Range is up to ± 500 ppm in steps of 1/16 ppm.

Table 18.43. 0x004E-0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DET-WIN_SEL	Values calculated by CBPro
0x004E	6:4	R/W	OOF1_DET-WIN_SEL	
0x004F	2:0	R/W	OOF2_DET-WIN_SEL	
0x004F	6:4	R/W	OOF3_DET-WIN_SEL	

Table 18.44. 0x0050 OOF_ON_LOS

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro

Table 18.45. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1 + Value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	
0x0053	3:0	R/W	FAST_OOF2_SET_THR	
0x0054	3:0	R/W	FAST_OOF3_SET_THR	

Table 18.46. 0x0055-0x0058

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1 + Value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	

Table 18.47. 0x0059 Fast OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	1:0	R/W	FAST_OOF0_DET-WIN_SEL	Values calculated by CBPro
0x0059	3:2	R/W	FAST_OOF1_DET-WIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DET-WIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DET-WIN_SEL	

Table 18.48. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 18.49. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by ClockBuilder Pro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 18.50. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by ClockBuilder Pro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 18.51. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by ClockBuilder Pro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 18.52. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Enables fast detection of LOL for PLLx. A large input frequency error will quickly assert LOL when this is enabled.
0x0092	1	R/W	LOL_FST_EN_PLLB	

Table 18.53. 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLA	Values calculated by ClockBuilder Pro
0x0093	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLB	

Table 18.54. 0x0095

Reg Address	Bit Field	Type	Setting Name	Description
0x0095	1:0	R/W	LOL_FST_VAL-WIN_SEL_PLLA	Values calculated by ClockBuilder Pro
0x0095	3:2	R/W	LOL_FST_VAL-WIN_SEL_PLLB	

Table 18.55. 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	

Table 18.56. 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	

Table 18.57. 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	0	R/W	LOL_SLOW_EN_PLLA	0: to disable LOL 1: To enable LOL
0x009A	1	R/W	LOL_SLOW_EN_PLLB	0: to disable LOL 1: To enable LOL

Table 18.58. 0x009B Slow LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:00	R/W	LOL_SLW_DET-WIN_SEL_PLLB	Values calculated by CBPro
0x009B	7:04	R/W	LOL_SLW_DET-WIN_SEL_PLLA	

Table 18.59. 0x009D LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Values calculated by CBPro
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	

Table 18.60. 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. See list below for selectable values.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. See list below for selectable values.

The following are the thresholds for the value that is placed in the top or bottom four bits of register 0x009E.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 18.61. 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. See list below for selectable values.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. See list below for selectable values.

Table 18.62. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	0 1	R/W	LOL_TIMER_EN_PLLA LOL_TIMER_EN_PLLB	0: To disable 1: To enable

Table 18.63. 0x00A4-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	29-bit value
0x00A5	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLA	

Table 18.64. 0x00A9-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLB	29-bit value. Sets the clear timer 0x00AA 15:8 R/W LOL_CLR_DLY for LOL. CBPro sets this value.
0x00AA	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLB	

ClockBuilder Pro is used to set these values.

Table 18.65. 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BLANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See for a detailed description of how to program the NVM.

Table 18.66. 0x00E5

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	

Table 18.67. 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 18.68. 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x00EA	7:0	R/W	FSTLK_TIMER_EXT_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FSTLK_TIMER_EXT_PLLB	
0x00EC	23:16	R/W	FSTLK_TIMER_EXT_PLLB	
0x00ED	28:24	R/W	FSTLK_TIMER_EXT_PLLB	

Table 18.69. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 18.70. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.

Reg Address	Bit Field	Type	Name	Description
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 18.71. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 18.72. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	0:1	R	LOL_INTR_PLL[B:A]	Set by CBPro.
0x00F9	5:4	R	HOLD_INTR_PLL[B:A]	Set by CBPro.

Table 18.73. 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page so that a page write is not ever required to read the DEVICE_READY status.

WARNING: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note this includes writes to the PAGE register.

18.2 Page 1 Registers Si5396C/D

Table 18.74. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers

Table 18.75. Register 0x0103 OUT0A Output Enable and R0A Divider Configuration

Reg Address	Bit Field	Type	Name	Description
0x0103	0	R/W	OUT0A_PDN	Powerdown output driver. 0: Normal Operation (default) 1: Powerdown output driver When powered down, outputs pins will be high impedance with a light pull down effect.
0x0103	1	R/W	OUT0A_OE	Enable/Disable individual output. 0: Disable output (default) 1: Enable output
0x0103	2	R/W	OUT0A_RDIV_FORCE2	Force R0A output divider divide-by-2. 0: R0A_REG sets divide value (default) 1: Divide value forced to divide-by-2

Setting R0A_REG=0 will not set the divide value to divide-by-2 automatically. OUT0A_RDIV_FORCE2 must be set to a value of 1 to force R0A to divide-by-2. Note that the R0A_REG value will be ignored while OUT0A_RDIV_FORCE2=1. See R0A_REG registers, 0x0247-0x0249, for more information.

Table 18.76. Register 0x0104 OUT0A Output Format and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0104	2:0	R/W	OUT0A_FORMAT	Select output format. 0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved

Reg Address	Bit Field	Type	Name	Description
0x0104	3	R/W	OUT0A_SYNC_EN	Synchronous Enable/ Disable selection. 0: Asynchronous Enable/ Disable (default) 1: Synchronous Enable/ Disable (Glitchless)
0x0104	5:4	R/W	OUT0A_DIS_STATE	Determines the logic state of the output driver when disabled: 0: Disable logic Low 1: Disable logic High 2-3: Reserved
0x0104	7:6	R/W	OUT0A_CMOS_DRV	LVCMOS output impedance selection. See 6.4.5 LVCMOS Output Impedance and Drive Strength Selectionfor valid selections.

Table 18.77. Register 0x0105 Output OUT0A Differential Amplitude and Common Mode

Reg Address	Bit Field	Type	Name	Description
0x0105	3:0	R/W	OUT0A_CM	OUT0A Common Mode Voltage selection. Only applies when OUT0A_FORMAT=1 or 2.
0x0105	6:4	R/W	OUT0A_AMPL	OUT0A Differential Amplitude setting. Only applies when OUT0A_FORMAT=1 or 2.

ClockBuilder Pro is used to select the correct settings for this register. See 6.4.9 Setting the Differential Output Driver to Non-Standard Amplitudes for details of the settings.

Table 18.78. Register 0x0106 Output OUT0A Source, VDD Select, and LVCMOS Inversion

Reg Address	Bit Field	Type	Name	Description
0x0106	2:0	R/W	OUT0A_MUX_SEL	OUT0A output source divider select. 0: N0 is the source for OUT0A 1: N1 is the source for OUT0A 2: N2 is the source for OUT0A 3: N3 is the source for OUT0A 4: N4 is the source for OUT0A 5-7: Reserved
0x0106	3	R/W	OUT0A_VDD_SEL_EN	Output Driver VDD Select Enable. Set to 1 for normal operation.

Reg Address	Bit Field	Type	Name	Description
0x0106	5:4	R/W	OUT0A_VDD_SEL	Output Driver VDD Select 0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0106	7:6	R/W	OUT0A_INV	OUT0A output LVCMOS inversion. Only applies when OUT0A_FORMAT= 4. See 6.4.7 LVCMOS Output Polarity for more information.

Each output can be independently configured to use one of the N0-N4 divider outputs as its source. Nx_NUM and Nx_DEN for each N-divider are set in registers 0x0302-0x0337 for N0 to N4. Five different frequencies can be set in the N-dividers (N0-N4) and each of the 12 outputs can be configured to use any of the five different frequencies.

All 12 output drivers are identical in terms of control. The single set of descriptions above for OUT0A also applies to OUT0-OUT9A:

Table 18.79. Output Registers Following the Same Definitions as OUT0A

Register Address	Description	(Same as) Address
0x0108	OUT0 Powerdown, Output Enable, and R0 Divide-by-2	0x0103
0x0109	OUT0 Signal Format and Configuration	0x0104
0x010A	OUT0 Differential Amplitude and Common Mode	0x0105
0x010B	OUT0 Source Selection and LVCMOS Inversion	0x0106
0x010D	OUT1 Powerdown, Output Enable, and R1 Divide-by-2	0x0103
0x010E	OUT1 Signal Format and Configuration	0x0104
0x010F	OUT1 Differential Amplitude and Common Mode	0x0105
0x0110	OUT1 Source Selection and LVCMOS Inversion	0x0106
0x0112	OUT2 Powerdown, Output Enable, and R2 Divide-by-2	0x0103
0x0113	OUT2 Signal Format and Configuration	0x0104
0x0114	OUT2 Differential Amplitude and Common Mode	0x0105
0x0115	OUT2 Source Selection and LVCMOS Inversion	0x0106
0x0117	OUT3 Powerdown, Output Enable, and R3 Divide-by-2	0x0103
0x0118	OUT3 Signal Format and Configuration	0x0104

Register Address	Description	(Same as) Address
0x0119	OUT3 Differential Amplitude and Common Mode	0x0105
0x011A	OUT3 Source Selection and LVCMOS Inversion	0x0106
0x011C	OUT4 Powerdown, Output Enable, and R4 Divide-by-2	0x0103
0x011D	OUT4 Signal Format and Configuration	0x0104
0x011E	OUT4 Differential Amplitude and Common Mode	0x0105
0x011F	OUT4 Source Selection and LVCMOS Inversion	0x0106
0x0121	OUT5 Powerdown, Output Enable, and R5 Divide-by-2	0x0103
0x0122	OUT5 Signal Format and Configuration	0x0104
0x0123	OUT5 Differential Amplitude and Common Mode	0x0105
0x0124	OUT5 Source Selection and LVCMOS Inversion	0x0106
0x0126	OUT6 Powerdown, Output Enable, and R6 Divide-by-2	0x0103
0x0127	OUT6 Signal Format and Configuration	0x0104
0x0128	OUT6 Differential Amplitude and Common Mode	0x0105
0x0129	OUT6 Source Selection and LVCMOS Inversion	0x0106
0x012B	OUT7 Powerdown, Output Enable, and R7 Divide-by-2	0x0103
0x012C	OUT7 Signal Format and Configuration	0x0104
0x012D	OUT7 Differential Amplitude and Common Mode	0x0105
0x012E	OUT7 Source Selection and LVCMOS Inversion	0x0106
0x0130	OUT8 Powerdown, Output Enable, and R8 Divide-by-2	0x0103
0x0131	OUT8 Signal Format and Configuration	0x0104
0x0132	OUT8 Differential Amplitude and Common Mode	0x0105
0x0133	OUT8 Source Selection and LVCMOS Inversion	0x0106
0x0135	OUT9 Powerdown, Output Enable, and R9 Divide-by-2	0x0103

Register Address	Description	(Same as) Address
0x0136	OUT9 Signal Format and Configuration	0x0104
0x0137	OUT9 Differential Amplitude and Common Mode	0x0105
0x0138	OUT9 Source Selection and LVCMOS Inversion	0x0106
0x013A	OUT9A Powerdown, Output Enable, and R9A Divide-by-2	0x0103
0x013B	OUT9A Signal Format and Configuration	0x0104
0x013C	OUT9A Differential Amplitude and Common Mode	0x0105
0x013D	OUT9A Source Selection and LVCMOS Inversion	0x0106

Table 18.80. 0x013F-0x0140

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	This setting is managed by CBPro during zero delay mode.
0x0140	11:8	R/W	OUTX_ALWAYS_ON	

Table 18.81. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	0	R/W	OUT_DIS_MSK_PLLA	
0x0141	1	R/W	OUT_DIS_MSK_PLLB	
0x0141	5	R/W	OUT_DIS_LOL_MSK	
0x0141	6	R/W	OUT_DIS_LOS-XAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	

Table 18.82. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1:0	R/W	OUT_DIS_MSK_LOL_PLL[B:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	5:4	R/W	OUT_DIS_MSK_HOLD_PLL[B:A]	

Bit 0 LOL_DSPLL_A mask

Bit 1 LOL_DSPLL_B mask

Table 18.83. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

18.3 Page 2 Registers Si5396C/D

Table 18.84. 0x0206 Pre-Scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the prescale divider for the input clock on XAXB.

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

This can only be used with external clock sources, not crystals.

Table 18.85. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configures the P-dividers which are located at the four input clocks seen in Section 3.1 DSPLL and MultiSynth. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 18.86. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 18.87. Registers that Follow the P0_NUM and P0_DEN Above

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D

Register Address	Description	Size	Same as Address
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the four input clocks seen in Section 3.1 DSPLL and MultiSynth. ClockBuilder Pro calculates the correct values for the P-dividers. The Px_Update bit (register 0x0230) for the appropriate channel must be updated for the new P value to take affect.

Table 18.88. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S	P0_UPDATE	0 - No update for P-divider value 1 - Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

The Px_Update bit must be asserted to update the P-Divider. The update bits are provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 18.89. 0x0231 P0 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.90. 0x0232 P1 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.91. 0x0233 P2 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.92. 0x0234 P3 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.93. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Dynamic PLL Changes are followed.

Table 18.94. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines inSection 4.2 Dynamic PLL Changes are followed.

Table 18.95. 0x023F MXAXB Update

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 18.96. Register 0x0247-0x0249 R0A Divider

Reg Address	Bit Field	Type	Name	Description
0x0247	7:0	R/W	R0A_REG	24-bit integer final R0A divider selection. R Divisor = (R0A_REG+1) x 2 However, note that setting R0A_REG = 0 will not set the output to divide-by-2. See notes below.
0x0248	15:8			
0x0249	23:16			

The final output R dividers are even dividers beginning with divide-by-2. While all other values follow the formula in the bit description above, divide-by-2 requires an extra bit to be set. For divide-by-2, set OUT0A_RDIV_FORCE2=1. See the description for register bit 0x0103[2] in this register map.

The R0-R9A dividers follow the same format as the R0A divider description above.

Table 18.97. Registers that Follow the R0A_REG

Register Address	Description	Size	Same as Address
0x024A-0x024C	R0_REG	24-bit Integer Number	0x0247-0x0249
0x024D-0x024F	R1_REG	24-bit Integer Number	0x0247-0x0249
0x0250-0x0252	R2_REG	24-bit Integer Number	0x0247-0x0249
0x0253-0x0255	R3_REG	24-bit Integer Number	0x0247-0x0249
0x0256-0x0258	R4_REG	24-bit Integer Number	0x0247-0x0249
0x0259-0x025B	R5_REG	24-bit Integer Number	0x0247-0x0249
0x025C-0x025E	R6_REG	24-bit Integer Number	0x0247-0x0249
0x025F-0x0261	R7_REG	24-bit Integer Number	0x0247-0x0249
0x0262-0x0264	R8_REG	24-bit Integer Number	0x0247-0x0249
0x0265-0x0267	R9_REG	24-bit Integer Number	0x0247-0x0249
0x0268-0x026A	R9A_REG	24-bit Integer Number	0x0247-0x0249

Table 18.98. 0x026B–0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Registers 0x026B - 0x0272 can also be used as User Scratch.

Table 18.99. 0x0278–0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: Si5396C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5396C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5396C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5396 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 18.100. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 18.101. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 18.102. 0x028A-0x028D OOFx_TRG_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 18.103. 0x028E-0x0291 OOFx_CLR_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028E	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028F	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x0290	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x0291	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 18.104. 0x0292 OOF_STOP_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro

Table 18.105. 0x0293 OOF_CLEAR_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro

Table 18.106. 0x0294

Reg Address	Bit Field	Type	Setting Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	

Table 18.107. 0x0296

Reg Address	Bit Field	Type	Setting Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	

Table 18.108. 0x0297

Reg Address	Bit Field	Type	Setting Name	Description
0x0297	0	R/W	FASTLOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN_PLLB	

Table 18.109. 0x0299

Reg Address	Bit Field	Type	Setting Name	Description
0x0299	0	R/W	FASTLOCK_DLY_ONLOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FASTLOCK_DLY_ONLOL_EN_PLLB	

Table 18.110. 0x029A-0x29C

Reg Address	Bit Field	Type	Setting Name	Description
0x029A	7:0	R/W	FASTLOCK_DLY_ONLOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FASTLOCK_DLY_ONLOL_PLLA	
0x029C	19:16	R/W	FASTLOCK_DLY_ONLOL_PLLA	

Table 18.111. 0x029D-0x29F

Reg Address	Bit Field	Type	Setting Name	Description
0x029D	7:0	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FAST-LOCK_DLY_ON-LOL_PLLB	

Table 18.112. 0x02A6-0x2A8

Reg Address	Bit Field	Type	Setting Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 18.113. 0x02A9-0x2AB

Reg Address	Bit Field	Type	Setting Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 18.114. 0x02B7

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	

Table 18.115. 0x02B8

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8	0	R/W	LOL_LOS_REFCLK_PLLA	Set by CBPro.
0x02B8	1	R/W	LOL_LOS_REFCLK_PLLB	Set by CBPro.

Table 18.116. 0x02B9

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	0	R/W	LOL_LOS_REFCLK_PLLA_FLG	Set by CBPro.
0x02B9	1	R/W	LOL_LOS_REFCLK_PLLB_FLG	Set by CBPro.

Table 18.117. 0x02BC

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

18.4 Page 3 Registers Si5396C/D

Table 18.118. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 18.119. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer.
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.120. 0x030C N0 Update

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. A Soft Reset will have the same effect.

Table 18.121. that Follow the N0_NUM and N0_DEN Definitions

Reg Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 18.122. 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

18.5 Page 4 Registers Si5396C/D

Table 18.123. 0x0407 DSPLL A Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 18.124. 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Parameters that create the normal PLL bandwidth
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.Appendix A—Custom Differential Amplitude Controls

The loop bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 18.125. 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST-LOCK_BW0_PLLA	Parameters that create the fast lock PLL bandwidth
0x040F	5:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	5:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	5:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	5:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	5:0	R/W	FAST-LOCK_BW5_PLLA	
0x0414	0	S	BW_UP-DATE_PLLA	0: No effect. 1: Update both the Normal and Fastlock BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 18.126. 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56-bit number
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.127. 0x041C-0x041F M Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.128. 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 18.129. 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 18.130. 0x0422 DSPLL A FINC/FDEC Masking

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Table 18.131. 0x0423-0x0429 DSPLLA M Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0415–0x041F.

Table 18.132. 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Table 18.133. 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 18.134. 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 18.135. 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DE-LAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 18.136. 0x0431

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	5- bit value

Table 18.137. 0x0432

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Values calculated by CBPro
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 18.138. 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Table 18.139. 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 18.140. 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Table 18.141. 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	6:4	R/W	IN1_PRIORI-TY_PLLA	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 18.142. 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORI-TY_PLLA	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORI-TY_PLLA	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 18.143. 0x043A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0,2,3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 1,2,3: Reserved

Table 18.144. 0x043B-0x043C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Set by CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 18.145. 0x043D

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Set by CBPro

Table 18.146. 0x043E

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Set by CBPro

Table 18.147. 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R/O	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R/O	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 18.148. 0x0442-0x0444

Reg Address	Bit Field	Type	Setting Name	Description
0x0442	7:0	R/W	FINE_ADJ_OVR_PLLA	Set by CBPro
0x0443	15:8	R/W	FINE_ADJ_OVR_PLLA	
0x0444	17:16	R/W	FINE_ADJ_OVR_PLLA	

Table 18.149. 0x0445

Reg Address	Bit Field	Type	Setting Name	Description
0x0445	1	R/W	FORCE_FINE_ADJ_PLLA	Set by CBPro

Table 18.150. 0x0488 HSW_FINE_PM_LEN_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	

Table 18.151. 0x0489 PFD_EN_DELAY_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	7:0	R/W	PFD_EN_DELAY_PLLA	
0x048A	12:8	R/W	PFD_EN_DELAY_PLLA	

Table 18.152. 0x048B

Reg Address	Bit Field	Type	Setting Name	Description
0x048B	19:0	R/W	HSW_MEAS_SETTLE_PLLA	Set by CBPro.

Table 18.153. 0x049B HOLDEXIT_BW_SEL0_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	Set by CBPro.
0x049B	2	R/W	HO_SKIP_PHASE_PLLA	Set by CBPro.
0x049B	4	R/W	HOLD_PRESERVE_HIST_PLLA	Set by CBPro.
0x049B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLA	Set by CBPro.
0x049B	6	R/W	HOLDEXIT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEXIT_STD_BO_PLLA	Set by CBPro.

Table 18.154. 0x049C

Reg Address	Bit Field	Type	Setting Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NOHIST_PLLA	Set by CBPro.

Table 18.155. 0x049D-0x04A2 DSPLL Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	7:0	R/W	BW0_HO_PLLA	DSPLL A Holdover Bandwidth parameters. Set by CBPro to set the PLL bandwidth when exiting holdover.
0x049E	7:0	R/W	BW1_HO_PLLA	
0x049F	7:0	R/W	BW2_HO_PLLA	
0x04A0	7:0	R/W	BW3_HO_PLLA	
0x04A1	7:0	R/W	BW4_HO_PLLA	
0x04A2	7:0	R/W	BW5_HO_PLLA	

Table 18.156. 0x04A4-0x04A5

Reg Address	Bit Field	Type	Setting Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Set by CBPro.
0x04A5	0	R/W	HSW_LIMIT_ACTION_PLLA	Set by CBPro.

Table 18.157. 0x04A6

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	Size of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	Ramp Switching Enable 0: Disable Ramp Switching 1: Enable Ramp Switching (default)

Table 18.158. 0x04AC-0x04B2

Reg Address	Bit Field	Type	Setting Name	Description
0x04AC	0	R/W	OUT_MAX_LIMIT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SETTLE_DET_EN_PLLA	Set by CBPro.
0x04AD	15:0	R/W	OUT_MAX_LIMIT_LMT_PLLA	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x04B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLA	Set by CBPro.

18.6 Page 5 Registers Si5396C/D

Table 18.159. 0x0507 DSPLL B Active Input

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock 0: IN0 1: IN1 2: IN2 3: IN3

Table 18.160. 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Parameters that create the normal PLL bandwidth
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 18.161. 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLLB	Parameters that create the fast lock PLL bandwidth
0x050F	5:0	R/W	FAST-LOCK_BW1_PLLB	
0x0510	5:0	R/W	FAST-LOCK_BW2_PLLB	
0x0511	5:0	R/W	FAST-LOCK_BW3_PLLB	
0x0512	5:0	R/W	FAST-LOCK_BW4_PLLB	
0x0513	5:0	R/W	FAST-LOCK_BW5_PLLB	
0x0514	0	S	BW_UP-DATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

This group of registers determines the DSPLL Fastlock bandwidth. In Clock Builder Pro, it is selectable from 10 Hz to 4 kHz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL

(0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 18.162. 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB[	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB[	
0x0517	23:16	R/W	M_NUM_PLLB[	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The M divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.163. 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.164. 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 18.165. 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1 for DSPLL B

Table 18.166. 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0522	1	R/W	M_FSTEPW_DEN_PLLB	

Table 18.167. 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEP_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEP_PLLB	
0x0525	23:16	R/W	M_FSTEP_PLLB	
0x0526	31:24	R/W	M_FSTEP_PLLB	
0x0527	39:32	R/W	M_FSTEP_PLLB	
0x0528	47:40	R/W	M_FSTEP_PLLB	
0x0529	55:48	R/W	M_FSTEP_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0515–0x051F.

Table 18.168. 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	0: Pin Control 1: Register Control

This is the input clock selection for manual register based clock selection.

Table 18.169. 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FASTLOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Table 18.170. 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLDEXIT_BW_SEL1_PLLB	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover
0x52C	7:5	R/W	RAMP_STEP_INTERVAL_PLLB	

Table 18.171. 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 18.172. 0x052F DSPLLB Holdover History Delay and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R	HOLD_HIST_DELAY_PLLB	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 18.173. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC_PLLB	5- bit value

Table 18.174. 0x0532

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Values calculated by CBPro
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 18.175. 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Table 18.176. 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 18.177. 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]

IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]

IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]

IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Table 18.178. 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 18.179. 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Table 18.180. 0x053A DSPLL B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1:Default setting, do not modify 0,2,3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1,2,3: Reserved

Table 18.181. 0x053B-0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 18.182. 0x053D

Reg Address	Bit Field	Type	Setting Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Set by CBPro.

Table 18.183. 0x053E

Reg Address	Bit Field	Type	Setting Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Set by CBPro.

Table 18.184. 0x053F DSPLL B Hold Valid History

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R/W	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop.

When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 18.185. 0x0542-0x0544 FINE_ADJ_OVR_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0542	7:0	R/W	FINE_ADJ_OVR_PLLB	Set by CBPro.
0x0543	15:8	R/W	FINE_ADJ_OVR_PLLB	
0x0544	17:16	R/W	FINE_ADJ_OVR_PLLB	

Table 18.186. 0x0545 FORCE_FINE_ADJ_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0545	1	R/W	FORCE_FINE_ADJ_PLLB	Set by CBPro.

Table 18.187. 0x0588

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	

Table 18.188. 0x0589

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	
0x0589	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 18.189. 0x058B

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	19:0	R/W	HSW_MEAS_SETTLE_PLLB	Set by CBPro.

Table 18.190. 0x059B HOLDEXIT_BW_SEL0_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	IN-IT_LP_CLOSE_HO_PLLB	Set by CBPro.
0x059B	2	R/W	HO_SKIP_PHASE_PLLB	
0x059B	4	R/W	HOLD_PRE-SERVE_HIST_PLLB	
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	
0x059B	6	R/W	HOLDEX-IT_BW_SEL0_PLLB	
0x059B	7	R/W	HOLDEX-IT_STD_BO_PLLB	

Table 18.191. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NOHIST_PLLB	Set by CBPro.

Table 18.192. 0x059D

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEX-IT_BW0_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.193. 0x059E

Reg Address	Bit Field	Type	Setting Name	Description
0x059E	5:0	R/W	HOLDEX-IT_BW1_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.194. 0x059F

Reg Address	Bit Field	Type	Setting Name	Description
0x059F	5:0	R/W	HOLDEX-IT_BW2_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.195. 0x05A0

Reg Address	Bit Field	Type	Setting Name	Description
0x05A0	5:0	R/W	HOLDEX-IT_BW3_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.196. 0x05A1

Reg Address	Bit Field	Type	Setting Name	Description
0x05A1	5:0	R/W	HOLDEX-IT_BW4_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.197. 0x05A2

Reg Address	Bit Field	Type	Setting Name	Description
0x05A2	5:0	R/W	HOLDEX-IT_BW5_PLLB	Set by CBPro to set the PLL bandwidth when exiting holdover

Table 18.198. 0x05A4-0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Set by CBPro.
0x05A5	0	R/W	HSW_LIMIT_AC-TION_PLLB	Set by CBPro.

Table 18.199. 0x05A6

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE_PLLB	Size of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection
0x05A6	3	R/W	RAMP_SWITCH_EN_PLLB	Ramp Switching Enable 0: Disable Ramp Switching 1: Enable Ramp Switching (default)

Table 18.200. 0x05AC-0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLB	Set by CBPro.
0x05AD	15:0	R/W	OUT_MAX_LIM-IT_LMT_PLLB	Set by CBPro.
0x05B1	15:0	R/W	HOLD_SET-TLE_TAR-GET_PLLB	Set by CBPro.

18.7 Page 9 Registers Si5396C/D

Table 18.201. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Table 18.202. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit selects between 1.8 V and 3.3 V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3 V-tolerant. Setting this to the default 1.8 V is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I2C or SPI host is operating at 3.3 V and the Si5397/96 at VDD=1.8 V, the host must write IO_VDD_SEL=1. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 18.203. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See for more information.

When a clock is disabled, it is powered down.

Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 18.204. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 18.205. 0x094E-0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro

Reg Address	Bit Field	Type	Setting Name	Description
0x094F	7:4	R/W	IN_CMOS_USE1P8	0 = selects the Pulsed CMOS input buffer mode 1 = selects the LVCMOS input buffer mode

Table 18.206. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTEGER	Set by CBPro

18.8 Page A Registers Si5396C/D

Table 18.207. 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Name	Description
0x0A03	1:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 18.208. 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Name	Description
0x0A04	1:0	R/W	N_PIBYP	Bypass fractional divider for N[1:0]. 0: Fractional (or Integer) division - Recommended if changing settings during operation 1: Integer-only division - best phase noise - Recommended for Integer N values Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 18.209. 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	1:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0]

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

18.9 Page B Registers Si5396C/D

Table 18.210. 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 18.211. 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 18.212. 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 18.213. 0x0B45

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	Set by CBPro.
0x0B45	1	R/W	CLK_DIS_PLLB	Set by CBPro.

Table 18.214. 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Controls the clock to the digital LOS circuitry. Must be set to 0 to enable the LOS function of the respective Inputs (IN3 IN2 IN1 IN0).

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 18.215. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set by CBPro.

Table 18.216. 0x0B48

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set by CBPro.

Table 18.217. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 18.218. 0x0B4E Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B4E	7:0	R/W	RESERVED	Internal use for initilization. See CBPro.

Table 18.219. 0x0B57 VCO_RESET_CALCODE

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CALCODE	12-bit value. Controls the VCO frequency when a reset occurs.
0x0B58	11:8	R/W	VCO_RESET_CALCODE	

18.10 Page C Registers Si5396C/D

Table 18.220. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 18.221. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 18.222. 0x0C05

Reg Address	Bit Field	Type	Name	Description
0x0C05	0	R/W	IN_CLK_VAL_EN_PLLA	Set by CBPro

Table 18.223. 0x0C06

Reg Address	Bit Field	Type	Name	Description
0x0C06	7:0	R/W	IN_CLK_VAL_TIME_PLLA	Set by CBPro

Table 18.224. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN_PLLB	Set by CBPro

Table 18.225. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME_PLLB	Set by CBPro

19. Revision History

Revision 1.1

February 2021

- Updated descriptions and register info for the launch of the Si5396C/D/L/M 12 output dual PLL grades.
- Added information about the longer settling time on the crystal reference for internal reference devices

Revision 1.0
January 2020

- Fixed Error in Register 0x0004 Device Grade. The internal reference grades had a numerical error.
- Added Section 5.2.3 Use Case Scenario: Using More Than Two Inputs.

Revision 0.9

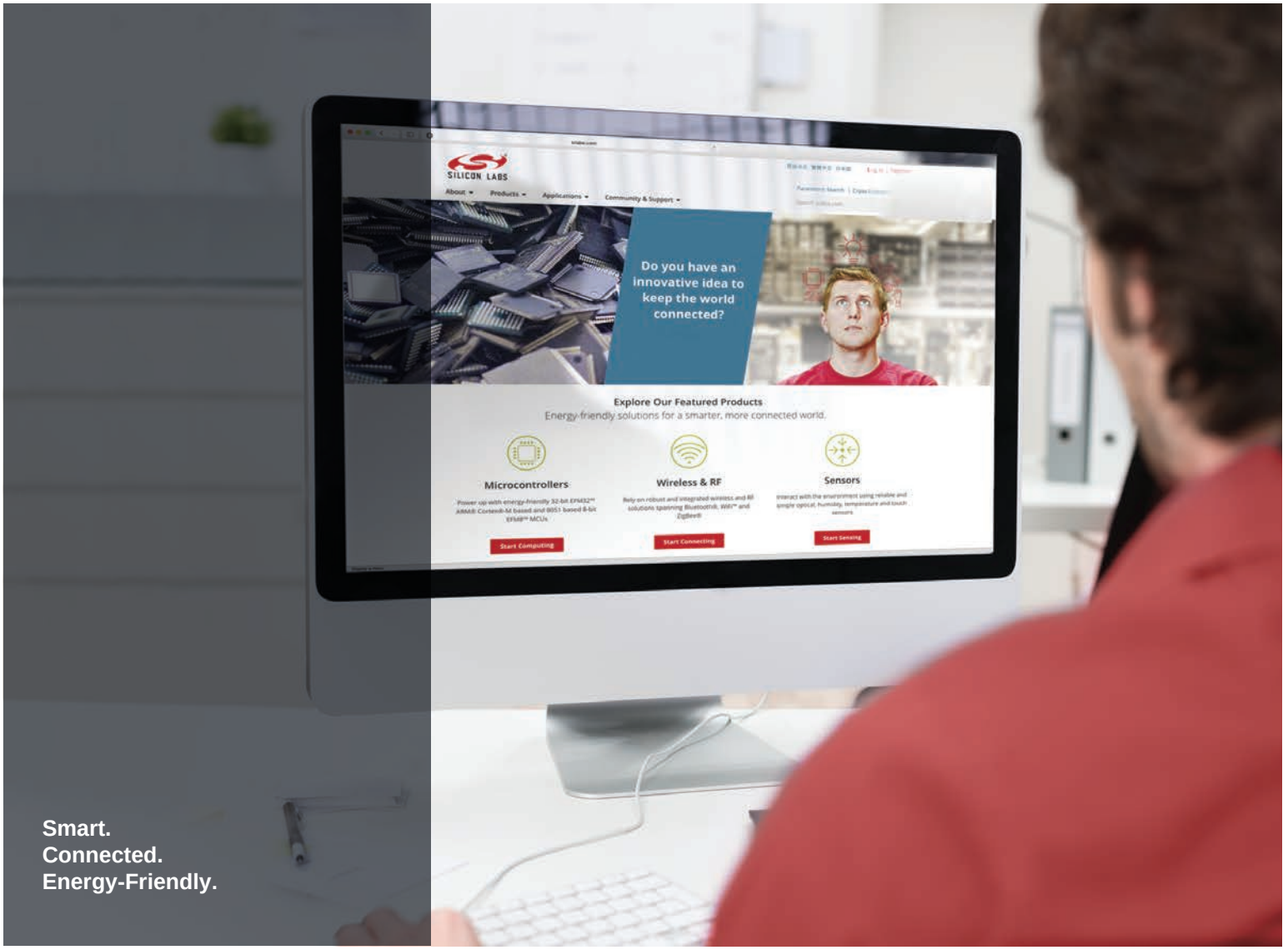
June 2019

- Updated CMOS input buffer section
- Added information for internal reference devices

Revision 0.1

June 2018

- Intitial Release



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com