A product Line of
Diodes Incorporated

**PI6CB33602**

# Very Low Power 6-Output PCIe Clock Buffer With On-Chip Termination

## Features

- 3.3V supply voltage
- HCSL input: 100MHz, also support 50MHz, 125MHz or 133.33MHz via SMBus
- 6 differential low power HCSL outputs with on-chip termination
- Default $Z_{OUT}$ = 85Ω
- Spread spectrum tolerant
- Individual output enable
- Programmable Slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Strapping pins or SMBus for configuration
- Differential output-to-output skew <50ps
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4/Gen5 CC compliant
  - PCIe Gen 2 and 3 SRiS and SRnS compliant
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

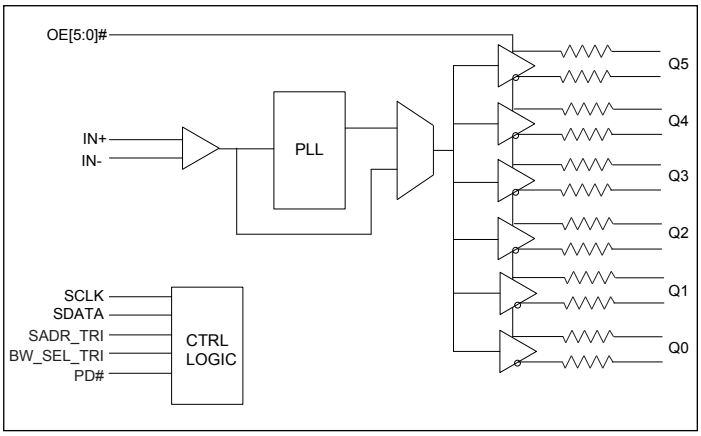
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green): 40-lead 5×5mm TQFN

## Description

The PI6CB33602 is a 6-output very low power PCIe Gen1/Gen2/Gen3/Gen4/Gen5 clock buffer. It takes a reference input to fanout six 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 24 external resistors and make layout easier. Individual OE pin for each output provides easier power management.

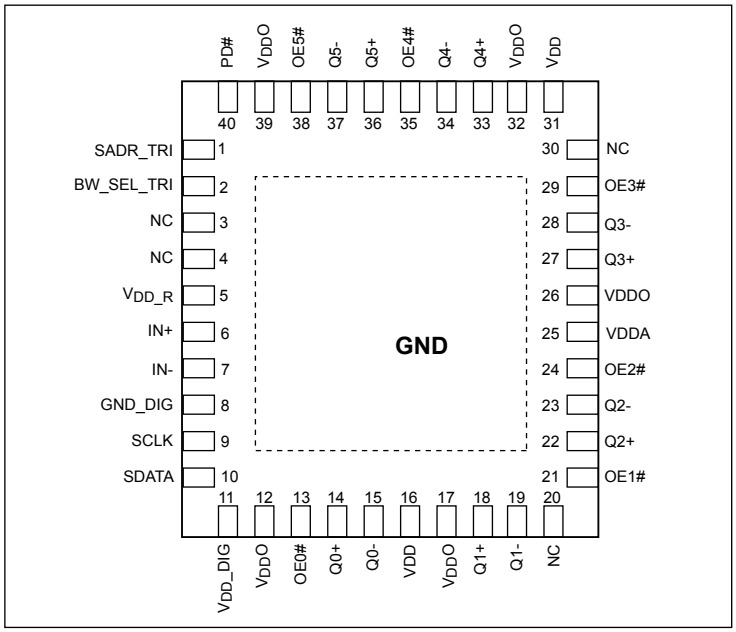
It uses Diodes proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4/Gen5 requirements. Other than PCIe 100MHz support, this device also support Ethernet application with 50MHz, 125MHz and 133.33MHz via SMBus. It provides various options such as different slew rate and amplitude through SMBUS so that users can configure the device easily to get the optimized performance for their individual boards.

## Block Diagram




**Notes:**
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration




## Pin Description

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 1 | SADR_TRI | Input | Tri-level | Latch to select SMBus Address. This pin has an internal pull-down |
| 2 | BW_SEL_TRI | Input | Tri-level | Latch to select low loop bandwidth, bypass PLL, and high loop bandwidth. This pin has both internal pull-up and pull-down |
| 3 | NC | | | Internal connected for feedback loop. Do not connect this pin |
| 4 | NC | | | Internal connected for feedback loop. Do not connect this pin |
| 5 | $V_{DD}$_R | Power | | Power supply for input differential buffers |
| 6 | IN+ | Input | | Differential true clock input |
| 7 | IN- | Input | | Differential complementary clock input |
| 8 | GND_DIG | Power | | Ground for digital circuitry |
| 9 | SCLK | Input | CMOS | SMBUS clock input, 3.3V tolerant |
| 10 | SDATA | Input/ Output | CMOS | SMBUS Data line, 3.3V tolerant |
| 11 | $V_{DD}$_DIG | Power | | Power supply for digital circuitry, nominal 3.3V |
| 12, 17, 26, 32, 39 | $V_{DDO}$ | Power | | Power supply for differential outputs |
| 13 | OE0# | Input | CMOS | Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 14 | Q0+ | Output | HCSL | Differential true clock output |
| 15 | Q0- | Output | HCSL | Differential complementary clock output |
| 16, 31 | $V_{DD}$ | Power | | Power supply, nominal 3.3V |
| 18 | Q1+ | Output | HCSL | Differential true clock output |

## Pin Description Cont.

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 19 | Q1- | Output | HCSL | Differential complementary clock output |
| 20 | NC | | | Do not connect this pin |
| 21 | OE1# | Input | CMOS | Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 22 | Q2+ | Output | HCSL | Differential true clock output |
| 23 | Q2- | Output | HCSL | Differential complementary clock output |
| 24 | OE2# | Input | CMOS | Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 25 | $V_{DDA}$ | Power | | Power supply for analog circuitry |
| 27 | Q3+ | Output | HCSL | Differential true clock output |
| 28 | Q3- | Output | HCSL | Differential complementary clock output |
| 29 | OE3# | Input | CMOS | Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 30 | NC | | | Do not connect this pin |
| 33 | Q4+ | Output | HCSL | Differential true clock output |
| 34 | Q4- | Output | HCSL | Differential complementary clock output |
| 35 | OE4# | Input | CMOS | Active low input for enabling Q4 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 36 | Q5+ | Output | HCSL | Differential true clock output |
| 37 | Q5- | Output | HCSL | Differential complementary clock output |
| 38 | OE5# | Input | CMOS | Active low input for enabling Q5 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 40 | PD# | Input | CMOS | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| | EPAD | Power | | Connect to Ground |

## SMBus Address Selection Table

| | SADR | Address | +Read/Write Bit |
|---|---|---|---|
| State of SADR on first application of PD# | 0 | 1101011 | X |
| | M | 1101100 | X |
| | 1 | 1101101 | X |

## Power Management Table

| PD# | IN | SMBus OE bit | OEn# | Qn+ | Qn- | PLL Status |
|---|---|---|---|---|---|---|
| 0 | X | X | X | Low(2) | Low(2) | Off |
| 1 | Running | 0 | X | Low(2) | Low(2) | On(1) |
| 1 | Running | 1 | 0 | Running | Running | On(1) |
| 1 | Running | 1 | 1 | Low(2) | Low(2) | On(1) |

**Note:**
1. If PLL Bypass mode is selected, the PLL will be off and outputs will be running.
2. The output state is set by B11[1:0] (Low/Low default)

## PLL Operating Mode Select Table

| BW_SEL_TRI | Operating Mode | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|---|---|---|---|
| 0 | PLL with low Bandwidth | 00 | 00 |
| M | PLL Bypass | 01 | 01 |
| 1 | PLL with high Bandwidth | 11 | 11 |

## Frequency Select table

| Freq. Select Byte 3 [4:3] | IN (MHz) | Qn (MHz) |
|---|---|---|
| 00 (default) | 100 | 100 |
| 01 | 50 | 50 |
| 10 | 125 | 125 |
| 11 | 133.33 | 133.33 |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, $V_{DDxx}$ .....–0.5V to +4.6V
Input Voltage ..... –0.5V to $V_{DD}$+0.5V, not exceed 4.6V
SMBus, Input High Voltage ..... 3.6V
ESD Protection (HBM) ..... 2000 V
Junction Temperature .....125 °C max

**Note:**
**Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

## Operating Conditions

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDA}$, $V_{DD}\_R$, $V_{DD}\_DIG$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Power Supply Voltage | | 0.95 | 1.05-3.3 | 3.465 | V |
| $I_{DDA}$ | Analog Power Supply Current | $V_{DDA}$, PLL mode, All outputs active @100MHz | | 21 | 25 | mA |
| $I_{DD}$ | Power Supply Current | $V_{DD}$ + $V_{DD\_DIG}$ + $V_{DD\_R}$, All outputs active @100MHz | | 34 | 40 | mA |
| $I_{DDO}$ | Power Supply Current for Outputs(2) | $V_{DDO}$, PLL mode, All outputs active @100MHz | | 22 | 27 | mA |
| $I_{DDA\_PD}$ | Analog Power Supply Power Down(1) Current | $V_{DDA}$, PLL mode, All outputs LOW/LOW | | 0.5 | 1 | mA |
| $I_{DD\_PD}$ | Power Supply Power Down(1) Current | $V_{DD}$ + $V_{DD\_DIG}$ + $V_{DD\_R}$, All outputs LOW/LOW | | 1 | 2 | mA |
| $I_{DDO\_PD}$ | Power Supply Current Power Down(1) for Outputs | $V_{DDO}$, All outputs LOW/LOW | | 0.04 | 0.1 | mA |
| $T_A$ | Ambient Temperature | Industrial grade | –40 | | 85 | °C |

**Note:**
1. Input clock is not running.
2. Outputs drive 5 inch trace.

## Input Electrical Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{pu}$ | Internal pull up resistance | | | 120 | | KΩ |
| $R_{dn}$ | Internal pull down resistance | | | 120 | | KΩ |
| $L_{PIN}$ | Pin inductance | | | | 7 | nH |

## SMBus Electrical Characteristics

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DDSMB}$ | Nominal bus voltage | | 2.7 | | 3.6 | V |
| $V_{IHSMB}$ | SMBus Input High Voltage | SMBus, $V_{DDSMB}$ = 3.3V | 2.1 | | 3.6 | V |
| | | SMBus, $V_{DDSMB}$ < 3.3V | 0.65 $V_{DDSMB}$ | | | |
| $V_{ILSMB}$ | SMBus Input Low Voltage | SMBus, $V_{DDSMB}$ = 3.3V | | | 0.8 | V |
| | | SMBus, $V_{DDSMB}$ < 3.3V | | | 0.8 | |
| $I_{SMBSINK}$ | SMBus sink current | SMBus, at $V_{OLSMB}$ | 4 | | | mA |
| $V_{OLSMB}$ | SMBus Output Low Voltage | SMBus, at $I_{SMBSINK}$ | | | 0.4 | V |
| $f_{MAXSMB}$ | SMBus operating frequency | Maximum frequency | | | 500 | kHz |
| $t_{RMSB}$ | SMBus rise time | (Max $V_{IL}$ - 0.15) to (Min $V_{IH}$ + 0.15) | | | 1000 | ns |
| $t_{FMSB}$ | SMBus fall time | (Min $V_{IH}$ + 0.15) to (Max $V_{IL}$ - 0.15) | | | 300 | ns |

## LVCMOS DC Electrical Characteristics

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | Single-ended inputs, except SMBus | 0.75 $V_{DD}$ | | $V_{DD}$ +0.3 | V |
| $V_{IM}$ | Input Mid Voltage | SADR_TRI, BW_SEL_TRI | 0.4$V_{DD}$ | 0.5$V_{DD}$ | 0.6$V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | Single-ended inputs, except SMBus | -0.3 | | 0.25 $V_{DD}$ | V |
| $I_{IH}$ | Input High Current | Single-ended inputs, $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | Single-ended inputs, $V_{IN}$ = 0V | -5 | | | µA |
| $I_{IH}$ | Input High Current | Single-ended inputs with pull up / pull down resistor, $V_{IN}$ = $V_{DD}$ | | | 50 | µA |
| $I_{IL}$ | Input Low Current | Single-ended inputs with pull up / pull down resistor, $V_{IN}$ = 0V | -50 | | | µA |
| $C_{IN}$ | Input Capacitance | | 1.5 | | 5 | pF |

## LVCMOS AC Electrical Characteristics

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{OELAT}$ | Output enable latency | Q start after OE# assertion<br>Q stop after OE# deassertion | 1 | | 3 | clocks |
| $t_{PDLAT}$ | PD# de-assertion | Differential outputs enable after PD# de-assertion | | 20 | 300 | us |

## HCSL Input Characteristics(1)

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IHDIF}$ | Diff. Input High Voltage(3) | IN+, IN-, single-end measurement | 600 | 800 | 1150 | mV |
| $V_{ILDIF}$ | Diff. Input Low Voltage(3) | IN+, IN-, single-end measurement | -300 | 0 | 300 | mV |
| $V_{COM}$ | Diff. Input Common Mode Voltage | | 150 | | 900 | mV |
| $V_{SWING}$ | Diff. Input Swing Voltage | Peak to peak value ($V_{IHDIF}$ - $V_{ILDIF}$) | 300 | | 2900 | mV |
| $f_{INBP}$ | Input Frequency | PLL Bypass mode | 1 | | 200 | MHz |
| $f_{IN100}$ | Input Frequency | 100MHz PLL | 99.9 | 100 | 100.1 | MHz |
| $f_{IN133}$ | Input Frequency | 133MHz PLL | 133.2 | 133.33 | 133.46 | MHz |
| $f_{IN125}$ | Input Frequency | 125MHz PLL | 124.87 | 125 | 125.12 | MHz |
| $f_{IN50}$ | Input Frequency | 50MHz PLL | 49.95 | 50 | 50.05 | MHz |
| $f_{MODI-PCIe}$ | Input SS Modulation Freq. PCIe | Allowable frequency for PCIe applications (Triangular Modulation) | 30 | | 33 | kHz |
| $f_{MODIN-non-PCIe}$ | Input SS Modulation Freq. non-PCIe | Allowable frequency for non-PCIe applications (Triangular Modulation) | 0 | | 46 | kHz |
| $t_{STAB}$ | Clock stabilization | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.75 | 1.0 | ms |
| $t_{RF}$ | Diff. Input Slew Rate(2) | Measured differentially | 0.4 | | | V/ns |
| $I_{IN}$ | Diff. Input Leakage Current | $V_{IN} = V_{DD}$, $V_{IN}$ = GND | -5 | 0.01 | 5 | uA |
| $t_{DC}$ | Diff. Input Duty Cycle | Measured differentially | 45 | | 55 | % |
| $tj_{c-c}$ | Diff. Input Cycle to cycle jitter | Measured differentially | | | 125 | ps |

**Note:**

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is ($V_{IH}$-$V_{IL}$)/2

## HCSL Output Characteristics

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage High(1) | Statistical measurement on single-ended signal using oscilloscope math function | 660 | 784 | 850 | mV |
| $V_{OL}$ | Output Voltage Low(1) | | -150 | | 150 | mV |
| $V_{OMAX}$ | Output Voltage Maximum(1) | Measurement on single ended signal using absolute value | | 816 | 1150 | mV |
| $V_{OMIN}$ | Output Voltage Minimum(1) | | -300 | -42 | | mV |
| $V_{OC}$ | Output Cross Voltage(1,2,4) | | 250 | 430 | 550 | mV |
| $DV_{OC}$ | $V_{OC}$ Magnitude Change(1,2,5) | | | 12 | 140 | mV |

**Note:**

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

## HCSL Output AC Characteristics

Temperature = $T_A$; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | 50 | 100 | 133.33 | MHz |
| BW | PLL bandwidth(1,8) | -3dB point in High Bandwidth Mode | 1.3 | 3.2 | 3.6 | MHz |
| | | -3dB point in Low Bandwidth Mode | 0.7 | 1.7 | 1.9 | MHz |
| $tj_{peak}$ | PLL Jitter Peaking(1) | Peak pass band gain | | 0.8 | 2 | dB |
| $t_{RF}$ | Slew rate(1,2,3) | Scope averaging on fast setting | 2.5 | 3.2 | 4.0 | V/ns |
| | | Scope averaging on slow setting | 2.2 | 3.0 | 3.7 | V/ns |
| $Dt_{RF}$ | Slew rate matching(1,2,4) | Scope averaging on | | 7 | 15 | % |
| $t_{SKEW}$ | Output Skew(1,2) | Averaging on, $V_T$ = 50% | | 21 | 50 | ps |
| $t_{PDELAY}$ | Propagation delay | PLL Bypass mode, $V_T$ = 50% | 2000 | 2500 | 3000 | ps |
| | | PLL mode, $V_T$ = 50% | -200 | 90 | 200 | ps |
| $t_{DC}$ | Duty Cycle(1,2) | Measured differentially, PLL Mode | 45 | 50 | 55 | % |
| $t_{DCD}$ | Duty Cycle Distortion(1,7) | Measured differentially, PLL Bypass Mode at 100MHz | -3.5 | 0 | 3.5 | % |
| $t_{DCD}$ | Duty Cycle Distortion(1,7) | Measured differentially, SE input, PLL Bypass Mode at 100MHz | -10 | 0 | 10 | % |
| $tj_{c-c}$ | Cycle to cycle jitter(1,2) | PLL mode | | 14 | 50 | ps |
| | | Additive jitter, Bypass mode | | 0.1 | 1 | ps |

## HCSL Output AC Characteristics (jitter)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Spec Limit | Units |
|---|---|---|---|---|---|---|---|
| $t_{jPHASEPLL}$ | Integrated phase jitter PLL mode (RMS)(1,5) | PCIe Gen 1(6) | | 25 | 35 | 86 | ps(p-p) |
| | | PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz | | 0.6 | 0.8 | 3 | ps |
| | | PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz) | | 0.7 | 1.2 | 3.1 | ps |
| | | PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz) | | 0.25 | 0.4 | 1 | ps |
| | | PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz) | | 0.25 | 0.4 | 0.5 | ps |
| | | PCIe Gen 5 (PLL BW of 500k to 1.8MHz. CDR =20MHz)(11) | | 0.07 | 0.12 | 0.15 | ps |
| | | 125MHz, 1.5MHz to 20MHz, -20dB/ decade Rollover < 1.5MHz, -40dB/de-cade rolloff > 10MHz | | 0.15 | 0.3 | | ps |
| | | 133.33MHz | | 0.15 | 0.3 | | ps |
| $t_{jPHASEA}$ | Additive Integrated phase jitter (RMS)(1,5,10) | PCIe Gen 1 | | 0.01 | 0.05 | | ps(p-p) |
| | | PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz | | 0.01 | 0.05 | | ps |
| | | PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz) | | 0.01 | 0.05 | | ps |
| | | PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz) | | 0.01 | 0.05 | | ps |
| | | PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz) | | 0.01 | 0.05 | | ps |
| | | PCIe Gen 5 (PLL BW of 500k to 1.8MHz. CDR =20MHz)(11) | | 0.01 | 0.05 | | ps |
| | | 125MHz, 1.5MHz to 20MHz, -20dB/ decade Rollover < 1.5MHz, -40dB/de-cade rolloff > 10MHz | | 0.01 | 0.05 | | ps |
| | | 133.33MHz | | 0.01 | 0.05 | | ps |
| | | 156.25MHz 12k to 20MHz | | 0.01 | 0.05 | | ps |

**Note:**

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. See http://www.pcisig.com for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of $10^{-12}$
7. Duty cycle distortion is the difference in duty cycle between the output and input clock when the device is operated in the PLL bypass mode
8. The Min and Max values of each BW setting track each other, low BW max will never occur with high BW min
9. Applies to all differential outputs
10. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)$^{*2}$ - (input jitter)$^{*2}$]
11. PCIe Gen 5 v0.9 specification

## SMBus Serial Data Interface

PI6CB33602 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | See SBMus Address Selection table | | | 1/0 |

Note: SMBus address is latched on SADR pin

### How to Write

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Add. | W(0) | Ack | Beginning Byte location = N | Ack | Data Byte count = X | Ack | Beginning Data Byte (N) | Ack | ..... | Data Byte (N+X-1) | Ack | Stop bit |

### How to Read

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Address | W(0) | Ack | Beginning Byte location = N | Ack | Repeat Start bit | Address | R(1) | Ack | Data Byte count = X | Ack | Beginning Data Byte (N) | Ack |

| | 8 bits | 1 bit | 1 bit |
|---|---|---|---|
| ..... | Data Byte (N+X-1) | NAck | Stop bit |

## Byte 0: Output Enable Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Q5_OE | Q5 output enable | RW | 1 | See B11[1:0] | Pin control |
| 6 | Q4_OE | Q4 output enable | RW | 1 | | |
| 5 | Reserved | | | 0 | | |
| 4 | Q3_OE | Q3 output enable | RW | 1 | | |
| 3 | Q2_OE | Q2 output enable | RW | 1 | | |
| 2 | Q1_OE | Q1 output enable | RW | 1 | | |
| 1 | Reserved | | | 0 | | |
| 0 | Q0_OE | Q0 output enable | RW | 1 | | |

**Note:**
1. A low on these bits will override the OE# pins and force the differential outputs to the state indicated by B11[1:0] (Low/Low default)

## Byte 1: PLL Operating Mode and Output Amplitude Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | PLLMODERB1 | PLL Mode Readback Bit1 | R | Latch | See PLL Operating Mode Table | |
| 6 | PLLMODERB0 | PLL Mode Readback Bit0 | R | Latch | | |
| 5 | PLLMODE_SWCTR | Enable SW control of PLL Mode | RW | 0 | Values in B1[7:6] set PLL Mode | Values in B1[4:3] set PLL Mode |
| 4 | PLLMODE1 | PLL Mode control Bit1 | RW(1) | 0 | See PLL Operating Mode Table | |
| 3 | PLLMODE0 | PLL Mode control Bit0 | RW(1) | 0 | | |
| 2 | Reserved | | | 1 | | |
| 1 | Amplitude1 | Control output amplitude | RW | 1 | '00' = 0.6V, '01' = 0.68V, '10' = 0.75V, '11' = 0.85V | |
| 0 | Amplitude0 | | RW | 0 | | |

**Note:**
1. B1[5] must be set to a 1 for these bits to have any effect on the part

## Byte 2: Differential Output Slew Rate Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | SLEWRATECTR_Q5 | Control slew rate of Q5 | RW | 1 | Slow setting | Fast setting |
| 6 | SLEWRATECTR_Q4 | Control slew rate of Q4 | RW | 1 | Slow setting | Fast setting |
| 5 | Reserved | | | 1 | | |
| 4 | SLEWRATECTR_Q3 | Control slew rate of Q3 | RW | 1 | Slow setting | Fast setting |
| 3 | SLEWRATECTR_Q2 | Control slew rate of Q2 | RW | 1 | Slow setting | Fast setting |
| 2 | SLEWRATECTR_Q1 | Control slew rate of Q1 | RW | 1 | Slow setting | Fast setting |
| 1 | Reserved | | | 1 | | |
| 0 | SLEWRATECTR_Q0 | Control slew rate of Q0 | RW | 1 | Slow setting | Fast setting |

## Byte 3: Frequency Select Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | 1 | | |
| 6 | Reserved | | | 1 | | |
| 5 | FREQ_SEL_EN | Enable SW selection of frequency | RW | 0 | SW Freq. selection disabled | SW Freq. selection enabled |
| 4 | FSEL1 | Freq. Select Bit 1 | RW(1) | 0 | See Frequency Select Table | |
| 3 | FSEL0 | Freq. Select Bit 0 | RW(1) | 0 | | |
| 2 | Reserved | | | 1 | | |
| 1 | Reserved | | | 1 | | |
| 0 | SLEWRATESEL FB | Adjust Slew Rate of Feedback signal | RW | 1 | Slow setting | Fast setting |

**Note:**
1. B3[5] must be set to a 1 for these bits to have any effect on the part

## Byte 4: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:0 | Reserved | | | 1 | | |

## Byte 5: Revision and Vendor ID Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | RID3 | Revision ID | R | 0 | rev = 0000 | |
| 6 | RID2 | | R | 0 | | |
| 5 | RID1 | | R | 0 | | |
| 4 | RID0 | | R | 0 | | |
| 3 | PVID3 | Vendor ID | R | 0 | Diodes = 0011 | |
| 2 | PVID2 | | R | 0 | | |
| 1 | PVID1 | | R | 1 | | |
| 0 | PVID0 | | R | 1 | | |

## Byte 6: Device Type/Device ID Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | DTYPE1 | Device type | RW | 0 | '00' = CG, '01' = ZDB, | |
| 6 | DTYPE0 | | RW | 1 | '10' = Reserve, '11' = ZDB | |
| 5 | DID5 | Device ID | RW | 0 | 000110 binary, 06Hex | |
| 4 | DID4 | | RW | 0 | | |
| 3 | DID3 | | RW | 0 | | |
| 2 | DID2 | | RW | 1 | | |
| 1 | DID1 | | RW | 1 | | |
| 0 | DID0 | | RW | 0 | | |

## Byte 7: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:0 | Reserved | | | 0x08 | | |

## Byte 8 and 9: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:0 | Reserved | | | B8 = 0x36<br>B9 = 0x00 | | |

## Byte 10: PD Restore

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | RW | 1 | | |
| 6 | PD Restore | PD Restore to default configuration | RW | 1 | Clear PD Config | Keep PD Config |
| 5:0 | Reserved | | R | 0 | | |

## Byte 11: Stop Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | FB_imp[1] | Feedback Zout | RW | 0 | 00=Reserved | 10=100 DIF Zout |
| 6 | FB_imp[0] | | RW | 1 | 01=85 DIF Zout | 11 = Reserved |
| 5:2 | Reserved | | | 0 | | |
| 1 | STP1 | True/ Compliment DIF Output Disable Sate | RW | 0 | 00= Low/Low | 10= High/ Low |
| 0 | STP0 | | RW | 0 | 01= HiZ/HiZ | 11= Low/High |

## Byte 12: Impedance Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Q2_Zout1 | Q2 Zout | RW | 01 | 00 = Reserved<br>01 = 85Ω<br>10 = 100Ω<br>11 = Reserved | |
| 6 | Q2_Zout0 | Q2 Zout | RW | | | |
| 5 | Q1_Zout1 | Q1 Zout | RW | | | |
| 4 | Q1_Zout0 | Q1 Zout | RW | | | |
| 3 | Reserved | | RW | | | |
| 2 | Reserved | | RW | | | |
| 1 | Q0_Zout1 | Q0 Zout | RW | | | |
| 0 | Q0_Zout0 | Q0 Zout | RW | | | |

## Byte 13: Impedance Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Q5_Zout1 | Q5 Zout | RW | 01 | 00 = Reserved<br>01 = 85Ω<br>10 = 100Ω<br>11 = Reserved | |
| 6 | Q5_Zout0 | Q5 Zout | RW | | | |
| 5 | Q4_Zout1 | Q4 Zout | RW | | | |
| 4 | Q4_Zout0 | Q4 Zout | RW | | | |
| 3 | Reserved | | RW | | | |
| 2 | Reserved | | RW | | | |
| 1 | Q3_Zout1 | Q3 Zout | RW | | | |
| 0 | Q3_Zout0 | Q3 Zout | RW | | | |

## Byte 14: OE Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | OE2_term1 | OE2 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 6 | OE2_term0 | OE2 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 5 | OE1_term1 | OE1 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 4 | OE1_term0 | OE1 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 3 | Reserved | | | 0 | | |
| 2 | Reserved | | | 1 | | |
| 1 | OE0_term1 | OE0 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 0 | OE0_term0 | OE0 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |

## Byte 15: OE Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | OE5_term1 | OE5 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 6 | OE5_term0 | OE5 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 5 | OE4_term1 | OE4 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 4 | OE4_term0 | OE4 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 3 | Reserved | | | 0 | | |
| 2 | Reserved | | | 1 | | |
| 1 | OE3_term1 | OE3 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 0 | OE3_term0 | OE3 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |

## Byte 16: Power Good Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:2 | Reserved | | | 0x00 | | |
| 1 | PWRGD_PD1 | Clock Power Good and Power Down Pull up or Pull down | RW | 1 | 00=None | 10= Pullup |
| 0 | PWRGD_PD0 | | RW | 0 | 01=Pulldown | 11=Pullup and Down |

## Byte 17: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:0 | Reserved | | | 0 | | |

## Byte 18: Enable Pin Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | OE5_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 6 | OE4_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 5 | Reserved | | | 0 | | |
| 4 | OE3_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 3 | OE2_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 2 | OE1_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 1 | Reserved | | | 0 | | |
| 0 | OE0_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |

## Byte 19: Power Down Pin Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7:1 | Reserved | | | 0 | | |
| 0 | PWRGD_PD | PWRGD_PD Active via Pull up or Pull down | RW | 0 | Power Down = Low | Power Down = High |

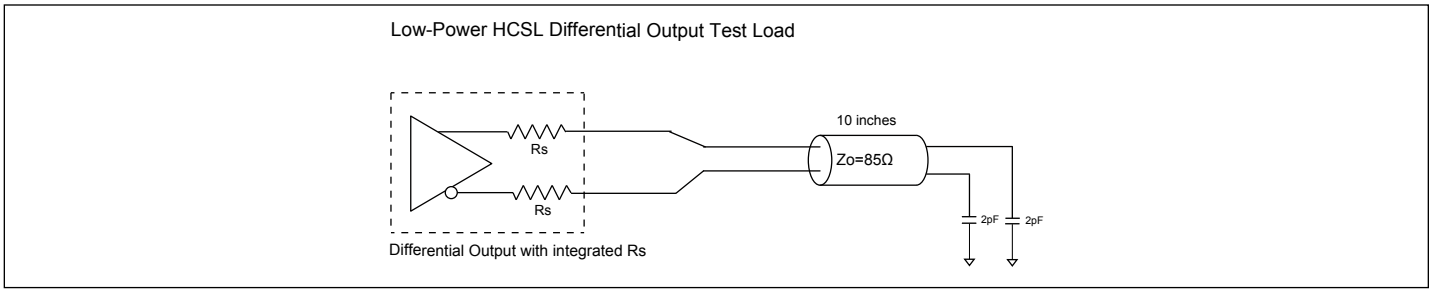



**Figure 1. Low Power HCSL Test Circuit**

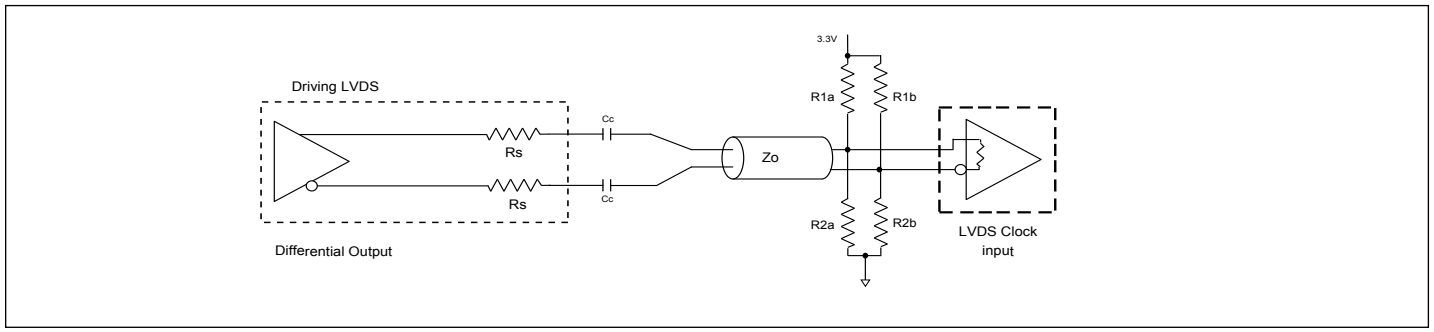



**Figure 2. Differential Output driving LVDS**

## Alternate Differential Output Terminations ($Z_O$ =85Ω)

| Component | Receiver with termination | Receiver without termination | Unit |
|---|---|---|---|
| $R_{1a}$, $R_{1b}$ | 10,000 | 130 | Ω |
| $R_{2a}$, $R_{2b}$ | 5,600 | 64 | Ω |
| $C_C$ | 0.1 | 0.1 | µF |
| $V_{CM}$ | 1.2 | 1.2 | V |

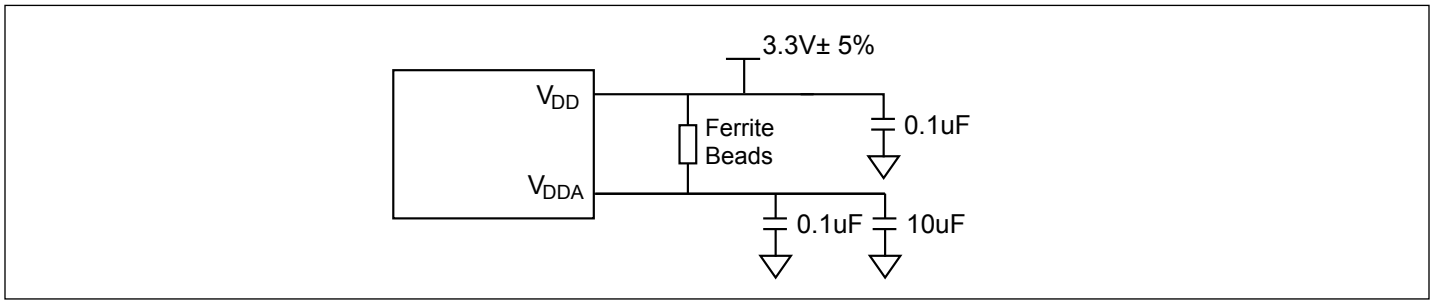
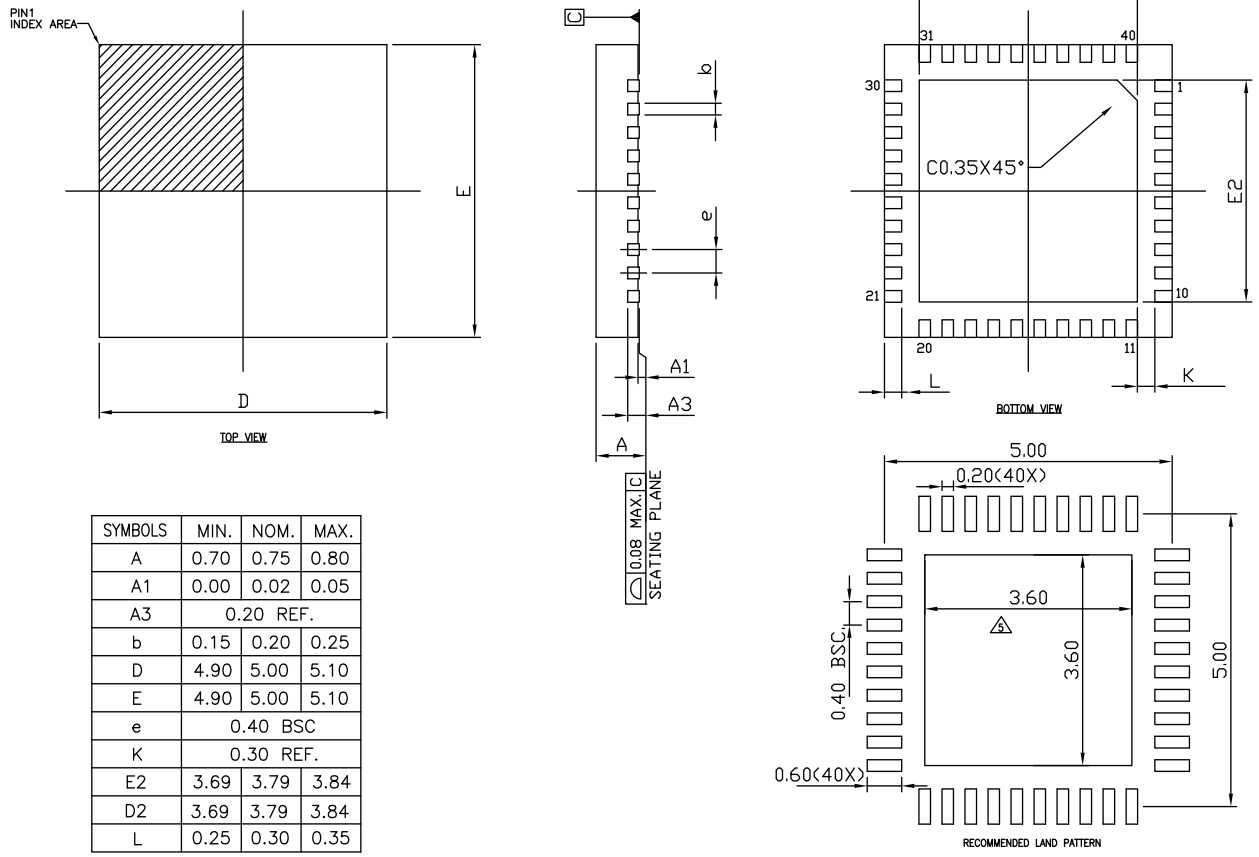



**Figure 3. Power Supply Filter**

## Part Marking


YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

## Packaging Mechanical: 40-TQFN (ZLA)




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| e | | 0.40 BSC | |
| K | | 0.30 REF. | |
| E2 | 3.69 | 3.79 | 3.84 |
| D2 | 3.69 | 3.79 | 3.84 |
| L | 0.25 | 0.30 | 0.35 |

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 03/14/15

DESCRIPTION: 40-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLA (ZLA40)

DOCUMENT CONTROL #: PD-2195 REVISION: --

15-0019

**For latest package info.**

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Ordering Information

| Ordering Code | Package Code | Package Description | Pin 1 Location |
|---|---|---|---|
| PI6CB33602ZLAIEX | ZLA | 40-Contact, Very Thin Quad Flat No-Lead (TQFN) | Top Right Corner |
| PI6CB33602ZLAIEX-13R | ZLA | 40-Contact, Very Thin Quad Flat No-Lead (TQFN) | Top Left Corner |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
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