AN2701

Digital Signal Processing Performance of the 8-bit AVR® Core

Introduction

Author: Lloyd D. Clark, Ph.D., Microchip Technology Inc.

The 8-bit AVR® microcontroller core can execute more than 100 distinct instructions, many of them in a single clock cycle. Modern implementations of the AVR® core (megaAVR® devices, as well as tinyAVR® 0- and 1-series devices) include a 2-cycle hardware multiplier. However, it is not always clear how raw processing power translates into application performance in the real world, especially when the effects of writing and compiling code in a high-level language are included. This white paper considers some digital signal processing (DSP) applications of the AVR® core and provides numbers for how much processor utilization they require. These applications use the on-chip analog-to-digital converter (ADC) to periodically sample an incoming analog signal and use the AVR® core to perform processing of the digitized signal. This means that the application must run in real-time and keep up with the incoming sample rate. The application code is written in C except for some assembly-language 16-bit by 16-bit multiplication functions that are called from C.

Table of Contents

1. Relevant Devices

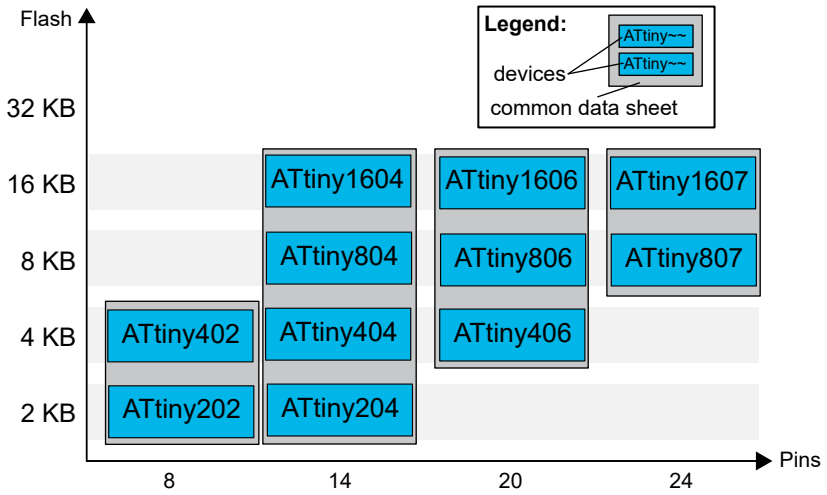
This chapter lists the relevant devices for this document.

1.1 tinyAVR® 0-series

The figure below shows the tinyAVR® 0-series, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin- and feature compatible.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

Figure 1-1. tinyAVR® 0-series Overview



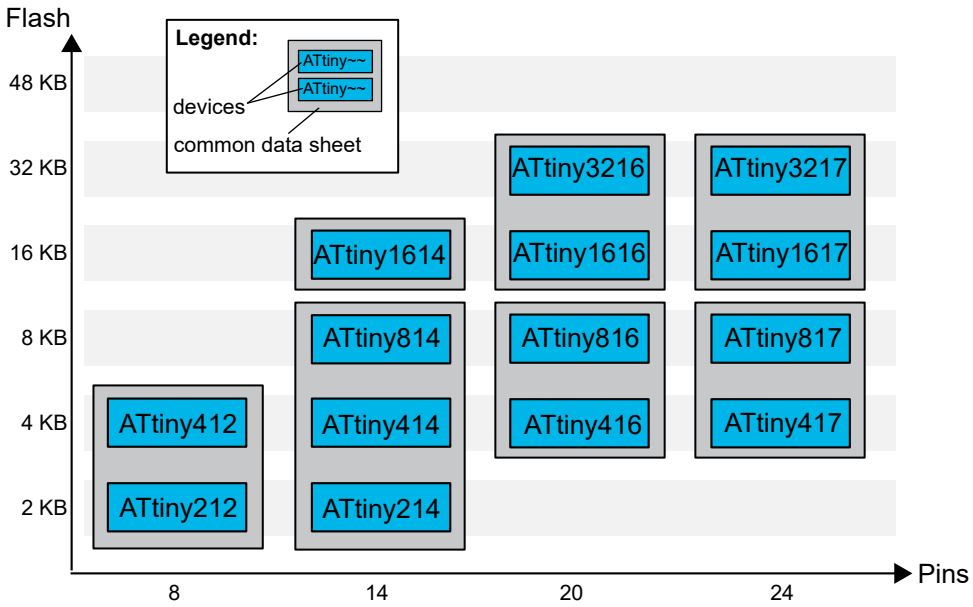
Devices with different Flash memory size typically also have different SRAM and EEPROM.

1.2 tinyAVR® 1-series

The figure below shows the tinyAVR® 1-series devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin compatible and provide the same or more features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

Figure 1-2. tinyAVR® 1-series Overview



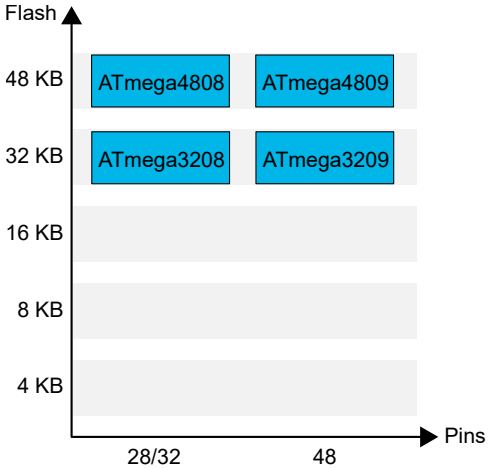
Devices with different Flash memory size typically also have different SRAM and EEPROM.

1.3 megaAVR® 0-series

The figure below shows the megaAVR® 0-series devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

Figure 1-3. megaAVR® 0-series Overview



Devices with different Flash memory size typically also have different SRAM and EEPROM.

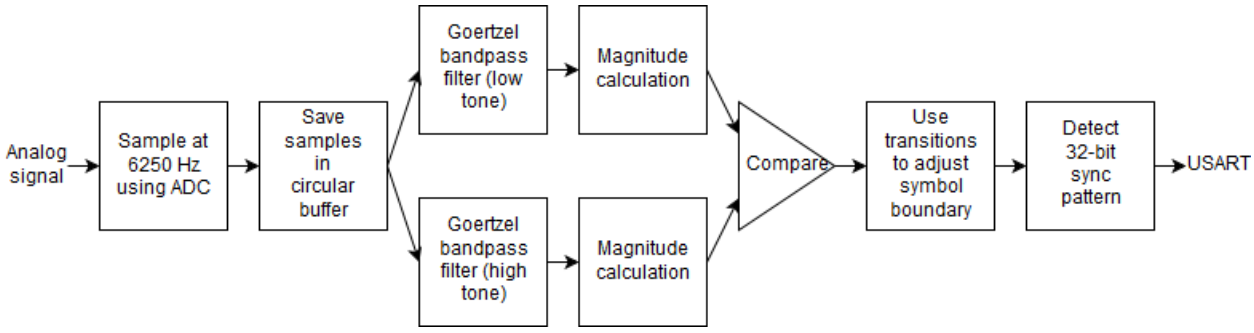
2. Audio Frequency Shift Keying Demodulator

The first application to be considered is an audio frequency shift keying (AFSK) demodulator for the Specific Area Message Encoding (SAME) protocol, running on the AVR® ATmega328P microcontroller. A detailed explanation of the protocol and demodulator design, as well as third-party C source code that was used as a starting point, can be found at the following URL: http://swfltek.com/avr/SAME/

In the SAME AFSK protocol, bits are transmitted with a duration of 1.92 milliseconds, and therefore a bit rate of 520.83 bits/second. Logic level zero is represented by three cycles of a 1562.5 Hz audio tone, and logic level one is represented by four cycles of a 2083.3 Hz audio tone. A 16-byte preamble is sent at the beginning of a transmission to allow the receiver to easily find the boundaries between bits before data transmission begins.

Although the demodulator was originally implemented on an ATmega328P device running at a clock frequency of 16 MHz, it could be easily adapted to other AVR® devices. The timer/counter and ADC on the device are set up to sample the incoming audio signal at four times the logic level zero frequency and three times the logic level one frequency, or 6250 Hz. This means that there are (16 MHz/6250 Hz) = 2560 CPU cycles available to process each ADC sample. A block diagram of the demodulator is provided in the figure below.

Figure 2-1. Demodulator Block Diagram



Each time a new ADC sample is received, it is added to a circular buffer of the most recent 12 ADC samples. Two digital Goertzel bandpass filters, one centered on the logic level zero frequency and the other centered on the logic level one frequency, are then run on the most recent 12 ADC samples, followed by an output magnitude calculation for each filter. The output magnitudes of the two filters are compared to determine whether the received signal represents a logic level zero or logic level one. Some additional processing is performed to find the bit transitions of the preamble and synchronize to them. After synchronization is achieved, demodulated ASCII characters are output to a USART.

AVR® core performance was determined by building the C source code using Atmel Studio 7.0.1645 and running it on an ATmega328P Xplained Mini evaluation kit. Some minor modifications were made to the code to include some calculations for measuring processor utilization, and to make it more tolerant of frequency errors in the transmitter. (The modified code, as well as all code used in the later sections of this document, can be found in the *FSK_demod_code_for_AVR_core.zip* file associated with this white paper at the Microchip website.) In the worst case, it was found that 749 CPU clock cycles are needed for obtaining and processing an ADC sample. This number includes all the filtering and synchronization operations as well as transmitting demodulated characters out on a USART. Given that there are 2560 CPU cycles per ADC sample, this is a core utilization of (749/2560)*100% = 29.3%.

There are several different ways of interpreting this result. This means that approximately 70% of the AVR® core processing power is still available if it is desired to add additional functionality to the

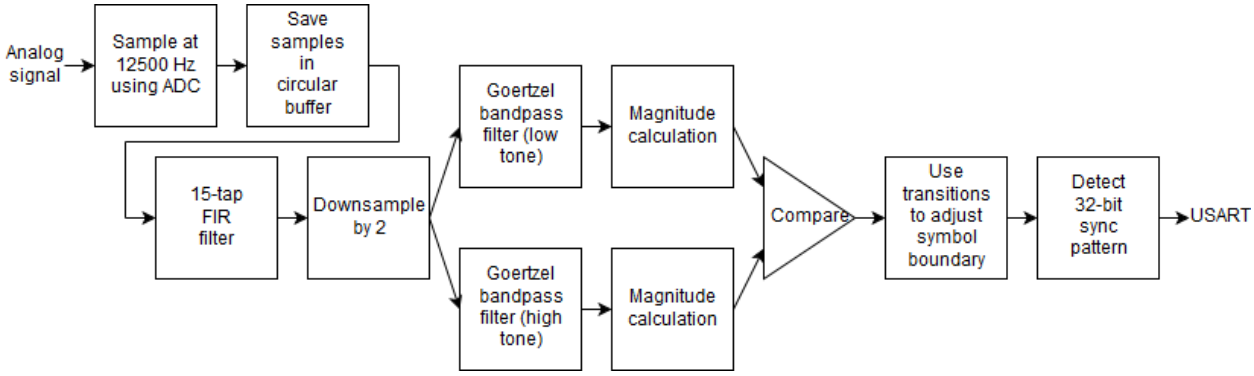
application. Another interpretation is that the CPU clock frequency could be reduced from 16 MHz to 4.8 MHz to reduce power consumption without compromising the functionality of the AFSK demodulator. Yet another interpretation is that the AFSK bit rate, audio frequency, and ADC sample rate parameters could be scaled by a factor of up to 3.4 to achieve bit rates of up to 1.77 kbit/second if the CPU clock remains at 16 MHz.

3. AFSK Demodulator with 2x Sampling Rate and Digital Filtering

The AFSK demodulator discussed in the previous section did not have any digital filtering to prevent aliasing of frequencies above half the sample rate (0.5*6250 Hz = 3125 Hz). For example, imagine that there is an interference tone on the incoming analog signal at a frequency of 4687.5 Hz. Because the sampling rate is 6250 Hz, once the 4687.5 Hz analog tone is sampled it would appear in the digital domain at an aliased frequency of (6250-4687.5) Hz = 1562.5 Hz. Since this is the same frequency as the FSK logic level zero signal, it would interfere with the FSK demodulator and prevent it from functioning properly. To prevent this interference, the only option with the previous demodulator code would have been to add a hardware analog filter prior to the ADC input to attenuate signal frequencies above 3125 Hz.

An alternative approach is to sample the analog signal at a higher rate, perform some digital filtering to attenuate frequencies above 3125 Hz, then downsample the signal. The downsampled signal can then be demodulated as before. The AFSK demodulator code described in the previous section was taken as a starting point and then modified to use this approach. A block diagram of this modified demodulator is provided in the figure below.

Figure 3-1. Demodulator Block Diagram



The modified code uses the ADC to sample the incoming analog signal at 12500 Hz, twice the previous sampling rate of 6250 Hz. The 12500 Hz samples are passed through a 15-tap FIR (Finite Impulse Response) filter that is designed to have greater than 44 dB attenuation beyond a cutoff frequency of 3125 Hz. The FIR filter taps are implemented with 10-bit precision, and the ADC values have 10-bit resolution, so 16-bit by 16-bit multiplication operations are used in the implementation of the FIR filter. The output of the FIR filter is downsampled by a factor of 2 to create a signal at the original sample rate of 6250 Hz, and then this is fed into the original FSK demodulator code designed for a 6250 Hz sample rate.

Consider what happens now with an interfering sine-wave signal at 4687.5 Hz. Because it is sampled at 12500 Hz, it will not be aliased – it will appear at 4687.5 Hz in the sampled version of the signal. Because the FIR filter has greater than 44 dB attenuation at frequencies above 3125 Hz, the interference signal will be reduced to less than 1% of its original amplitude at the output of the FIR filter. After the signal is downsampled to 6250 Hz, aliasing will then occur and the signal will appear at 1562.5 Hz, but it has been reduced in amplitude so much that it will have a negligible effect on the FSK demodulator performance.

Doubling the sample rate to 12500 Hz with a 16 MHz AVR® core clock means that there are now (16 MHz/12500 Hz) = 1280 CPU cycles available per ADC sample. CPU utilization of this code was found to be at most 792 samples per ADC sample, for an AVR® core utilization of (792/1280)*100% = 62%.

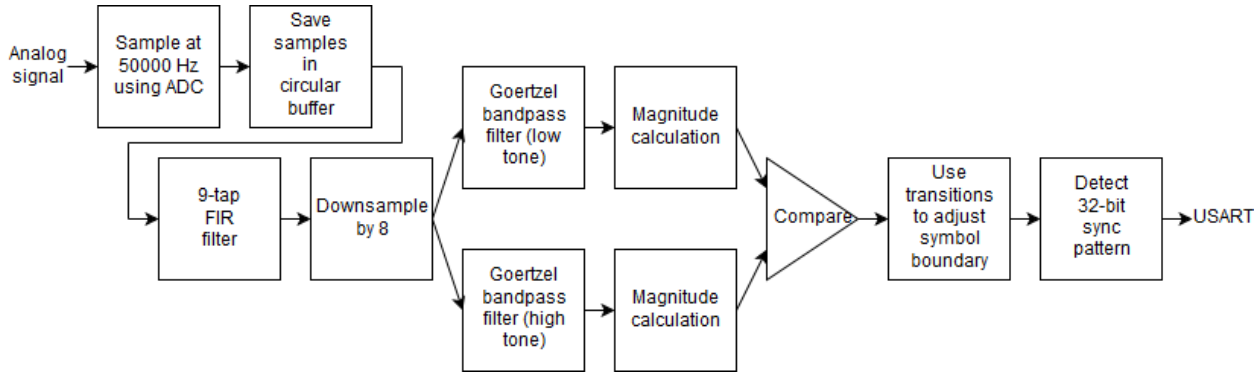
As before, this number can be interpreted in various ways. It means that 38% of the core is still available for adding functionality to the application. Another interpretation is that the CPU clock frequency can be reduced from 16 MHz to 10 MHz without compromising the demodulator performance. Yet another interpretation is that the AFSK bit rate, audio frequency, and ADC sample rate parameters could be scaled by a factor of up to 1.6 to achieve FSK bit rates of up to 833 bit/second if the CPU clock remains at 16 MHz.

4. Near-Ultrasonic FSK Demodulator with 8x Sampling Rate and Digital Filtering

The application code was further modified to demodulate a more challenging FSK signal – still with a bit duration of 1.92 milliseconds, but with near-ultrasonic frequencies of 16666.7 Hz for logic level one and 17187.5 Hz for logic level zero. This corresponds to exactly 32 or 33 cycles of a sine-wave during the 1.92 millisecond bit interval.

For this application, the timer/counter and ADC on the device are set up to sample the analog signal at a frequency of 50 kHz. A block diagram of this demodulator is provided in the figure below.

Figure 4-1. Demodulator Block Diagram



An interrupt service routine saves incoming ADC samples in a circular buffer so that they can be processed by a main processing loop. In the main processing loop, the 50 kHz samples are passed through a 9-tap FIR filter that is designed to have greater than 40 dB attenuation below 10 kHz so that typical human voice frequencies are removed from the signal. The FIR filter taps are implemented with 10-bit precision, and the ADC values have 10-bit resolution, so 16-bit by 16-bit multiplication operations are used in the implementation of the FIR filter.

The output of the FIR filter is downsampled by a factor of 8 to result in a signal sampled at 6250 Hz. The near-ultrasonic frequencies of 16666.7 Hz and 17187.5 Hz are aliased to (3*6250 – 16666.7) Hz and (3*6250 – 17187.5) Hz, or 2083.3 Hz and 1562.5 Hz in the downsampled signal, respectively. This means that the original FSK demodulator code can still be used from this point onward.

Given that the core is running at 16 MHz, this means that there are 320 CPU cycles per 50 kHz ADC sample interval and 2560 CPU cycles per 6250 Hz downsample interval. Processor utilization was determined to be as follows:

- Interrupt service routine: 65 cycles per 50 kHz sample = (65/320)*100% = 20.3% CPU utilization
- 9-tap FIR filter & overhead: 468 cycles per 6250 Hz downsample = (468/2560)*100% = 18.3% CPU utilization
- FSK demodulator (including USART sending): 718 cycles per 6250 Hz downsample = (718/2560)*100% = 28.0% CPU utilization

Total CPU utilization is then 20.3% + 18.3% + 28.0% = 66.6%, so about one-third of the CPU is still available for other processing if desired. Alternatively, the processor clock could be reduced from 16 MHz to 10.7 MHz without affecting the demodulator. If the processor clock remains at 16 MHz, FSK bit rates and frequencies could be scaled proportionally by a factor of up to 1.5.

5. Conclusion

The AVR® core utilization results are summarized in the table below. A column for a CPU clock of 20 MHz is also provided since many AVR® devices have this clock speed as an upper limit.

Table 5-1. AVR Core Utilization Results

Demodulator Type	ADC Sample Rate	FIR Filter Taps	Downsampling Factor	AVR® Core Utilization (16 MHz Clock)	AVR® Core Utilization (20 MHz Clock)
AFSK	6250 Hz	-	1	29.3%	23.4%
AFSK with additional filtering	12500 Hz	15	2	61.9%	49.5%
Near-ultrasonic FSK	50000 Hz	9	8	66.6%	53.3%

These results confirm that the 8-bit AVR® core is capable of high levels of performance, even when the application requires some digital signal processing and is written in a high-level language. Next time you're evaluating microcontrollers for a project that involves sampling an analog signal with an ADC and performing some processing of that signal, consider prototyping it on an 8-bit AVR® microcontroller. Its performance, coupled with its low-power consumption and low cost, may surprise you.

6. Revision History

Doc. Rev.	Date	Comments
B	09/2018	Changed the document title and some figures are updated
A	05/2018	Initial document release.

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at http://www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN: 978-1-5224-3489-4

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-67-3636 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820