Alveo UL3422 Ultra Low Latency Trading Data Sheet

DS1016 (v1.0) October 14, 2024 **Product Specification**

Summary

The AMD Alveo™ UL3422 card, shown below, is designed for ultra low latency applications for the fintech market. It consists of an AMD UltraScale+™ device with ultra-low latency GTF transceivers and DDR memory. There are two QSFP-DD NIC ports supporting 16 GTF TX/RX pairs along with high-speed expansion connectors supporting 16 additional GTF TX/RX pairs.

The UL3422 is a full height, ½ length, single slot PCIe® CEM 4.0 compliant card which supports passive cooling for closed-loop thermal control in the server PCIe expansion slot. It has a PCIe x16 physical connector with the upper eight lanes unconnected.

Figure 1: **UL3422 Card**

Designs can be developed with the AMD Vivado™ Design Suite where the full resources of the programmable logic device are made available for development.

Product Details

The following table lists high-level product details for the UL3422 card.

Table 1: **Alveo UL3422 Product Details**

Specification	UL3422
Product SKU	A-UL3422-P16G-PQ-G
Total electrical card load	180W
Thermal design power (TDP)	120W
Thermal cooling solution	Passive
Weight	561.5g
Form factor	Full-height, ½ length, single slot
Network interface	Two QSFP-DD
PCIe interface	PCIe Gen4 x8[1]
Expansion ports	Two ARF6 + one PicoClasp for sideband
DDR4	16 GB 64b + 8b ECC at 2400 MT/s
1 PPS	• 1PPS IN Port • 1PPS OUT Port
Qualified for deployment	Yes
Vivado tools part number	XCVU2P-FSVJ2104-3-E
Card management	External SC MSP432P4011IRGCT
Power management	Power management with power management bus (PMBus) for voltage, current, and temperature monitoring including telemetry for major regulators
External power source (optional)	12V PCIe AUX 2x4
ADK2 Enabled	Yes
Configuration option	• 2 Gbit QSPI • JTAG over Micro-USB or ADK2
Debug interface	• UARTs over Micro-USB • PMBus, SMBus over ADK2 Debug Connector
Card security	None

Notes:

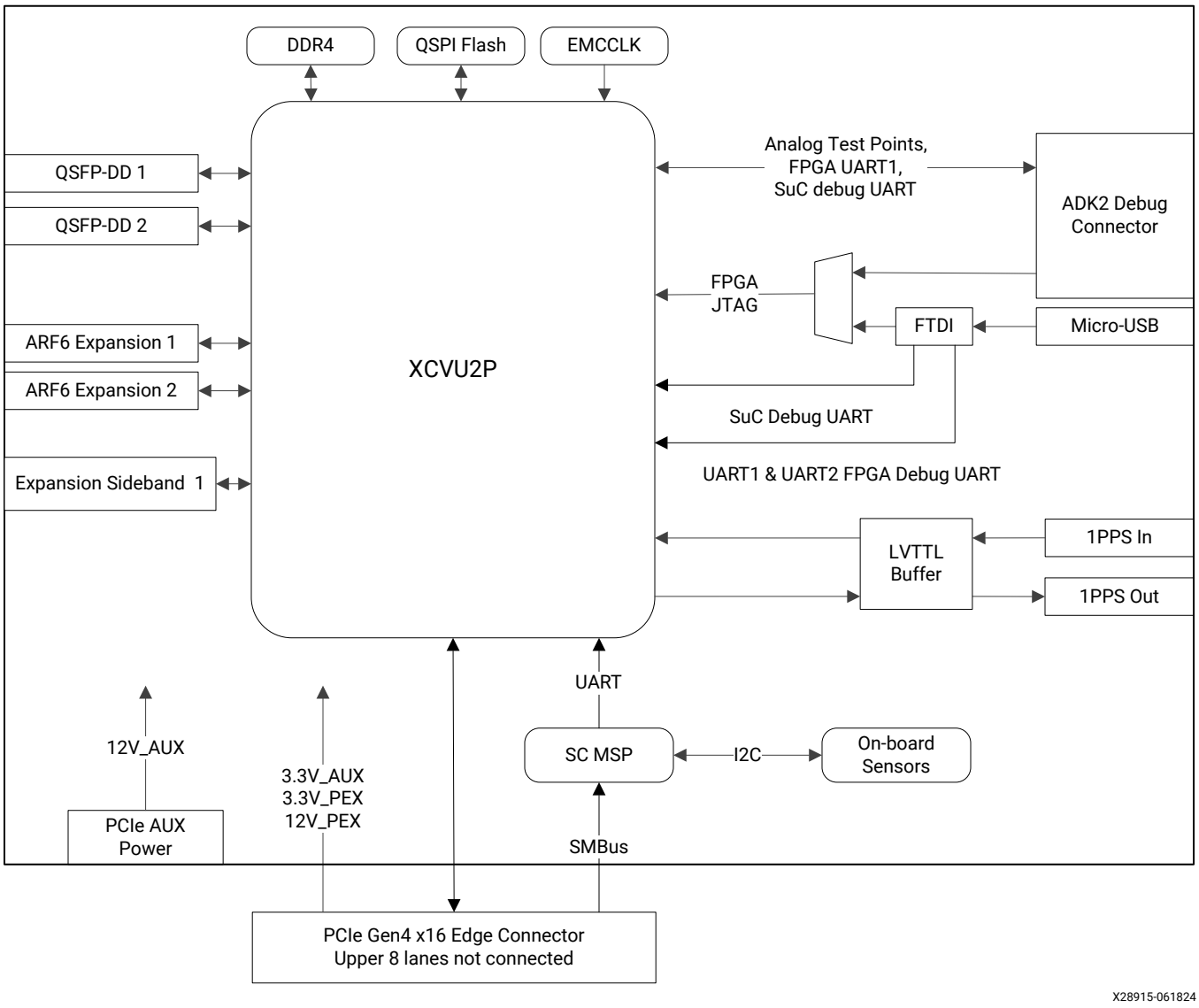
1. The UL3422 is PCIe Gen4 compatible but not compliant. See *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

Card Specifications

Block Diagram

The high-level block diagram for the UL3422 card is given in the following figure.

Figure 2: **UL3422 High-Level Block Diagram**



Card Interfaces

The Alveo UL3422 card is available in a passive cooling configuration and is designed for installation into a data center server where controlled air flow provides direct cooling to the card. The following figure shows the Alveo UL3422 card, highlighting the following interfaces:

- A PCIe card connector
- Two QSFP-DD NIC ports supporting 16 GTF TX/RX lanes
- Two ARF6 connectors supporting 16 GTF TX/RX lanes
- Micro-USB maintenance connector
- ADK2 debug connector
- PCIe AUX power connector

Figure 3: **UL3422 Card Interfaces**

Note: Block diagrams, register maps, and the XDC file reference the QSFP-DD ports as QSFP-DD1 and QSFP-DD2. These references map to the card QSFP-DD labeling Port #1 and Port #2, see Network Port Labels for details.

FPGA Resources

The UL3422 card is populated with the AMD XCVU2P-3FSVJ2104E FPGA. The high-level FPGA resources for this device are given in the following table.

Table 2: **Available FPGA Resources**

Specification	Resources
System logic cells (K)	1722
LUTs (K)	787
BRAM (Mbits)	76
URAM (Mbits)	180
HPIO	416
HDIO	48
GTYP transceivers	8
GTF transceivers	72[1]
PCIE4C Gen4 x8	1
Package, mm	47.5 x 47.5/1 mm ball pitch
Speed grade	-3

Notes:

1. While the FPGA has 72 GTF transceivers, only 32 are used by the card.

FPGA Bank I/O Mapping

The following figure and associated table gives the FPGA bank I/O allocation. This includes additional details for assigned function and VCCO allocation. Both HDIO (high density I/O) and HPIO (high performance I/O) banks are used. Allocation of bank type is dependent on the required function (i.e., memory interface or UART). Bank 0 is a dedicated bank allocated for JTAG and configuration QSPI interface. It is not detailed in the table.

Figure 4: **FPGA Bank Allocation**

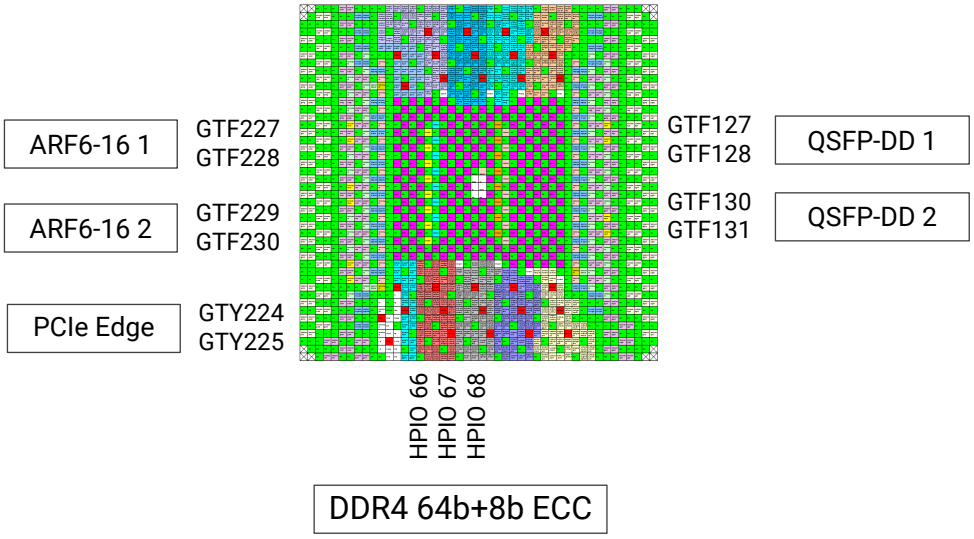


Table 3: **FPGA Bank Allocation**

FPGA Bank	Bank Type	Function(s)	VCCO
65	HPIO	• RX recovered clocks • EMCCLK	1.8
66 - 68	HPIO	DDR4 Controller	1.2
88	HDIO	• Three UARTs • QSFP-DD LEDs • PPS IN / OUT	3.3
93	HDIO	• Expansion Sideband 1 & 2 • QSFP-DD Sideband	3.3
127 - 128	GTF	QSFP-DD 1 • TX / RX 1-4 assigned to bank 127 • TX / RX 5-8 assigned to bank 128	N/A
130- 131	GTF	QSFP-DD 2 • TX / RX 1-4 assigned to bank 130 • TX / RX 5-8 assigned to bank 131	N/A
224 - 225	GTY	PCIe x8 to Edge Connector • PCIe Lane 3-0 on bank 225 • PCIe Lane 7-4 on bank 224 • Upper 8 lanes of PCIe x16 connector are not connected.	N/A
227 - 228	GTF	ARF6 1 Expansion Connector • TX / RX 1-4 assigned to bank 227 • TX / RX 5-8 assigned to bank 228	N/A
229 - 230	GTF	ARF6 2 Expansion Connector • TX / RX 1-4 assigned to bank 229 • TX / RX 5-8 assigned to bank 230	N/A

I2C Register Map

The following table provides the I2C base address register map for accessible devices. Registers are grouped under similar areas. Accessibility from FPGA, BMC, or SC is noted in the table. For I2C register details, see the manufacturer's respective device datasheet.

Table 4: **I2C Base Address Register Map for Accessible Devices**

	8-bit (HEX)	7-bit (HEX)		
Register Name	**Address**		**Description**	**Device**
DDR4 Power and Clocks CLKGEN_SCL / SDA—*Accessible from the FPGA only*				
Clock generator	0x12	0x09	Clock generator component	Renesas RC21008AQ
Jitter cleaner	0xB0	0x58	Enable QSFP-DD/ARF6 jitter cleaner	Renesas RC38612A002GN2
DDR4 power control	0x42	0x21	Enable power to DDR4[1]	TI TCA6408PWR
QSFP-DD—*Accessible from the FPGA only*				
QSFP-DD Power Control QSFP-DD1, QSFP-DD2	0x42	0x21	QSFP-DD ports[1] power control	TI TCA6408APWR
QSFP-DD I/O Expander QSFP-DD1, QSFP-DD2	0x40	0x20	QSFP-DD ports[1] I/O expander	TI TCA6408APWR
QSFP-DD1 or QSFP-DD2 Register Access	0xA0	0x50	Pass-through to QSFP-DD module	Access to QSFP-DD1 and QSFP-DD2 QSFPDD I2C registers. Access indirectly via QSFPDD Mux. Address is QSFPDD module dependent. See module data sheet.
MUX0	0xE0	0x70	See note 1.	PCA9545A
ARF6 Expansion Port—*Accessible from the FPGA only*				
Expansion port I2C			Future use	
System I2C_MAIN_SCL / SDA—*Accessible from the SC only*				
Various Controls	0x40	0x20	Provide various controls including: • EEPROM WP • ADK2 Present • Other	TI TCA6416AR
MFG EEPROM	0xA4 / 0xB4	0x52 / 0x5A	Manufacturing EEPROM. Provides card data including serial number, power, and other capabilities.	STM M24C64
FPGA thermal diode sensor	0x9C	0x4E	FPGA temperature	TI TMP411CDGKT
Temperature sensor (left)	0x90	0x48	Card outlet temperature	NXP LM75BTP
Temperature sensor (right)	0x92	0x49	Card inlet temperature	NXP LM75BTP
Power PMBUS_SCL / SDA—*Accessible from Server BMC or SC only*				
Input power monitor	0x80	0x40	Input voltage/current/power monitor for the following power rails: • 3.3V PCIe • 12V PCIe • 12V PCIe AUX	TI INA3221A

Table 4: **I2C Base Address Register Map for Accessible Devices** *(cont'd)*

	8-bit (HEX)	7-bit (HEX)		
Register Name	**Address**		**Description**	**Device**
VRM controller	0xC0	0x60	Multi-rail power controller.	Renesas ISL68224IRAZ

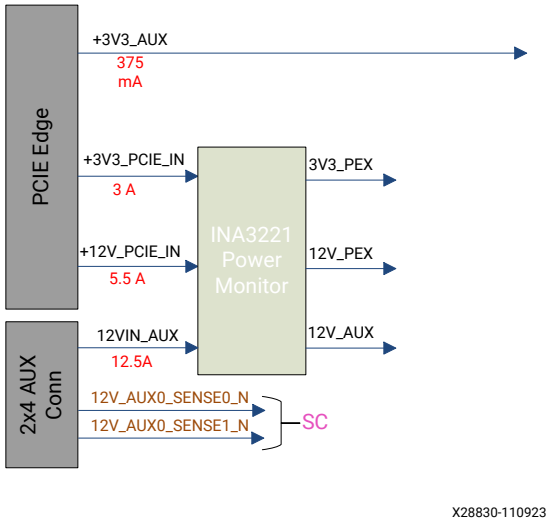
Notes:

1. See the UL3422 Early Access Secure Site for support details.

Card Power System

The following figure shows the high-level input power tree.

Figure 5: **Card Input Power Tree**



Key details include:

- The card is powered from PCIe edge connector. Additional power can be supplied via the PCIe AUX connector.
- Main FPGA power is delivered by ISL68224 controller with ISL99360 and RAA2213404GNP power stages.
- VCCINT power is generated by three power phases, taking input power from the following:
  - PCIe 12V edge connector (12V_PEX)
    - Powering one VCCINT power phase
  - PCIe 12V Auxiliary (12V_AUX)
    - Powering two VCCINT power phases
- Each QSFP-DD port uses isolated power, delivered by a dedicated regulator, which provides power enable and over-current control.

There are four power rails with the names and sources given in the following table.

***Note*:** The card can operate without AUX power connected, however card power will be reduced, including the QSFP modules which will be limited to 3.5W.

Table 5: **Power Rails**

Power Rail Name	Source
12V_PEX	PCIe Edge Connector
3V3_PEX	PCIe Edge Connector
3V3_AUX	PCIe Edge Connector
12V_AUX	PCIe AUX Connector 1

PCIe Connector

The Alveo UL3422 card has a PCIe Gen4 x8 interface compliant with PCIe CEM 4.0 configured as a PCIe Endpoint. It has a PCIe x16 physical connector with the upper eight lanes unconnected and does not support bifurcation.

For information about PCIe FPGA bank allocation and clocking details, see FPGA Bank I/O Mapping and Clocking. Detailed AMD UltraScale+™ device and PCIe pin connections can be found at UL3422 Early Access Secure Site.

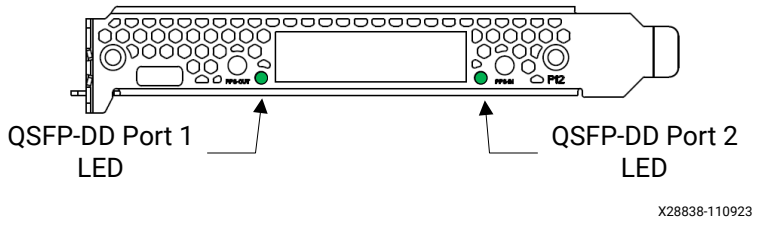
Power Brake (PCIe)

The Alveo UL3422 card is designed to support the Power Brake feature (also known as Emergency Power Reduction or eBrake) through the PCIe® connector. The PWRBRK# is connected to PMC bank 501 MIO 37. Implementation of the logic to act upon the PWRBRK# signal is left to the user.

LED Indicators

The card has two QSFP-DD user-definable LEDs visible through a cutout in the PCIe I/O bracket, as shown in the following figure.

Figure 6: **PCIe I/O Bracket LED Location**



The following table details the LED definition along with the FPGA pin.

Table 6: **Network Status LEDs**

LED Name	Description	FPGA Pin
QSFP-DD Link	User-definable green LED.	AP13 for QSFP-DD Port #1 AP14 for QSFP-DD Port #2

Network Interfaces

The Alveo UL3422 card hosts two 8-lane small form-factor pluggable (QSFP-DD) connectors that are housed within a ganged 1x2 QSFP-DD cage assembly with heatsink. It can be populated with QSFP or QSFP-DD direct attach copper or optical modules supporting up to 7W. The QSFP-DD can connect interfaces up to 100G using optical modules or cables. A 161.1328125 MHz clock is provided to the QSFP-DD interface such that different Ethernet IP cores can be enabled.

Network Port Labels

The QSFP-DD network ports on the card are labeled Port #1 through Port #2, with their locations shown in Figure 3.

Note: Block diagrams, register maps, and the XDC file reference the QSFP-DD ports as QSFP-DD1 through QSFPDD2. These references map to the card QSFP-DD labeling Port #1 through Port #2 as outlined in the following table. Similar labeling occurs with the ARF6 ports.

Table 7: **QSFP-DD Card Port Label to XDC / Block Diagram Net Port Label**

QSFP-DD Port Label	Net / Block Diagram Port Label
QSFP-DD Port #1	QSFP-DD1
QSFP-DD Port #2	QSFP-DD2

Network MAC Address

Each card has 32 contiguous MAC addresses.

Determine Allocated MAC Addresses

Use the following steps to determine the allocated MAC addresses.

Determine the Base MAC Address

To determine the base MAC address, use the Satellite Controller to display the board information, or look at a sticker on the physical card.

Use Satellite Controller to Display Board Info

Using the Satellite Controller, display *Board Info*. Board MAC0 is the base MAC address. See UL3422 Early Access Secure Site for support details.

Identify Base MAC Address From Sticker

On the PCIe® interface of the card, a sticker displays two MAC addresses:

- **MAC1:** Denotes the base MAC address.
- **MAC32:** Represents the last allocated MAC address.

Use Formula to Compute Allocated MAC Addresses

With the base MAC address, use the following formula to compute the allocated MAC addresses.

$$MAC(i) = MAC\ base\ address + i$$

Where i is an integer from 0 to 31.

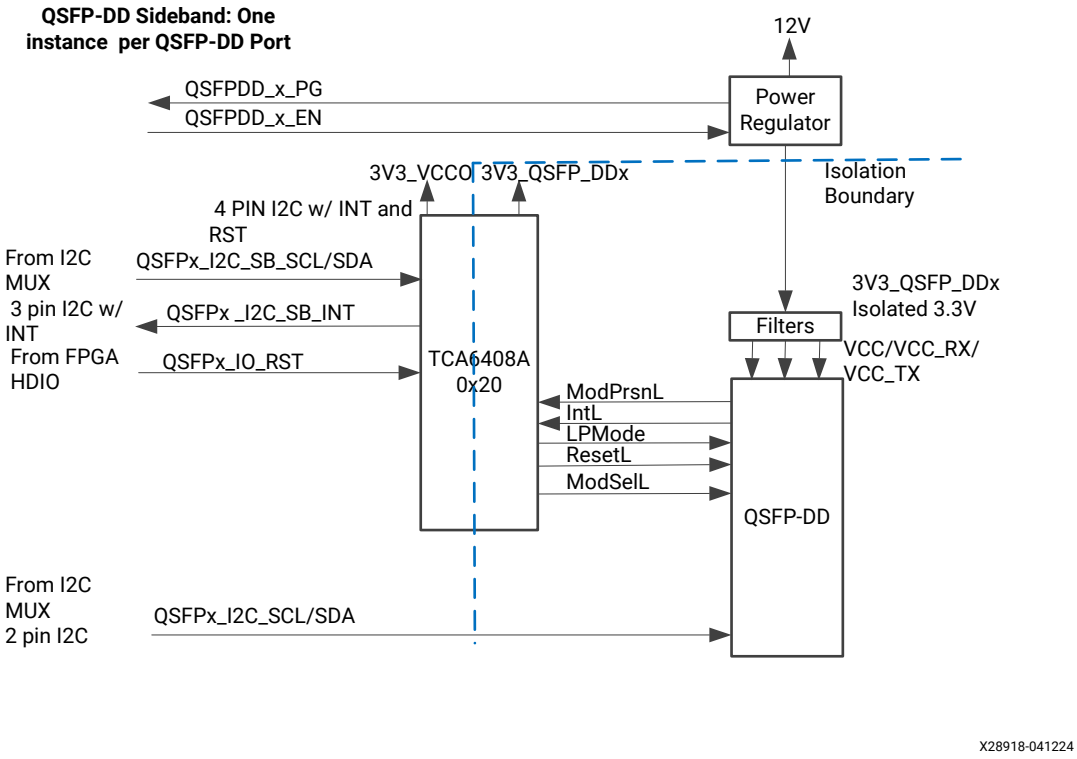
Network Port LEDs

See LED Indicators.

QSFP-DD Isolation Logic

To ensure the I2C bus is not taken down, in the case of a malfunctioning QSFP-DD module, the sideband I/O expander consists of an electrical isolation boundary and short-circuit protection logic (shown in the following image).

Figure 7: **QSFP-DD Electrical Isolation Block Diagram**



QSFP-DD Sideband Management

The QSFP-DD connector sideband signals are accessible directly from the FPGA via the I2C interface. See the UL3422 Early Access Secure Site for support details.

QSFP-DD to GTF Lane Mapping

QSFP-DD GTF interface lane mapping and high-speed connections are detailed in the UL3422 XDC file. See the UL3422 Early Access Secure Site for support details.

Connectivity Considerations

The following lists considerations for various direct attach copper (DAC) cable usage scenarios.

Table 8: **QSFP-DD Connector Considerations**

	Cable Type	
Consideration	**QSFP-DD**	**QSFP+/QSFP28**
Lanes of connectivity	8 lanes of connectivity span 2 GTF quads.	4 lanes of connectivity to a single GTF quad.
Legacy / DD support	Consists of legacy pins (lanes 1-4) and DD pins (lanes 5-8).	Connects only to the legacy pins (lanes 1-4) of the QSFP-DD connector.
Legacy pin connection	Legacy pins are connected to quads 127 and 130 (QSFP 1 and 2)	Connect to quads 127 and 130 (QSFP 1 and 2).
DD pin connections	DD pins are connected to quads 128 and 131.	Not connected
Card jitter attenuation support	Provides access to jitter cleanup device via dedicated REFCLK outputs on quads 127 and 130 (QSFP-DD 1 and QSFP-DD 2), or via HPIO (bank 65).	Requires use of HPIO (bank 65) to provide recovered clock to jitter cleanup device.

Suggested DAC Cables

Any industry standards compliant QSFP+/QSFP28/QSFP-DD DAC cable can be used with the above mentioned considerations. The Amphenol-branded cable is suggested for a QSFP-DD to 8xSFP+ splitter DAC cable.

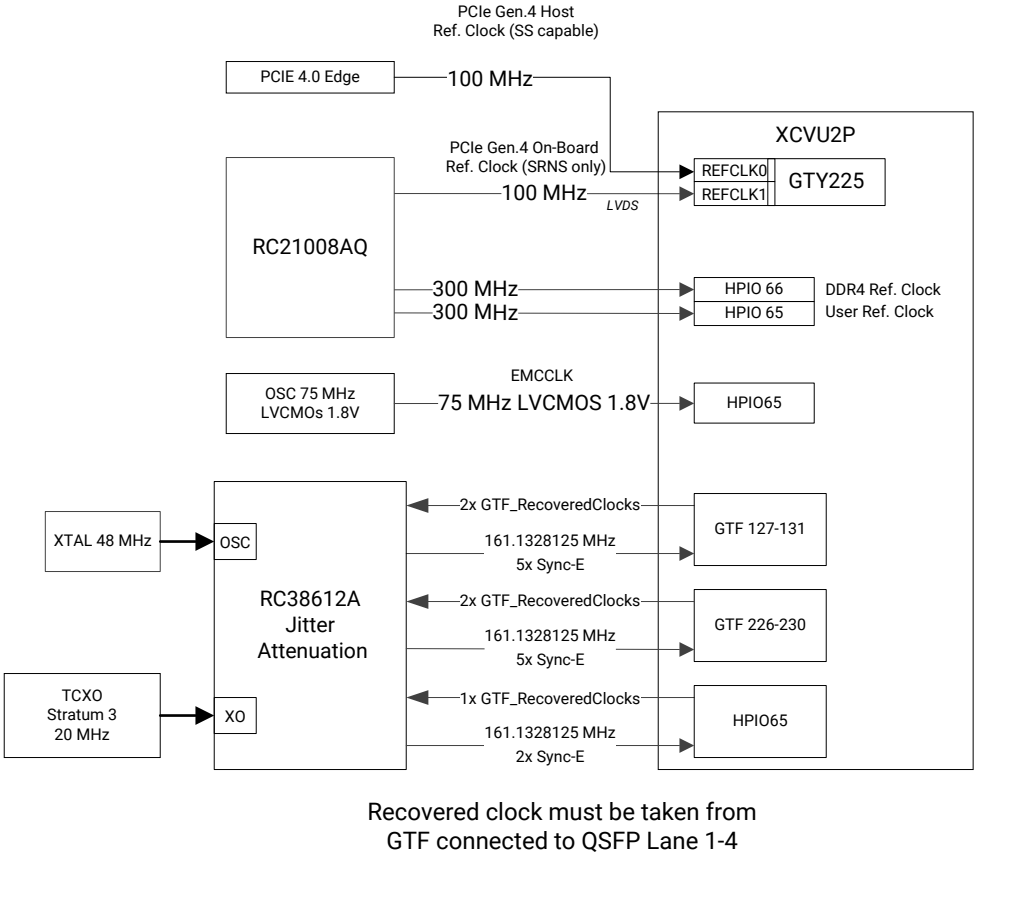
Clocking

The card provides the following reference clocks:

- PCIe® reference clocks
- Memory controller (DDR4) reference clocks
- User reference clock
- Ethernet reference clocks

The following high-level clock tree diagram shows the advanced clocking and jitter attenuator logic. See the following section for additional details.

Figure 8: **UL3422 Clocking Tree**



The card uses the Renesas RC21008AQ clock generator to provide reference clocks for PCIe, user reference, as well as a DDR4 memory controller. The following table lists the Renesas clock output reference and frequency, along with the FPGA destination bank and XDC net names. Renesas clock output references that are not provided in the table are not connected.

Table 9: **Renesas RC21008AQ Clock Generator Output Frequencies**

Renesas RC21008AQ Clock Output Reference	Frequency (MHz)	Destination FPGA Bank	Block Reference Clock	XDC Net Name
OUT1	100	225	PCIe	clk_pcie_lvds_100_n clk_pcie_lvds_100_p
OUT2	300	65	User	clk_sys_lvds_300_n clk_sys_lvds_300_p
OUT3	300	66	DDR4 memory controller	clk_ddr_lvds_300_n clk_ddr_lvds_300_p

User Clock

A 300 MHz user reference clock is generated by the clock generator and connected directly to FPGA bank 65.

DDR4 Memory Controller Clock

A 300 MHz DDR4 reference clock is generated by the clock generator and connected directly to FPGA bank 67.

PCIe Reference Clocks

The following two clocks are provided to support PCIe clocking.

Table 10: **PCIe Reference Clocks**

Clock Source	Description
PCIe Edge Connector	100 MHz clock originating from the PCIe edge connector and connected to GTY 225 MGTREFCLK0 inputs. The clock signal is AC coupled.
Internal clock generator	100 MHz clock originating from the Renesas RC21008AQ clock generator and connected to GTY 225 MGTREFCLK1 inputs. The clock signal is AC coupled and meets PCIe Gen3/Gen4 jitter specifications.

FPGA EMCCLK Programming Clock

To minimize clock startup time, a 75 MHz FPGA external master configuration clock (EMCCLK) is sourced from an onboard oscillator. It is connected directly to the dedicated (EMCCLK), on bank 65.

Ethernet Reference Clocks

A 161.1328125 MHz Ethernet reference clock is generated.

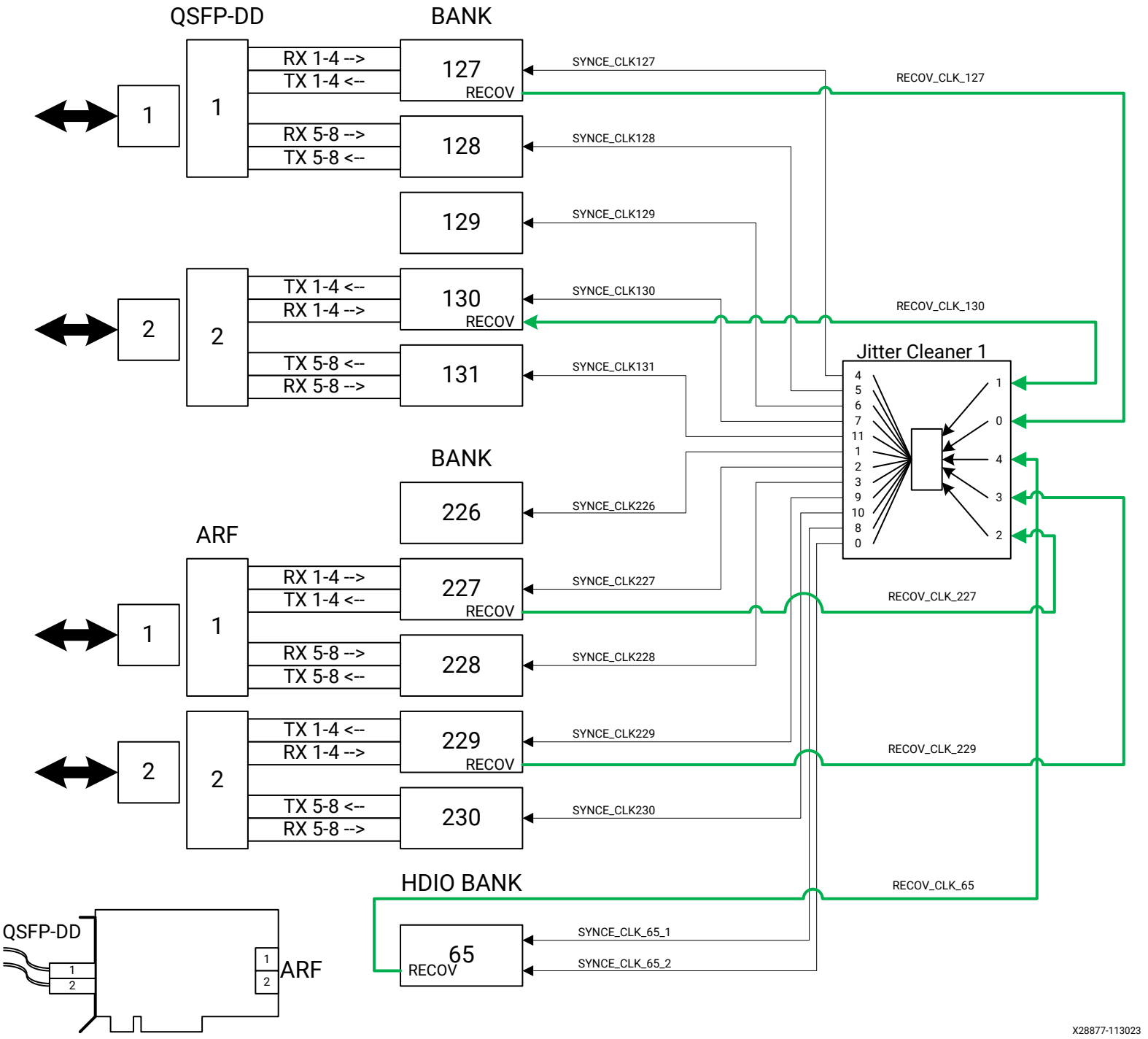
Jitter Attenuator

The jitter attenuator logic for the QSFP-DD and ARF6 ports consists of various temperature-controlled crystal oscillators and ultra-low jitter components that provide exceptional jitter attenuation and clock fidelity. The Resesas RC38612 jitter attenuator device is the heart of the jitter attenuation logic. It has the ability to program different configurations by routing input clocks through an array of internal digitally controlled oscillators (DCOs) or digital phase locked loops (DPLLs) before routing to a set of output pins.

The following figure shows the high-level connections between the QSFP-DD and ARF6 expansion port GTFs, and the Renesas jitter attenuator. The jitter attenuator can select one of five recovered clock inputs:

- Two recovered clocks are dedicated routes from QSFP-DD GTF ports.
- Two recovered clocks are dedicated routes from the ARF6 ports.
- One recovered clock is indirectly routed from the GTF banks via FPGA bank 65.

Figure 9: **QSFP-DD and Expansion Port Jitter Attenuation Connections**



The jitter attenuator generates twelve attenuated output clocks.

- Four of the generated clocks are routed to the GTF banks associated with the QSFP-DD ports.
- Four generated clocks are routed to the GTF banks associated with the ARF6 ports.
- Two generated clocks are routed to GTF banks 129 and 226 allowing additional clock sources adjacent to the QSFP-DD and ARF6 ports.

- The two remaining generated clocks are routed to HDIO pins in bank 65 for use in the FPGA fabric.

See FPGA Bank Destination and Associated XDC Net Name for clock to bank mapping.

Designers should closely examine the Renesas RC38612 Datasheet to fully understand how to configure and use the device. The jitter attenuator is programmed via an I2C bus to configure its features such as selecting input clocks, configuring PLLs, and phase aligning output clocks with the internal FPGA reference clocks. The output clocks can be flexibly assigned to specific PLLs to create clocking subgroups. While the jitter attenuator has some flexibility in routing outputs to internal DCO/DPLLs, it does not allow all twelve outputs to be connected to the same DCO/DPLL.

IMPORTANT! *The four external recovery clocks from banks 127 (RECOV_CLK127), 130 (RECOV_CLK130), 227 (RECOV_CLK227), and 229 (RECOV_CLK229) are hardwired to the jitter attenuator. The recovery clock RECOV_CLK_65 is internally routed through bank 65 and can be sourced from any of the GTF banks through the FPGA fabric.*

Renesas Recovered Clock FPGA Bank Source and Associated XDC Net Name

The following table provides the FPGA bank source and associated XDC net name of the signals connected from the QSFP-DD and ARF6 expansion port to the clock input pins of the Renesas jitter attenuator. See the UL3422 Early Access Secure Site for support details.

Table 11: **QSFP-DD, ARF6, and Bank 65 to Jitter Attenuator Recovered Clock Connections**

Renesas Recovered Clock Reference	Source Bank	FPGA Pin	XDC Net Name
CLK0	127	AE37	recov_clk_127_lvds_n
		AE36	recov_clk_127_lvds_p
CLK1	130	N37	recov_clk_130_lvds_n
		N36	recov_clk_130_lvds_p
CLK2	227	AG10	recov_clk_227_lvds_n
		AG11	recov_clk_227_lvds_p
CLK3	229	W10	recov_clk_229_lvds_n
		W11	recov_clk_229_lvds_p
CLK4	65[1]	BF19	recov_clk_65_lvds_n
		BF20	recov_clk_65_lvds_p

Notes:

1. The recovery clock RECOV_CLK65 is internally routed through bank 65 and can be sourced from any of the GTF banks through the FPGA fabric.

FPGA Bank Destination and Associated XDC Net Name

The following tables provide the FPGA bank destination and associated XDC net name of the signals connected from the Renesas jitter attenuator's clock outputs to the QSFP-DD, ARF6 expansion port, and Bank 65 clock reference pins. See the UL3422 Early Access Secure Site for support details.

Table 12: **Jitter Attenuator to QSFP-DD Port SYNC-E Clock Connection**

Renesas Recovered Clock Reference	Source Bank	FPGA Pin	XDC Net Name
Q4	127	AG37	synce_clk_127_lvds_n
		AG36	synce_clk_127_lvds_p
Q5	128	AC37	synce_clk_128_lvds_n
		AC36	synce_clk_128_lvds_p
Q6	129	W37	synce_clk_129_lvds_n
		W36	synce_clk_129_lvds_p
Q7	130	R37	synce_clk_130_lvds_n
		R36	synce_clk_130_lvds_p
Q11	131	L37	synce_clk_131_lvds_n
		L36	synce_clk_131_lvds_p

Table 13: **Jitter Attenuator to ARF6 Expansion Port SYNC-E Clock Connections**

Renesas Recovered Clock Reference	Source Bank	FPGA Pin	XDC Net Name
Q1	226	AN10	synce_clk_226_lvds_n
		AN11	synce_clk_226_lvds_p
Q2	227	AJ10	synce_clk_227_lvds_n
		AJ11	synce_clk_227_lvds_p
Q3	228	AE10	synce_clk_228_lvds_n
		AE11	synce_clk_228_lvds_p
Q9	229	AA10	synce_clk_229_lvds_n
		AA11	synce_clk_229_lvds_p
Q10	230	U10	synce_clk_230_lvds_n
		U11	synce_clk_230_lvds_p

Table 14: **Jitter Attenuator to Bank 65 HDIO Connections**

Renesas Recovered Clock Reference	Source Bank	FPGA Pin	XDC Net Name
Q0	65	BB20	synce_clk_65_2_lvds_n
		BA20	synce_clk_65_2_lvds_p
Q8	65	BA17	synce_clk_65_1_lvds_n
		AY17	synce_clk_65_1_lvds_p

Renesas Default and Predefined Configuration Settings

The Renesas RC38612A device used on the UL3422 card has an internal one-time programmable (OTP) memory with four predefined configuration register settings (configuration 12 through 15) shown in Renesas Clock Routing. The configuration register settings represent possible values that the Renesas device takes on power-up or reset. Configuration 15 is the default setting and is loaded on power-up or device reset.

GPIO[3:0] (JITT1_GPOI0 to JITT1_GPOI3) port values dictate the default configuration used from the OTP memory. The following table shows the configuration selection as a function of GPIO[3:0]. The UL3422 card has GPIO[3:0] pulled High (4'b1111) with setting configuration 15 as the default configuration which is loaded on power-up. The GPIO values can be changed after power-up resulting in a different configuration loaded after device reset. The GPIO to configuration selection is given in the following table.

Table 15: **Jitter Cleaner Configuration Selection**

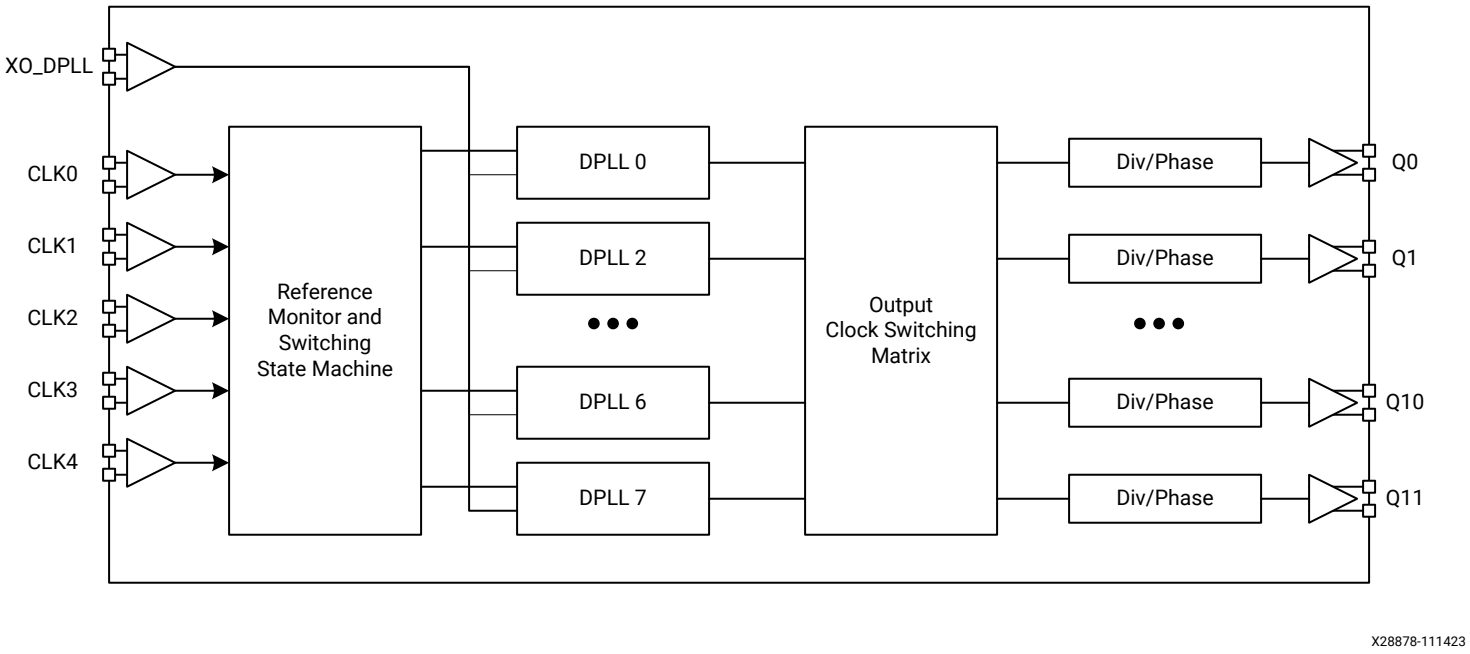
GPIO[3:0]	Configuration Selection
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

In addition, the Renesas register values can be changed after power-up or reset via the serial port. However, any changes are lost when the device is reset or power-cycled unless programmed into OTP as an additional or replacement configuration.

Renesas Clock Routing

The Renesas jitter attenuator has two primary switch matrices to route input clocks to the DPLL array and to the output clock pins. The following figure is a high-level depiction of how this routing is organized.

Figure 10: **Clock to DPLL Routing Example**



Each of the four predefined configurations includes settings for these switching matrices. The following tables describe the clock input and output routing for the four predefined configurations.

The frequency column for the input clock/DPLL routing corresponds to the frequency of the DPLL's generated clock to which the device is tuned in order to reduce jitter and generate a stable clock. The frequency column for the output clock/DPLL routing corresponds to the expected output clock frequency of the corresponding pin.

Note: The DPLLs for configurations 12 and 13 have direct connections to specific input clocks. For configurations 14 and 15, DPLL0 and DPLL2 use the internal clock selection state machine to determine which clock sources are valid and which are selected for their input clock source. The remaining DPLLs are sourced from the DPLL0 feedback path to provide a synchronous reference for the generated output clocks. Contact your AMD FAE for additional details on specific usage.

Table 16: **Renesas Input Configuration Setting 12**

Channel	Frequency (MHz)	Primary Source
DPLL0	625	CLK4
DPLL1	625	CLK2
DPLL2	625	CLK3
DPLL3	625	CLK0
DPLL5	625	CLK4
DPLL7	625	CLK1

Table 17: **Renesas Output Configuration Setting 12**

Source	Output	Frequency (MHz)
DPLL0	Q0	156.25
DPLL1	Q1	156.25
DPLL1	Q2	156.25

Table 17: **Renesas Output Configuration Setting 12** *(cont'd)*

Source	Output	Frequency (MHz)
DPLL1	Q3	156.25
DPLL3	Q4	156.25
DPLL3	Q5	156.25
DPLL3	Q6	156.25
DPLL7	Q7	156.25
DPLL5	Q8	156.25
DPLL2	Q9	156.25
DPLL2	Q10	156.25
DPLL7	Q11	156.25

Table 18: **Renesas Input Configuration Setting 13**

Channel	Frequency (MHz)	Primary Source
DPLL0	644.53125	CLK4
DPLL1	644.53125	CLK2
DPLL2	644.53125	CLK3
DPLL3	644.53125	CLK0
DPLL5	644.53125	CLK4
DPLL7	644.53125	CLK1

Table 19: **Renesas Output Configuration Setting 13**

Source	Output	Frequency (MHz)
DPLL0	Q0	161.1328
DPLL1	Q1	161.1328
DPLL1	Q2	161.1328
DPLL1	Q3	161.1328
DPLL3	Q4	161.1328
DPLL3	Q5	161.1328
DPLL3	Q6	161.1328
DPLL7	Q7	161.1328
DPLL5	Q8	161.1328
DPLL2	Q9	161.1328
DPLL2	Q10	161.1328
DPLL7	Q11	161.1328

Table 20: **Renesas Input Configuration Setting 14**

Channel	Frequency (MHz)	Primary Source
DPLL0	625	Automatic
DPLL1	625	FB DPLL0
DPLL2	625	CLKs: 0,1,2,3,4

Table 20: **Renesas Input Configuration Setting 14** *(cont'd)*

Channel	Frequency (MHz)	Primary Source
DPLL3	625	FB DPLL0
DPLL5	625	FB DPLL0
DPLL7	625	FB DPLL0

Table 21: **Renesas Output Configuration Setting 14**

Source	Output	Frequency (MHz)
DPLL0	Q0	156.25
DPLL1	Q1	156.25
DPLL1	Q2	156.25
DPLL1	Q3	156.25
DPLL3	Q4	156.25
DPLL3	Q5	156.25
DPLL3	Q6	156.25
DPLL7	Q7	156.25
DPLL5	Q8	156.25
DPLL5	Q9	156.25
DPLL5	Q10	156.25
DPLL7	Q11	156.25

Table 22: **Renesas Input Configuration Setting 15 (Default Configuration)**

Channel	Frequency (MHz)	Primary Source
DPLL0	644.53125	Automatic
DPLL1	644.53125	FB DPLL0
DPLL2	644.53125	CLKs: 0,1,2,3,4
DPLL3	644.53125	FB DPLL0
DPLL5	644.53125	FB DPLL0
DPLL7	644.53125	FB DPLL0

Table 23: **Renesas Output Configuration Setting 15 (Default Configuration)**

Source	Output	Frequency (MHz)
DPLL0	Q0	161.1328
DPLL1	Q1	161.1328
DPLL1	Q2	161.1328
DPLL1	Q3	161.1328
DPLL3	Q4	161.1328
DPLL3	Q5	161.1328
DPLL3	Q6	161.1328
DPLL7	Q7	161.1328
DPLL5	Q8	161.1328

Table 23: **Renesas Output Configuration Setting 15 (Default Configuration)** *(cont'd)*

Source	Output	Frequency (MHz)
DPLL5	Q9	161.1328
DPLL5	Q10	161.1328
DPLL7	Q11	161.1328

Renesas Reset Sequence

Renesas Reset Sequence

During its reset sequence, the RC38612 jitter cleaner:

- Loads its initial configuration.
- Enables internal regulators.
- Establishes and enables internal clocks.
- Performs initial calibration of the Analog PLL.
- Locks it to the reference on the OSCI/OSCO pins.

For complete details, see the Renesas RC38612 datasheet.

Loading a Configuration

The following high-level steps detail the how to load a configuration. For complete details, see the Renesas RC38612 datasheet.

1. Set the required CONFIG Value on JITT1_GPIO0-GPIO3 (for example, Config 15 – 1111 or Config 14 – 1110).
2. Assert JITT_RESETn to logic 0 (resets the RC38612 devices).
3. Give some delay (> 10 ms).
4. Assert JITT_RESETn to logic 1 (gets the RC38612 devices out of reset).
5. Monitor JITT1_GPIO5. JITT1_GPIO5 asserted to logic 1 indicates that the TX clocks generated by the RC38612 devices are in sync with the recovered clock.

Satellite Controller

The satellite controller (SC) provides independent supervisory and card management functions including power and temperature monitoring. The host server board management controller (BMC) can interact with the satellite controller to monitor and control the card through out-of-band (OOB) communication.

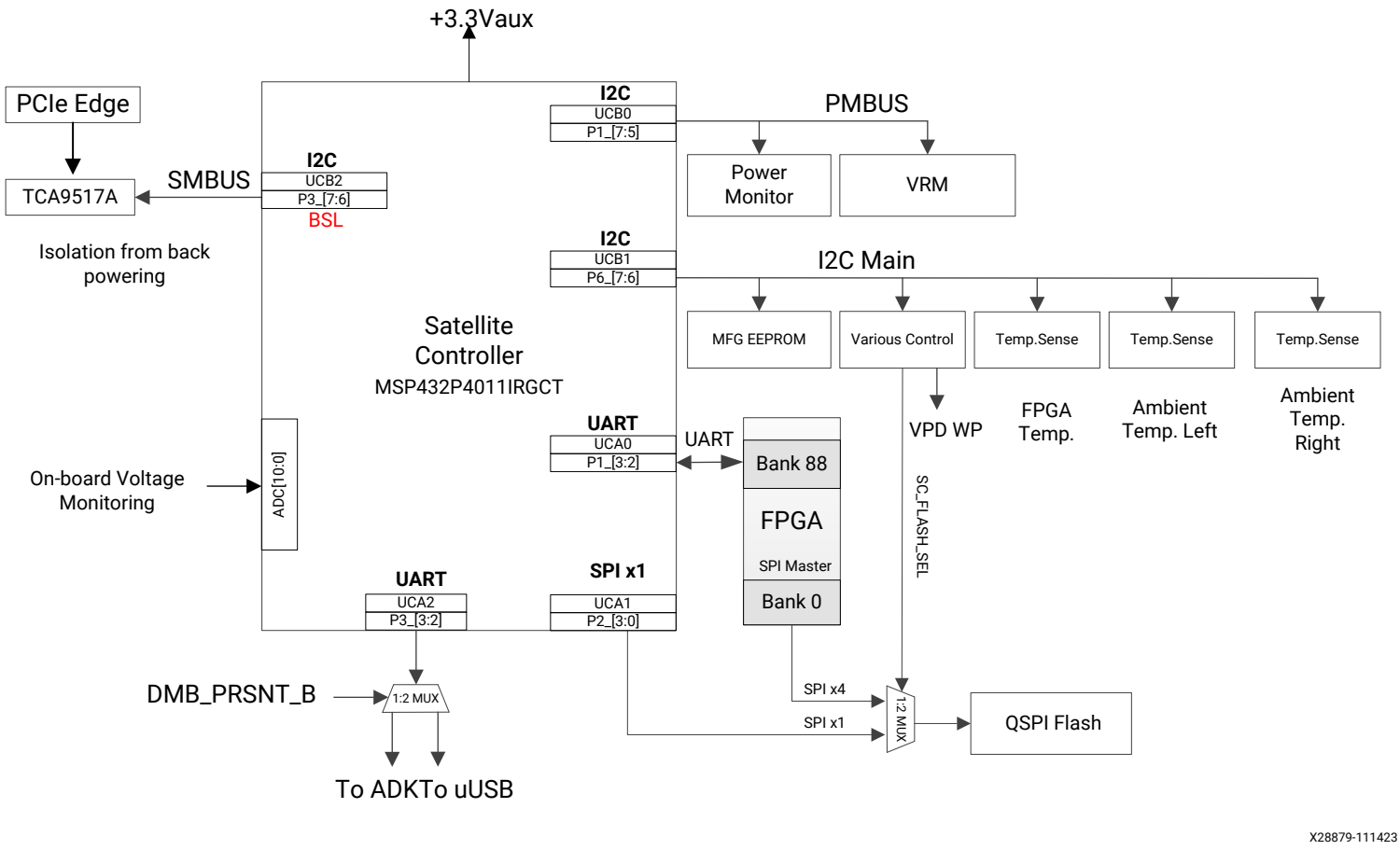
The following table details the SC component used.

Table 24: **Satellite Controller Device Details**

Parameter	Description
Manufacturer	TI
Part number	MSP432P4011IRGCT
Details	Low power MCU

The following figure shows the interfaces and devices that are accessible by the SC.

Figure 11: **Satellite Controller Interface and Device Access**



Out-of-Band Support

The Alveo Card Out-of-Band Management Specification for Server BMC documentation describes out-of-band (OoB) support implemented in the SC firmware, supporting communication with the server board management controller (BMC) over the SMBus/I2C interface on the PCIe edge connector. The underlying protocols supported are standard I2C protocol and PLDM over MCTP over SMBus.

The *Card Management Solution Subsystem Product Guide* (PG348) provides card management solution IP allowing you to quickly develop and interact with the satellite controller from the FPGA.

Satellite Firmware Update

To update the SC firmware, you must generate an AMD Vivado™ design that implements the CMS IP.

Satellite Sensor Data Access

The SC has access to the following temperature sensors. See *System I2C_MAIN_SCL / SDA* and *Power PMBUS_SCL / SDA* in I2C Register Map, for register details.

- FPGA temperature sensor
- Card inlet and outlet temperature sensors

To read the SC sensor information, a design using the CMS IP and host application to communicate with the CMS IP is required. See the UL3422 Early Access Secure Site for support details.

Card Thermal and Electrical Protections

Built-in shutdown logic protects the card from damage by removing power to the FPGA when either electrical or thermal limits (given in the following table) reach or exceed their respective card shutdown thresholds. VCCINT current and temperature are monitored by the card regulator while FPGA temperature is monitored by the satellite controller (SC). Power to the card SC remains on during card shutdown. Card shutdown protection logic is always enabled and cannot be disabled.

Note: When card shutdown occurs, the card is pulled off the PCIe bus and consequently is not seen by the host. No AXI firewall trip is issued. A cold reboot of the server is required to recover.

The following table lists the card shutdown power and thermal thresholds.

Table 25: **Thermal and Electrical Protection Thresholds**

Sensor Description	Card Shutdown Threshold	
	PCIe AUX Power Not Connected	PCIe AUX Power Connected
VCCINT Current	60A (One phase at 60A per phase)	180A (Three phases at 60A per phase)
VCCINT Temperature	125°C	
FPGA Temperature	107°C	

PPS In and Out

One pulse per second (1PPS) input and output interfaces, located on the PCIe I/O bracket, provide synchronization between external system clock synchronization units. Both 1PPS interfaces are compatible with plug-type SSMB adaptors and cables (such as Pasternack PE3139LF series cables). The 1PPS input is terminated with a 50Ω load. The following table provides the XDC net name and associated pin assignment.

Table 26: **PPS Pin Assignment**

Net Name	Pin Assignment
PPS_IN_FPGA	BF14
PPS_OUT_FPGA	BF15

PCIe AUX Power

The card has an 8-pin PCIe auxiliary power connector. The card can operate without AUX power connected, however card power will be reduced, including the QSFP modules which will be limited to 3.5W.

Depending on your server or computer, an additional PCI Express auxiliary power cable or adapter might be needed. Consult your computer documentation for additional information.

Note: This 8-pin connector is not compatible with an ATX12V/EPS12V power cable source. Ensure that the appropriate PCIe auxiliary power source is available, not an ATX12V/EPS12V power source. For more details see Answer Record 72298.

For card installation and connecting the PCIe AUX power cable, see the *Alveo UL3422 Installation Guide* (UG1643).

DDR4 Specifications

There is a total of 16 GB DDR4 memory on the UL3422 card comprising five x16 Micron components. The following table details the DDR4 memory component used.

Table 27: **DDR4 Component Specification**

Parameter	Description
Manufacturer	Micron
Part number	MT40A2G16TBB-062E:F
Total number parts on card	4 + 1
Details	• 32 Gb DDR4 (16 GB total on the card) • Single rank • Supports ECC error detection and corrections • Supports 64 b + 8 b ECC at 2400 MT/s

Note: The DDR4 memory subsystem has a separate power control from FPGA and must be enabled prior to use. See the UL3422 Early Access Secure Site for support details.

Expansion Ports

The expansion ports provide capabilities to add additional QSFP-DD connections and sideband control. These ports consist of the following:

- Two high-speed SAMTEC ARF6-16-S-D-A connectors (see https://www.samtec.com/) providing 16 expansion GTF TX/RX pairs over cable using the SAMTEC ARF6 solution.
- One PicoClasp 10-pin connectors for sideband signals (Molex 5044491007 part).
- The TX lanes are AC coupled, which allows multiple cards to be interconnected.

GTF to Expansion Connector Lane Mapping

The GTF to expansion connector lane mapping and high-speed connection details can be found in the UL3422 Early Access Secure Site.

Expansion Sideband Connector

One vertical 10-pin PicoClasp connectors provide sideband access. The following table lists the ARF6 I2C details along with the respective reset per ARF6.

Table 28: **Sideband Connector to FPGA Pinout**

Port Name	FPGA Pin	Sideband Connector Pin	Description
ARF_I2C_SCL	M14	6	Expansion port I2C interface.
ARF_I2C_SDA	M13	5	Expansion port I2C interface.
ARF_IO0_RST	K15	3	Expansion port ARF6-0 reset.
ARF_IO1_RST	L15	4	Expansion port ARF6-1 reset.
ARF_MUX_INTN	L13	8	MUXed expansion port interrupt.
ARF_MUX_RESET	K16	7	MUX expansion port reset.
3.3V		1	Power
GND		10	Ground

***Note*:** The RX polarity of the GTs need to be inverted on the ARF connector when using a loopback cable.

FPGA Configuration Memory

The card is populated with 2 Gb QSPI flash memory, which provides space to store up to four maximum-sized FPGA bitstreams. The following table details the QSPI component.

Table 29: **QSPI Device Details**

Parameter	Description
Manufacturer	Micron
Part number	MT25QU02GCBB8E12
Details	Speed 75 MHz Density 2 Gb (256M x 8)

Two FPGA configuration modes are supported:

- Master SPI x4
- JTAG (over Micro-USB or ADK2 debug connector)

The FPGA bank 0 mode pins are hardwired to master SPI mode M[2:0] = 001 with pull-up/pull-down resistors. At power up, the FPGA is configured by the Quad SPI NOR flash device using the primary serial configuration mode.

Table 30: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable – JTAG overrides	x1	Not applicable

Manufacturing EEPROM

A manufacturing EEPROM provides card data to the Satellite Controller (SC) for card operation. While it is accessible via the I2C main interface, it is not meant for user access.

Maintenance Interfaces

The card comes with two maintenance interfaces:

- micro USB
- ADK2 debug connector

Each is described in more detail in subsequent sections. The following table shows the protocols supported for each interface.

Table 31: **ADK2 Debug Connector and micro USB Supported Protocols**

Protocol	micro USB	ADK2
FPGA JTAG	YES	YES
FPGA UART0	YES	NO
FPGA UART1	YES	YES
MSP debug UART	YES	YES
MSP JTAG	NO	YES
SMBus	NO	YES
PMBus	NO	YES

Note: Internal logic is shared between the interfaces. For selecting an interface, refer to ADK2 and USB Port Precedence.

Micro USB Interface

The card has one micro USB0 interface which provides access to the FPGA JTAG/UART + SC UART. It is located on the I/O bracket and is accessible outside the chassis. Micro USB0 might be partially covered by the server chassis, which can make it difficult to plug into. See Card Interfaces for physical location. For accessing the ADK2 or USB interface, see ADK2 and USB Port Precedence.

ADK2 Debug Connector

The ADK2 debug connector, with the AMD Alveo™ debug kit (ADK), provides communication between the card and a host computer or an off-the-shelf debugger. It provides access to the on-board sensors, satellite controller, and QSPI flash programming. For setup details, see *Alveo Card Debug Kit User Guide* (UG1538).

ADK2 Debug Connector Pinout

The following table lists the ADK2 debug connector pin signals for the UL3422 card.

Note: Both *SC* and *SUC* are synonymous with satellite controller.

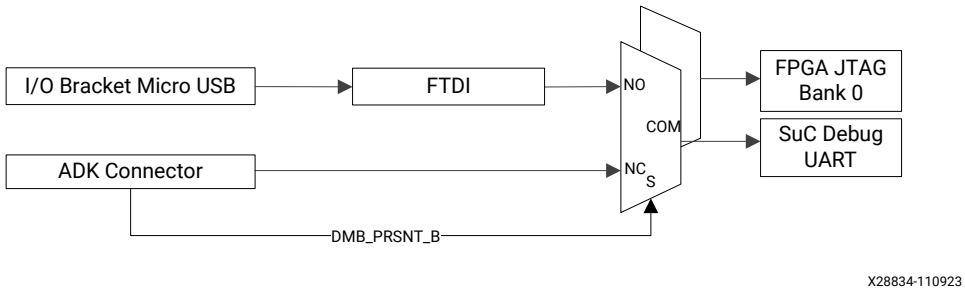
Table 32: **ADK2 Debug Connector Pinout Signals for the UL3422 Card**

Pin	Description	Pin	Description
A1	No Connect	B1	FPGA_JTAG_VREF (+3V3_SYS)
A2	No Connect	B2	FPGA _JTAG_TCK
A3	No Connect	B3	FPGA _JTAG_TMS
A4	No Connect	B4	FPGA _JTAG_TDI
A5	No Connect	B5	FPGA _JTAG_TDO
A6	No Connect	B6	No Connect
A7	No Connect	B7	No Connect
A8	GND	B8	GND
A9	No Connect	B9	+3V3_SYS_FPGA
A10	No Connect	B10	FPGA_UART1_RXD
A11	No Connect	B11	FPGA_UART1_TXD
A12	GND	B12	No Connect
A13	ALL_PSU_ON_R	B13	SUC_ DEBUG _RXD
A14	SUC_JTAG_TCK	B14	SUC_ DEBUG _TXD
A15	No Connect	B15	No Connect
A16	SUC_JTAG_TDI	B16	No Connect
A17	SUC_JTAG_TMS	B17	No Connect
A18	SUC_JTAG_TDO	B18	No Connect
A19	FPGA_MODE_CNTRL	B19	No Connect
A20	No Connect	B20	+3V3_AUX
A21	PMBus_SDA	B21	SMBUS_SDA
A22	PMBus_SCL	B22	SMBUS_SCL
A23	PMBus_ALERTB	B23	No Connect
A24	GND	B24	GND
A25	DDR4_VPP, divided 1:2 divided 2:5	B25	VCCINT (0.9V)
A26	+3V3_SYS_AUX, divided 1:2	B26	+1V8_MGT VCCAUX
A27	5V0, divided 1:5	B27	0V9_MGTAVCC
A28	1V8_SYS	B28	1V2_MGTAVTT
A29	1V5_SYS	B29	1V2_VCCO
A30	DMB_PRSNT_B	B30	GND

ADK2 and USB Port Precedence

The ADK2 and micro USB UART and JTAG interfaces share internal logic to access the various protocols. The following figure shows the shared internal logic. The MUX is controlled by DMB_PRSNT_B, which is internally set when the ADK2 debug module is connected.

Figure 12: **USB and ADK2 Debug Connector Shared Logic**



Access control is granted based on the following precedence rules:

- If the ADK2 debug module is connected, it has control of the shared ports.
- If ADK2 debug module is not connected, USB has control of the shared ports.

Mechanical

The UL3422 card dimensions, shown in the following table, are compliant with PCIe CEM rev.4.0 full height, ½ length card specifications.

Table 33: **Card Dimensions**

Parameter	Dimension
Height	111.15 mm
Primary side width	14.47 mm Max
Secondary side width	2.67 mm Max
Length	167.65 mm
Weight	561.5g

Thermal

Operating and Storage Temperature Conditions

The following table provides the operating and storage temperatures, and humidity conditions.

Table 34: **Operating and Storage Temperatures and Humidity Conditions**

Specification	Condition
Operating temperature	5°C to 45°C
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Storage humidity, non-condensing	5% to 95%

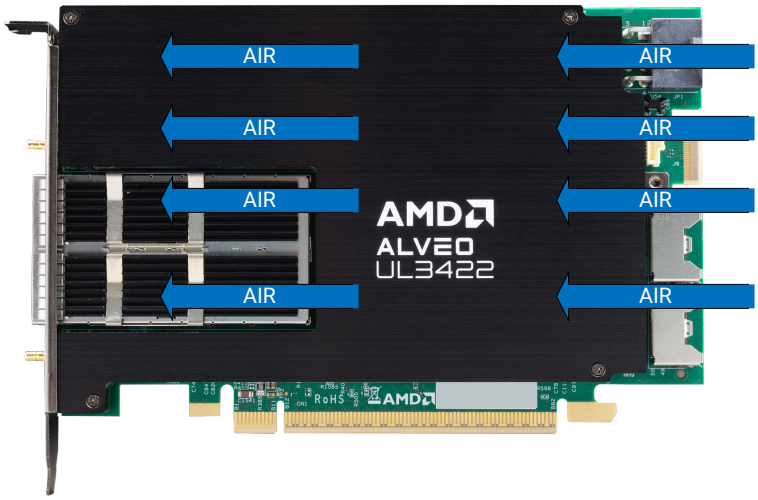
Notes:

1. Refer to Airflow Requirements for operating temperatures and their corresponding airflow and airspeed.

Airflow Direction Support

The UL3422 card is designed for passive cooling and requires an external mechanism to ensure proper airflow for cooling. The card supports normal (forward) airflow direction from retainer bracket to I/O bracket, as illustrated in the following figure. Passive cards should not be powered without a forced airflow mechanism in place.

Figure 13: **Supported Airflow Directions for UL3422 Card**



Note: Other environmental conditions are possible, including bidirectional flow. However, this is specific to server configurations, and testing is performed by individual OEMs. Contact your server provider for more information and options.

Airflow Requirements

Inlet temperature versus airflow requirement in server for normal flow are given in the following table.

Note: The thermal characterization values presented are estimates only.

Table 35: **UL3422 Inlet Temperature vs. Airflow (out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at Sea Level for 123W Total Card Power with QSFP power at 3.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure (inwg)
25	5.2	239	0.18
30	6.0	280	0.22
35	7.2	335	0.29
40	8.9	413	0.38
45	11.4	530	0.55

Table 36: **UL3422 Inlet Temperature vs. Airflow (out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at 1800m above Sea Level for 123W Total Card Power with QSFP power at 3.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure (inwg)
25	5.7	267	0.21
30	6.7	312	0.26
35	8.1	374	0.33
40	9.9	462	0.45
45	12.8	594	0.65

Regulatory Compliance Statements

FCC Class A Products

***Note*:** These devices are for use with UL Listed Servers or I.T.E.

Safety Compliance

The following safety standards apply to all products listed above.

- EU LVD Directive 2014/35/EU
- IEC 62368-1:2020/A11:2020

EMC Compliance

The following standards apply.

Class A Products

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)
- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- Electromagnetic Compatibility Regulations 2016 (UK)
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS15936, C6459
- CNS 15663 - RoHS (Taiwan)
- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)

- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings

When required, these products are provided with the following Product Certification Markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark
- UKCA mark
- FCC markings
- VCCI marking
- Australian C-Tick mark
- Korea MSIP mark
- Taiwan BSMI mark

FCC Class A User Information

The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT! *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.*

IMPORTANT! *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

WICHTIG! *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

CAUTION! *If the device is changed or modified without permission from AMD, the user may void his or her authority to operate the equipment.*

ATTENTION! *Si l'appareil est modifié sans l'autorisation de AMD, l'utilisateur peut annuler son abilité à utiliser l'équipement.*

VORSICHT! *Wenn das Gerät ohne Erlaubnis von AMD geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.*

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

China RoHS Compliance

- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- RoHS 3 directive 2015/863
- EU 2015/863

VCCI Class A Statement

この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。
この場合には使用者が適切な対策を構ずるよう要求されることがあります。 VCCI-A

KCC Notice Class A (Republic of Korea Only)

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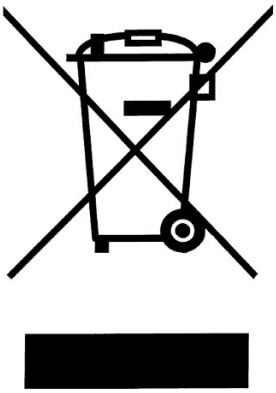
CLASS A device (commercial broadcasting and communication equipment	This device has been appoved by EMC registration. Distributors or users pay attention to this point. This device is usually aimed to be used in other area except at home

BSMI Class A Notice (Taiwan)

警告使用者:

此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適對當的對策。

EU WEEE Logo



Manufacturer Declaration European Community

Manufacturer Declaration

AMD declares that the equipment described in this document is in conformance with the requirements of the European Council Directive listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

This declaration is based upon compliance of the Class A products listed above to the following standards:

EN 55032 (CISPR 32 Class A) RF Emissions Control.

EN 55024:2010 (CISPR 24) Immunity to Electromagnetic Disturbance.

EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

CAUTION! *In a domestic environment, Class A products may cause radio interference, in which case the user may be required to take adequate measures.*

ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

AMD, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

References

These documents provide supplemental material useful with this data sheet:

1. *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213)
2. *Card Management Solution Subsystem Product Guide* (PG348)
3. *Alveo Card Debug Kit User Guide* (UG1538)
4. Alveo UL Cards Master Release Notes
5. *Renesas RC36812 datasheet* https://www.renesas.com/us/en/document/dst/rc38612-datasheet

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
10/14/2024 Version 1.0	
Initial release.	N/A

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