NCS10135AEP

Datasheet

Angular rate and acceleration sensor



Features

- z-axis angular rate sensor
  - Full-scale range of ±125 dps, ±250 dps or ±350 dps
  - Low offset and low offset drift over automotive temperature range
  - Low-pass filter with 3 dB frequency options of 12.5 Hz to 400 Hz
  - Optional single pole high-pass filter with fast startup
- xyz acceleration sensor
  - Ranges from ±1.50 *g* to ±34 *g* nominal full-scale range
  - Independent signal chains from ADC to communications interface
  - Low offset and low offset drift over automotive temperature range
  - Low-pass filter with 3 dB frequency options of 15 Hz to 400 Hz
  - Optional single pole high-pass filter with fast startup
- −40 °C to +105 °C operating temperature range
- 3.3 V single supply operation
- SafeSPI out-of-frame compatible
  - Register read and write commands
  - 16-bit data
  - 2-bit status field
  - 3-bit CRC
- Internal diagnostics
  - Angular rate
    - User-controlled angular rate self-test
    - Angular rate signal clip monitoring
    - Angular rate DSP self-test
  - Acceleration
    - User-controlled acceleration self-test
    - Acceleration signal clip monitoring
    - Acceleration DSP self-test
  - General
    - NVM with ECC
    - Runtime memory lock and 4-bit CRC verification
    - Internal voltage regulators with undervoltage and overvoltage detection
    - SPI-bus contention detection
    - Software reset control
- Pb-free 24-pin QFN 6 mm × 6 mm × 1.90 mm package

Description

NCS10135 is a SafeSPI compatible z-axis angular rate sensor and xyz acceleration sensor.

1 Ordering information

Table 1. Ordering information

Type number	Package	
	Name	Description
NCS10135	HQFN24	thermal enhanced quad flat package; no leads; 24 terminals; 0.1 mm dimple wettable flank; 0.8 mm pitch; 6 mm × 6 mm × 1.9 mm body

1.1 Ordering options

Table 2. Ordering options

Part number	Angular rate		Acceleration					
	ARC axis	Range	ACC0 axis	ACC0 range	ACC1 axis	ACC1 range	ACC2 axis	ACC2 range
NCS10135AEPR2	Ωz	125 dps, 250 dps, 350 dps	x	1.5 g to 34 g	y	1.5 g to 34 g	z	1.5 g to 34 g

2 Application diagram

Figure 1. **Application diagram**

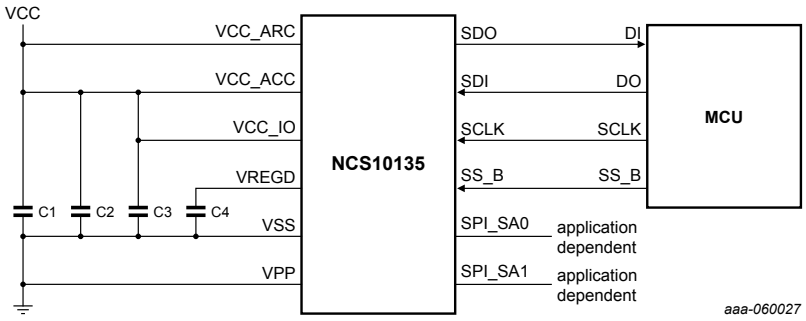
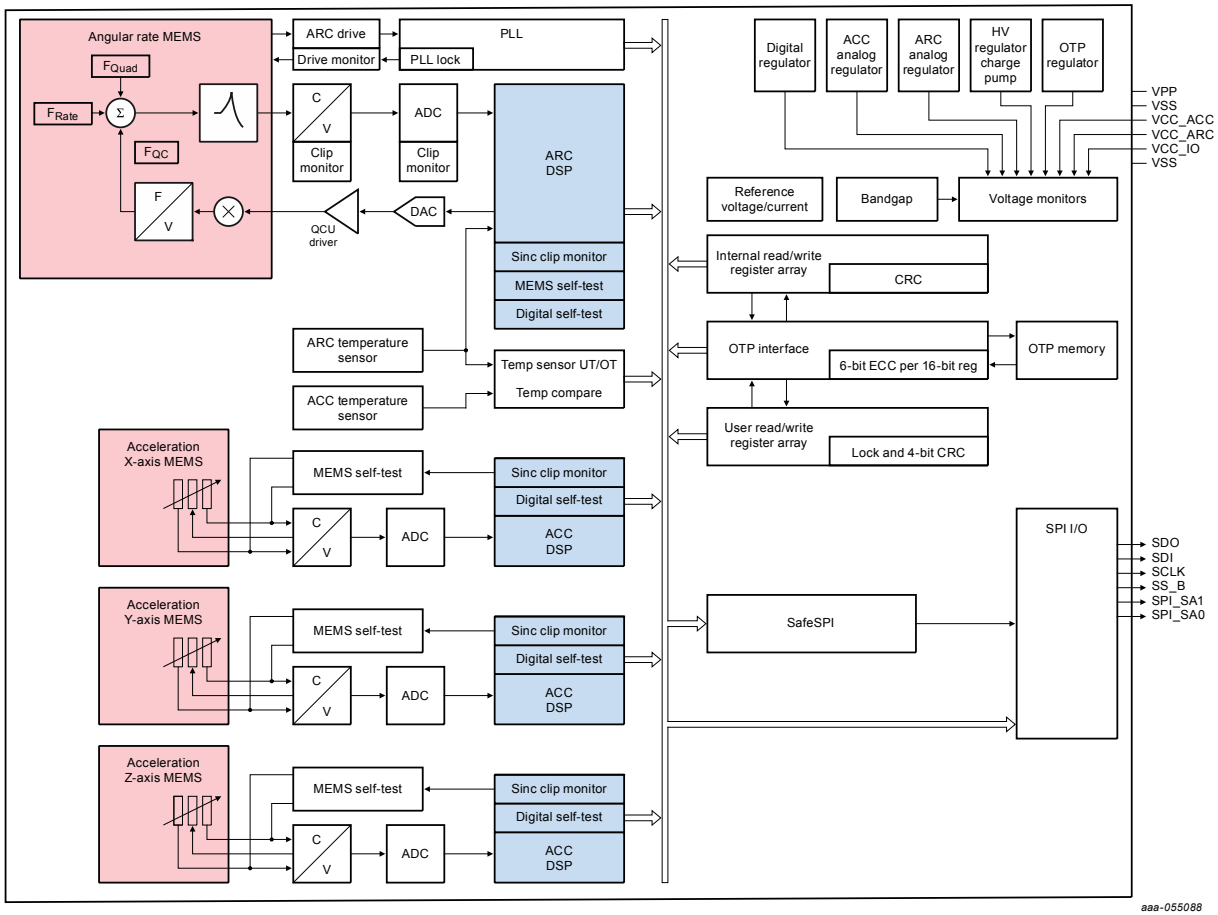


Table 3. **External component recommendations**

Component	Type	Description	Purpose
C1	ceramic	1 µF, 20 %, 10 V minimum, X7R	V_{CC_ARC} and V_{CC_ACC} power supply decoupling capacitor
C2	ceramic	0.1 µF, 20 %, 10 V minimum, X7R	V_{CC_ARC} and V_{CC_ACC} power supply decoupling capacitor
C3	ceramic	0.1 µF, 20 %, 10 V minimum, X7R	V_{CC_IO} power supply decoupling capacitor
C4	ceramic	0.1 µF, 20 %, 10 V minimum, X7R	V_{REGD} internal digital power supply decoupling capacitor (external capacitor for the internal digital supply)

3 Block diagram

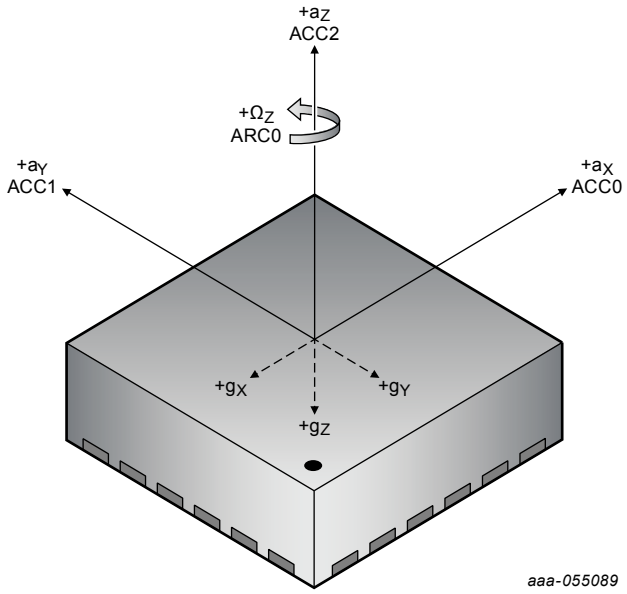
Figure 2. **Block diagram**



4 Orientation

Both accelerometer and gyroscope sensors share a common xyz reference frame. This single reference frame provides a right-handed xyz coordinate system for the combo data. Accelerometer data matches the gravity negative convention where earth gravity is reported as +1 g when aligned but opposite to the measurement axis. Angular rate polarity obeys the right-hand rule.

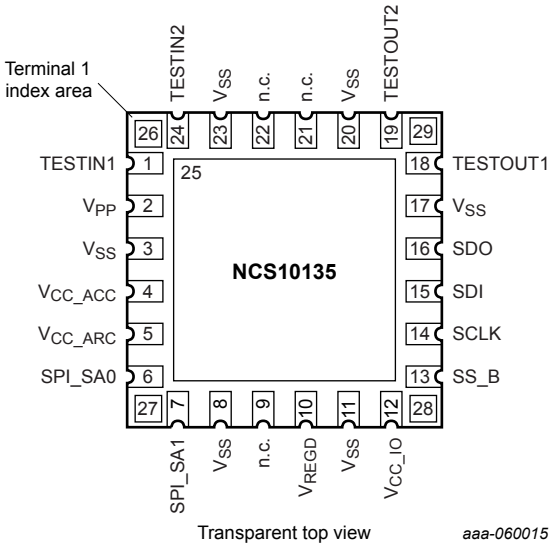
Figure 3. Sensor frame of reference



5 Pinning information

Pinning

Figure 4. Pin configuration diagram



Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
TESTINx	1, 24	input test pin	These pins are input test pins and must be connected to ground.
V_{PP}	2	test supply	This pin must be connected to ground.
V_{SS}	3, 8, 11, 17, 20, 23	supply return	These pins provide ground for the sensor and must be connected to ground.
V_{CC_ACC}	4	supply	This pin is the positive supply for the acceleration circuitry. Pins 4, 5 and 12 must be tied to the same supply voltage. A bypass capacitor is required as shown in Section 2: Application diagram.
V_{CC_ARC}	5	supply	This pin is the positive supply for the angular rate circuitry. Pins 4, 5 and 12 must be tied to the same supply voltage. A bypass capacitor is required as shown in Section 2: Application diagram.
SPI_SA0	6	sensor address select 0	This pin and pin 7 (SPI_SA1) define the 2-bit device sensor address for SafeSPI transfers. An internal pulldown device is connected to this pin; see Section 11.7: SafeSPI revision 2.0 protocol.
SPI_SA1	7	sensor address select 1	This pin and pin 6 (SPI_SA0) define the 2-bit device sensor address for SafeSPI transfers. An internal pulldown device is connected to this pin; see Section 11.7: SafeSPI revision 2.0 protocol.
n.c.	9, 21, 22	not connected	These pins are not connected.
V_{REGD}	10	digital supply	This pin is connected to the internal supply for the digital circuitry. An external capacitor must be connected between this pin and V_{SS} as shown in Section 2: Application diagram.
V_{CC_IO}	12	supply	This pin is the positive supply for the input and output pins. Pins 4, 5 and 12 must be tied to the same supply voltage. A bypass capacitor is required as shown in Section 2: Application diagram.
SS_B	13	sensor select	This input pin provides the sensor selection for the SPI port. An internal pull-up device is connected to this pin.
SCLK	14	SPI clock	This input pin provides the serial clock. An internal pull-down device is connected to this pin.

Symbol	Pin	Type	Description
SDI	15	sensor data input	This pin functions as the sensor serial data input to the SPI port. An internal pull-down device is connected to this pin.
SDO	16	sensor data output	This pin functions as the sensor serial data output to the SPI port.
TESTOUTx	18, 19	test output pin	These pins are output test pins and must be left unconnected.
PAD	25	die attach pad	This pin is the die attach flag and must be connected to V_{SS}; see Section 13: Package outline for die attach pad connection details.
	26, 27, 28, 29	corner pads	The corner pads are internally connected to the die attach flag and to V_{SS}; see Section 13: Package outline for corner pad details.

6 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{CC_ARC}	(1)	−0.3	-	+5.5	V
		on pin V_{CC_ACC}	(1)	−0.3	-	+5.5	V
		on pin V_{CC_IO}	(1)	−0.3	-	+5.5	V
V_{PP}	programming voltage		(1)	−0.3	-	+15.0	V
V_{CC}	supply voltage	on pin VREGD	(1)	−0.3	-	+2.0	V
		on pins SCLK, SS_B, SDI, SDO, SPI_SA0, SPI_SA1, TESTIN1, TESTIN2, TESTOUT1, TESTOUT2	(1)	−0.3	-	V_{CC_IO} + 0.3	V
g_{shock}	unpowered shock	qualification: six sides, 0.5 ms duration	(2)	−2000	-	+2000	g
g_{pms}	powered shock	evaluation: six sides, 0.1 ms duration	(1)	−5000	-	+5000	g
h_{drop}	drop shock	AEC-Q100; concrete surface; any orientation; 6 drops	(2)	-	1.2	-	m
Ω_{max}	maximum angular rate		(3)	−3000	-	+3000	dps
V_{ESD}	electrostatic discharge voltage	AEC-Q100; HBM (100 pF, 1.5 kΩ)	(2)	−2000	-	+2000	V
		AEC-Q100; CDM (R = 0 Ω)	(2)	−750	-	+750	V
T_{stg}	storage temperature		(2)	−40	-	+150	°C
T_j	junction temperature		(3)	−40	-	+150	°C

1. *Parameter verified by functional evaluation.*
2. *Parameter verified by qualification testing.*
3. *Functionality verified by modeling, simulation and/or design verification.*

7 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	(1)(2)(3)(4)	3.10	-	3.60	V
T_{amb}	ambient temperature	(3)	−40	-	+105	°C
$V_{P(POR)}$	power-on reset supply voltage	0 V to 3.3 V in 1 s (3)	3.3	-	-	V/s
		0 V to 3.3 V in 1 µs (4)	-	-	3.3	V/µs
V_{PDR}	power-down reset voltage	3.3 V to 0 V in 1 s (3)	−3.3	-	-	V/s
		3.3 V to 0 V in 1 µs (4)	-	-	3.3	V/µs

1. *Parameter tested 100 % at final test. Temperature = 25 °C and V_{CC} = 3.3 V, unless otherwise stated.*
2. *Parameter verified by qualification testing.*
3. *Parameter verified by characterization.*
4. *Functionality verified by modeling, simulation and/or design verification.*

8 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	(1)(2)	31	K/W

1. *Functionality verified by modeling, simulation and/or design verification.*
2. *Thermal resistance provided with device mounted to a JEDEC JESD51-7 4 layer, 2s2p PCB.*

9 Static characteristics

Table 8. Supply and I/O

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	average over a 50 ms period; 5000 samples minimum (1)	-	-	20.0	mA
$V_{th(rst)}$	reset threshold voltage	V_{CC} falling (2) (3)	2.72	2.86	3.09	V
V_{OH}	HIGH-level output voltage	on pin SDO; I_{load} = −1 mA (2) (3)	V_{CC} − 0.2	-	-	V
V_{OL}	LOW-level output voltage	on pin SDO; I_{load} = 1 mA (2) (3)	-	-	0.4	V
V_{IH}	HIGH-level input voltage	on pins SS_B, SCLK, SDI, SPI_SA0, SPI_SA1; V_{CC_IO} = 3.3 V (2) (3)	$0.7V_{CC_IO}$	-	-	V
V_{IL}	LOW-level input voltage	on pins SS_B, SCLK, SDI, SPI_SA0, SPI_SA1; V_{CC_IO} = 3.3 V (2) (3)	-	-	$0.3V_{CC_IO}$	V
I_{IH}	HIGH-level input current	on pins SCLK, SDI, SPI_SA0, SPI_SA1; V_I = 3.3 V (1)	10	-	70	µA
I_{IL}	LOW-level input current	on pin SS_B; V_I = 3.3 V (1)	−70	-	−10	µA
I_{LO}	output leakage current	on pin SDO (3)	−10	-	+10	µA

1. *Parameter tested 100 % at final test. Temperature = 25 °C and V_{CC} = 3.3 V, unless otherwise stated.*
2. *Parameter verified by pass/fail testing at final test.*
3. *Parameter verified by characterization.*

Table 9. Temperature sensor signal chain

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_j	junction temperature	(1)(2)	−50	-	+160	°C
T_{sen}	sensor temperature	T_{amb} = 25 °C (1)(3)	20480	23040	25600	LSB
		16-bit unsigned data (1)(2)(4)	0	-	65535	LSB
S_{temp}	temperature sensitivity	−50 °C < T_{amb} < +160 °C (1)(3)	-	256	-	LSB/°C
T_{acc}	temperature accuracy	−50 °C < T_{amb} < +160 °C (1)(3)	−10	-	+10	°C
$T_{n(o)(RMS)}$	RMS output noise temperature	standard deviation of 1000 readings; f_{sample} = 100 Hz (1)(3)	-	-	256	LSB
$T_{th(act)utp}$	undertemperature protection activation threshold temperature	(1)(3)	-	−60	-	°C
$T_{th(act)otp}$	overtemperature protection activation threshold temperature	(1)(3)	-	180	-	°C

1. *Functionality verified by modeling, simulation and/or design verification.*
2. *Parameter verified by functional evaluation.*
3. *Parameter verified by characterization.*
4. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*

Table 10. Angular rate sensor signal chain

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S_{ar125}	angular rate sensitivity	full-scale range: ±125 dps	(1)	254.27	262.14	270.00	LSB/dps
S_{ar250}	angular rate sensitivity	full-scale range: ±250 dps	(2)	127.14	131.07	135.00	LSB/dps
S_{ar350}	angular rate sensitivity	full-scale range: ±350 dps	(2)	63.568	65.534	67.500	LSB/dps
OFF_{ar}	angular rate offset	offset cancellation disabled; full-scale range: ±125 dps; average of 2000 samples at > 1 kHz sample rate	(1)	−787	-	+787	LSB
OFF_{ar25}	angular rate offset	T_{amb} = 25 °C; offset cancellation disabled; full-scale range: ±125 dps; average of 2000 samples at > 1 kHz sample rate	(1)	−262	-	+262	LSB
$OFF_{ar(oc)}$	angular rate offset	offset cancellation enabled; full-scale range: ±125 dps; average of 2000 samples at > 1 kHz sample rate	(2)(3)(4)	−26	-	+26	LSB
$OFF_{ar(temp)}$	angular rate offset	−40 °C < T_{amb} < +105 °C; ΔT = 5 °C/min; full-scale range: ±125 dps; maximum delta between min and max values over any 60 °C window	(2)(5)	-	-	525	LSB
$OFF_{ar(drift)}$	angular rate offset drift	full-scale range: ±125 dps; maximum drift from power on to 5 minutes after power on	(2)	−78	-	+78	LSB
		constant T_{amb}; full-scale range: ±125 dps; sample rate > 1 kHz; maximum difference among 1 min moving averages over a 15 min period	(2)	-	-	52	LSB
$OFF_{ar(repeat)}$	angular rate offset repeatability	ΔT < 5 °C/min; repeatability of offset at any one temperature after temperature cycling; full-scale range: ±125 dps	(2)	−78	-	+78	LSB
$S_{yz(ar)}$	angular rate cross-axis sensitivity	y-axis to z-axis	(2)	−2.5	-	+2.5	%
$S_{xz(ar)}$	angular rate cross-axis sensitivity	x-axis to z-axis	(2)	−2.5	-	+2.5	%
NL_{ar100}	angular rate nonlinearity	least squares best fit straight line (BFSL); integral nonlinearity up to ±100 dps; full-scale range: ±125 dps	(2)	-	-	131	LSB
NL_{ar350}	angular rate nonlinearity	least squares BFSL; integral nonlinearity up to ±350 dps; full-scale range: ±350 dps	(2)	-	-	66	LSB
MNL_{ar}	angular rate micrononlinearity	maximum deviation from BFSL; 2.5 dps intervals; full-scale range: ±125 dps	(2)	−5.0	-	+5.0	%
NAV_{ar}	angular rate noise average	one standard deviation; full-scale range: ±125 dps; minimum 2000 samples; minimum f_s = 1 kHz; f_{LPF} = 50 Hz; 4-pole	(2)	-	-	30.0	LSB
AST_{ar}	angular rate analog self-test	on-demand self-test; full-scale range: ±125 dps	(1)	±1440	±2881	±4322	LSB
ΔST_{ar}	angular rate self-test accuracy	delta from value stored in ARC0_ST_CMP[15:0]	(1)	−20	-	+20	%
DST_{ar}	angular rate digital self-test	full-scale range: ±125 dps; offset cancellation disabled; digital self-test Ch	(1)(4)(6)	16723	16724	16725	LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DST_{ar}	angular rate digital self-test	full-scale range: ±125 dps; offset cancellation disabled; digital self-test Dh (1)(4)(6)	−18486	−18485	−18484	LSB
		full-scale range: ±125 dps; offset cancellation disabled; digital self-test Eh (1)(4)(6)	1395	1396	1397	LSB
		full-scale range: ±125 dps; offset cancellation disabled; digital self-test Fh (1)(4)(6)	−2614	−2613	−2612	LSB

1. *Parameter tested 100 % at final test. Temperature = 25 °C and V_{CC} = 3.3 V, unless otherwise stated.*
2. *Parameter verified by characterization.*
3. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*
4. *Parameter verified by functional evaluation.*
5. *Parameter verified by qualification testing.*
6. *Functionality verified by modeling, simulation and/or design verification.*

Table 11. Acceleration sensor signal chain

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$S_{a(1g5)}$	acceleration sensitivity	±1.50 g range (1)	21180	21835	22490	LSB/g
OFF_a	acceleration offset	offset cancellation disabled; ±1.50 g range; average of 2000 samples at > 1 kHz sample rate (1)	−1638	-	+1638	LSB
$OFF_{a(oc)}$	acceleration offset	offset cancellation enabled; ±1.50 g range; average of 2000 samples at > 1 kHz sample rate (2)(3)(4)	−16	0	+16	LSB
$OFF_{a(temp)}$	acceleration offset due to temperature	−40 °C < T_{amb} < +105 °C; ΔT = 5 °C/min; offset cancellation disabled; ±1.50 g range; maximum delta between min and max values over any 60 °C window (2)(5)	-	-	655	LSB
$OFF_{a(drift)}$	acceleration offset drift	offset cancellation disabled; ±1.50 g range; average of 2000 samples at > 1 kHz sample rate; maximum drift from power on to 5 minutes after power on; constant temperature (2)	−218	-	+218	LSB
$OFF_{a(drift)t}$	acceleration offset drift over time	offset cancellation disabled; ±1.50 g range; sample rate > 1 kHz; maximum difference among 1 minute moving averages over a 15 minute period (2)	-	-	218	LSB
$S_{zx(a)}$	acceleration cross-axis sensitivity	z-axis to x-axis (2)	−2.5	-	+2.5	%
$S_{yx(a)}$	acceleration cross-axis sensitivity	y-axis to x-axis (2)	−2.5	-	+2.5	%
$S_{zy(a)}$	acceleration cross-axis sensitivity	z-axis to y-axis (2)	−2.5	-	+2.5	%
$S_{xy(a)}$	acceleration cross-axis sensitivity	x-axis to y-axis (2)	−2.5	-	+2.5	%
$S_{xz(a)}$	acceleration cross-axis sensitivity	x-axis to z-axis (2)	−2.5	-	+2.5	%
$S_{yz(a)}$	acceleration cross-axis sensitivity	y-axis to z-axis (2)	−2.5	-	+2.5	%
$A_{n(a)(RMS)(60)}$	RMS acceleration noise average	one standard deviation; ±1.50 g range; minimum 2000 samples; minimum f_s = 2 kHz; f_{LPF} = 60 Hz; 2-pole (2)	-	-	74.2	LSB
$INL_{a1.5}$	acceleration integral non-linearity	least squares BFSL; ±1.5 g range (2)	-	-	328	LSB
INL_{a6}	acceleration integral non-linearity	least squares BFSL; ±6.0 g range (2)	-	-	82	LSB
INL_{a24}	acceleration integral non-linearity	least squares BFSL; ±24.0 g range (2)	-	-	328	LSB
INL_{a34}	acceleration integral non-linearity	least squares BFSL; ±34.0 g range (2)	-	-	579	LSB
MNL_{a24}	acceleration micrononlinearity	maximum deviation from BFSL for 0.1 g interval up to ±24 g (2)	−5.0	-	+5.0	%
ST_{xl}	x-axis self-test	low self-test (1)	512	1462	2412	LSB
ST_{xh}	x-axis self-test	high self-test (1)	1382	3948	6514	LSB
ST_{yl}	y-axis self-test	low self-test (1)	512	1462	2412	LSB
ST_{yh}	y-axis self-test	high self-test (1)	1382	3948	6514	LSB
ST_{zl}	z-axis self-test	low self-test (1)	414	1182	1950	LSB
ST_{zh}	z-axis self-test	high self-test (1)	1064	3039	5014	LSB
ΔST_{aplx}	x-axis low positive acceleration self-test accuracy	delta from value stored in ACC0_STL_P[15:0] (1)	−10	-	+10	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔST_{anlx}	x-axis low negative acceleration self-test accuracy	delta from value stored in ACC0_STL_N[15:0] (1)	−10	-	+10	%
ΔST_{aphx}	x-axis high positive acceleration self-test accuracy	delta from value stored in ACC0_STH_P[15:0] (1)	−10	-	+10	%
ΔST_{anhx}	x-axis high negative acceleration self-test accuracy	delta from value stored in ACC0_STH_N[15:0] (1)	−10	-	+10	%
ΔST_{aply}	y-axis low positive acceleration self-test accuracy	delta from value stored in ACC1_STL_P[15:0] (1)	−10	-	+10	%
ΔST_{anly}	y-axis low negative acceleration self-test accuracy	delta from value stored in ACC1_STL_N[15:0] (1)	−10	-	+10	%
ΔST_{aphy}	y-axis high positive acceleration self-test accuracy	delta from value stored in ACC1_STH_P[15:0] (1)	−10	-	+10	%
ΔST_{anhy}	y-axis high negative acceleration self-test accuracy	delta from value stored in ACC1_STH_N[15:0] (1)	−10	-	+10	%
ΔST_{aplz}	z-axis low positive acceleration self-test accuracy	delta from value stored in ACC2_STL_P[15:0] (1)	−10	-	+10	%
ΔST_{anlz}	z-axis low negative acceleration self-test accuracy	delta from value stored in ACC2_STL_N[15:0] (1)	−10	-	+10	%
ΔST_{aphz}	z-axis high positive acceleration self-test accuracy	delta from value stored in ACC2_STH_P[15:0] (1)	−10	-	+10	%
ΔST_{anhz}	z-axis high negative acceleration self-test accuracy	delta from value stored in ACC2_STH_N[15:0] (1)	−10	-	+10	%
DST	digital self-test	1 × gain; offset cancellation disabled; digital self-test Ch (1)(4)(6)	−6101	−6100	−6099	LSB
		1 × gain; offset cancellation disabled; digital self-test Dh (1)(4)(6)	4023	4024	4025	LSB
		1 × gain; offset cancellation disabled; digital self-test Eh (1)(4)(6)	−4069	−4068	−4067	LSB
		1 × gain; offset cancellation disabled; digital self-test Fh (1)(4)(6)	2005	2006	2007	LSB
DST	digital self-test	8 × gain; offset cancellation disabled; digital self-test Ch (1)(4)(6)	−32767	−32767	−32767	LSB
		8 × gain; offset cancellation disabled; digital self-test Dh (1)(4)(6)	32196	32197	32198	LSB
		8 × gain; offset cancellation disabled; digital self-test Eh (1)(4)(6)	−32542	−32541	−32540	LSB
		8 × gain; offset cancellation disabled; digital self-test Fh (1)(4)(6)	16054	16055	16056	LSB

1. *Parameter tested 100 % at final test. Temperature = 25 °C and V_{CC} = 3.3 V, unless otherwise stated.*
2. *Parameter verified by characterization.*
3. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*
4. *Parameter verified by functional evaluation.*
5. *Parameter verified by qualification testing.*
6. *Functionality verified by modeling, simulation and/or design verification.*

10 Dynamic characteristics

Table 12. SafeSPI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SCLK}	SCLK period	10 % of V_{CC} to 10 % of V_{CC} (1)	88	-	-	ns
$t_{clk(H)}$	clock HIGH time	90 % of V_{CC} to 90 % of V_{CC} (1)	30	-	-	ns
$t_{clk(L)}$	clock LOW time	10 % of V_{CC} to 10 % of V_{CC} (1)	30	-	-	ns
$t_{r(clk)}$	clock rise time	10 % of V_{CC} to 90 % of V_{CC} (2)	-	10	25	ns
$t_{f(clk)}$	clock fall time	90 % of V_{CC} to 10 % of V_{CC} (2)	-	10	25	ns
$t_{SPILEAD}$	SPI enable lead time	SS_B asserted to SCLK HIGH; SS_B = 10 % of V_{CC} to SCLK = 10 % of V_{CC} (1)	50	-	-	ns
t_{SPIA}	SPI access time	SS_B asserted to SDO valid; C_{SDO} < 100 pF; R_{SDO} < 10 kΩ; SS_B = 10 % of V_{CC} to SDO = 0 % to 90 % OR 100 % to 10 % of V_{CC} (1)	-	-	50	ns
$t_{su(D)}$	data input set-up time	SDI = 0 % to 90 % OR 100 % to 10 % of V_{CC} to SCLK = 10 % of V_{CC} (1)	20	-	-	ns
$t_{h(SDI)}$	SDI hold time	SCLK = 90 % of V_{CC} to SDI = 0 % to 90 % OR 100 % to 10 % of V_{CC} (1)	10	-	-	ns
$t_{h(SDO)}$	SDO hold time	C_{SDO} < 100 pF; R_{SDO} < 10 kΩ; SCLK = 90 % of V_{CC} to SDO = 0 % to 90 % OR 100 % to 10 % of V_{CC} (1)	0	-	-	ns
$t_{v(SDO)}$	SDO valid time	SCLK LOW to data valid; C_{SDO} < 100 pF; R_{SDO} < 10 kΩ; SCLK = 10 % of V_{CC} to SDO = 0 % to 90 % OR 100 % to 10 % of V_{CC} (1)	-	-	30	ns
t_{SPILAG}	SPI enable lag time	SCLK LOW to SS_B HIGH; SCLK = 10 % of V_{CC} to SS_B = 90 % of V_{CC} (1)	60	-	-	ns
$t_{dis(SDO)}$	SDO disable time	SS_B HIGH to SDO disable; C_{SDO} < 100 pF; R_{SDO} < 10 kΩ; SS_B = 90 % of V_{CC} to SDO = high-Z (1)	-	-	60	ns
$t_{WH(S)}$	chip select pulse width HIGH	SS_B HIGH to SS_B LOW; SS_B = 90 % of V_{CC} to SS_B = 90 % of V_{CC}; following register reads or writes (1)	450	-	-	ns
		SS_B HIGH to SS_B LOW; SS_B = 90 % of V_{CC} to SS_B = 90 % of V_{CC}; following register writes to UF_REGION_W register (1)	50	-	-	µs
$t_{SPILEAD}$	SPI enable lead time	SCLK LOW to SS_B LOW; SCLK = 10 % of V_{CC} to SS_B = 90 % of V_{CC} (1)	50	-	-	ns
$t_{d(SS_BH-SCLKH)}$	delay time from SS_B HIGH to SCLK HIGH	SS_B HIGH to SCLK HIGH; SS_B = 90 % of V_{CC} to SCLK = 90 % of V_{CC} (1)	50	-	-	ns
$t_{d(o)(\omega)}$	angular rate output delay time	(2)(3)	-	-	$t_{d(s)}$	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(o)(a)}$	acceleration output delay time	interpolation bypassed (2)(3)	-	-	$t_{d(s)(a)}$	µs
		interpolation enabled (2)(3)	$t_{d(s)(a)}$	-	$2 \times t_{d(s)(a)}$	µs
C_{SDO}	capacitance on pin SDO	(2)	-	-	10	pF
C_{SDI}	capacitance on pin SDI	(2)	-	-	10	pF
C_{SCLK}	capacitance on pin SCLK	(2)	-	-	10	pF
C_{SS_B}	capacitance on pin SS_B	(2)	-	-	10	pF

1. *Parameter verified by characterization.*
2. *Functionality verified by modeling, simulation and/or design verification.*
3. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*

Table 13. Angular rate sensor signal chain

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(s)}$	sampling delay time	ARC0_SAMPLERATE[1:0] = 0h (1)(2)	333	400	500	µs
		ARC0_SAMPLERATE[1:0] = 1h (1)(2)	667	800	1000	µs
		ARC0_SAMPLERATE[1:0] = 2h (1)(2)	1333	1600	2000	µs
$f_{-3dB(ARC)}$	ARC cut-off frequency	ARC0_LPF[1:0] = 0h; ARC0_SAMPLERATE[1:0] = 0h (1)(2)	47.70	49.60	51.30	Hz
		ARC0_LPF[1:0] = 0h; ARC0_SAMPLERATE[1:0] = 1h (1)(2)	24.10	24.90	25.70	Hz
		ARC0_LPF[1:0] = 0h; ARC0_SAMPLERATE[1:0] = 2h (1)(2)	12.00	12.50	12.90	Hz
		ARC0_LPF[1:0] = 1h; ARC0_SAMPLERATE[1:0] = 0h (1)(2)	47.60	49.50	51.20	Hz
		ARC0_LPF[1:0] = 1h; ARC0_SAMPLERATE[1:0] = 1h (1)(2)	24.00	24.90	25.70	Hz
		ARC0_LPF[1:0] = 1h; ARC0_SAMPLERATE[1:0] = 2h (1)(2)	12.00	12.50	12.90	Hz
		ARC0_LPF[1:0] = 2h; ARC0_SAMPLERATE[1:0] = 0h (1)(2)	56.70	59.10	61.20	Hz
		ARC0_LPF[1:0] = 2h; ARC0_SAMPLERATE[1:0] = 1h (1)(2)	28.70	29.80	30.80	Hz
		ARC0_LPF[1:0] = 2h; ARC0_SAMPLERATE[1:0] = 2h (1)(2)	14.40	14.90	15.40	Hz
		ARC0_LPF[1:0] = 3h; ARC0_SAMPLERATE[1:0] = 0h (1)(2)	273.7	356.4	425.3	Hz
		ARC0_LPF[1:0] = 3h; ARC0_SAMPLERATE[1:0] = 1h (1)(2)	191.5	232.6	264.3	Hz
		ARC0_LPF[1:0] = 3h; ARC0_SAMPLERATE[1:0] = 2h (1)(2)	111.5	129.2	143.0	Hz
$t_{startup(oc)(\omega)}$	angular rate offset cancellation startup time	maximum time from ±1000 LSB offset to within OC parameter range (1)(2)	-	-	30	ms
$f_{-3dB(oc)(ARC)}$	ARC offset cancellation cut-off frequency	normal mode; phase 6a (1)(2)	-	0.040	-	Hz
		normal mode; phase 6b (1)(2)	-	0.005	-	Hz
$t_{upd(o)}$	output update time	ARC rate limiting (1)(2)	-	0.125	-	s
$\omega_{RL(step)(125)}$	ARC rate limiting step size option 0	ARC_DATATYPEx[1:0] = 0h (1)(2)	-	1	-	LSB
$\omega_{RL(step)(250)}$	ARC rate limiting step size option 1	ARC_DATATYPEx[1:0] = 1h (1)(2)	-	0.5	-	LSB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\omega_{RL(step)(350)}$	ARC rate limiting step size option 2	ARC_DATATYPEx[1:0] = 2h	(1)(2)	-	0.25	-	LSB
t_{resp}	response time	ARC self-test activation or deactivation; all LPF selections	(1)(2)	-	-	30	ms
		ARC digital self-test activation or deactivation to final value; f_{LPF} = 50 Hz; 4-pole	(1)(2)	-	-	40	ms
		ARC fixed pattern self-test activation or deactivation	(1)(2)	-	-	100	µs
t_{det}	detection time	railed signal to ARC0_SIGCLIP set; ARC0_SIGCLIP_FILT[1:0] = 00	(1)(2)	0.750	1.024	1.250	ms
		railed signal to ARC0_SIGCLIP set; ARC0_SIGCLIP_FILT[1:0] = 01	(1)(2)	3.000	4.096	5.000	ms
		railed signal to ARC0_SIGCLIP set; ARC0_SIGCLIP_FILT[1:0] = 10	(1)(2)	6.000	8.192	10.000	ms
		railed signal to ARC0_SIGCLIP set; ARC0_SIGCLIP_FILT[1:0] = 11	(1)(2)	12.000	16.384	20.000	ms

1. *Functionality verified by modeling, simulation and/or design verification.*
2. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*

Table 14. Acceleration sensor signal chain

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(s)(a)}$	acceleration sampling delay time	ACCx_SAMPLERATE[1:0] = 0h (16 kHz)	(1)(2)	52.10	62.50	78.13	µs
		ACCx_SAMPLERATE[1:0] = 1h (8 kHz)	(1)(2)	104.2	125.0	156.3	µs
		ACCx_SAMPLERATE[1:0] = 2h (4 kHz)	(1)(2)	208.3	250.0	312.5	µs
$f_{-3dB(ACC)}$	ACC cut-off frequency	x-axis and y-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	58.00	60.00	61.80	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	29.00	30.00	30.90	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	14.50	15.00	15.50	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	245.80	261.10	272.00	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	126.80	131.80	136.20	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	63.90	66.10	68.20	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	352.90	387.00	408.70	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	188.40	197.70	205.00	Hz

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{-3dB(ACC)}$	ACC cut-off frequency	x-axis and y-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	95.90	99.40	102.60	Hz
		x-axis and y-axis; ACCx_LPF[1:0] = 3h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	344.78	387.1	415.99	Hz
$f_{-3dB(ACC)}$	ACC cut-off frequency	z-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	57.40	59.80	61.80	Hz
		z-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	29.00	30.00	30.90	Hz
		z-axis; ACCx_LPF[1:0] = 0h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	14.50	15.00	15.50	Hz
		z-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	214.20	247.90	266.10	Hz
		z-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	121.40	130.00	135.40	Hz
		z-axis; ACCx_LPF[1:0] = 1h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	63.20	65.80	68.10	Hz
		z-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 0h	(1)(2)	277.70	348.90	389.80	Hz
		z-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 1h	(1)(2)	172.50	191.70	202.40	Hz
		z-axis; ACCx_LPF[1:0] = 2h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	93.50	98.60	102.30	Hz
		z-axis; ACCx_LPF[1:0] = 3h; ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	274.47	349.84	396.56	Hz
$t_{startup(oc)(a)}$	acceleration offset cancellation startup time	maximum time from ±1000 LSB offset to within OC parameter range	(1)(2)	-	-	30	ms
$f_{-3dB(oc)(ACC)}$	ACC offset cancellation cut-off frequency	normal mode; phase 6a	(1)(2)	-	0.040	-	Hz
		normal mode; phase 6b	(1)(2)	-	0.005	-	Hz
$t_{upd(o)}$	output update time	ACC rate limiting	(1)(2)	-	0.061	-	s
$A_{RL(step)}$	acceleration offset cancellation output rate limiting	rate limiting output step size	(1)(2)	-	1	-	LSB
t_{resp}	response time	analog self-test response; ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 2h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 2h or ACCx_LPF[1:0] = 3h and ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	-	-	13	ms
t_{resp}	response time	analog self-test response; ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	-	-	45	ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{resp}	response time	digital self-test response; ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 1h and ACCx_SAMPLERATE[1:0] = 2h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 0h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 2h and ACCx_SAMPLERATE[1:0] = 2h or ACCx_LPF[1:0] = 3h and ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	-	-	25	ms
		digital self-test response; ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 1h or ACCx_LPF[1:0] = 0h and ACCx_SAMPLERATE[1:0] = 2h	(1)(2)	-	-	100	ms
		ACC fixed pattern self-test activation or deactivation	(1)(2)	-	-	100	µs
t_{det}	detection time	railed signal to ACC0_SIGCLIP set; ACC0_SIGCLIP_FILT[1:0] = 00; railed signal to ACC1_SIGCLIP set; ACC1_SIGCLIP_FILT[1:0] = 00; railed signal to ACC2_SIGCLIP set; ACC2_SIGCLIP_FILT[1:0] = 00	(1)(2)	0.750	1.024	1.250	ms
		railed signal to ACC0_SIGCLIP set; ACC0_SIGCLIP_FILT[1:0] = 01; railed signal to ACC1_SIGCLIP set; ACC1_SIGCLIP_FILT[1:0] = 01; railed signal to ACC2_SIGCLIP set; ACC2_SIGCLIP_FILT[1:0] = 01	(1)(2)	3.000	4.096	5.000	ms
t_{det}	detection time	railed signal to ACC0_SIGCLIP set; ACC0_SIGCLIP_FILT[1:0] = 10; railed signal to ACC1_SIGCLIP set; ACC1_SIGCLIP_FILT[1:0] = 10; railed signal to ACC2_SIGCLIP set; ACC2_SIGCLIP_FILT[1:0] = 10	(1)(2)	6.000	8.192	10.000	ms
		railed signal to ACC0_SIGCLIP set; ACC0_SIGCLIP_FILT[1:0] = 11; railed signal to ACC1_SIGCLIP set; ACC1_SIGCLIP_FILT[1:0] = 11; railed signal to ACC2_SIGCLIP set; ACC2_SIGCLIP_FILT[1:0] = 11	(1)(2)	12.000	16.384	20.000	ms

1. *Functionality verified by modeling, simulation and/or design verification.*
2. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*

Table 15. Supply and support circuitry

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{startup}$	startup time	power on to SPI communications ready; excluding V_{CC} voltage ramp time power up ($V_{CC} = V_{CC(min)}$) to first SPI command with response	(1)(2)(3)	-	-	3.00	ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{startup}$	startup time	power on to ARC sensor data ready; excluding V_{CC} voltage ramp time power up (V_{CC} = $V_{CC(min)}$) to ARC0_DEVINIT = 0	(1)(2)(3)	-	-	110	ms
		power on to ACC sensor data ready; excluding V_{CC} voltage ramp time power up (V_{CC} = $V_{CC(min)}$) to ACCx_DEVINIT = 0	(1)(2)(3)	-	-	110	ms
$t_{v(data)}$	data valid time	ARC DSP setting changes to angular rate sensor data valid; ARC_SAMPLERATE[1:0] = 00	(1)(2)(3)	-	-	22	ms
		ARC DSP setting changes to angular rate sensor data valid; ARC_SAMPLERATE[1:0] = 01	(1)(2)(3)	-	-	44	ms
		ARC DSP setting changes to angular rate sensor data valid; ARC_SAMPLERATE[1:0] = 10	(1)(2)(3)	-	-	88	ms
$t_{v(data)}$	data valid time	ACC DSP setting changes to acceleration sensor data valid; ACCx_SAMPLERATE[1:0] = 00	(1)(2)(3)	-	-	22	ms
		ACC DSP setting changes to acceleration sensor data valid; ACCx_SAMPLERATE[1:0] = 01	(1)(2)(3)	-	-	44	ms
		ACC DSP setting changes to acceleration sensor data valid; ACCx_SAMPLERATE[1:0] = 10	(1)(2)(3)	-	-	88	ms
t_{act}	activation time	soft reset activation time; SS_B HIGH after last soft reset command to device reset		-	-	700	ns

1. *Functionality verified by modeling, simulation and/or design verification.*
2. *Circuit integrity assured through IDDQ and scan testing. The internal system clock frequency determines the timing.*
3. *Parameter verified by functional evaluation.*

11 Functional description

11.1 User-accessible data array

A user-accessible data array allows for each device to be customized. The array consists of an ST one time programmable (OTP) block, a user programmable block, and read-only registers for data and device status. The memory includes error detection as documented in Section 11.3: OTP and read/write register array error detection.

11.1.1 General device information

Table 16. General device information

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
R	00	COUNT_L	COUNT.7	COUNT.6	COUNT.5	COUNT.4	COUNT.3	COUNT.2	COUNT.1	COUNT.0
R	01	COUNT_H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	COUNT.9	COUNT.8
R	02	DEVSTAT_SUM_L	ARC0_ERR	RESERVED	RESERVED	ACC0_ERR	ACC1_ERR	ACC2_ERR	COMM_ERR	MEMTEMP_ERR
R	03	DEVSTAT_SUM_H	TESTMODE	DEVRES	ARC0_DEVINIT	RESERVED	RESERVED	ACC0_DEVINIT	ACC1_DEVINIT	ACC2_DEVINIT
R	04	DEVSTAT_DET_L	ARC0_PLL_ERR	ARC0_DAU_ERR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R	05	DEVSTAT_DET_H	F_OTP_ERR	RESERVED	U_RW_ERR	CONT_ERR	RESERVED	RESERVED	TEMP_SNS_ERR	SDO_ERR
R	06	ACC0_STAT	ACC0_SIGCLIP	ACC0_OCPHASE[2:0]			ACC0_ST_INC	ACC0_ST_ ACTIVE	RESERVED	RESERVED
R	07	ACC1_STAT	ACC1_SIGCLIP	ACC1_OCPHASE[2:0]			ACC1_ST_INC	ACC1_ST_ ACTIVE	RESERVED	RESERVED
R	08	ACC2_STAT	ACC2_SIGCLIP	ACC2_OCPHASE[2:0]			ACC2_ST_INC	ACC2_ST_ ACTIVE	RESERVED	RESERVED
R	09	ARC0_STAT	ARC0_SIGCLIP	ARC0_OCPHASE[2:0]			ARC0_ST_INC	ARC0_ST_ ACTIVE	RESERVED	RESERVED
R	0A to 0D	RESERVED	RESERVED							
R	0E	TEMPERATURE_L	TEMPERATURE[7:0]							
R	0F	TEMPERATURE_H	TEMPERATURE[15:8]							

11.1.2 Communication information

Table 17. **Communication information**

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
R/W	10	DEVLOCK_WR	ENDINIT	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESET[1:0]	
R/W	11 to 13	RESERVED	RESERVED							
R/W	14	F_REGION_W	REGION_LOAD[3:0]				0	0	0	0
R	15	F_REGION_R	REGION_ACTIVE[3:0]				0	0	0	0
R/W	16 to 3D	RESERVED	RESERVED							
R	3E	SPI_ SADDR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SPI_SA[1:0]	
R	3F	RESERVED	RESERVED							

11.1.3 Sensor specific information

Table 18. **Sensor specific information**

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
R/W	40	ARC0_CFG_U1	RESERVED	RESERVED	ARC0_LPF[1:0]		ARC0_SAMPLERATE[1:0]		RESERVED	RESERVED
R/W	41	RESERVED	RESERVED							
R/W	42	ARC0_CFG_U3	ARC0_DATATYPE0[2:0]			ARC0_DATATYPE1[2:0]			RESERVED	RESERVED
R/W	43	ARC0_CFG_U4	ARC0_RESET_OC	RESERVED	ARC0_OC_FILT[1:0]		RESERVED	RESERVED	ARC0_SIGCLIP_FLT[1:0]	
R/W	44	ARC0_CFG_U5	ARC0_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
R/W	45 to 57	RESERVED	RESERVED							
R/W	58	ACC0_CFG_U1	ACC0_LPF1[1:0]		ACC0_LPF0[1:0]		ACC0_SAMPLERATE[1:0]		ACC0_USER_SNS_SHIFT[1:0]	
R/W	59	ACC0_CFG_U2	ACC0_U_SNS_MULT[7:0]							
R/W	5A	ACC0_CFG_U3	ACC0_DATATYPE0[2:0]			ACC0_DATATYPE1[2:0]			RESERVED	RESERVED
R/W	5B	ACC0_CFG_U4	ACC0_RESET_OC	RESERVED	ACC0_OC_FILT[1:0]		RESERVED	RESERVED	ACC0_SIGCLIP_FLT[1:0]	
R/W	5C	ACC0_CFG_U5	ACC0_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
R/W	5D to 5F	RESERVED	RESERVED							
R/W	60	ACC1_CFG_U1	ACC1_LPF1[1:0]		ACC1_LPF0[1:0]		ACC1_SAMPLERATE[1:0]		ACC1_USER_SNS_SHIFT[1:0]	

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
R/W	61	ACC1_CFG_U2	ACC1_U_SNS_MULT[7:0]							
R/W	62	ACC1_CFG_U3	ACC1_DATATYPE0[2:0]			ACC1_DATATYPE1[2:0]			RESERVED	RESERVED
R/W	63	ACC1_CFG_U4	ACC1_RESET_OC	RESERVED	ACC1_OC_FILT[1:0]		RESERVED	RESERVED	ACC1_SIGCLIP_FLT[1:0]	
R/W	64	ACC1_CFG_U5	ACC1_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
R/W	65 to 67	RESERVED	RESERVED							
R/W	68	ACC2_CFG_U1	ACC2_LPF1[1:0]		ACC2_LPF0[1:0]		ACC2_SAMPLERATE[1:0]		ACC2_USER_SNS_SHIFT[1:0]	
R/W	69	ACC2_CFG_U2	ACC2_U_SNS_MULT[7:0]							
R/W	6A	ACC2_CFG_U3	ACC2_DATATYPE0[2:0]			ACC2_DATATYPE1[2:0]			RESERVED	RESERVED
R/W	6B	ACC2_CFG_U4	ACC2_RESET_OC	RESERVED	ACC2_OC_FILT[1:0]		RESERVED	RESERVED	ACC2_SIGCLIP_FLT[1:0]	
R/W	6C	ACC2_CFG_U5	ACC2_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
R/W	6D to 71	RESERVED	RESERVED							
R	72	ARC0_SNSDATA0_L	ARC0_SNSDATA0[7:0]							
R	73	ARC0_SNSDATA0_H	ARC0_SNSDATA0[15:8]							
R	74	ARC0_SNSDATA1_L	ARC0_SNSDATA1[7:0]							
R	75	ARC0_SNSDATA1_H	ARC0_SNSDATA1[15:8]							
R	76	ARC0_ST_L	ARC0_ST[7:0]							
R	77	ARC0_ST_H	ARC0_ST[15:8]							
R	78 to 89	RESERVED	RESERVED							
R	8A	ACC0_SNSDATA0_L	ACC0_SNSDATA0[7:0]							
R	8B	ACC0_SNSDATA0_H	ACC0_SNSDATA0[15:8]							
R	8C	ACC0_SNSDATA1_L	ACC0_SNSDATA1[7:0]							
R	8D	ACC0_SNSDATA1_H	ACC0_SNSDATA1[15:8]							
R	8E to 91	RESERVED	RESERVED							
R	92	ACC1_SNSDATA0_L	ACC1_SNSDATA0[7:0]							
R	93	ACC1_SNSDATA0_H	ACC1_SNSDATA0[15:8]							
R	94	ACC1_SNSDATA1_L	ACC1_SNSDATA1[7:0]							
R	95	ACC1_SNSDATA1_H	ACC1_SNSDATA1[15:8]							
R	96 to 99	RESERVED	RESERVED							

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
R	9A	ACC2_SNSDATA0_L	ACC2_SNSDATA0[7:0]							
R	9B	ACC2_SNSDATA0_H	ACC2_SNSDATA0[15:8]							
R	9C	ACC2_SNSDATA1_L	ACC2_SNSDATA1[7:0]							
R	9D	ACC2_SNSDATA1_H	ACC2_SNSDATA1[15:8]							
R	9E and 9F	RESERVED	RESERVED							

Table 19. Sensor parametric stored data

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
F (1)	A0	ARC0_ST_CMP_L	ARC0_ST_CMP[7:0]							
F (1)	A1	ARC0_ST_CMP_H	ARC0_ST_CMP[15:8]							
F(1)	A2	ARC0_FDRIVE_L	ARC0_FDRIVE[7:0]							
F(1)	A3	ARC0_FDRIVE_H	ARC0_FDRIVE[15:8]							
F (2)	A4 to AF	RESERVED	RESERVED							
F (3)	B0	ACC0_STL_P_L	ACC0_STL_P[7:0]							
F (3)	B1	ACC0_STL_P_H	ACC0_STL_P[15:8]							
F(3)	B2	ACC0_STH_P_L	ACC0_STH_P[7:0]							
F(3)	B3	ACC0_STH_P_H	ACC0_STH_P[15:8]							
F(3)	B4	ACC0_STL_N_L	ACC0_STL_N[7:0]							
F(3)	B5	ACC0_STL_N_H	ACC0_STL_N[15:8]							
F(3)	B6	ACC0_STH_N_L	ACC0_STH_N[7:0]							
F(3)	B7	ACC0_STH_N_H	ACC0_STH_N[15:8]							
F (4)	B8	ACC1_STL_P_L	ACC1_STL_P[7:0]							
F (4)	B9	ACC1_STL_P_H	ACC1_STL_P[15:8]							
F(4)	BA	ACC1_STH_P_L	ACC1_STH_P[7:0]							
F(4)	BB	ACC1_STH_P_H	ACC1_STH_P[15:8]							
F(4)	BC	ACC1_STL_N_L	ACC1_STL_N[7:0]							
F(4)	BD	ACC1_STL_N_H	ACC1_STL_N[15:8]							
F(4)	BE	ACC1_STH_N_L	ACC1_STH_N[7:0]							
F(4)	BF	ACC1_STH_N_H	ACC1_STH_N[15:8]							

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
F [5]	C0	ACC2_STL_P_L	ACC2_STL_P[7:0]							
F [5]	C1	ACC2_STL_P_H	ACC2_STL_P[15:8]							
F[5]	C2	ACC2_STH_P_L	ACC2_STH_P[7:0]							
F[5]	C3	ACC2_STH_P_H	ACC2_STH_P[15:8]							
F[5]	C4	ACC2_STL_N_L	ACC2_STL_N[7:0]							
F[5]	C5	ACC2_STL_N_H	ACC2_STL_N[15:8]							
F[5]	C6	ACC2_STH_N_L	ACC2_STH_N[7:0]							
F[5]	C7	ACC2_STH_N_H	ACC2_STH_N[15:8]							

1. *Factory programmable, readable register, ARC0 information.*
2. *Factory programmable, readable register, reserved.*
3. *Factory programmable, readable register, ACC0 information.*
4. *Factory programmable, readable register, ACC1 information.*
5. *Factory programmable, readable register, ACC2 information.*

Table 20. Sensor traceability information

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
F [1]	C8	ICTYPEID	ICTYPEID[7:0]							
F [1]	C9	DEVICE_REV	DEVICE_REV[7:0]							
F [2]	CA	ASICREVID	ASICREVID[7:0]							
F [3]	CB	ARCMEMS0REVID	ARCMEMS0REVID[7:0]							
F [4]	CC	ACCMEMS0REVID	ACCMEMS0REVID[7:0]							
F [5]	CD to CF	RESERVED	RESERVED							
F[1]	D0	PN0	PN0[7:0]							
F[1]	D1	PN1	PN1[7:0]							
F[1]	D2	SERIALNUMBER0	SERIALNUMBER[7:0]							
F[1]	D3	SERIALNUMBER1	SERIALNUMBER[15:8]							
F[1]	D4	LOTNUMBER0	LOTNUMBER[7:0]							
F[1]	D5	LOTNUMBER1	LOTNUMBER[15:8]							
F[1]	D6	ASSY_LOT0	ASSY_LOT[7:0]							
F[1]	D7	ASSY_LOT1	ASSY_ LOT[15:8]							

Type	Address (hex)	Register	Bit							
			7	6	5	4	3	2	1	0
F[1]	D8	ASSY_LOT2	ASSY_ LOT[23:16]							
F[1]	D9	ASSY_ LOT 3	ASSY_ LOT[31:24]							
F[1]	DA	ASSY_ LOT 4	ASSY_ LOT[39:32]							
F[1]	DB	ASSY_ LOT 5	ASSY_ LOT[47:40]							
F[1]	DC	ASSY_ LOT 6	ASSY_ LOT[55:48]							
F[1]	DD	ASSY_ LOT 7	ASSY_ LOT[63:56]							
F[1]	DE	ASSY_ LOT 8	ASSY_ LOT[71:64]							
F[1]	DF	ASSY_ LOT 9	ASSY_ LOT[79:72]							
F [5]	E0 to FF	RESERVED	RESERVED							

1. *Factory programmable, readable register, device information.*
2. *Factory programmable, readable register, ASIC information.*
3. *Factory programmable, readable register, ARC0 information.*
4. *Factory programmable, readable register, ACC0 information.*
5. *Factory programmable, readable register, reserved.*

11.2 Register definitions

11.2.1 Rolling counter register (COUNT)

The count register is a read-only register, which provides the current value of a free-running 10-bit counter derived from the primary oscillator. For the typical oscillator frequency, derived from the 20 kHz typical drive frequency, the value in the register increases by one count every 97.66 µs (10.24 kHz) and the counter rolls over every 100 ms.

Table 21. COUNT register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
00	COUNT_L	COUNT.7	COUNT.6	COUNT.5	COUNT.4	COUNT.3	COUNT.2	COUNT.1	COUNT.0
01	COUNT_H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	COUNT.9	COUNT.8
Reset value		0	0	0	0	0	0	0	0

11.2.2 Device status registers (DEVSTAT_SUM, DEVSTAT_DET, ARC0_STAT, ACCx_STAT)

The device status registers are read-only registers, which contain device status information.

Table 22. Device status registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
02	DEVSTAT_SUM_L	ARC0_ERR	RESERVED	RESERVED	ACC0_ERR	ACC1_ERR	ACC2_ERR	COMM_ERR	MEMTEMP_ERR
Reset value		1	X	X	1	1	1	0	0
03	DEVSTAT_SUM_H	TESTMODE	DEVRES	ARC0_DEVINIT	RESERVED	RESERVED	ACC0_DEVINIT	ACC1_DEVINIT	ACC2_DEVINIT
Reset value		0	1	1	X	X	1	1	1
04	DEVSTAT_DET_L	ARC0_PLL_ERR	ARC0_DAU_ERR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset Value		0	0	X	X	X	X	X	X
05	DEVSTAT_DET_H	F_OTP_ERR	RESERVED	U_RW_ERR	CONT_ERR	RESERVED	RESERVED	TEMP_SNS_ERR	SDO_ERR
Reset value		0	X	0	0	X	X	0	0
06	ACC0_STAT	ACC0_SIGCLIP	ACC0_OCPHASE[2:0]			ACC0_ST_INC	ACC0_ST_ACTIVE	RESERVED	RESERVED
Reset value		0	0	0	0	1	0	0	X
07	ACC1_STAT	ACC1_SIGCLIP	ACC1_OCPHASE[2:0]			ACC1_ST_INC	ACC1_ST_ACTIVE	RESERVED	RESERVED
Reset value		0	0	0	0	1	0	0	X
08	ACC2_STAT	ACC2_SIGCLIP	ACC2_OCPHASE[2:0]			ACC2_ST_INC	ACC2_ST_ACTIVE	RESERVED	RESERVED
Reset value		0	0	0	0	1	0	0	X
09	ARC0_STAT	ARC0_SIGCLIP	ARC0_OCPHASE[2:0]			ARC0_ST_INC	ARC0_ST_ACTIVE	RESERVED	RESERVED
Reset value		0	0	0	0	1	0	X	X

11.2.2.1 *ARC0 error flag (ARC0_ERR)*

The ARC0 error flag is a logical OR of the following ARC specific error bits:

ARC0_ERR = ARC0_STAT.ARC0_ST_INC OR DEVSTAT_DET.ARC0_PLL_ERR OR DEVSTAT_DET.ARC0_DAU_ERR

11.2.2.2 *Acceleration error flags (ACC0_ERR, ACC1_ERR, ACC2_ERR)*

The acceleration error flag is a logical OR of the following acceleration specific error bits:

ACC0_ERR = ACC0_STAT.ACC0_ST_INC

ACC1_ERR = ACC1_STAT.ACC1_ST_INC

ACC2_ERR = ACC2_STAT.ACC2_ST_INC

11.2.2.3 *Communication error flag (COMM_ERR)*

The communication error bit is a copy of the SDO_ERR bit in the DEVSTAT_DET register.

11.2.2.4 *Memory or temperature error flag (MEMTEMP_ERR)*

The memory error flag is a logical OR of the following internal device error bits:

MEMTEMP_ERR = F_OTP_ERR OR U_RW_ERR OR CONT_ERR OR TEMP_SNS_ERR

11.2.2.5 *Test mode flag (TESTMODE)*

If the user SPI mode is not enabled on the device, the test mode status bit is set. Once set, only a device reset can clear the TESTMODE bit.

Table 23. Test mode flag

TESTMODE	Operating mode
0	user SPI mode enabled
1	user SPI mode not enabled

Note: If the TESTMODE bit is set, the device responds with an invalid response (invalid SPI CRC) until the device is reset. For this reason, it is not possible to complete a read of the DEVSTAT_SUM register with the TESTMODE bit set.

11.2.2.6 *Device reset flag (DEVRES)*

The device reset bit is set following a device reset. A read of the DEVSTAT_SUM register clears this status bit.

Table 24. Device reset flag

DEVRES	Error condition
0	normal operation
1	device reset occurred

11.2.2.7 *Angular rate channel device initialization flag (ARC0_DEVINIT)*

The angular rate device initialization bit is set following either a device reset or a change to the DSP configuration bits as specified in Section 11.2.7: ARC0 user configuration 1 register (ARC0_CFG_U1). The status bit is automatically cleared once the angular rate sensor data is available for read ($t_{startup}$ or $t_{v(data)}$).

Note: Some LPF selections have a step response time longer than the $t_{v(data)}$ delay. If the system uses any of these filters, it is possible that the filter has not reached the final value once ARC0_DEVINIT has cleared.

Table 25. Angular rate channel device initialization flag

ARC0_DEVINIT	Condition
0	angular rate sensor data available

ARC0_DEVINIT	Condition
1	angular rate DSP initialization in process

11.2.2.8 *Acceleration device initialization flags (ACCx_DEVINIT)*

The acceleration device initialization bits are set following either a device reset or a change to the DSP configuration bits for the associated channel, as specified in Section 11.2.11: ACC user configuration 1 registers (ACC0_CFG_U1, ACC1_CFG_U1, ACC2_CFG_U1). The status bit is automatically cleared once the acceleration sensor data is available for read ($t_{startup}$ or $t_{v(data)}$).

Note: Some LPF selections have a step response time longer than the $t_{v(data)}$ delay. If the system uses any of these filters, it is possible that the filter has not reached the final value once ACCx_DEVINIT has cleared.

Table 26. Acceleration device initialization flags

ACCx_DEVINIT	Condition
0	acceleration sensor data available
1	acceleration DSP initialization in process

11.2.2.9 *ARC0 PLL error flag (ARC0_PLL_ERR)*

If the PLL loses lock, or the drive amplitude falls out of range, the ARC0 PLL error bit is set.

When the error is no longer present, a read of the DEVSTAT_DET register clears the status bit.

Table 27. ARC0 PLL error flag

ARC0_PLL_ERR	Error condition
0	normal operation
1	PLL loss of lock or drive amplitude out of range

11.2.2.10 *ARC0 DAU error flag (ARC0_DAU_ERR)*

If an ARC0 transducer drive error condition exists, the ARC0 drive actuation unit error bit is set. When the error is no longer present, a read of the DEVSTAT_DET register clears the status bit.

Table 28. ARC0 DAU error flag

ARC0_DAU_ERR	Error condition
0	normal operation
1	ARC0 transducer drive error condition detected

11.2.2.11 *ST OTP array error flag (F_OTP_ERR)*

If a fault is detected in the ST OTP register array by any of the following sources, the ST OTP array error bit is set.

- An ECC 2-bit error is detected in the internal ST OTP array used for internal trim and configuration
- A CRC error is detected in the internal ST register array
- An ECC 2-bit error is detected in the ST programmed and user readable OTP, user accessible array: A0h to FFh

A device reset clears the F_OTP_ERR bit.

Table 29. ST OTP array error flag

F_OTP_ERR	Error condition
0	no error detected

F_OTP_ERR	Error condition
1	error detected in the factory OTP array

11.2.2.12 *User read/write array error flag (U_RW_ERR)*

If a fault is detected in the user read/write array, the user read/write array error bit is set. When the error is no longer present, a read of the DEVSTAT_DET register clears the status bit. User read/write error detection is enabled only when ENDINIT is set in the DEVLOCK_WR register. Reference Section 11.2.4.1: End initialization bit (ENDINIT) for details regarding the ENDINIT bit function.

Table 30. User read/write array error flag

U_RW_ERR	Error condition
0	no error detected
1	error detected in the user read/write array

11.2.2.13 *Continuity monitor error flag (CONT_ERR)*

The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. If a discontinuity is detected in the connection, the error bit is set. A device reset clears the CONT_ERR bit.

Table 31. Continuity monitor error flag

CONT_ERR	Error condition
0	no error detected
1	error detected in the continuity of the perimeter connection

11.2.2.14 *Temperature sensor error (TEMP_SNS_ERR)*

Two temperature sense elements are present on the ASIC. One is used by the angular rate signal chain, while the acceleration signal chains share the other. The outputs of the two temperature calibration signal paths are continuously compared during device operation. The following conditions set the TEMP_SNS_ERR flag:

- If the difference between the two temperature sensors exceeds the specified compare threshold
- If either temperature sensor rises above the overtemperature threshold
- If either temperature sensor falls below the undertemperature threshold

When the error is no longer present, a read of the DEVSTAT_DET register clears the status bit.

Table 32. Temperature sensor error

TEMP_SNS_ERR	Error condition
0	no error detected
1	temperature sensor out of range or mismatch detected

11.2.2.15 *SPI SDO data mismatch error (SDO_ERR)*

The SDO data mismatch error bit is set when a SDO data mismatch fault occurs. When the error is no longer present, a SPI transmission including the error status clears the status bit.

Table 33. SPI SDO data mismatch error

SDO_ERR	Error condition
0	normal operation
1	SDO data mismatch

Note: If the SDO_ERR bit is set, the device responds with the SPI error response until the error condition is removed. The SPI error response qualifies as a SPI transmission including the error status. For this reason, it is not possible to complete a read of the DEVSTAT_DET register with the SDO_ERR bit set.

11.2.2.16 ARC0 signal clipped status bit (ARC0_SIGCLIP)

If the output of the C2V or sinc filter exceeds the maximum or minimum value for longer than the times specified in Section 11.2.9.3: ARC0 signal clip filter selection bits (ARC0_SIGCLIP_FILT[1:0]), the angular rate signal clipped status bit is set. When the error is no longer present, the ARC0_SIGCLIP bit is cleared on a read of the ARC0_STAT register. Reference Table 13. Angular rate sensor signal chain for details on the ARC0_SIGCLIP detection time.

11.2.2.17 ACCx signal clipped status bit (ACC0_SIGCLIP, ACC1_SIGCLIP, ACC2_SIGCLIP)

If the output of the C2V or sinc filter exceeds the maximum or minimum value on the associated channel for longer than the times specified in Section 11.2.14.3: ACC signal clip filter selection bits (ACCx_SIGCLIP_FILT[1:0]), the acceleration signal clipped status bit is set. When the error is no longer present, the ACCx_SIGCLIP bit is cleared on a read of the ACCx_STAT register. Reference Table 14. Acceleration sensor signal chain for details on the ACCx_SIGCLIP detection time.

11.2.2.18 ARC0 and ACCx offset cancellation phase status (ARC0_OCPHASE[2:0], ACCx_OCPHASE[2:0])

The angular rate and acceleration offset cancellation phase status bits indicate the current phase of the offset cancellation filter as described in Section 11.4.2.3: Angular rate offset cancellation and Section 11.5.2.5: Acceleration offset cancellation.

11.2.2.19 ARC0 and ACCx self-test incomplete (ARC0_ST_INC, ACCx_ST_INC)

The self-test incomplete bit is set after a device reset and is automatically cleared when one of the self-test modes is enabled for the associated channel.

Table 34. ARC0 and ACCx self-test incomplete

AxCx_ST_INC	Condition
0	self-test has been activated since the last reset
1	no self-test has been activated since the last reset

11.2.2.20 ARC0 and ACCx self-test active flag (ARC0_ST_ACTIVE, ACCx_ST_ACTIVE)

If any self-test mode is active for the associated channel, the self-test active bit is set. The self-test active bit is automatically cleared when no self-test mode is active.

ARC0_ST_ACTIVE = ARC0_ST_CTRL.3 OR ARC0_ST_CTRL.2 OR ARC0_ST_CTRL.1 OR ARC0_ST_CTRL.0

ACC0_ST_ACTIVE = ACC0_ST_CTRL.3 OR ACC0_ST_CTRL.2 OR ACC0_ST_CTRL.1 OR ACC0_ST_CTRL.0

ACC1_ST_ACTIVE = ACC1_ST_CTRL.3 OR ACC1_ST_CTRL.2 OR ACC1_ST_CTRL.1 OR ACC1_ST_CTRL.0

ACC2_ST_ACTIVE = ACC2_ST_CTRL.3 OR ACC2_ST_CTRL.2 OR ACC2_ST_CTRL.1 OR ACC2_ST_CTRL.0

11.2.3 Temperature registers (TEMPERATURE_H, TEMPERATURE_L)

The temperature registers are read-only registers, which contain a temperature value from the internal angular rate temperature sensor. The characteristics of the temperature sensor are specified in Table 9. Temperature sensor signal chain and the output scaling is documented in Section 11.6: Temperature sensor.

Note: The device is only guaranteed to operate within the temperature limits specified in Section 7: Recommended operating conditions.

Table 35. Temperature registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
0E	TEMPERATURE_L	TEMPERATURE[7:0]							

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
0F	TEMPERATURE_H	TEMPERATURE[15:8]							

11.2.4 Lock register writing register (DEVLOCK_WR)

The lock register writing register is a user programmed read/write register, which contains the ENDINIT bit and reset control bits.

All bits in the DEVLOCK_WR register except the ENDINIT bit are writable regardless of the state of the ENDINIT bit.

Table 36. Lock register writing register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
10	DEVLOCK_WR	ENDINIT	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESET[1:0]	
Reset value		0	0	0	0	0	0	0	0

11.2.4.1 End initialization bit (ENDINIT)

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, only a device reset can clear the ENDINIT bit.

When ENDINIT is set, the following occurs:

- An error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code.
- The offset cancellation filter is forced to its final stage.
- Self-test is disabled and inhibited.
- Register writes are inhibited except for the RESET[1:0] bits in the DEVLOCK_WR register.

11.2.4.2 Reset control bits (RESET[1:0])

A series of three consecutive register write operations to the reset control bits result in a device reset. To reset the device, the following register write operations must be performed in consecutive commands and in the order shown below or the device is not reset.

Table 37. Reset control bits

Register write to DEVLOCK_WR	RESET.1	RESET.0	Effect
Register write 1	0	0	no effect
Register write 2	1	1	no effect
Register write 3	0	1	device reset

The response to a register write returns the new register value, including the values written to the RESET[1:0] bits. After the third register write command, the device initiates a reset and therefore does not transmit a response to this command. The response to a register read returns 00b for RESET[1:0] and terminates the reset sequence. The reset control bits are not included in the read/write array error detection.

11.2.5 F region selection registers (F_REGION_x)

The F region load register is a user read/write register that contains the address bits for accessing the readable OTP regions. This register is included in the user read/write array error detection. The F region active register is a read-only register that contains the address bits for the OTP region currently loaded into the shared block of registers. This register is included in the user read/write array error detection.

The F_REGION_W register is writable until the ENDINIT bit is set in the DEVLOCK_WR register. The F_REGION_R register is read only.

Table 38. F region selection registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
14	F_REGION_W	REGION_LOAD[3:0]				0	0	0	0
15	F_REGION_R	REGION_ACTIVE[3:0]				0	0	0	0
Factory default		1	0	1	0	0	0	0	0

The OTP regions Axh to Fxh share a block of 16 registers. Prior to reading the registers, the user must ensure that the desired OTP registers are loaded into the registers. Below is the procedure to ensure proper reading of the shared registers.

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the F_REGION_W register

Table 39. REGION_LOAD[3:0] bits

REGION_LOAD[3:0]				OTP register addresses loaded into the readable registers
0000 to 1001				reserved
1	0	1	0	address range A0h to AFh
1	0	1	1	address range B0h to BFh
1	1	0	0	address range C0h to CFh
1	1	0	1	address range D0h to DFh
1	1	1	0	address range E0h to EFh
1	1	1	1	address range F0h to FFh

2. Delay a minimum of $t_{WH(S)}$
3. Execute a register read of the F_REGION_R register and confirm that the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the F_REGION_W register.

Table 40. REGION_ACTIVE[3:0] bits

REGION_ACTIVE[3:0]				OTP register addresses loaded into the readable registers
0000 to 1001				not applicable
1	0	1	0	address range A0h to AFh
1	0	1	1	address range B0h to BFh
1	1	0	0	address range C0h to CFh
1	1	0	1	address range D0h to DFh
1	1	1	0	address range E0h to EFh
1	1	1	1	address range F0h to FFh

4. Execute a register read of the desired register addresses.

Notes:

- The user must take care to ensure that the desired registers are addressed. For example, if the REGION_LOAD bits are set to Ah and the user executes a read of address C2h, the contents of register A2h is transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.
- Once the ENDINIT bit is set, writes to registers other than the RESET[1:0] bits are inhibited. For this reason, reads of the A0h to FFh registers are only possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.
- Although the contents of the OTP is not writable, the shared block of registers is writable. The user must take care not to overwrite the contents of the shared block of registers.

11.2.6 SafeSPI address register (SPI_SADDR)

The SafeSPI address register contains the value of the 2-bit sensor address for SafeSPI. This register is included in the user read/write array error detection.

Reference Section 11.7.1: SafeSPI sensor addressing for details regarding the sensor address in SafeSPI.

Table 41. SafeSPI address register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
3E	SPI_SADDR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SPI_SA[1:0]	
Reset value		0	0	0	0	0	0	0	0

Table 42. Sensor address value explains the sensor address value based on the SPI address pin states.

Table 42. Sensor address value

Pin state		SPI sensor address
SPI_SA1	SPI_SA0	SA[1:0]
V_{SS}	V_{SS}	00
V_{SS}	V_{CC}	01
V_{CC}	V_{SS}	10
V_{CC}	V_{CC}	11

11.2.7 ARC0 user configuration 1 register (ARC0_CFG_U1)

The ARC0 user configuration 1 register is a user programmable read/write register, which contains ARC DSP specific configuration information. This register is included in the read/write array error detection.

The ARC0_CFG_U1 register is writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 43. ARC0 user configuration 1 register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
40	ARC0_CFG_U1	RESERVED	RESERVED	ARC0_LPF[1:0]		ARC0_SAMPLERATE[1:0]		RESERVED	RESERVED
Reset value		0	0	0	0	0	0	0	0

11.2.7.1 ARC0 low-pass filter selection bits (ARC0_LPF[1:0])

The ARC0 low-pass filter selection bits and sample rate bits select the low-pass filter for the angular rate signal chain. Reference Section 11.4.2.2: Angular rate low-pass filter and Table 44. ARC0 user sample rate selection bits for details regarding the low-pass filter.

Changes to the ARC0_LPF[1:0] bits reset the angular rate DSP and set the ARC0_DEVINIT bit in the DEVSTAT_SUM register. ARC0_DEVINIT remains set for a maximum time of $t_{v(data)}$ as specified in Table 15. Supply and support circuitry. Sensor data is not valid until the ARC0_DEVINIT bit is cleared.

11.2.7.2 *ARC0 user sample rate selection bits (ARC0_SAMPLERATE[1:0])*

The ARC0 low-pass filter selection bits and sample rate bits select the low-pass filter for the angular rate signal chain. Reference Section 11.4.2.2: Angular rate low-pass filter and Table 44. ARC0 user sample rate selection bits for details regarding the low-pass filter.

Changes to the ARC0_SAMPLERATE[1:0] bits reset the angular rate DSP and set the ARC0_DEVINIT bit in the DEVSTAT_SUM register. ARC0_DEVINIT remains set for a maximum time of $t_{v(data)}$ as specified in Table 15. Supply and support circuitry. Sensor data is not valid until the ARC0_DEVINIT bit is cleared.

Table 44. ARC0 user sample rate selection bits

LPF number	ARC0_LPF[1:0]		ARC0_SAMPLERATE[1:0]		Typical cut-off frequency (Hz)	Order	Internal sample time (µs)
0	0	0	0	0	50	4	400
1			0	1	25	4	800
2			1	0	12.5	4	1600
			1	1	reserved		
4	0	1	0	0	50	2	400
5			0	1	25	2	800
6			1	0	12.5	2	1600
			1	1	reserved		
8	1	0	0	0	60	2	400
9			0	1	30	2	800
10			1	0	15	2	1600
			1	1	reserved		
12	1	1	0	0	356	4	400
13			0	1	230	4	800
14			1	0	130	4	1600
			1	1	reserved		

11.2.8 ARC0 user configuration 3 register (ARC0_CFG_U3)

The ARC0 user configuration 3 register is a user programmable read/write register, which contains ARC DSP specific configuration information. This register is included in the read/write array error detection.

The ARC0_CFG_U3 register is writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 45. ARC0 user configuration 3 register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
42	ARC0_CFG_U3	ARC0_DATATYPE0[2:0]			ARC0_DATATYPE1[2:0]			RESERVED	RESERVED
Reset value		0	0	0	0	0	0	0	0

11.2.8.1 *ARC0 data type 0 and data type 1 selection bits (ARC0_DATATYPE0, ARC0_DATATYPE1)*

The ARC0 data type 0 selection bits select the type of data to be included in the ARC0_SNSDATA0_L and ARC0_SNSDATA0_H registers according to Table 46. ARC0 data type 0 and data type 1 selection bits. The ARC0 data type 1 selection bits select the type of data to be included in the ARC0_SNSDATA1_L and ARC0_SNSDATA1_H registers according to Table 46. ARC0 data type 0 and data type 1 selection bits.

Table 46. ARC0 data type 0 and data type 1 selection bits

ARC0_DATATYPEx[2:0]			Typical output data range	Offset cancellation
0	0	0	125 dps	bypassed
0	0	1	250 dps	bypassed
0	1	0	350 dps	bypassed
0	1	1	reserved	reserved
1	0	0	125 dps	enabled
1	0	1	250 dps	enabled
1	1	0	350 dps	enabled
1	1	1	reserved	reserved

11.2.9 ARC0 user configuration 4 register (ARC0_CFG_U4)

The ARC0 user configuration 4 register is a user programmable read/write register, which contains angular rate specific configuration information. This register is included in the read/write array error detection.

The ARC0_CFG_U4 register is writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 47. ARC0 user configuration 4 register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
43	ARC0_CFG_U4	ARC0_RESET_OC	RESERVED	ARC0_OC_FILT[1:0]		RESERVED	RESERVED	ARC0_SIGCLIP_FLT[1:0]	
Reset value		0	0	0	0	0	0	0	0

11.2.9.1 *ARC0 reset offset cancellation startup bit (ARC0_RESET_OC)*

When the ARC0 reset offset cancellation startup bit is written to logic 1, the offset cancellation is reset to the startup fast offset cancellation to remove quickly any startup offset according to the parameters in Table 13. Angular rate sensor signal chain. The ARC0_RESET_OC bit is cleared when the offset cancellation phase reaches phase 1.

11.2.9.2 *ARC0 offset cancellation filter selection bits (ARC0_OC_FILT[1:0])*

The ARC0 offset cancellation filter selection bits select the filter type to be used for offset cancellation. Reference Section 11.4.2.3: Angular rate offset cancellation for details regarding offset cancellation.

Table 48. ARC0 offset cancellation filter selection bits

ARC0_OC_FILT[1:0]		Offset cancellation IIR filter	Offset cancellation rate limiting
0	0	0.04 Hz	bypassed
0	1	0.04 Hz	enabled
1	0	0.005 Hz	bypassed
1	1	reserved	

11.2.9.3 *ARC0 signal clip filter selection bits (ARC0_SIGCLIP_FILT[1:0])*

The ARC0 signal clip filter selection bits select the filter time to be used for the ARC0 signal clip detection. The signal clip filter is an up/down counter with equal weighting for up and down counting and a range equal to 2 times the threshold time selected in Table 49. ARC0 signal clip filter selection bits.

Table 49. ARC0 signal clip filter selection bits

ARC0_SIGCLIP_FILT[1:0]		Filter time for ARC0_SIGCLIP
0	0	1.024 ms
0	1	4.096 ms
1	0	8.192 ms
1	1	16.384 ms

11.2.10 ARC0 user configuration 5 register (ARC0_CFG_U5)

The ARC0 user configuration 5 register is a user programmable read/write register, which contains ARC0 DSP specific configuration information. This register is included in the read/write array error detection.

The ARC0_CFG_U5 register is writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 50. ARC0 user configuration 5 register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
44	ARC0_CFG_U5	ARC0_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
Reset value		0	0	0	0	0	0	0	0

11.2.10.1 *ARC0 self-test control bits (ARC0_ST_CTRL[3:0])*

The ARC0 self-test control bits select one of the various analog and digital self-test features of the device as shown in Table 51. ARC0 self-test control bits.

Table 51. ARC0 self-test control bits

ARC0_ST_CTRL[3:0]				Function	ARC0_SNSDATAx register contents	ARC0_ST register contents	ARC0_ST_INC	ARC0_ST_ACTIVE
0	0	0	0	DSP writes to the ARC0_SNSDATAx registers	ARC0 sensor data	ARC0 self-test off data	no effect	clear when active
0	0	0	1				clear on activation	set when active
0	0	1	0				clear on activation	set when active
0	0	1	1				clear on activation	set when active
0	1	0	0	fixed pattern self-test; DSP writes to registers inhibited	0000h		clear on activation	set when active
0	1	0	1		AAAAh		clear on activation	set when active
0	1	1	0		5555h		clear on activation	set when active
0	1	1	1		FFFFh		clear on activation	set when active
1	0	0	0	analog self-test	ARC0 sensor data	ARC0 self-test on data; Section 11.4.1.1: Startup angular rate analog self-test	clear on activation	set when active
1	0	0	1	reserved	reserved	reserved	clear on activation	set when active
1	0	1	0	reserved	reserved	reserved	clear on activation	set when active
1	0	1	1	reserved	reserved	reserved	clear on activation	set when active

ARC0_ST_CTRL[3:0]				Function	ARC0_SNSDATAx register contents	ARC0_ST register contents	ARC0_ST_INC	ARC0_ST_ACTIVE
1	1	0	0	digital self-test	reference Table 10. Angular rate sensor signal chain and Section 11.4.1.2: Startup angular rate digital self-test	ARC0 self-test off data	clear on activation	set when active
1	1	0	1				clear on activation	set when active
1	1	1	0				clear on activation	set when active
1	1	1	1				clear on activation	set when active

11.2.11 ACC user configuration 1 registers (ACC0_CFG_U1, ACC1_CFG_U1, ACC2_CFG_U1)

The ACC user configuration 1 registers are user programmable read/write registers, which contain acceleration specific configuration information. These registers are included in the read/write array error detection.

The ACCx_CFG_U1 registers are writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 52. ACC user configuration 1 registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
58	ACC0_CFG_U1	ACC0_LPF1[1:0]		ACC0_LPF0[1:0]		ACC0_SAMPLERATE[1:0]		ACC0_USER_SNS_SHIFT[1:0]	
60	ACC1_CFG_U1	ACC1_LPF1[1:0]		ACC1_LPF0[1:0]		ACC1_SAMPLERATE[1:0]		ACC1_USER_SNS_SHIFT[1:0]	
68	ACC2_CFG_U1	ACC2_LPF1[1:0]		ACC2_LPF0[1:0]		ACC2_SAMPLERATE[1:0]		ACC2_USER_SNS_SHIFT[1:0]	
Reset value		0	0	0	0	0	0	0	0

11.2.11.1 *ACC user low-pass filter 1 selection bits (ACCx_LPF1[1:0])*

The ACC LPF1 bits select coefficients for the acceleration low-pass filter 1. These bits, along with the sample rate selection bits, select the nominal cut-off frequency and filter order for LPF1. Refer to Table 53. ACC user sample rate selection bits LPF1 for details.

Changes to the ACCx_LPF1[1:0] bits reset the acceleration DSP and set the ACCx_DEVINIT bit in the DEVSTAT_SUM register. ACCx_DEVINIT remains set for a maximum time of $t_{v(data)}$ as specified in Table 15. Supply and support circuitry. Sensor data is not valid until the ACCx_DEVINIT bit is cleared.

11.2.11.2 *ACC user low-pass filter 0 selection bits (ACCx_LPF0[1:0])*

The ACC LPF0 bits select coefficients for the acceleration low-pass filter 0. These bits, along with the sample rate selection bits, select the nominal cut-off frequency and filter order for LPF0. Refer to Table 54. ACC user sample rate selection bits LPF0 for details.

Changes to the ACCx_LPF0[1:0] bits reset the acceleration DSP and set the ACCx_DEVINIT bit in the DEVSTAT_SUM register. ACCx_DEVINIT remains set for a maximum time of $t_{v(data)}$ as specified in Table 15. Supply and support circuitry. Sensor data is not valid until the ACCx_DEVINIT bit is cleared.

11.2.11.3 *ACC user sample rate selection bits (ACCx_SAMPLERATE[1:0])*

The ACC sample rate selection bits determine the decimation ratio for the selected low-pass filters. The sample rate bits select a common sample rate for both LPF0 and LPF1. Refer to Table 53. ACC user sample rate selection bits LPF1 and Table 54. ACC user sample rate selection bits LPF0 for details.

Changes to the ACCx_SAMPLERATE[1:0] bits reset the acceleration DSP and set the ACCx_DEVINIT bit in the DEVSTAT_SUM register. ACCx_DEVINIT remains set for a maximum time of $t_{v(data)}$ as specified in Table 15. Supply and support circuitry. Sensor data is not guaranteed until the ACCx_DEVINIT bit is cleared.

Table 53. **ACC user sample rate selection bits LPF1**

LPF1 number	ACCx_LPF1[1:0]		ACCx_SAMPLERATE[1:0]		Cut-off frequency (Hz)		Order	Internal sample time (µs)
					System BW (xy-axis)	System BW (z-axis)		
0	0	0	0	0	60	60	2	62.5
1			0	1	30	30	2	125
2			1	0	15	15	2	250
			1	1	reserved			
4	0	1	0	0	260	250	3	62.5
5			0	1	132	130	3	125
6			1	0	66	66	3	250
			1	1	reserved			
8	1	0	0	0	387	350	3	62.5
9			0	1	200	190	3	125
10			1	0	100	100	3	250
			1	1	reserved			
12	1	1	0	0	reserved			
13			0	1	reserved			
14			1	0	387	350	3	250
			1	1	reserved			

Table 54. **ACC user sample rate selection bits LPF0**

LPF0 number	ACCx_LPF0[1:0]		ACCx_SAMPLERATE[1:0]		Cut-off frequency (Hz)		Order	Internal sample time (µs)
					System BW (xy-axis)	System BW (z-axis)		
0	0	0	0	0	60	60	2	62.5
1			0	1	30	30	2	125
2			1	0	15	15	2	250
			1	1	reserved			
4	0	1	0	0	260	250	3	62.5
5			0	1	132	130	3	125
6			1	0	66	66	3	250
			1	1	reserved			
8	1	0	0	0	387	350	3	62.5
9			0	1	200	190	3	125
10			1	0	100	100	3	250
			1	1	reserved			
12	1	1	0	0	reserved			
13			0	1	reserved			
14			1	0	387	350	3	250
			1	1	reserved			

11.2.11.4 *ACC user sensitivity shift selection bits (ACCx_U_SNS_SHIFT[1:0])*

The ACC user sensitivity selection bits are used along with the ACC user sensitivity multiplier bits to scale the output sensitivity of the channel. Reference Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0]) for details.

11.2.12 ACC user configuration 2 registers (ACC0_CFG_U2, ACC1_CFG_U2, ACC2_CFG_U2)

The ACC user configuration 2 registers are user programmable read/write registers, which contain acceleration specific configuration information. These registers are included in the read/write array error detection.

The ACCx_CFG_U2 registers are writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 55. ACC user configuration 2 registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
59	ACC0_CFG_U2	ACC0_U_SNS_MULT[7:0]							
61	ACC1_CFG_U2	ACC1_U_SNS_MULT[7:0]							
69	ACC2_CFG_U2	ACC1_U_SNS_MULT[7:0]							
Reset value		0	0	0	0	0	0	0	0

11.2.12.1 *ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])*

The ACC user sensitivity multiplier bits are used along with the ACC user sensitivity shift bits to scale the output sensitivity of the device. The equations below describe the scaling:

$$OutputSensitivity\left(G8\right) = TrimSensitivity \times \frac{SensitivityShiftFactor}{2} \times \frac{256 + SensitivityMultiplier}{511}$$

$$OutputSensitivity\left(\boldsymbol{G}1\right) = TrimSensitivity \times \frac{SensitivityShiftFactor}{16} \times \frac{256 + SensitivityMultiplier}{511}$$

Where:

OutputSensitivity(G8) = the output sensitivity at 8 × gain selected by the ACCx_DATATYPEx field as specified in Section 11.2.13: ACC user configuration 3 registers (ACC0_CFG_U3, ACC1_CFG_U3, ACC2_CFG_U3)

OutputSensitivity(G1) = the output sensitivity at 1 × gain selected by the ACCx_DATATYPEx field as specified in Section 11.2.13: ACC user configuration 3 registers (ACC0_CFG_U3, ACC1_CFG_U3, ACC2_CFG_U3)

TrimSensitivity = the trimmed sensitivity of the device at maximum gain ($S_{a(1g5)}$), as specified in Table 11. Acceleration sensor signal chain

SensitivityMultiplier = the unsigned multiplier value contained in the ACCx_U_SNS_MULT[7:0] bits

SensitivityShiftFactor = the shift factor selected by the ACCx_U_SNS_SHIFT[1:0] bits as described in Table 56. Sensitivity shift factor

Table 56. Sensitivity shift factor

ACCx_U_SNS_SHIFT[1:0]		Sensitivity shift factor
0	0	0.25
0	1	0.50
1	0	1
1	1	2

Table 57. Acceleration sensitivity selection table shows some example user shift and multiplier values for typical full-scale ranges.

Note: Table 57. Acceleration sensitivity selection table includes some typical device ranges. Other ranges are possible with the user selected shift and multiplier values.

Table 57. **Acceleration sensitivity selection table**

Desired range g		User sensitivity shift factor ACCx_U_SNS_SHIFT		User multiplier value ACCx_U_SNS_MULT		Sensor data, 1 × range, 8 × gain (G8)		Sensor data, 8 × range, 1 × gain (G1)	
1 × range, 8 × gain	8 × range, 1 × gain	Hex	Shift factor	Hex	Decimal	Actual typical range g	Actual typical sensitivity LSB/g	Actual typical range g	Actual typical sensitivity LSB/g
1.50	12.00	3	2	FF	255	1.501	21834.67	12.01	2729.333
2.00	16.00	3	2	7F	127	2.002	16365.32	16.02	2045.665
3.00	24.00	2	1	FF	255	3.001	10917.33	24.01	1364.667
3.50	28.00	2	1	B6	182	3.502	9357.714	28.01	1169.714
3.75	30.00	2	1	99	153	3.750	8738.139	30.00	1092.267
4.00	32.00	2	1	7F	127	4.004	8182.659	32.04	1022.832
5.00	40.00 (overrange)	2	1	33	51	4.996	6558.946	39.97	819.8682
5.99	47.92 (overrange)	2	1	00	0	5.991	5469.349	45 (digital clip)	683.6686
6.00	48.00 (overrange)	1	0.5	FF	255	6.003	5458.667	45 (digital clip)	682.3333
7.50	60.00 (overrange)	1	0.5	99	153	7.500	4369.070	45 (digital clip)	546.1337
8.00	64.00 (overrange)	1	0.5	7F	127	8.009	4091.329	45 (digital clip)	511.4162
10.00	80.00 (overrange)	1	0.5	33	51	9.992	3279.473	45 (digital clip)	409.9341
12.00	96.00 (overrange)	0	0.25	FF	255	12.01	2729.333	45 (digital clip)	341.1666
15.00	120.00 (overrange)	0	0.25	99	153	15.00	2184.534	45 (digital clip)	273.0669
20.00	160.00 (overrange)	0	0.25	33	51	19.98	1639.736	45 (digital clip)	204.9671
24.00	192.00 (overrange)	0	0.25	00	0	23.96	1367.337	45 (digital clip)	170.9172

11.2.13 ACC user configuration 3 registers (ACC0_CFG_U3, ACC1_CFG_U3, ACC2_CFG_U3)

The ACC user configuration 3 registers are user programmable read/write registers, which contain acceleration specific configuration information. These registers are included in the read/write array error detection.

The ACCx_CFG_U3 registers are writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 58. **ACC user configuration 3 registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
5A	ACC0_CFG_U3	ACC0_DATATYPE0[2:0]			ACC0_DATATYPE1[2:0]			RESERVED	RESERVED
62	ACC1_CFG_U3	ACC1_DATATYPE0[2:0]			ACC1_DATATYPE1[2:0]			RESERVED	RESERVED

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
6A	ACC2_CFG_U3	ACC2_DATATYPE0[2:0]			ACC2_DATATYPE1[2:0]			RESERVED	RESERVED
Reset value		0	0	0	0	0	0	0	0

11.2.13.1 *ACC data type 0 selection bits (ACCx_DATATYPE0)*

The ACC data type 0 selection bits select the type of data to be included in the ACCx_SNSDATA0_L and ACCx_SNSDATA0_H registers for each channel. Reference Section 11.5.2.7: Acceleration output scaling for details regarding the data output scaling.

Table 59. ACC data type 0 selection bits

ACCx_DATATYPE0[2:0]			Data transmitted			
			LPF selection	Range selection	Interpolation	Offset cancellation selection
0	0	0	LPF0	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	selected by OC_FILT[1:0]
0	0	1	LPF0	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	no offset cancellation
0	1	0	LPF0	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	selected by OC_FILT[1:0]
0	1	1	LPF0	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	no offset cancellation
1	0	0	LPF1	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	selected by OC_FILT[1:0]
1	0	1	LPF1	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	no offset cancellation
1	1	0	LPF1	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	selected by OC_FILT[1:0]
1	1	1	LPF1	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	enabled	no offset cancellation

11.2.13.2 *ACC data type 1 selection bits (ACCx_DATATYPE1)*

The ACC data type 1 selection bits select the type of data to be included in the ACCx_SNSDATA1_L and ACCx_SNSDATA1_H registers for each channel. Reference Section 11.5.2.7: Acceleration output scaling for details regarding the data output scaling.

Table 60. ACC data type 1 selection bits

ACCx_DATATYPE1[2:0]			Data transmitted			
			LPF selection	Range selection	Interpolation	Offset cancellation selection
0	0	0	LPF0	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	selected by OC_FILT[1:0]
0	0	1	LPF0	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	no offset cancellation
0	1	0	LPF0	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	selected by OC_FILT[1:0]
0	1	1	LPF0	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	no offset cancellation
1	0	0	LPF1	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	selected by OC_FILT[1:0]
1	0	1	LPF1	G8 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	no offset cancellation
1	1	0	LPF1	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	selected by OC_FILT[1:0]
1	1	1	LPF1	G1 gain/range as defined in Section 11.2.12.1: ACC user sensitivity multiplier bits (ACCx_U_SNS_MULT[7:0])	bypassed	no offset cancellation

11.2.14 ACC user configuration 4 registers (ACC0_CFG_U4, ACC1_CFG_U4, ACC2_CFG_U4)

The ACC user configuration 4 registers are user programmable read/write registers, which contain acceleration specific configuration information. These registers are included in the read/write array error detection.

The ACCx_CFG_U4 registers are writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 61. **ACC user configuration 4 registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
5B	ACC0_CFG_U4	ACC0_RESET_OC	RESERVED	ACC0_OC_FILT[1:0]		RESERVED	RESERVED	ACC0_SIGCLIP_FLT[1:0]	
63	ACC1_CFG_U4	ACC1_RESET_OC	RESERVED	ACC1_OC_FILT[1:0]		RESERVED	RESERVED	ACC1_SIGCLIP_FLT[1:0]	
6B	ACC2_CFG_U4	ACC2_RESET_OC	RESERVED	ACC2_OC_FILT[1:0]		RESERVED	RESERVED	ACC2_SIGCLIP_FLT[1:0]	
Reset value		0	0	0	0	0	0	0	0

11.2.14.1 *ACC reset offset cancellation startup bit (ACCx_RESET_OC)*

When the ACC reset offset cancellation startup bit is written to logic 1, the offset cancellation is reset to the startup fast offset cancellation to remove quickly any startup offset according to the parameters in Table 14. Acceleration sensor signal chain. The ACCx_RESET_OC bit is cleared when the offset cancellation phase reaches phase 1.

11.2.14.2 *ACC offset cancellation filter selection bits (ACCx_OC_FILT[1:0])*

The ACC offset cancellation filter selection bits select the filter type to be used for offset cancellation. Reference Section 11.5.2.5: Acceleration offset cancellation for details regarding offset cancellation.

Table 62. **ACC offset cancellation filter selection bits**

ACCx_OC_FILT[1:0]		Offset cancellation IIR filter	Offset cancellation rate limiting
0	0	0.04 Hz	bypassed
0	1	0.04 Hz	enabled
1	0	0.005 Hz	bypassed
1	1	reserved	

11.2.14.3 *ACC signal clip filter selection bits (ACCx_SIGCLIP_FILT[1:0])*

The ACC signal clip filter selection bits select the filter time to be used for the associated ACC signal clip detection.

Table 63. **ACC signal clip filter selection bits**

ACCx_SIGCLIP_FILT[1:0]		Filter time for ACCx_SIGCLIP
0	0	1.024 ms
0	1	4.096 ms
1	0	8.192 ms
1	1	16.384 ms

11.2.15 ACC user configuration 5 registers (ACC0_CFG_U5, ACC1_CFG_U5, ACC2_CFG_U5)

The ACC user configuration 5 registers are user programmable read/write registers, which contain acceleration specific configuration information. These registers are included in the read/write array error detection.

The ACCx_CFG_U5 registers are writable until the ENDINIT bit is set in the DEVLOCK_WR register.

Table 64. **ACC user configuration 5 registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
5C	ACC0_CFG_U5	ACC0_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
64	ACC1_CFG_U5	ACC1_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
6C	ACC2_CFG_U5	ACC2_ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
Reset value		0	0	0	0	0	0	0	0

11.2.15.1 *ACC self-test control bits (ACCx_ST_CTRL[3:0])*

The ACC self-test control bits select the analog and digital self-test features of the device as shown in Table 65. ACC self-test control bits.

Table 65. **ACC self-test control bits**

ACCx_ST_CTRL[3:0]				Function	Sensor data	ACCx_ST_INC	ACCx_ST_ACTIVE
0	0	0	0	DSP writes to the ACCx_SNSDATAx registers	sensor data	no effect	clear when active
0	0	0	1			clear on activation	set when active
0	0	1	0			clear on activation	set when active
0	0	1	1			clear on activation	set when active
0	1	0	0	fixed pattern self-test; DSP writes to registers inhibited	0000h	clear on activation	set when active
0	1	0	1		AAAAh	clear on activation	set when active
0	1	1	0		5555h	clear on activation	set when active
0	1	1	1		FFFFh	clear on activation	set when active
1	0	0	0	positive analog self-test - low	sensor data	clear on activation	set when active
1	0	0	1	negative analog self-test - low		clear on activation	set when active
1	0	1	0	positive analog self-test - high		clear on activation	set when active
1	0	1	1	negative analog self-test - high		clear on activation	set when active
1	1	0	0	digital self-test	reference Table 11. Acceleration sensor signal chain	clear on activation	set when active
1	1	0	1			clear on activation	set when active
1	1	1	0			clear on activation	set when active
1	1	1	1			clear on activation	set when active

11.2.16 ARC and ACC sensor data 0 registers (ARC0_SNSDATA0, ACCx_SNSDATA0)

The ARC0 and ACC sensor data 0 registers are read-only registers, which contain the 16-bit sensor data. The data type for the sensor data 0 registers is selected by the DATATYPE0 bits in the xxx_CFG_U3 register. Reference Section 11.2.8: ARC0 user configuration 3 register (ARC0_CFG_U3) and Section 11.2.13: ACC user configuration 3 registers (ACC0_CFG_U3, ACC1_CFG_U3, ACC2_CFG_U3).

Table 66. **ARC and ACC sensor data 0 registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
72	ARC0_SNSDATA0_L	ARC0_SNSDATA0[7:0]							

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
73	ARC0_SNSDATA0_H	ARC0_SNSDATA0[15:8]							
8A	ACC0_SNSDATA0_L	ACC0_SNSDATA0[7:0]							
8B	ACC0_SNSDATA0_H	ACC0_SNSDATA0[15:8]							
92	ACC1_SNSDATA0_L	ACC1_SNSDATA0[7:0]							
93	ACC1_SNSDATA0_H	ACC1_SNSDATA0[15:8]							
9A	ACC2_SNSDATA0_L	ACC2_SNSDATA0[7:0]							
9B	ACC2_SNSDATA0_H	ACC2_SNSDATA0[15:8]							
Factory default		0	0	0	0	0	0	0	0

11.2.17 ARC and ACC sensor data 1 registers (ARC0_SNSDATA1, ACCx_SNSDATA1)

The ARC0 and ACC sensor data 1 registers are read-only registers, which contain the 16-bit sensor data. The data type for the sensor data 1 registers is selected by the DATATYPE1 bits in the xxx_CFG_U3 register. Reference Section 11.2.8: ARC0 user configuration 3 register (ARC0_CFG_U3) and Section 11.2.13: ACC user configuration 3 registers (ACC0_CFG_U3, ACC1_CFG_U3, ACC2_CFG_U3).

Table 67. ARC and ACC sensor data 1 registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
74	ARC0_SNSDATA1_L	ARC0_SNSDATA1[7:0]							
75	ARC0_SNSDATA1_H	ARC0_SNSDATA1[15:8]							
8C	ACC0_SNSDATA1_L	ACC0_SNSDATA1[7:0]							
8D	ACC0_SNSDATA1_H	ACC0_SNSDATA1[15:8]							
94	ACC1_SNSDATA1_L	ACC1_SNSDATA1[7:0]							
95	ACC1_SNSDATA1_H	ACC1_SNSDATA1[15:8]							
9C	ACC2_SNSDATA1_L	ACC2_SNSDATA1[7:0]							
9D	ACC2_SNSDATA1_H	ACC2_SNSDATA1[15:8]							
Factory default		0	0	0	0	0	0	0	0

11.2.18 ARC0 self-test registers (ARC0_ST_L, ARC0_ST_H)

The ARC0 self-test registers are read-only registers, which contain the 16-bit self-test value. When the ARC0 analog self-test is active, the value in this register can be compared to the limits specified in Table 10. Angular rate sensor signal chain. Refer to Section 11.4.1.1: Startup angular rate analog self-test for details regarding angular rate self-test.

Table 68. ARC0 self-test registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
76	ARC0_ST_L	ARC0_ST[7:0]							
77	ARC0_ST_H	ARC0_ST[15:8]							

11.2.19 ARC0 self-test storage registers (ARC0_ST_CMP_L, ARC0_ST_CMP_H)

The ARC self-test storage registers are factory programmed, read-only registers, which contain the self-test value for the angular rate signal. The 16-bit stored value is a 16-bit two's complement signed value. The angular rate self-test value can be a positive or negative value. If the stored value is a positive value, the angular rate self-test value is expected to be positive. If the stored value is a negative value, the angular rate self-test value is expected to be negative. The ARC0_ST_CMP registers are included in the ST OTP array error detection.

The ARC0_ST_CMP registers use a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 69. ARC0 self-test storage registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
A0	ARC0_ST_CMP_L	ARC0_ST_CMP[7:0]							
A1	ARC0_ST_CMP_H	ARC0_ST_CMP[15:8]							

Example angular rate self-test stored values and the associated comparison are shown in Table 70. Example angular rate self-test stored values.

Table 70. Example angular rate self-test stored values

Example register values Self-test stored value ARC0_ST_CMP			Example user measured self-test Measured value, self-test inactive ARC0_ST			Example user measured self-test Measured value, self-test active ARC0_ST			Self-test accuracy	
Address	Register value (LSB, hex)	Register value (LSB, decimal)	Address	Register value (LSB, hex)	Register value (LSB, decimal)	Address	Register value (LSB, hex)	Register value (LSB, decimal)	[%]	Pass/ fail
Example 1										
A1 and A0	0BFF	+3071	77 and 76	0011	17	77 and 76	09FF	+2559	-17.2	pass
Example 2										
A1 and A0	F200	-3584	77 and 76	0000	0	77 and 76	E00	+3584	wrong polarity	fail
Example 3										
A1 and A0	0CA5	+3237	77 and 76	0011	17	77 and 76	0CA5	+3237	-0.53	pass
Example 4										
A1 and A0	F333	-3277	77 and 76	0000	0	77 and 76	E533	-5851	+78.5	fail

11.2.20 ARC0 drive frequency (ARC0_FDRIVE)

The ARC0 drive frequency registers are factory programmed, read-only registers, which contain the ARC0 drive frequency. The stored value is a 16-bit unsigned value with a range from 0 Hz to 65535 Hz and a resolution of 1 Hz. The ARC0_FDRIVE registers are included in the ST OTP array error detection.

The ARC0_FDRIVE registers use a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 71. **ARC0 drive frequency**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
A2	ARC0_FDRIVE_L	ARC0_FDRIVE[7:0]							
A3	ARC0_FDRIVE_H	ARC0_FDRIVE[15:8]							

11.2.21 ACC self-test deflection storage registers

The ACC self-test deflection registers are factory programmed, read-only registers, which contain the nominal self-test values for the various self-tests at 25 °C. These registers are included in the ST OTP array error detection.

The ACCx_ST registers use a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 72. **ACC self-test deflection storage registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
B0	ACC0_STL_P_L	ACC0_STL_P[7:0]							
B1	ACC0_STL_P_H	ACC0_STL_P[15:8]							
B2	ACC0_STH_P_L	ACC0_STH_P[7:0]							
B3	ACC0_STH_P_H	ACC0_STH_P[15:8]							
B4	ACC0_STL_N_L	ACC0_STL_N[7:0]							
B5	ACC0_STL_N_H	ACC0_STL_N[15:8]							
B6	ACC0_STH_N_L	ACC0_STH_N[7:0]							
B7	ACC0_STH_N_N	ACC0_STH_N[15:8]							
B8	ACC1_STL_P_L	ACC1_STL_P[7:0]							
B9	ACC1_STL_P_H	ACC1_STL_P[15:8]							
BA	ACC1_STH_P_L	ACC1_STH_P[7:0]							
BB	ACC1_STH_P_H	ACC1_STH_P[15:8]							
BC	ACC1_STL_N_L	ACC1_STL_N[7:0]							
BD	ACC1_STL_N_H	ACC1_STL_N[15:8]							
BE	ACC1_STH_N_L	ACC1_STH_N[7:0]							
BF	ACC1_STH_N_H	ACC1_STH_N[15:8]							
C0	ACC2_STL_P_L	ACC2_STL_P[7:0]							
C1	ACC2_STL_P_H	ACC2_STL_P[15:8]							
C2	ACC2_STH_P_L	ACC2_STH_P[7:0]							
C3	ACC2_STH_P_H	ACC2_STH_P[15:8]							
C4	ACC2_STL_N_L	ACC2_STL_N[7:0]							
C5	ACC2_STL_N_H	ACC2_STL_N[15:8]							
C6	ACC2_STH_N_L	ACC2_STH_N[7:0]							
C7	ACC2_STH_N_H	ACC2_STH_N[15:8]							

The self-test stored values are positive and negative deflection values, measured at ST production test, and programmed for each device. Table 73. Register definitions describes the data stored in each register. All self-test and offset values are scaled to a user gain of 1. ACCx_U_SNS_SHIFT[1:0] = 2h, ACCx_U_SNS_MULT[7:0] = 00h and with the 1 × gain selection.

Table 73. Register definitions

Register name	Description
ACC0_STL_P	the ACC0 positive low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 8h	$ACC0_SNSDATA0_{ST_CTRL=8h} - ACC0_SNSDATA0_{ST_CTRL=0h}$
ACC0_STH_P	the ACC0 positive high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Ah	$ACC0_SNSDATA0_{ST_CTRL=Ah} - ACC0_SNSDATA0_{ST_CTRL=0h}$
ACC0_STL_N	the ACC0 negative low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 9h	$ACC0_SNSDATA0_{ST_CTRL=9h} - ACC0_SNSDATA0_{ST_CTRL=0h}$
ACC0_STH_N	the ACC0 negative high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Bh	$ACC0_SNSDATA0_{ST_CTRL=Bh} - ACC0_SNSDATA0_{ST_CTRL=0h}$
ACC1_STL_P	the ACC1 positive low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 8h	$ACC1_SNSDATA0_{ST_CTRL=8h} - ACC1_SNSDATA0_{ST_CTRL=0h}$
ACC1_STH_P	the ACC1 positive high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Ah	$ACC1_SNSDATA0_{ST_CTRL=Ah} - ACC1_SNSDATA0_{ST_CTRL=0h}$
ACC1_STL_N	the ACC1 negative low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 9h	$ACC1_SNSDATA0_{ST_CTRL=9h} - ACC1_SNSDATA0_{ST_CTRL=0h}$
ACC1_STH_N	the ACC1 negative high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Bh	$ACC1_SNSDATA0_{ST_CTRL=Bh} - ACC1_SNSDATA0_{ST_CTRL=0h}$
ACC2_STL_P	the ACC2 positive low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 8h	$ACC2_SNSDATA0_{ST_CTRL=8h} - ACC2_SNSDATA0_{ST_CTRL=0h}$
ACC2_STH_P	the ACC2 positive high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Ah	$ACC2_SNSDATA0_{ST_CTRL=Ah} - ACC2_SNSDATA0_{ST_CTRL=0h}$
ACC2_STL_N	the ACC2 negative low self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = 9h	$ACC2_SNSDATA0_{ST_CTRL=9h} - ACC2_SNSDATA0_{ST_CTRL=0h}$
ACC2_STH_N	the ACC2 negative high self-test magnitude at device manufacturing: signed 16-bit
ST_CTRL = Bh	$ACC2_SNSDATA0_{ST_CTRL=Bh} - ACC2_SNSDATA0_{ST_CTRL=0h}$

When the user activates the self-test, the sensor data can be compared to the values in these registers. Reference Section 11.5.1.2: Acceleration analog delta self-test deflection verification for more details on calculating the self-test limits. Before comparing self-test values, the measured self-test must be scaled to a user gain of 1. An example of scaling and comparison is shown in Table 74. Example of scaling and comparison for both positive and negative self-test. Reference the latest application notes for the recommended procedures.

Table 74. **Example of scaling and comparison**

Example register values				Example user measured self-test				Self-test accuracy [%]
Address	Register	Register value	Self-test stored value LSB, 16-bit	User gain	User range [g]	Measured self-test at user gain LSB, 16-bit	Self-test adjusted to gain of 1 LSB, 16-bit	
Example 1								
B3 and B2	ACC0_STH_P	219Eh	8606	1.711	3.5	14628	8550	-0.65
B5 and B4	ACC0_STH_N	DE30h	-8656	1.711	3.5	-14885	-8700	+0.51
Example 2								
B3 and B2	ACC0_STH_P	2200h	8704	1.711	3.5	14628	8550	-1.77
B5 and B4	ACC0_STH_N	DE20h	-8672	1.711	3.5	-14885	-8700	+0.32

11.2.22 IC type register

The IC type register is a factory programmed, read-only register, which contains the IC type as defined in Table 75. IC type register. This register is included in the ST OTP array error detection.

The ICTYPEID register uses a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 75. **IC type register**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
C8	ICTYPEID	0	0	0	1	0	1	0	0

11.2.23 Device revision ID register

The device revision ID register is an ST programmed, read-only register, which includes device revision information for traceability purposes. This register is included in the ST OTP array error detection.

The DEVICE_REV register uses a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 76. **Device revision ID register**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
C9	DEVICE_REV	DEVICE_REV[7:0]							

11.2.24 ASIC revision register

The ASIC revision register is an ST programmed, read-only register, which contains the ASIC revision. The upper nibble contains the main ASIC revision. The lower nibble contains the sub-ASIC revision. This register is included in the ST OTP array error detection.

The ASCIREVID register uses a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 77. **ASIC revision register**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
CA	ASICREVID	ASICREVID[7:0]							

11.2.25 Angular rate MEMS revision register

The angular rate MEMS revision register is an ST programmed, read-only register, which contains revision information for the angular rate MEMS silicon in the device. This register is included in the ST OTP array error detection.

The ARCMEMS0REVID register uses a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 78. Angular rate MEMS revision register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
CB	ARCMEMS0REVID	ARCMEMS0REVID[7:0]							

11.2.26 Acceleration MEMS revision register

The acceleration MEMS revision register is an ST programmed, read-only register, which contains revision information for the acceleration MEMS silicon in the device. This register is included in the ST OTP array error detection.

The ACCMEMS0REVID register uses a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 79. Acceleration MEMS revision register

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
CC	ACCMEMS0REVID	ACCMEMS0REVID[7:0]							

11.2.27 Part number registers

The part number registers are ST programmed, read-only registers, which include the numeric portion of the device part number. These registers are included in the ST OTP array error detection.

The PN registers use a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

Table 80. Part number registers

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
D0	PN0	PN0[7:0]							
Reset value		0	0	1	1	0	1	0	1
D1	PN1	PN1[7:0]							
Reset value		0	0	0	0	0	0	0	1

11.2.28 Device serial number registers

The serial number registers are ST programmed, read-only registers, which include the unique serial number of the device.

The serial number registers use a shared register read block. Reference Section 11.2.5: F region selection registers (F_REGION_x) for the procedure to read data using the shared register block.

The serial number registers include the following registers:

- A 16-bit numeric assembly serial number
- A 16-bit numeric assembly lot number and an 80-bit alphanumeric assembly lot number

Table 81. **Device serial number registers**

Location		Bit							
Address (hex)	Register	7	6	5	4	3	2	1	0
D2	SERIALNUMBER0	SERIALNUMBER[7:0]							
D3	SERIALNUMBER1	SERIALNUMBER[15:8]							
D4	LOTNUMBER0	LOTNUMBER[7:0]							
D5	LOTNUMBER1	LOTNUMBER[15:8]							
D6	ASSY_LOT0	ASSY_LOT[7:0]							
D7	ASSY_LOT1	ASSY_ LOT[15:8]							
D8	ASSY_LOT2	ASSY_ LOT[23:16]							
D9	ASSY_ LOT3	ASSY_ LOT[31:24]							
DA	ASSY_ LOT4	ASSY_ LOT[39:32]							
DB	ASSY_ LOT5	ASSY_ LOT[47:40]							
DC	ASSY_ LOT6	ASSY_ LOT[55:48]							
DD	ASSY_ LOT7	ASSY_ LOT[63:56]							
DE	ASSY_ LOT8	ASSY_ LOT[71:64]							
DF	ASSY_ LOT9	ASSY_ LOT[79:72]							

11.2.29 Reserved registers

A register read command to a reserved register or a register with reserved bits results in a valid response. The data for the reserved bits is logic 0 or logic 1.

A register write command to a reserved register or a register with reserved bits executes and results in a valid response. The data for the reserved bits is logic 0 or logic 1. A write to the reserved bits must always be logic 0 for normal device operation and performance.

11.2.30 Invalid register addresses

A register read command to a register address outside the addresses listed in Section 11.1: User-accessible data array result in a valid response. The data for the registers is 00h.

A register write command to a register address outside the addresses listed in Section 11.1: User-accessible data array does not execute but result in a valid response. The data for the registers is 00h.

A register write command to a read-only register does not execute but result in a valid response. The data for the registers is the current contents of the register.

11.3 OTP and read/write register array error detection

11.3.1 ST OTP array

All registers noted with an F are user readable registers with OTP. The OTP ECC verifies these registers.

11.3.2 Read/write registers

All registers of type R/W are user read/write registers, except the DEVLOCK_WR register. A continuous 4-bit CRC that is calculated on the entire array once ENDINIT is set verifies them. The CRC verification uses a generator polynomial of $g(x) = x^4 + x^3 + 1$, with a seed value = 0000. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

11.4 Angular rate sensor signal path

11.4.1 Angular rate self-test

A deflection is generated by applying an electrostatic force to the sense resonator that is in phase with the position of the drive resonator. The signal is recovered by sensing the capacitance change associated with the movement of the sense resonator in the quadrature phase.

11.4.1.1 Startup angular rate analog self-test

When the ENDINIT bit is not set, the user can activate the analog self-test by writing to the ST_CTRL[3:0] bits in the ARC_CFG_U5 register.

The angular rate self-test value is provided in the ARC0_ST register. The absolute value of the 16-bit value read from the ARC0_ST register can be averaged and compared against the limits listed in Table 10. Angular rate sensor signal chain using the equation below.

$$ARC0SelfTest = |ARC0_ST_{STEnabled} - ARC0_ST_{STDisabled}|$$

The angular rate self-test value can also be verified against the nominal temperature self-test value recorded at the time the device was produced. The production self-test value is stored in the ARC0 self-test storage registers as defined in Section 11.2.19: ARC0 self-test storage registers (ARC0_ST_CMP_L, ARC0_ST_CMP_H). The following equations determine the delta self-test limits.

$$\Delta ST_{ARC0MaxLimit} = ARC0_ST_CMP^{*}(1 - \Delta ST_{ARC0})$$

Note: This value is truncated.

$$\Delta ST_{ARC0MaxLimit} = ARC0_ST_CMP^{*}(1 + \Delta ST_{ARC0})$$

Note: This value is rounded up.

Where:

ΔST_{ARC0} is the accuracy of the self-test deflection relative to the stored deflection as specified in Table 10. Angular rate sensor signal chain

ARC0_ST_CMP is the value stored in the ARC0 self-test storage register as defined in Section 11.2.19: ARC0 self-test storage registers (ARC0_ST_CMP_L, ARC0_ST_CMP_H)

11.4.1.2 Startup angular rate digital self-test

When the ENDINIT bit is not set, the user can activate a digital self-test by writing to the ST_CTRL[3:0] bits in the ARC0_CFG_U5 register. The digital self-test inputs a known signal stream into the front end of the DSP. After a delay defined by the low-pass filter selected, the output sensor data reaches a fixed value. The user can verify this value. The digital self-test values are listed in Table 10. Angular rate sensor signal chain.

On deactivation of digital self-test C, D and E (ST_CTRL = Ch, Dh, Eh), the ARC0_SIGCLIP bit is set in the ARC0_STAT register. A read of the ARC0_STAT register clears the ARC0_SIGCLIP bit.

11.4.1.3 Startup angular rate fixed pattern self-test

When the ENDINIT bit is not set, the user can activate a fixed pattern self-test by writing to the ST_CTRL[3:0] bits in the ARC_CFG_U5 register. Fixed pattern self-tests force the DSP output to a set of known values enabling the user to verify each bit of the sensor data. Fixed pattern self-test values are listed in Section 11.2.10.1: ARC0 self-test control bits (ARC0_ST_CTRL[3:0]).

11.4.2 Angular rate digital signal processor

A DSP is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 5. Angular rate signal processing flow.

Figure 5. Angular rate signal processing flow

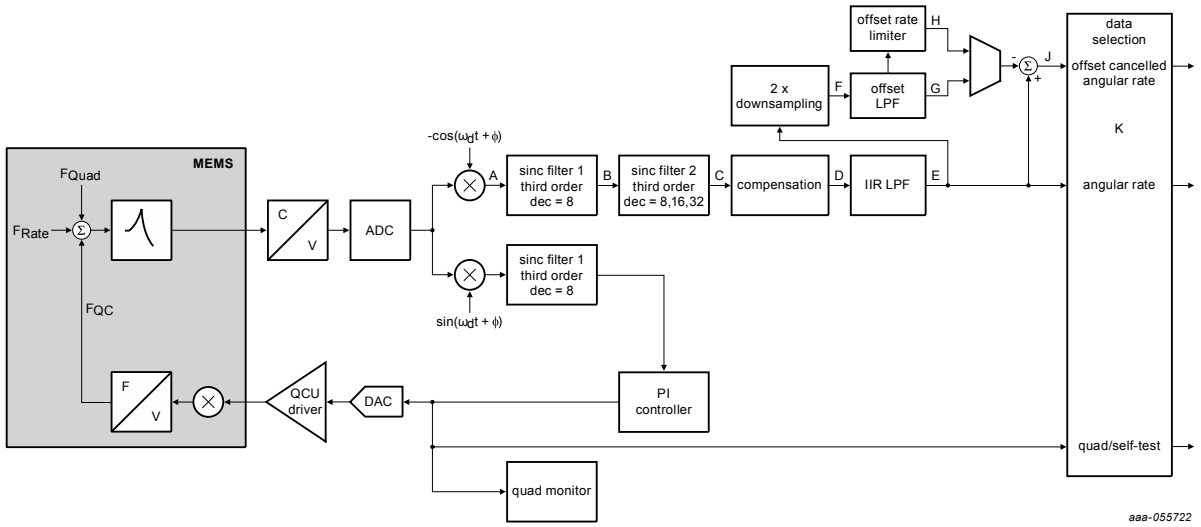


Table 82. Angular rate signal processing flow parameters

	Description	Sample time (µs)	Reference
A	ΣΔ	6.25	
B	sinc filter 1	50	
C	sinc filter 2	400, 800, 1600	
D	compensation and digital clipping	400, 800, 1600	Section 11.4.2.1: Angular rate signal trim, compensation, and digital clipping
E	low-pass filter	400, 800, 1600	Section 11.4.2.2: Angular rate low-pass filter
F	downsampling	800, 1600, 3200	Section 11.4.2.3: Angular rate offset cancellation
G	offset low-pass filter	800, 1600, 3200	Section 11.4.2.3: Angular rate offset cancellation
H	offset rate limiting	800, 1600, 3200	Section 11.4.2.3: Angular rate offset cancellation
J	offset subtraction	800, 1600, 3200	Section 11.4.2.3: Angular rate offset cancellation
K	output range selection	400, 800, 1600	Section 11.4.2.4: Angular rate output scaling

11.4.2.1 *Angular rate signal trim, compensation, and digital clipping*

The device includes digital trim to compensate the sensor offset, sensitivity, and nonlinearity over temperature. Once this signal is compensated, the signal is digitally clipped to maximize the symmetry between the positive and negative electrical dynamic range.

11.4.2.2 *Angular rate low-pass filter*

An IIR low-pass filter processes the angular rate signal.

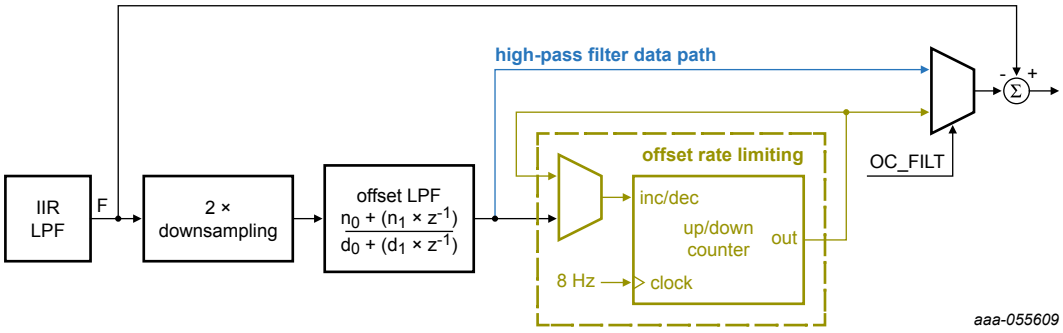
The device provides the option for one of several low-pass filters. The filter is selected with the ARC0_LPF[1:0] bits in the ARC0_CFG_U1 registers.

The filter selection options are listed in Section 11.2.7: ARC0 user configuration 1 register (ARC0_CFG_U1). Response parameters for the low-pass filter are specified in Table 13. Angular rate sensor signal chain.

11.4.2.3 *Angular rate offset cancellation*

The device provides an optional offset cancellation circuit to remove the internal offset error. A simplified block diagram of the offset cancellation is shown in Figure 6. Angular rate offset cancellation block diagram.

Figure 6. Angular rate offset cancellation block diagram



Response parameters are specified in Table 13. Angular rate sensor signal chain.

During startup, multiple phases of the offset low-pass filter are used to allow for fast convergence of the internal offset error during initialization. The offset rate limiting is bypassed during startup regardless of the state of the OC_FILT bits in the ARC_CFG_U4 register.

In normal mode, the offset low-pass filter frequency can be selected, and output rate limiting can be applied to the output of the offset low-pass filter via the OC_FILT bits in the ARC0_CFG_U4 register. Rate limiting can only be enabled if the 0.04 Hz offset LPF is selected. If rate limiting is enabled, $\omega_{RL(step)(125)}$ or $\omega_{RL(step)(250)}$ or $\omega_{RL(step)(350)}$, LSB updates the offset cancellation output every $t_{upd(o)}$.

The offset cancellation circuit output value is frozen when analog or digital self-test is active (ST_CTRL = 8h to Fh) regardless of the offset cancellation phase. When analog or digital self-test is deactivated, the offset cancellation output value freeze is extended for 30 ms and the ARC0_RESET_OC bit is set, enabling reinitialization of the offset cancellation filter.

11.4.2.4 *Angular rate output scaling*

Sensor data is in signed two's complement format. Table 83. Angular rate data output versus input angular rate shows typical sensor data readings for each range.

Table 83. Angular rate data output versus input angular rate

Angular rate input (dps)	125 dps range sens = 262.1 LSB/dps (LSB, 16 bit)	250 dps range sens = 131.1 LSB/dps (LSB, 16 bit)	500 dps range sens = 65.53 LSB/dps (LSB, 16 bit)
-350.0	-32767	-32767	-22937
-349.0	-32767	-32767	-22871
-348.0	-32767	-32767	-22806
…	…	…	…
-250.0	-32767	-32767	-16384
-249.0	-32767	-32636	-16318
-248.0	-32767	-32505	-16252
…	…	…	…
-2.0	-524	-262	-131
-1.0	-262	-131	-66
0.0	0	0	0
1.0	262	131	66

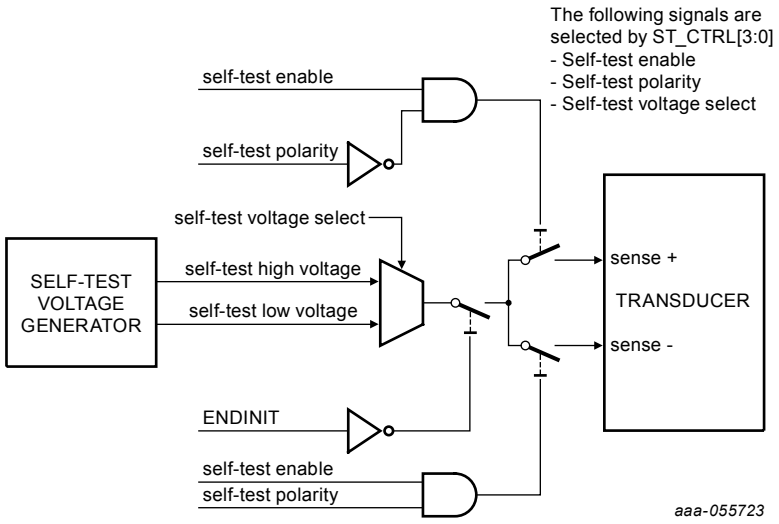
Angular rate input (dps)	125 dps range sens = 262.1 LSB/dps (LSB, 16 bit)	250 dps range sens = 131.1 LSB/dps (LSB, 16 bit)	500 dps range sens = 65.53 LSB/dps (LSB, 16 bit)
2.0	524	262	131
…	…	…	…
248.0	32767	32505	16252
249.0	32767	32636	16318
250.0	32767	32767	16384
…	…	…	…
348.0	32767	32767	22806
349.0	32767	32767	22871
350.0	32767	32767	22937

11.5 Acceleration sensor signal path

11.5.1 Acceleration sensor self-test interface

The analog self-test interface applies a voltage to the g-cell, causing deflection of the proof mass. The resulting sensor data can be compared against the values stored in the self-test deflection storage registers (reference Section 11.2.21: ACC self-test deflection storage registers). The self-test interface is controlled through register write operations to the ACCx_ST_CTRL[3:0] bits in the ACCx_CFG_U5 register described in Section 11.2.15.1: ACC self-test control bits (ACCx_ST_CTRL[3:0]). A diagram of the self-test interface is shown in Figure 7. Acceleration self-test interface.

Figure 7. Acceleration self-test interface



Two self-test magnitudes are available for each device range. The self-test magnitude is selected via the ACCx_ST_CTRL[3:0] bits.

11.5.1.1 Acceleration analog self-test deflection verification

The raw self-test deflection can be verified against raw self-test limits in Table 11. Acceleration sensor signal chain.

11.5.1.2 *Acceleration analog delta self-test deflection verification*

The raw self-test deflection can be verified against the nominal temperature self-test deflection value recorded at the time the device was produced. The production self-test deflection is stored in the self-test deflection storage registers as defined in Section 11.2.21: ACC self-test deflection storage registers. The following equations determine the delta self-test deflection limits.

$$\Delta ST_{ACCMINLIMIT} = STDATA \times (1 - \Delta ST_{ACC})$$

Note: This value is truncated.

$$\Delta ST_{ACCMAXLIMIT} = STDATA \times (1 + \Delta ST_{ACC})$$

Note: This value is rounded up.

Where:

ΔST_{ACC} is the accuracy of the self-test deflection relative to the stored deflection as specified in Table 11. Acceleration sensor signal chain

STDATA is the value stored in the appropriate self-test deflection storage register as defined in Section 11.2.21: ACC self-test deflection storage registers

11.5.1.3 *Acceleration startup digital self-test*

When the ENDINIT bit is not set, the user can activate a digital self-test by writing to the ACCx_ST_CTRL[3:0] bits in the ACCx_CFG_U5 register. The digital self-test inputs a known signal stream into the front end of the DSP. After a delay defined by the low-pass filter selected, the output sensor data reaches a fixed value. The user can verify this value. The digital self-test values are listed in Table 11. Acceleration sensor signal chain.

11.5.1.4 *Acceleration fixed pattern self-test*

When the ENDINIT bit is not set, the user can activate a fixed pattern self-test by writing to the ACCx_ST_CTRL[3:0] bits in the ACCx_CFG_U5 register. Fixed pattern self-tests force the DSP output to a set of known values enabling the user to verify each bit of the sensor data. Fixed pattern self-test values are listed in Section 11.2.15.1: ACC self-test control bits (ACCx_ST_CTRL[3:0]).

11.5.2 Acceleration sensor digital signal processor

A DSP is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 8. Acceleration signal processing flow.

Figure 8. Acceleration signal processing flow

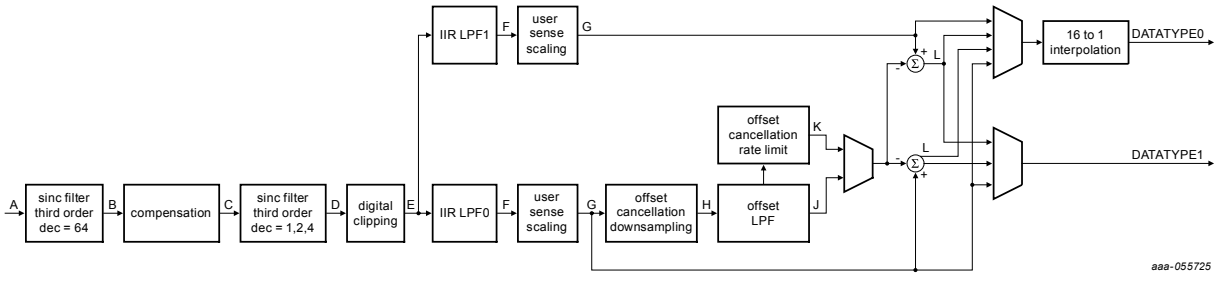


Table 84. Acceleration signal processing flow parameters

	Description	Sample time (µs)	Reference
A	ΣΔ	0.9766	
B	sinc filter 1	62.5	
C	compensation	62.5	Section 11.5.2.1: Acceleration signal trim and compensation

	Description	Sample time (µs)	Reference
D	sinc filter 2	62.5, 125, 250	
E	digital clipping	62.5, 125, 250	Section 11.5.2.2: Acceleration digital clipping
F	low-pass filter 0 and 1	62.5, 125, 250	Section 11.5.2.3: Acceleration low-pass filter
G	user scaling	62.5, 125, 250	Section 11.5.2.4: Acceleration user sensitivity scaling
H	offset cancellation downsampling	1000	Section 11.5.2.5: Acceleration offset cancellation
J	offset low-pass filter	1000	Section 11.5.2.5: Acceleration offset cancellation
K	offset rate limiting	1000	Section 11.5.2.5: Acceleration offset cancellation
L	offset subtraction	250, 500, 1000	Section 11.5.2.5: Acceleration offset cancellation
	output range selection	3.906, 7.813, 15.63	Section 11.5.2.7: Acceleration output scaling
	interpolation	3.906, 7.813, 15.63	Section 11.5.2.6: Acceleration data interpolation

11.5.2.1 *Acceleration signal trim and compensation*

The device includes digital trim to compensate for sensor offset, sensitivity, and nonlinearity over temperature.

11.5.2.2 *Acceleration digital clipping*

The device includes a digital clipping block to maximize the symmetry between the positive and negative electrical dynamic range of the device.

11.5.2.3 *Acceleration low-pass filter*

An IIR low-pass filter processes data from the sinc filter. Each acceleration channel provides the option for two independent low-pass filters as shown in Section 11.5.2: Acceleration sensor digital signal processor. The filter type is selected with the ACCx_LPF0[1:0] and ACCx_LPF1[1:0] bits in the ACCx_CFG_U1 registers. Reference Section 11.2.11: ACC user configuration 1 registers (ACC0_CFG_U1, ACC1_CFG_U1, ACC2_CFG_U1).

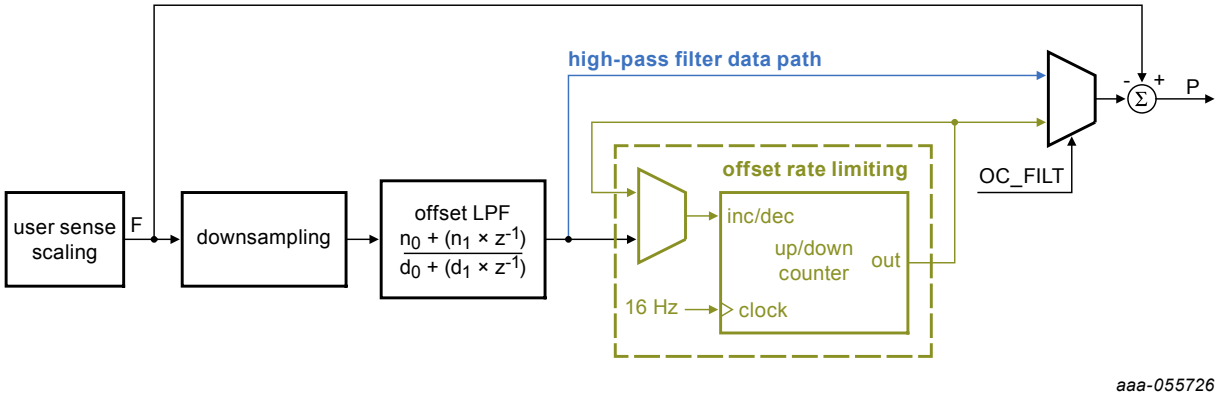
11.5.2.4 *Acceleration user sensitivity scaling*

The device includes user-controlled sensitivity scaling as described in Section 11.2.11: ACC user configuration 1 registers (ACC0_CFG_U1, ACC1_CFG_U1, ACC2_CFG_U1) and Section 11.2.12: ACC user configuration 2 registers (ACC0_CFG_U2, ACC1_CFG_U2, ACC2_CFG_U2).

11.5.2.5 *Acceleration offset cancellation*

The device provides an optional offset cancellation circuit to remove the internal offset error. A simplified block diagram of the offset cancellation is shown in Figure 9. Acceleration offset cancellation block diagram.

Figure 9. **Acceleration offset cancellation block diagram**



Response parameters are specified in Table 14. Acceleration sensor signal chain.

During startup, multiple phases of the offset low-pass filter are used to allow for fast convergence of the internal offset error during initialization. The offset rate limiting is bypassed during startup regardless of the state of the OC_FILT bits in the ACCx_CFG_U4 register.

In normal mode, the offset low-pass filter frequency can be selected, and output rate limiting can be applied to the output of the offset low-pass filter via the OC_FILT bits in the ACCx_CFG_U4 register. Rate limiting can only be enabled if the 0.04 Hz offset LPF is selected. If rate limiting is enabled, $A_{RL(step)}$ LSB updates the offset cancellation output every $t_{upd(o)}$.

The offset cancellation circuit output value is frozen when analog or digital self-test is active (ST_CTRL = 8h to Fh) regardless of the offset cancellation phase. When analog or digital self-test is deactivated, the offset cancellation output value freeze is extended for 30 ms and the ACCx_RESET_OC bit is set, enabling reinitialization of the offset cancellation filter.

11.5.2.6 *Acceleration data interpolation*

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. Transmitted data is interpolated from the two previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1/16 of the sample time.

11.5.2.7 *Acceleration output scaling*

Sensor data is in signed two's complement format.

Table 85. Acceleration data output versus input acceleration shows typical sensor data readings for an example configuration.

Table 85. **Acceleration data output versus input acceleration**

Acceleration input (g)	6 g range sens = 5458 LSB/g (LSB, 16 bit)	48 g range sens = 682.3 LSB/g (LSB, 16 bit)
-34.0	-32767	-23199
-33.9	-32767	-23131
-33.8	-32767	-23063
…	…	…
-6.0	-32752	-4094
-5.9	-32206	-4026
-5.8	-31660	-3958
…	…	…
-0.2	-1092	-136

Acceleration input (g)	6 g range sens = 5458 LSB/g (LSB, 16 bit)	48 g range sens = 682.3 LSB/g (LSB, 16 bit)
-0.1	-546	-68
0.0	0	0
0.1	546	68
0.2	1092	136
…	…	…
5.8	31660	3958
5.9	32206	4026
6.0	32752	4094
…	…	…
33.8	32767	23063
33.9	32767	23131
34.0	32767	23199

11.6 Temperature sensor

The device includes a temperature sensor for signal compensation. The output of the temperature sensor is provided for user readability. Temperature sensor parameters are specified in Table 9. Temperature sensor signal chain.

The following equation is used to convert temperature readings.

$$T_{DEGC} = \frac{T_{LSB} - T_{25}}{S_{temp}} + 25$$

Where:

T_{DEGC} is the temperature output in degree Celsius

T_{LSB} is the temperature output in LSB

T_{25} is the expected temperature output in LSB at 25 °C (reference Table 9. Temperature sensor signal chain)

S_{temp} is the expected temperature sensitivity in LSB/°C (reference Table 9. Temperature sensor signal chain)

11.7 SafeSPI revision 2.0 protocol

The device supports the following SafeSPI revision 2.0 protocols:

- Out-of-frame protocol with dedicated sensor select
- Out-of-frame protocol with shared sensor select

SafeSPI revision 2.0 protocol uses the following protocol settings:

- The message length = 32 bit
- The MSB is transmitted first
- CPOL = 0
  - SCLK must be LOW when SS_B is asserted
  - SCLK must be LOW when SS_B is deasserted
- CPHA = 0
  - SDO data changes on the falling edge of SCLK
  - SDI data is captured on the rising edge of SCLK

11.7.1 SafeSPI sensor addressing

Each SPI sensor accessed using SafeSPI is associated with a 2-bit sensor address. The sensor address is embedded in each command and response transfer. If and only if the sensor address in the command matches the sensor address assigned to the device, commands are executed and responses transferred. Sensor address assignment options are summarized in Table 86. SPI address pin selection.

Table 86. SPI address pin selection

Pin state		Sensor address
SPI_SA1	SPI_SA0	SA[1:0]
V_{SS}	V_{SS}	00
V_{SS}	V_{CC}	01
V_{CC}	V_{SS}	10
V_{CC}	V_{CC}	11

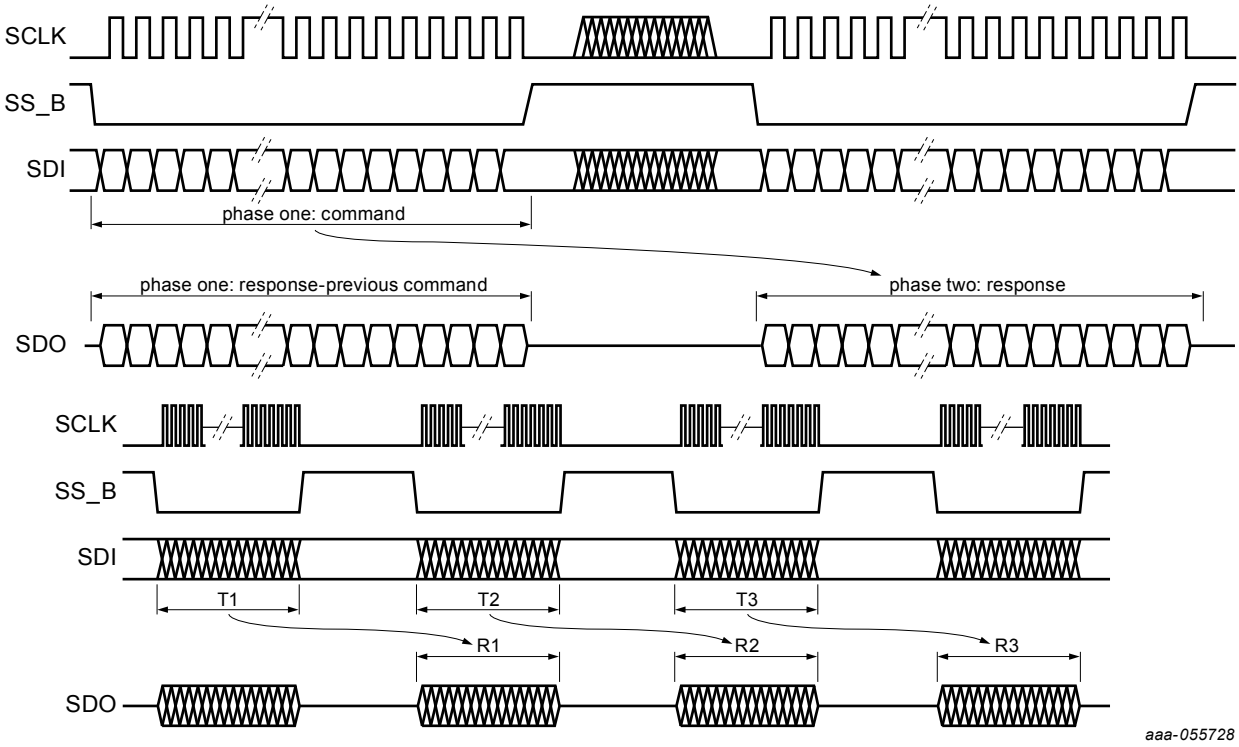
Notes:

- If SS_B is connected to a shared sensor select signal, a unique sensor address must be assigned using the SPI_SA1 and SPI_SA0 pins.
- The state of the SPI_SA1 and SPI_SA0 pins is not latched. The pin states are continuously monitored. A change to the state of the pins immediately impacts the sensor address state.
- If the sensor address included in a command does not match the device sensor address, the device monitors SDI for a valid command but does not respond (SDO remains in high-impedance state) during the subsequent transfer.

11.7.2 SafeSPI protocol timing

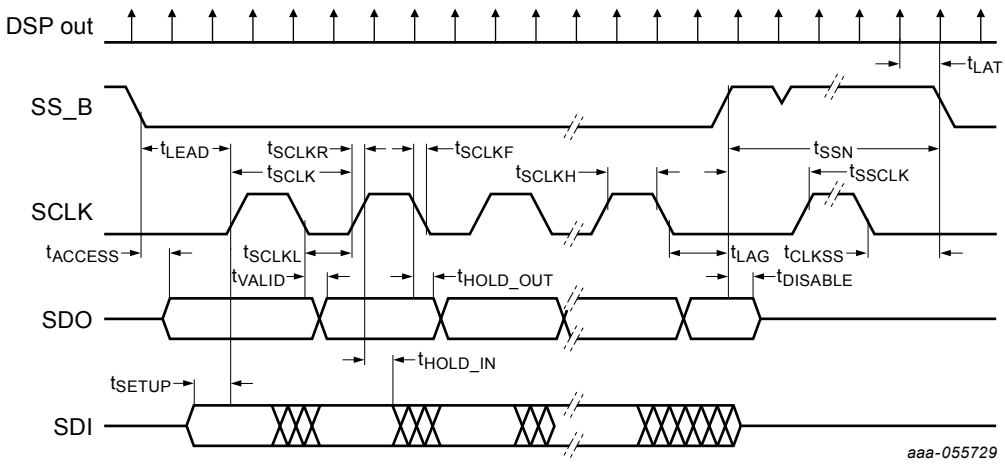
SafeSPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI controller to the device. During the second phase, response data is transmitted from the sensor device. SDI and SCLK transitions are ignored and SDO is placed in a high-impedance state when SS_B is not asserted.

Figure 10. SafeSPI protocol transfer timing



SafeSPI timing parameters are shown in Figure 11. SafeSPI protocol timing diagram and specified in Table 12. SafeSPI.

Figure 11. SafeSPI protocol timing diagram



11.7.3 SafeSPI command and response summary

11.7.3.1 SafeSPI protocol command format

Table 87. SafeSPI command format

MSB																												LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register read access command																															
Sensor address			register address							R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3-bit CRC		
SA[1:0]			RA[7:1]						X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[2:0]		
Register write access command																															
Sensor address			register address							R/W	0	0	register data															3-bit CRC		
SA[1:0]			RA[7:1]						X	1	0	0	RD[15:0]															CRC[2:0]		

11.7.3.2 SafeSPI protocol response format

Table 88. SafeSPI response format

MSB																												LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Normal response to register read access request																															
D	sensor address		register address							0	S1	register data																S0	3-bit CRC		
D	SA[1:0]		RA[7:1]							0	S1	RD[15:0]																S0	CRC[2:0]		
Normal response to register write access request																															
D	sensor address		register address							0	S1	register data																S0	3-bit CRC		
D	SA[1:0]		RA[7:1]							0	S1	RD[15:0]																S0	CRC[2:0]		
Error response																															
D	sensor address		register address							0	S1	register data																S0	3-bit CRC		
0	SA[1:0]		RA[7:1]							0	0	RD[15:0]																1	CRC[2:0]		
SPI error response																															
D	sensor address		register address							0	S1	register data																S0	3-bit CRC		
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

11.7.3.3 *SafeSPI protocol register read command*

The register read command uses the upper 7 bits of the addresses defined in Section 11.1: User-accessible data array to address two 8-bit registers in the register map. The response to the command includes the contents of RA[7:1] high byte (RA.0 = 1) in the upper byte and the contents of RA[7:1] low byte (RA.0 = 0) in the lower byte.

The register read response includes the register contents at the rising edge of SS_B for the register read command. The register contents are transmitted in the response regardless of the state of the S[1:0] bits.

11.7.3.3.1 SafeSPI protocol register read request command message format

Table 89. SafeSPI protocol register read request command message format

MSB																													LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sensor address		register address								R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3-bit CRC		
SA[1:0](1)		RA[7:1](2)							X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[2:0](3)		

1. *Reference Section 11.2.6.*
2. *RA[7:1] contains the word address of the register to be read.*
3. *Reference Section 11.7.4.1.*

11.7.3.3.2 SafeSPI protocol register read request response message format

Table 90. SafeSPI protocol register read request response message format

MSB																													LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D(1)	sensor address		register address							0	S1(2)	data: contents of RA[7:1](3) high byte								data: contents of RA[7:1](3) low byte								S0(2)	3-bit CRC		
D(1)	SA[1:0](4)		RA[7:1](3)							0	S1(2)	RD[15:8](5)								RD[7:0](6)								S0(2)	CRC[2:0](7)		

1. *D = 1: sensor data, D = 0: non-sensor data.*
2. *SafeSPI status; reference Section 11.7.5.1.*
3. *RA[7:1] contains the word address of the register to be read.*
4. *Reference Section 11.2.6.*
5. *The contents of the register addressed by RA[7:1] high byte (RA.0 = 1).*
6. *The contents of the register addressed by RA[7:1] low byte (RA.0 = 0).*
7. *Reference Section 11.7.4.1.*

11.7.3.4 *SafeSPI protocol register write command*

The register write command uses the upper 7 bits of the addresses defined in Section 11.1: User-accessible data array to write the value in RD[15:0] to two 8-bit registers in the register map. The response to the command includes the new contents of RA[7:1] high byte (RA.0 = 1) in the upper byte and the contents of RA[7:1] low byte (RA.0 = 0) in the lower byte.

The register is not written until the transfer during which the register write was requested has been completed.

If and only if the ENDINIT bit is cleared as documented in Section 11.2.4.1: End initialization bit (ENDINIT), the register write is executed and a response is transmitted on the next SPI message.

The register write response includes the register contents at the rising edge of SS_B for the register write command.

11.7.3.4.1 SafeSPI protocol register write request command message format

Table 91. SafeSPI protocol register write request command message format

MSB																													LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sensor address		register address								R/W	0	0	data to be written to RA[7:1][1] high byte							data to be written to RA[7:1][1] low byte								3-bit CRC		
SA[1:0][2]		RA[7:1][1]							X	1	0	0	RD[15:8][3]							RD[7:0][4]								CRC[2:0][5]		

1. *RA[7:1] contains the word address of the register to be read.*
2. *Reference Section 11.2.6.*
3. *The new contents of the register addressed by RA[7:1] high byte (RA.0 = 1).*
4. *The new contents of the register addressed by RA[7:1] low byte (RA.0 = 0).*
5. *Reference Section 11.7.4.1*

11.7.3.4.2 SafeSPI protocol register write request response message format

Table 92. SafeSPI protocol register write request response message format

MSB																													LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D	sensor address		register address							0	S1[1]	data: contents of RA[7:1][2] high byte								data: contents of RA[7:1][2] low byte								S0[1]	3-bit CRC		
0	SA[1:0][3]		RA[7:1][2]							0	S1[1]	RD[15:8][4]								RD[7:0][5]								S0[1]	CRC[2:0][6]		

1. *SafeSPI status; reference Section 11.7.5.1.*
2. *RA[7:1] contains the word address of the register, which has been written to.*
3. *Reference Section 11.2.6.*
4. *The new contents of the register addressed by RA[7:1] high byte (RA.0 = 1).*
5. *The new contents of the register addressed by RA[7:1] low byte (RA.0 = 0).*
6. *Reference Section 11.7.4.1*

11.7.4 SafeSPI protocol 3-bit CRC error checking

A 3-bit CRC with the polynomial 5h ($x^3 + x^1 + x^0$) is used with a start value of 101b and a target value of 000b. The start value is added before the MSB of the SPI frame.

11.7.4.1 SafeSPI protocol example 3-bit CRC calculations

Table 93. SafeSPI protocol 3-bit CRC examples for register commands

Operation	Bits[31:30]	Bits[29:22]	Bit 21	Bits[20:19]	Bits[18:3]	Bits[2:0]	32-bit SDI data word
	sensor address	register address	R/W	--	register data	3-bit CRC	
Read DEVSTAT_SUM	0	03h and 02h	0	00	0000h	7	0080 0007h
Read ARC0_SNSDATA1	0	75h and 74h	0	00	0000h	3	1D00 0003h
Read ACC0_STL_P	0	B1h and B0h	0	00	0000h	3	2C00 0003h
Read ACC0_SNSDATA0	0	8Bh and 8Ah	0	00	0000h	3	2280 0003h
Write REGION_LOAD, data: B0h	0	15h and 14h	1	00	00B0h	6	0520 0586h
Write DEVLOCK_WR, data: 80h (ENDINIT)	0	11h and 10h	1	00	0080h	6	0420 0406h
Write DEVLOCK_WR, data: 00h (reset, step 1)	0	11h and 10h	1	00	0000h	5	0420 0005h
Write DEVLOCK_WR, data: 03h (reset, step 2)	0	11h and 10h	1	00	0003h	0	0420 0018h
Write DEVLOCK_WR, data: 01h (reset, step 3)	0	11h and 10h	1	00	0001h	6	0420 000Eh

11.7.5 SafeSPI protocol exception handling

11.7.5.1 SafeSPI protocol sensor status conditions

Each SPI response includes two status bits, S1 and S0, with the definitions shown in Table 94. SafeSPI protocol status bit definitions. Status for all responses is determined at the rising edge of SS_B from the previous message.

Table 94. SafeSPI protocol status bit definitions

S1	S0	Device status condition	ENDINIT	Priority
0	0	device in normal mode: valid sensor data	1	4
0	1	error condition	X	1
1	0	device in initialization, self-test active, valid sensor data	0	2
1	1	device in initialization, valid sensor data	0	3

11.7.5.2 *SafeSPI protocol SPI error*

The following external SPI conditions result in a SPI error:

- SCLK is HIGH when SS_B is asserted
- The number of SCLK rising edges detected while SS_B is asserted, is not equal to 32
- SCLK is HIGH when SS_B is deasserted
- A command message CRC error is detected (SDI)
- A register write command to any register other than the DEVLOCK_WR register is received while ENDINIT is set

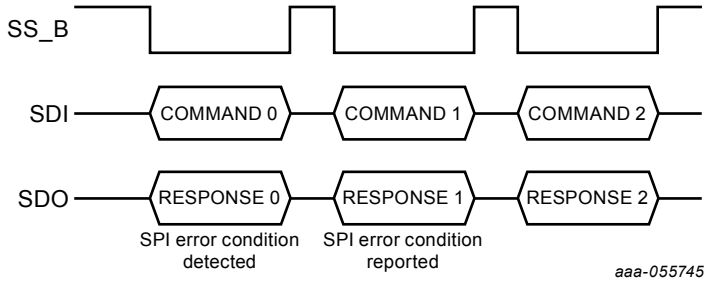
If a SPI error is detected, the device responds with the error response as shown below. The error is cleared on a transmission of the SPI error response.

Table 95. SPI error response

MSB																														LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D	sensor address		register address							0	S1	register data																S0	3-bit CRC CRC[2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

SPI errors detected in one transfer are reported in the subsequent response.

Figure 12. SafeSPI protocol SPI error response



12 Part marking

Figure 13. **Part marking**

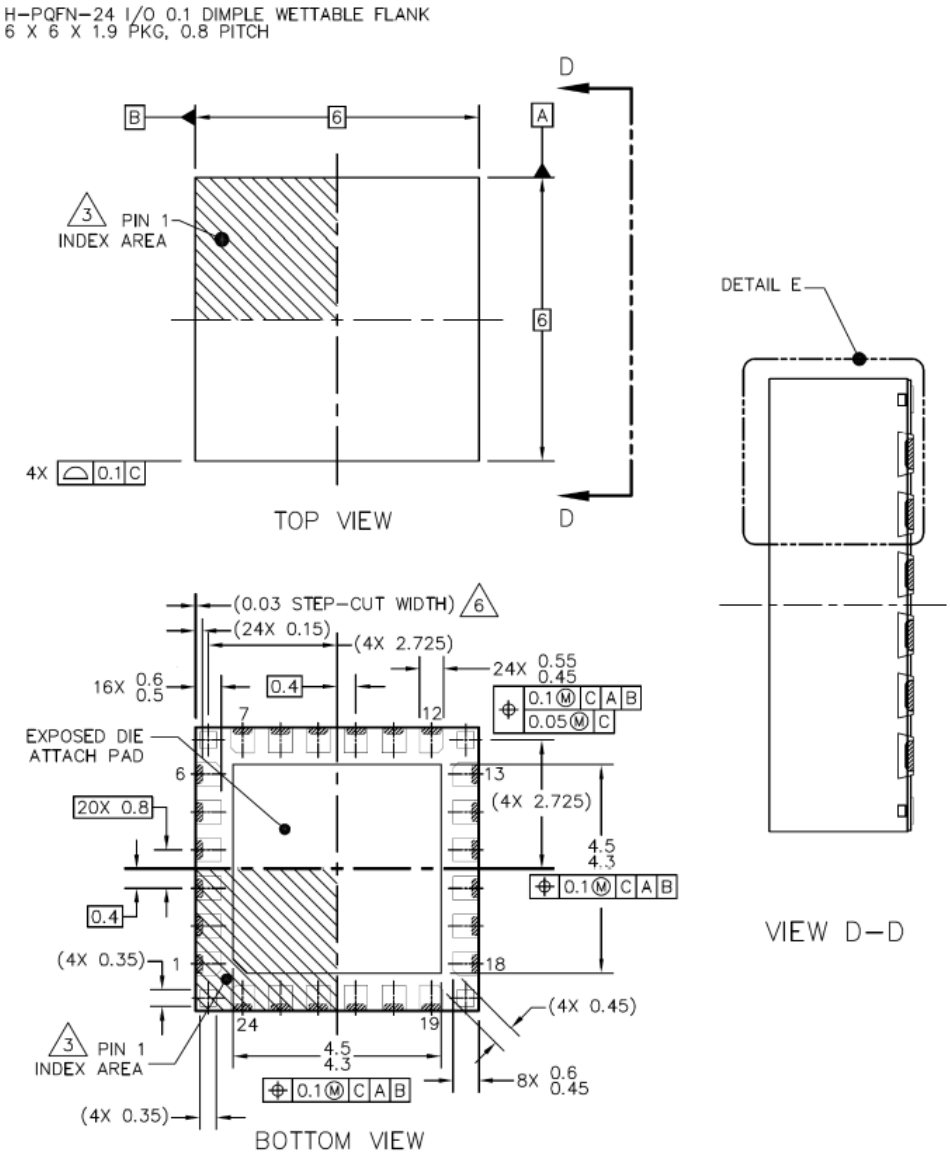


Date code legend
AA: Single or dual alpha characters representing the assembly site
WL: Dual alpha characters representing the wafer lot
Y: Single numerical character representing the year
WW: Dual numerical characters representing the work week
ZZ: Single or dual alpha character representing the assembly lot split

aaa-055090

13 Package outline

Figure 14. **HQFN24 6 mm × 6 mm × 1.9 mm package outline and mechanical data**



DM01230473_1

Figure 15. **Package outline detail for HQFN24**

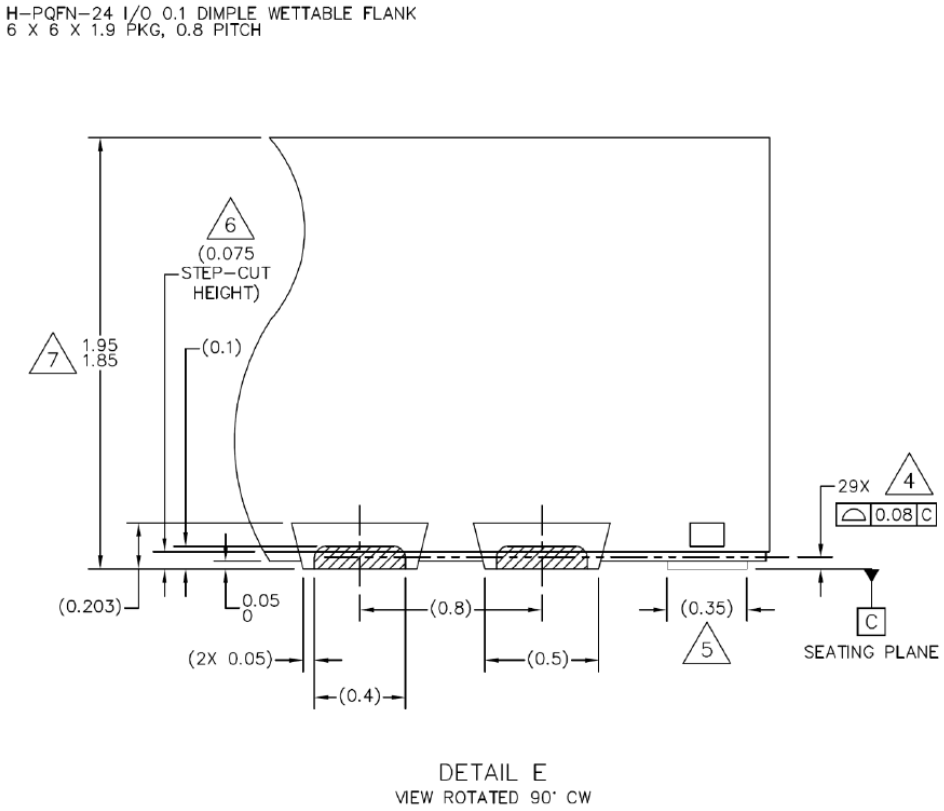


Figure 16. **Package outline notes for HQFN24**

H–PQFN–24 I/O 0.1 DIMPLE WETTABLE FLANK
6 X 6 X 1.9 PKG, 0.8 PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. ANCHORING PADS.
6. STEP–CUT IS APPLIED FOR BURR REMOVAL ONLY.
7. SPUTTER LAYER OF STAINLESS STEEL SUS316 IS INCLUDED IN THE TOP SIDE SURFACE.

Figure 17. **PCB design guidelines - solder mask opening pattern**

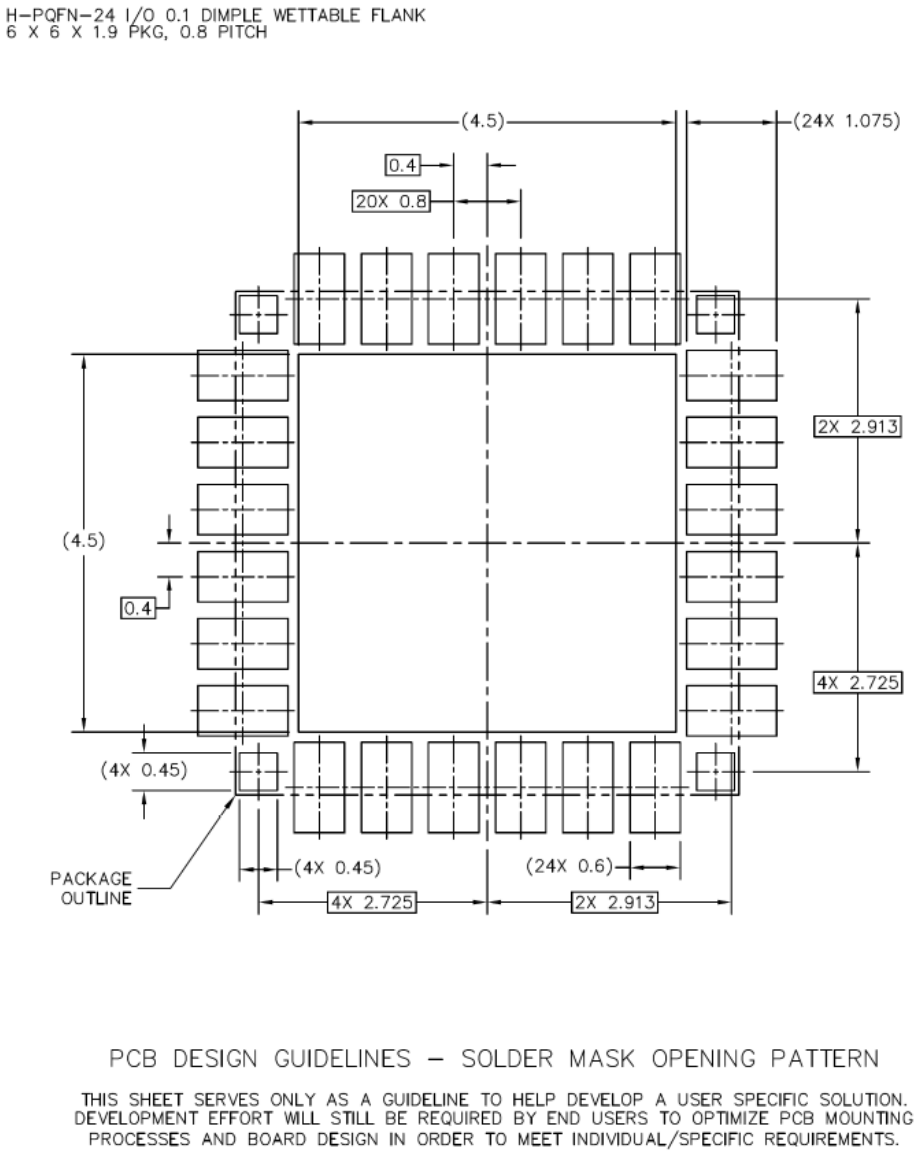


Figure 18. **PCB design guidelines - I/O pads and solderable area**

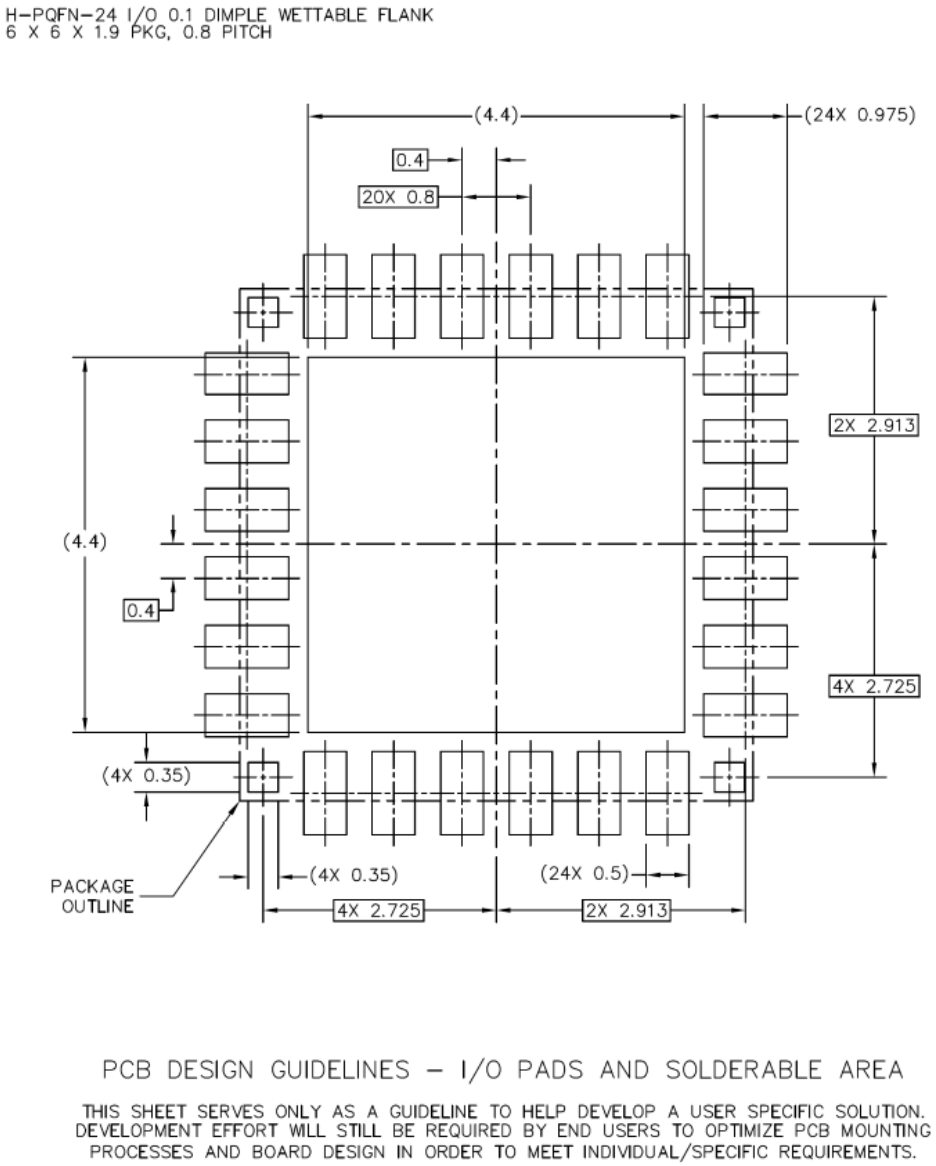
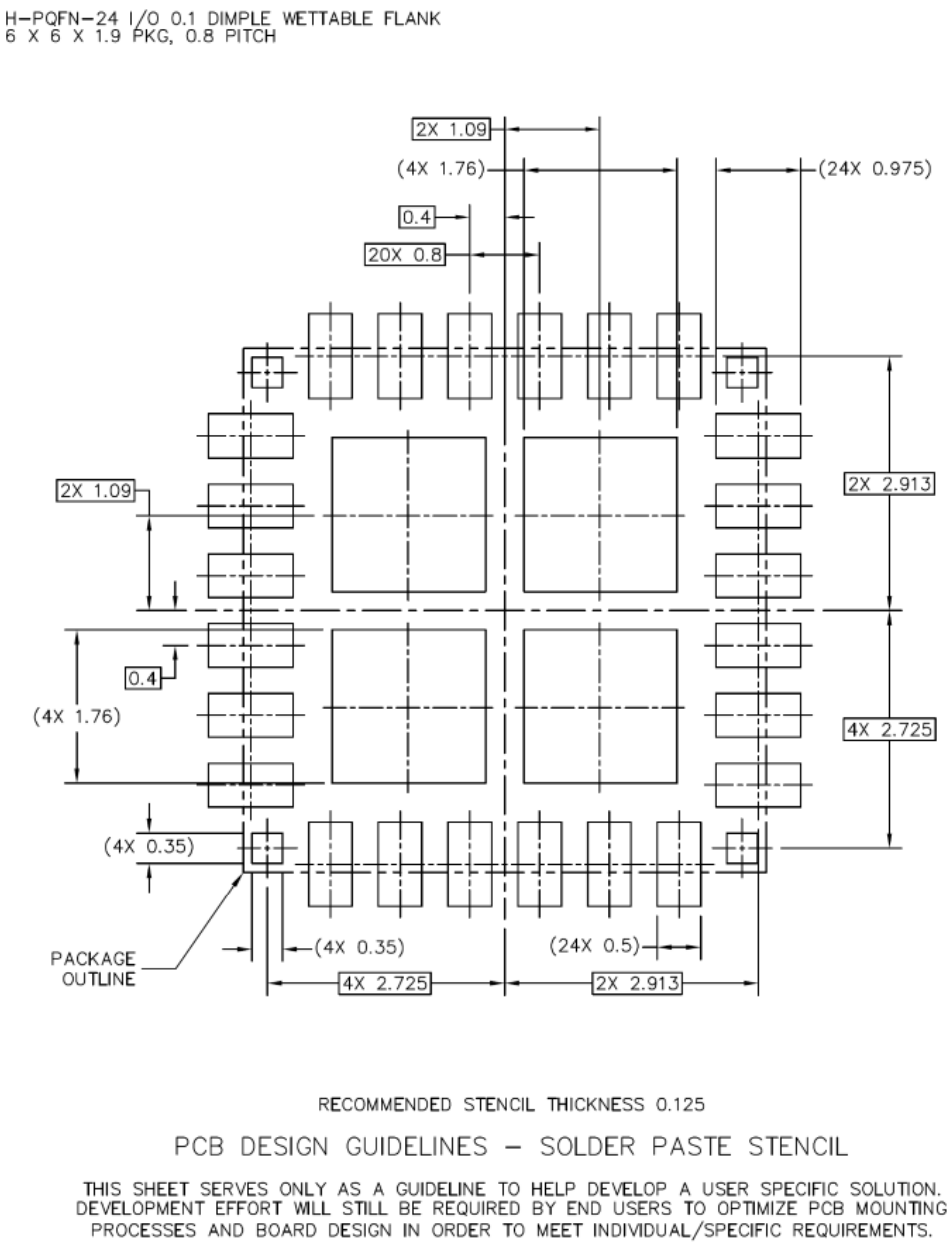


Figure 19. **PCB design guidelines - solder paste stencil**



14 Acronym definitions

Table 96. **Acronyms**

Acronym	Meaning	Definition
ACC	acceleration channel	
ADC	analog-to-digital converter	
AEC	Automotive Electronics Council	
AFE	analog front-end	the analog portion of the signal chain including the C2V and the sigma-delta modulator
ARC	angular rate channel	
ASIC	application-specific integrated circuit	
AST	analog self-test	a method to test the signal chain that includes moving the MEMS by electronic methods and measuring the device output
BW	bandwidth	
C2V	capacitance to voltage (converter)	
CDM	charged device model	a method for evaluating the susceptibility of a device to ESD
CPHA	clock phase	determines the clock polarity for the SPI CPHA = 0: data is captured on the first clock edge and changed on the second CPHA = 1: data is changed on the first clock edge and captured on the second
CPOL	clock polarity	determines the clock polarity for the SPI CPOL = 0: clock idles at 0 and each clock pulse is a 1 CPOL = 1: clock idles a 1 and each clock pulse is a 0
CRC	cyclic redundancy check	a method to detect errors in memory
DAU	drive actuation unit	
DS ΔΣ	delta sigma (modulator)	an ADC that generates a pulse stream in which the frequency of pulses is proportional to the input analog voltage
DSP	digital signal processor	the digital portion of the signal chain including compensation and filtering
DST	digital self-test	a method to test the digital portion of the acceleration signal chain by forcing a value or a sequence of values at the input of the DPS and measuring the device output
ECC	error correcting code	a method to detect and correct errors in memory
ESD	electrostatic discharge	
HBM	human body model	a method for evaluating the susceptibility of a device to ESD
HPF	high-pass filter	
IIR	infinite impulse response	
LPF	low-pass filter	
LSB	least significant bit	
MA	moving average	
MEMS	microelectromechanical system	
NC	no connect	
NVM	non-volatile memory	
OC	offset cancellation	
OTP	one time programmable (memory)	
PCM	pulse code modulation	a method to represent digitally a sampled analog signal which when filtered with a frequency lower than the sample rate can reproduce the analog signal

Acronym	Meaning	Definition
PLL	phase-locked loop	a method to generate a clock with a phase that tracks the input frequency and a frequency that is a multiple of the input frequency
POR	power-on reset	
QFN	quad flat no lead	
RL	rate limiter	
SafeSPI	serial peripheral interface for automotive safety	
SCLK	serial clock	The SCLK signal is output from the SPI controller to all the devices on the bus.
SD, ΣΔ	sigma-delta (modulator)	an ADC that generates a pulse stream in which the frequency of pulses is proportional to the input analog voltage
SDI	sensor data input	the SPI data output from the SPI controller to the sensor
SDO	sensor data output	the SPI data input from the sensor to the SPI controller
SS_B	sensor select bar	an active LOW signal output from the SPI controller to select the sensor
SPI	serial peripheral interface	a full duplex, synchronous serial interface
ST	self-test	

Revision history

Table 97. **Document revision history**

Date	Version	Changes
16-Jul-2026	1	Initial release
12-Oct-2026	2	Updated Features Updated Figure 2. Block diagram Updated Table 16. General device information and Table 22. Device status registers Updated Section 11.2.2.2: Acceleration error flags (ACC0_ERR, ACC1_ERR, ACC2_ERR) Updated Figure 8. Acceleration signal processing flow and Figure 9. Acceleration offset cancellation block diagram

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