# Ultra Efficient Wide Input Power Range Energy Manager with Hybrid Boost Architecture, Regulated Buck Output and 5 V Charger

## Features and Benefits

### Wide Input Power Range
- Hybrid boost architecture for wide input power range
- Source current range from 5 µA to 1 A.
- Automatic low / high power mode transition.
- Conversion efficiency up to 97 %.
- Harvest from 300 mV after cold start.

### Maximum Power Point Tracking
- Source regulation configurable to constant voltage mode or open-circuit ratio mode.
- Optimal harvesting from various types of harvesters (PV cells, RF, vibration, pulsed sources...).

### Cold start from 275 mV / 1.5 µW input
- Startup at ultra-low power from the source input.

### Configurable overdischarge & overcharge protection
- Supports various types of rechargeable storage elements (LiC, Li-ion, LiPo, Li-ceramic pouch...).

### Regulated output for application circuit
- Buck regulator conversion efficiency up to 96 %.
- Selectable output voltage between 0.6 V and 3.3 V.
- Output current up to 100 mA.

### Thermal monitoring
- Storage element protection against over-temperature and under-temperature during charging and discharging, independently.

### Average Power Monitoring
- Provides data to determine how much energy has been transferred to the storage from each boost converter and from the 5 V charger, as well as the energy drained from the storage to supply the application circuit.

### System configuration by GPIO or I²C communication
- All settings dynamically configurable through GPIO or I²C (Fast Mode Plus).
- System data available through I²C.

### Shipping mode
- Storage element charge and discharge disabling during shipment.

### External 5 V charging capability
- Extra charging input for 5 V power supplies.
- Configurable CC and CV modes (max. 135 mA).
- Provides a fast charging alternative when no source is available for a long time.

## Applications

| | |
|---|---|
| Headphones / Headsets | Toll badges |
| Laptops / E-readers | Robotics |
| CCTV cameras | Fleet management |

## Description

The AEM15820 is a fully integrated and compact power management circuit that extracts DC power from a harvesting source to store energy in a rechargeable storage element and supply an application circuit. A 5 V input can also be used to charge the storage element (e.g., if it gets depleted). This compact and ultra-efficient PMIC allows for extending battery lifetime and eliminating the primary energy storage in a large range of applications.

The AEM15820 low and high power boost converters, along with its Maximum Power Point Tracking (MPPT) module with open-circuit ratio mode or constant voltage mode, allows for harvesting the maximum available power in a wide input range, for optimal performance under varying conditions.

With its unique cold-start circuit, it can start operating with an input voltage as low as 275 mV (min. 1.5 µW power).

The configurable protection thresholds prevent overcharging and overdischarging the storage element. No external components are required to set those thresholds. The thermal monitoring prevents charging and discharging the storage element outside a configurable temperature range.

The Average Power Monitoring (APM) allows the application circuit to get an estimate of the energy harvested from the source to the battery and from the battery to the application circuit. A shipping mode is available to avoid charging and discharging the storage element during shipping or storage.

A buck regulator with selectable output voltage allows an application circuit to be supplied with high efficiency.

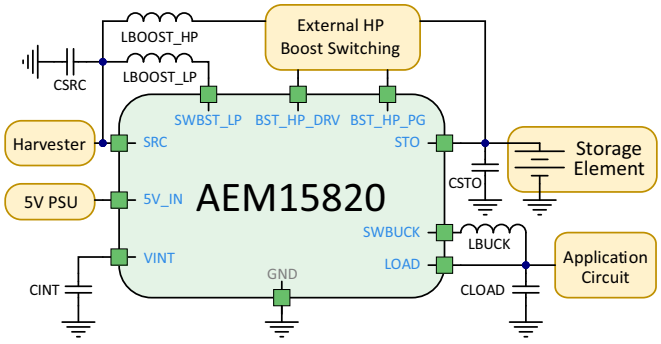
I²C communication allows users to control every setting of the AEM15820 from the application circuit MCU.

## Device Information

| Part Number | Package | Body size |
|---|---|---|
| 10AEM15820J0000 | QFN 40-pin | 5 x 5 mm |

## Evaluation Board

| Part number |
|---|
| 2AAEM15820J001 |



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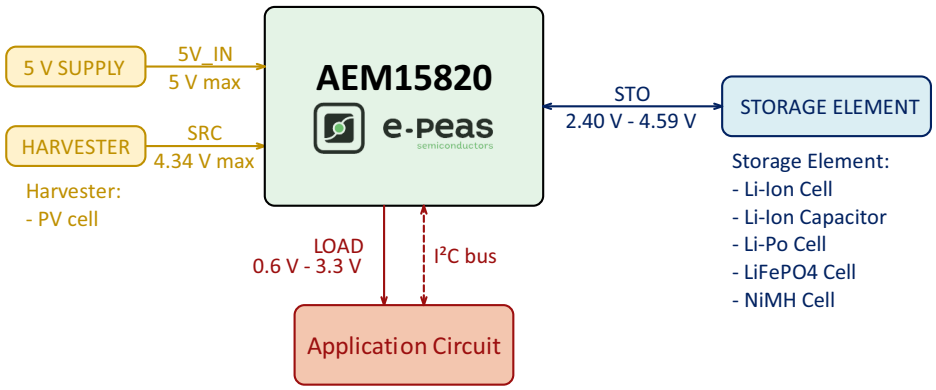



*Figure 1: Simplified schematic view*

# 1. Introduction

The AEM15820 is a full-featured energy efficient power management circuit able to harvest energy from a harvester (connected to SRC) to charge a storage element (connected to STO) and to supply an application circuit (connected to LOAD). The storage element can also be charged from a 5 V power supply. This is done with a minimal bill of material.

The heart of the AEM15820 is composed of two boost converters (one low-power boost with internal switching and one high-power boost with external switching) for energy harvesting and a buck converter for supplying the load. All three have high power conversion efficiency.

The AEM15820 can be configured either by configuration pins or by a set of registers accessed through an I²C bus. Furthermore, some advanced configurations are accessible only through the I²C registers.

A 5 V power input 5V_IN allows for charging the storage element. This is done using a CC/CV (constant current / constant voltage) method. The CC mode maximum current can be configured between 13.5 mA and 135 mA with an external resistor. The CV mode can be enabled by I²C with a configurable charge stop voltage ($V_{5V,STOP}$).

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 1.5 µW is available on SRC, the AEM15820 coldstarts. After the cold start, the AEM15820 extracts the power available from the source if the working input voltage is above $V_{SRC,REG}$ (constant voltage mode) or $V_{MPP}$ (MPPT mode). Cold start can also be done from the 5 V power supply input 5V_IN.

The storage element protection thresholds are configured through three configuration pins (STO_CFG[2:0]), from which the user can select a specific operating mode out of 8 modes that cover most application requirements without any dedicated external component. If none of those 8 modes fits the user's storage element, the protection thresholds can also be configured individually through I²C registers to allow the user to define a mode with custom specifications.

The ST_LOAD status pin provides information about the storage element readiness to supply an application through the AEM15820 LOAD output.

The SRC input of the AEM15820 can work in Maximum Power Point tracking (MPPT) mode or in constant voltage mode. The mode is configured with a dedicated pin SRC_MODE or through the I²C registers.

When in MPPT mode, the Maximum Power Point tracking (MPPT) ratio can be set through three configuration pins (SRC_CFG[2:0]) to ensure an optimum biasing of the harvester and maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins (SRC_CFG[4:3]) that sets the periodicity and the duration of the MPP evaluations. The MPPT ratio and the MPPT timings can also be configured through the I²C registers.

When in constant voltage mode, the source regulation voltage $V_{SRC,REG}$ can be configured thanks to five configuration pins (SRC_CFG[4:0]). The constant voltage can also be configured through I²C registers for higher resolution and extended range of values.

If the storage element is sufficiently charged, the buck converter provides a regulated output voltage on the LOAD pin, allowing an application circuit to be supplied. The regulated voltage can be set through the LOAD_CFG[2:0] pins or through the I²C registers.

A shipping mode feature can be enabled through the SHIP_MODE pin, disabling the boost converters, the buck converter as well as the 5 V input, thus, preventing any charge or discharge of the storage element.

## 2. Pin Configuration and Functions

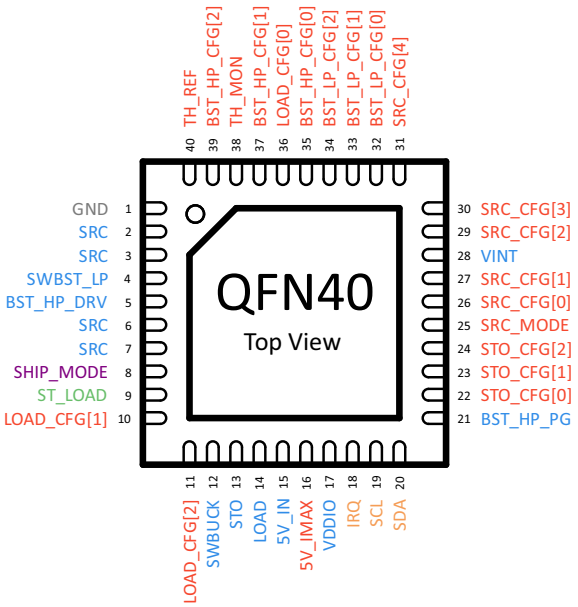



*Figure 2: Pinout diagram*

| NAME | PIN NUMBER | FUNCTION |
|---|---|---|
| **Power Pins** | | |
| SRC | 2, 3, 6, 7 | Connection to the energy source harvester.<br>Please make sure to connect all four pins. |
| SWBST_LP | 4 | Switching node of the low-power boost converter. |
| BST_HP_DRV | 5 | Connection for driving the low-side transistor of the high-power boost converter. |
| BST_HP_PG | 21 | Connection for the power gating of the high-power boost converter. |
| STO | 13 | Connection to the energy storage element (rechargeable storage element). |
| SWBUCK | 12 | Switching node of the buck converter.<br>If not used:<br>- Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VLOAD register field.<br>- Leave the SWBUCK pin floating. |
| LOAD | 14 | Output voltage of the buck converter to supply an application circuit.<br>If not used:<br>- Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VLOAD register field.<br>- Leave the LOAD pin floating. |
| 5V_IN | 15 | Input of the 5 V DC power supply.<br>Leave floating if not used. |
| VDDIO | 17 | Voltage reference for the I²C interface, as well as for the IRQ pin.<br>- If used, connect to a DC power supply.<br>- If not used, connect to GND. |
| VINT | 28 | Connection for $C_{INT}$ buffering capacitor.<br>AEM15820 internal power supply (do not connect any external circuit on VINT). |

Table 1: Pins description (part 1)

| NAME | | PIN NUMBER | LOGIC LEVEL | | FUNCTION |
|---|---|---|---|---|---|
| | | | LOW | HIGH | |
| **Configuration Pins** | | | | | |
| SRC_MODE | | 25 | GND | VINT | Used to configure SRC voltage regulation mode (see Section 5.2.1):<br>- LOW: constant voltage mode.<br>- HIGH: MPPT ratio mode.<br>Read as HIGH if left floating. |
| SRC_CFG[4:0] | SRC_CFG[4] | 31 | GND | VINT | Used to configure SRC regulation voltage (see Section 6.2).<br>SRC_MODE = LOW (constant voltage mode):<br>- SRC_CFG[4:0] are used to set SRC constant regulation voltage.<br>SRC_MODE = HIGH (MPPT ratio mode):<br>- SRC_CFG[2:0] are used to set SRC MPPT ratio.<br>- SRC_CFG[4:3] are used to set SRC MPPT timings.<br>Read as HIGH if left floating. |
| | SRC_CFG[3] | 30 | GND | VINT | |
| | SRC_CFG[2] | 29 | GND | VINT | |
| | SRC_CFG[1] | 27 | GND | VINT | |
| | SRC_CFG[0] | 26 | GND | VINT | |
| BST_LP_CFG[2:0] | BST_LP_CFG[2] | 34 | GND | VINT | Used to configure the low-power boost converter timings, as described in Section 6.5.<br>Read as HIGH if left floating. |
| | BST_LP_CFG[1] | 33 | GND | VINT | |
| | BST_LP_CFG[0] | 32 | GND | VINT | |
| BST_HP_CFG[2:0] | BST_HP_CFG[2] | 39 | GND | VINT | Used to configure the high-power boost converter timings, as described in Section 6.5.<br>Read as HIGH if left floating. |
| | BST_HP_CFG[1] | 37 | GND | VINT | |
| | BST_HP_CFG[0] | 35 | GND | VINT | |
| STO_CFG[2:0] | STO_CFG[2] | 24 | GND | VINT | Used to configure the storage element protection thresholds (see Section 6.4).<br>Read as HIGH if left floating. |
| | STO_CFG[1] | 23 | GND | VINT | |
| | STO_CFG[0] | 22 | GND | VINT | |
| LOAD_CFG[2:0] | LOAD_CFG[2] | 11 | GND | VINT | Used to configure the LOAD output regulation voltage (see Section 6.6).<br>Read as HIGH if left floating. |
| | LOAD_CFG[1] | 10 | GND | VINT | |
| | LOAD_CFG[0] | 36 | GND | VINT | |
| 5V_IMAX | | 16 | Analog Pin | | Connection to an external resistor to set the charging current from the 5V_IN supply to STO (see Section 6.8).<br>Leave floating if the 5V_IN power supply is not used. |
| TH_REF | | 40 | Analog Pin | | Reference voltage for thermal monitoring (see Section 5.4).<br>Leave floating if not used. |
| TH_MON | | 38 | Analog Pin | | Connection for the mid-point of the thermistor voltage divider (see Section 5.4).<br>Connect to VINT if not used. |

Table 2: Pins description (part 2)

| NAME | PIN NUMBER | LOGIC LEVEL | | FUNCTION |
|---|---|---|---|---|
| | | LOW | HIGH | |
| **Control Pin** | | | | |
| SHIP_MODE | 8 | GND | STO | Used to configure the shipping mode.<br>When HIGH:<br>- Minimum consumption from the storage element.<br>- Storage element charge is disabled (Boost converters are disabled).<br>- Buck (LOAD) is disabled.<br>- VINT is only supplied from SRC if energy is available.<br>Read as LOW if left floating. |
| **I²C Pins** | | | | |
| SCL | 19 | GND | VDDIO | Unidirectional serial clock for I²C communication.<br>Connect a pull-up resistor to VDDIO if used (see Section 6.1.2).<br>Connect to GND if not used. |
| SDA | 20 | GND | VDDIO | Bidirectional data line for I²C communication.<br>Connect a pull-up resistor to VDDIO if used (see Section 6.1.2).<br>Connect to GND if not used. |
| IRQ | 18 | GND | VDDIO | Logic output signal to indicate AEM15820 events to an external circuit GPIO.<br>Leave floating if not used. |
| **Status Pin** | | | | |
| ST_LOAD | 9 | GND | LOAD | Logic output, used when $V_{LOAD}$ is configured ≥ 1.2 V.<br>- ST_LOAD is set HIGH if the buck converter is enabled, the temperature is within the range, and:<br>  - $V_{STO}$ rises above $V_{CHRDY,BUCK}$ when the 5 V charger is not connected, or<br>  - $V_{STO}$ rises above $V_{OVDIS,BUCK}$ when the 5 V charger is connected.<br>- ST_LOAD is set LOW if:<br>  - The buck converter is disabled, or<br>  - The temperature is outside the range, or<br>  - $V_{STO}$ remains below $V_{OVDIS,BUCK}$ for $T_{CRIT,ST}$.<br>Leave floating if not used. |
| **Other pins** | | | | |
| GND | Exposed Pad, 1 | | | Ground connection, each terminal must be strongly tied to the PCB ground plane. |

Table 3: Pins description (part 3)

# 3. Specifications

## 3.1. Absolute Maximum Ratings

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| Operating junction temperature $T_J$ | | -40 | 85 | °C |
| Storage temperature $T_{stg}$ | | -65 | 150 | °C |
| Input voltage | SRC, SWBST_LP, STO, SWBUCK, 5V_IN, VDDIO, LOAD, BST_HP_PG, BST_HP_DRV, SHIP_MODE, 5V_IMAX, LOAD_CFG[2], LOAD_CFG[1], SCL, SDA, IRQ, ST_LOAD. | -0.3 | 5.50 | V |
| | VINT, SRC_MODE, SRC_CFG[4:0], BST_LP_CFG[2:0], BST_HP_CFG[2:0], STO_CFG[2:0], LOAD_CFG[0], TH_REF, TH_MON. | -0.3 | 2.75 | V |

Table 4: Absolute maximum ratings

**CAUTION: Please always make sure that the source voltage ($V_{SRC}$) is lower than the storage element voltage ($V_{STO}$).**

## 3.2. ESD Ratings

| Parameter | | Value | Unit |
|---|---|---|---|
| Electrostatic discharge $V_{ESD}$ | Human-Body Model (HBM)[1] | ± 2000 | V |
| | Charged-Device Model (CDM)[2] | ± 1000 | V |

Table 5: ESD ratings

*1. ESD Human-Body Model (HBM) value tested according to JEDEC standard JS-001-2024.*
*2. ESD Charged-Device Model (CDM) value tested according to JEDEC standard JS-002-2022.*

| ESD CAUTION | |
|---|---|
|  | ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE<br>These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality |

## 3.3. Thermal Resistance

| Package | θJA | θJC | Unit |
|---|---|---|---|
| QFN-40 | 50 | 5 | °C/W |

Table 6: Thermal data

## 3.4. Electrical Characteristics at 25 °C

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power conversion** | | | | | | |
| $P_{SRC,CS}$ | Minimum source power required for cold start. | | | 1.5 | | µW |
| $V_{SRC,CS}$ | Minimum source voltage required for cold start. | | | 0.275 | | V |
| $V_{MPP}$ | Target regulation voltage on SRC when extracting power. | SRC_MODE = HIGH. | max (0.315, $V_{OC}$/2) | | $V_{STO}$ - 0.25 | V |
| $V_{SRC,REG}$ | Target regulation voltage of the source, depending on GPIO or I²C configuration. | SRC_MODE = LOW, configured by SRC_CFG[4:0]. | 0.30 | | min (3.18, $V_{STO}$ - 0.25)[1] | V |
| | | SRC_MODE = LOW, configured by I²C register. | 0.300 | | min (4.318, $V_{STO}$ - 0.25)[1] | V |
| $V_{OC}$ | Open-circuit voltage of the source. | | 0.00[2] | | min ($V_{STO}$, $V_{SRC}$ x 2)[3] | V |
| $V_{5V\_IN}$ | Voltage on the 5V_IN pin to allow for charging the storage element. | | max (3.60, $V_{STO}$ + 0.20)[4] | | 5.50 | V |
| $I_{5V,CC}$ | Maximum charging current of the 5 V charger (5V_IN input). Configured by the $R_{5V\_IMAX}$ resistor. | In constant current (CC) mode when $V_{STO} > V_{OVDIS}$. | 13.50 | | 135 | mA |
| $I_{5V,OVDIS,CC}$ | Charging current of the 5 V charger (5V_IN input) in overdischarge. | In constant current (CC) mode when $V_{STO} < V_{OVDIS}$. | | 6.75 | | mA |
| $V_{VDDIO}$ | Voltage on VDDIO. | | 1.50 | | 5.00 | V |

Table 7: Electrical characteristics (part 1)

*1. The maximum value of $V_{SRC,REG}$ is determined by the highest configurable $V_{SRC,REG}$, but it must never be higher than $V_{STO}$ - 250 mV to ensure proper operation.*
*2. When the open-circuit voltage is below the source regulation voltage (MPPT or constant voltage), the AEM15820 does not extract power from the source. Voltages down to GND voltage does not damage the AEM15820 though.*
*3. The maximum value of $V_{OC}$ is $V_{STO}$ but it must never be higher than $V_{SRC}$ x 2 to ensure proper operation (with $V_{SRC}$ being either $V_{SRC,REG}$ or $V_{MPP}$ depending on the source regulation mode).*
*4. The 5 V charger is considered connected when the voltage on 5V_IN is greater than or equal to 3.60 V and at least 200 mV higher than the voltage on STO. It can be actively charging or not.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Timing** | | | | | | |
| $T_{MPPT,WAIT}$ | Wait time before $V_{OC}$ measurement begins during MPP evaluation (see Section 5.2.2). | Configured by SRC_CFG[4:3]. | 1.8 | | 233 | ms |
| | | Configured by I²C. | | | 465 | |
| $T_{MPPT,MEASURE}$ | Duration of $V_{OC}$ measurement during MPP evaluation. | | | 1.36 | | ms |
| $T_{MPPT,PERIOD}$ | Time between two MPP evaluations (see Section 5.2.2). | Configured by SRC_CFG[4:3]. | 0.116 | | 14.895 | s |
| | | Configured by I²C. | | | | |
| $T_{CRIT,ST}$ | Delay for the AEM15820 to notify the application about an overdischarged storage element, a temperature out of discharge temperature range, and to schedule LOAD output disable (see Section 5.3). | | | 1.86 | | s |
| $T_{CRIT}$ | Delay for the AEM15820 to go in OVDIS STATE and to disable the LOAD output (see Section 5.9). | | | 2.56 | | s |
| $T_{GPIO,MON}$ | GPIO monitoring rate. | | | 1.86 | | s |
| $T_{STO,MON}$ | Storage element voltage monitoring rate. | When the buck converter is disabled and the 5 V charger is not connected[1]. | | 116 | | ms |
| | | When the buck converter is enabled or the 5 V charger is connected[1]. | | 15 | | ms |
| $T_{TEMP,MON}$ | Temperature monitoring rate. | | | 7.45 | | s |
| $T_{5V,RISE}$ | Minimum rise time from 0 V to 5 V on the 5V_IN pin (see Section 6.8). | | | 50 | | µs |

Table 8: Electrical characteristics (part 2)

*1. The 5 V charger is considered connected when the voltage on 5V_IN is greater than or equal to 3.60 V and at least 200 mV higher than the voltage on STO. It can be actively charging or not.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Storage element** | | | | | | |
| $V_{STO}$ | Voltage on the storage element. | | 2.40[1] | | 4.59[2] | V |
| $V_{OVDIS}$ | Voltage below which the storage element is considered to be fully depleted, and must not be discharged any further (see Section 6.4). | Configured by STO_CFG[2:0]. | 2.51 | | 3.51 | V |
| | | Configured by I²C.[3] | 2.400 | | 3.581 | V |
| $V_{CHRDY}$ | In START STATE, voltage required on the storage element to switch to SUPPLY STATE (see Section 6.4). | Configured by STO_CFG[2:0]. | 2.61 | | 3.60 | V |
| | | Configured by I²C.[3] | 2.456 | | 4.312 | V |
| $V_{OVCH}$ | Maximum voltage accepted on the storage element before disabling its charging (see Section 6.4). | Configured by STO_CFG[2:0]. | 3.49 | | 4.35 | V |
| | | Configured by I²C.[3] | 2.700 | | 4.594 | V |
| $V_{OVDIS,BUCK}$ | Minimum voltage accepted on the storage element before:<br>- Starting to supply the LOAD if the 5 V charger is charging,<br>- Stopping to supply the LOAD when the storage element voltage is too low.<br>(See Section 6.4). | | | max ($V_{OVDIS}$, $V_{LOAD}$) | | V |
| $V_{CHRDY,BUCK}$ | Minimum voltage accepted on the storage element before starting to supply the LOAD if the 5 V charger is not charging (see Section 6.4). | Configured by STO_CFG[2:0] depending on $V_{LOAD}$. | 2.61 | | 3.60 | V |
| | | Configured by I²C.[4] | 2.456 | | 4.312 | V |
| $V_{5V,STOP}$ | Voltage on STO at which the 5 V charger (5V_IN input) stops charging the storage element in constant voltage (CV) mode (see Section 5.7). | | 2.65 | | 4.70 | V |
| **Internal supply & quiescent current** | | | | | | |
| $V_{INT}$ | Internal voltage supply. | | | 2.25 | | V |
| $V_{INT,RESET}$ | Minimum voltage on VINT before switching to RESET STATE (from any other state). | | | 2.00 | | V |
| $V_{INT,CS}$ | Minimum voltage on VINT to allow the AEM15820 to switch from RESET STATE to SENSE STO STATE. | | | 2.30 | | V |
| $I_{Q,SUPPLY}$ | AEM15820 internal quiescent current on STO in SUPPLY STATE.[5] | Buck enabled (LOAD). | | 645 | | nA |
| | | Buck disabled (LOAD). | | 460 | | nA |
| $I_{Q,SLEEP}$ | AEM15820 internal quiescent current on STO in SLEEP STATE. | Buck enabled (LOAD). | | 435 | 1000 | nA |
| | | Buck disabled (LOAD). | | 275 | 1000 | nA |
| $I_{Q,SHIP}$ | AEM15820 internal quiescent current on STO in shipping mode (SHIP_MODE set HIGH). | | | 15 | | nA |
| $I_{Q,RESET}$ | AEM15820 internal quiescent current on STO in RESET STATE. | | | | | |

Table 9: Electrical characteristics (part 3)

*1. As set by the battery overdischarge threshold configuration.*
*2. As set by the battery overcharge threshold configuration.*
*3. Ensure that $V_{OVDIS} < V_{CHRDY} < V_{OVCH}$ with sufficient margin to prevent unintended state changes due to small voltage variation on the storage element.*
*4. If $V_{CHRDY,BUCK}$ is configured by I²C below $V_{OVDIS,BUCK}$, it will be automatically set equal to $V_{OVDIS,BUCK}$. Nevertheless, a minimum margin of 100 mV must always be maintained between $V_{OVDIS,BUCK}$ and $V_{CHRDY,BUCK}$ to prevent toggling of the buck converter enable state.*
*5. Both boost converters are enabled but not extracting current from SRC. The LOAD pin is left floating.*

## 3.5. Recommended Operating Conditions

| Symbol | Parameter | | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **External components** | | | | | | |
| $L_{BOOST\_LP}$ | Low-power boost converter inductor (mandatory). | | 3.3[2] | 33[3] | | µH |
| $L_{BOOST\_HP}$ | High-power boost converter inductor (mandatory[4]). | | | 3.3 | | µH |
| $C_{SRC}$ | SRC terminals decoupling capacitors (mandatory). | | See Section 3.5.3 | | | |
| $R_{PG\_PU}$ | Resistor pulling the $Q_{P\_PG}$ gate HIGH when BST_HP_PG pin is LOW, turning the high-power boost converter off (mandatory[4]). | | | 330 | | kΩ |
| $R_{DRV\_PD}$ | Resistor pulling BST_HP_DRV pin low (mandatory[4]). | | | 330 | | kΩ |
| $L_{BUCK}$ | Buck converter inductor (optional[5]). | | 1.7[2] | 10[3] | | µH |
| $C_{LOAD}$ | Buck converter decoupling capacitor (optional[5]). | | 10 | 22 | | µF |
| $C_{INT}$ | VINT terminal decoupling capacitor (mandatory). | | 5 | 10 | | µF |
| $C_{STO}$ | STO terminal decoupling capacitor (mandatory). | | 22[6] | 47 | | µF |
| $C_{BST,HP}$ | High-power boost converter decoupling capacitor (mandatory[4]). | | | 47 | | µF |
| $C_{5V}$ | 5V_IN terminal decoupling capacitor (optional[7]). | | 22 | 47 | | µF |
| $R_{5V\_IMAX}$ | Resistor connected to the 5V_IMAX pin for configuring the 5 V charger current when in constant current (CC) mode (optional[7]). | | 0.37 | | 3.7 | kΩ |
| $R_{SDA}$<br>$R_{SCL}$ | I²C interface pull-up resistors (optional[8]). | | | 1 | | kΩ |
| $R_{TH}$ | NTC thermistor used for thermal monitoring operation (optional[9]). | R0 | | 10[10] | 250 | kΩ |
| | | Beta | | 3380[10] | | K |
| $R_{DIV}$ | Resistor used to create a resistive divider with $R_{TH}$ for thermal monitoring operation (optional[9]). | | 4 | 22[10] | 40 | kΩ |

Table 10: Recommended external components

*1. All minimum and maximum values are effective components values, taking into account tolerances, derating, temperatures, voltages and any operating conditions (special care must be taken with capacitor derating).*
*2. Those minimum values are only applicable with minimum timings (see Sections 9.6 and 9.7).*
*3. $L_{BOOST\_LP}$ and $L_{BUCK}$ typical values recommended for best trade-off between boost/buck efficiency and current capability.*
*4. Required component if the high-power boost converter is used in addition to the low-power boost converter.*
*5. Mount only if buck converter is used.*
*6. Minimum effective value for $C_{STO}$ when using $L_{BOOST\_HP}$ = 3.3 µH and $T_{MULT}$ = x6.*
*7. Mount only if the 5 V charger is used.*
*8. Mount only if the I²C interface is used. For more information on how to select the value of these resistors, refer to "Pull-up resistor sizing" section in NXP's UM10204 "I²C-bus specification and user manual".*
*9. Mount only if the temperature monitoring feature is used.*
*10. Those values allow for having the default temperature thresholds at startup shown in Table 16.*

### 3.5.1. External Inductors Information

The AEM15820 operates with three external inductors. All inductors must support a minimum switching frequency of 10 MHz. Using inductors with low equivalent series resistance (ESR) improves the power-conversion efficiency of both the boost and buck converters.

**$L_{BOOST\_LP}$**

With the recommended operating conditions (33 µH inductor, $T_{MULT}$ = x3), the boost inductor $L_{BOOST\_LP}$ must support a minimum peak current of 135 mA.

**$L_{BOOST\_HP}$**

With the recommended operating conditions (3.3 µH inductor, $T_{MULT}$ = x6), the boost inductor $L_{BOOST\_HP}$ must support a minimum peak current of 3 A.

**$L_{BUCK}$**

With the recommended operating conditions (10 µH inductor, $T_{MULT}$ = x2), the buck inductors $L_{BUCK}$ must support a minimum peak current of 135 mA.

### 3.5.2. External Capacitors Information

The AEM15820 operates with external miniature capacitors to ensure stable operation of the boost converters input, buck converter output, storage element output, and internal supply. Each capacitor serves as a local energy buffer that limits voltage fluctuations caused by switching activity or dynamic load transition.

To maintain optimal performances and minimized quiescent current, all capacitors must exhibit a low leakage current and follow the recommended nominal values listed in Table 10, with a tolerance of ± 20 %.

### 3.5.3. Source Capacitance Value

The minimum required source capacitance ($C_{SRC}$) strongly depends on the selected $L_{BOOST\_HP}$, the high-power boost $T_{MULT}$ configuration, and the source regulation voltage. When using the recommended operating conditions ($L_{BOOST\_HP}$ = 3.3 µH, $T_{MULT}$ = x6), the minimum effective $C_{SRC}$ value can be determined from Figure 3. For any other configuration, please contact our support team for guidance.

If using the MPPT source regulation mode, make sure to consider as well the characteristics of the energy harvester and the available source power when selecting $C_{SRC}$ value in order to ensure an accurate source voltage regulation (see Section 6.3).

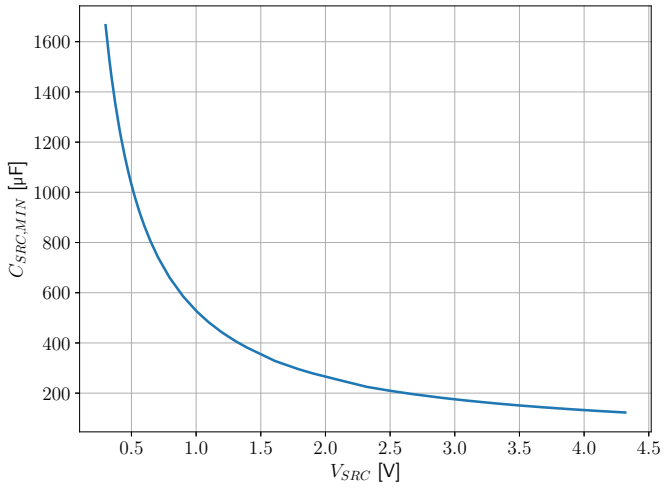



*Figure 3: $C_{SRC}$ minimum effective value (with $L_{BOOST\_HP}$ = 3.3 µH, $T_{MULT}$ = x6)*

### 3.5.4. External High-Power Boost Components Information

To ensure reliable operation of the high-power boost converter, the selected external components must meet the following requirements. The most critical components are:

**$L_{BOOST\_HP}$**

See detailed specifications and selection guidelines in Section 3.5.1.

**$Q_{DRV}$**

With the recommended operating conditions ($L_{BOOST\_HP}$ = 3.3 µH inductor, $T_{MULT}$ = x6), use a MOSFET with the lowest possible Rds(on), a gate charge below 20 nC, and a Vgs(th) compatible with a maximum gate drive of 2 V.

**$D_{BOOST\_HP}$**

Select a diode with the lowest possible forward voltage and a minimum peak current rating matching the one of $L_{BOOST\_HP}$ (see Section 3.5.1)

## 3.6. Typical Characteristics

### 3.6.1. Boost Converters Conversion Efficiency

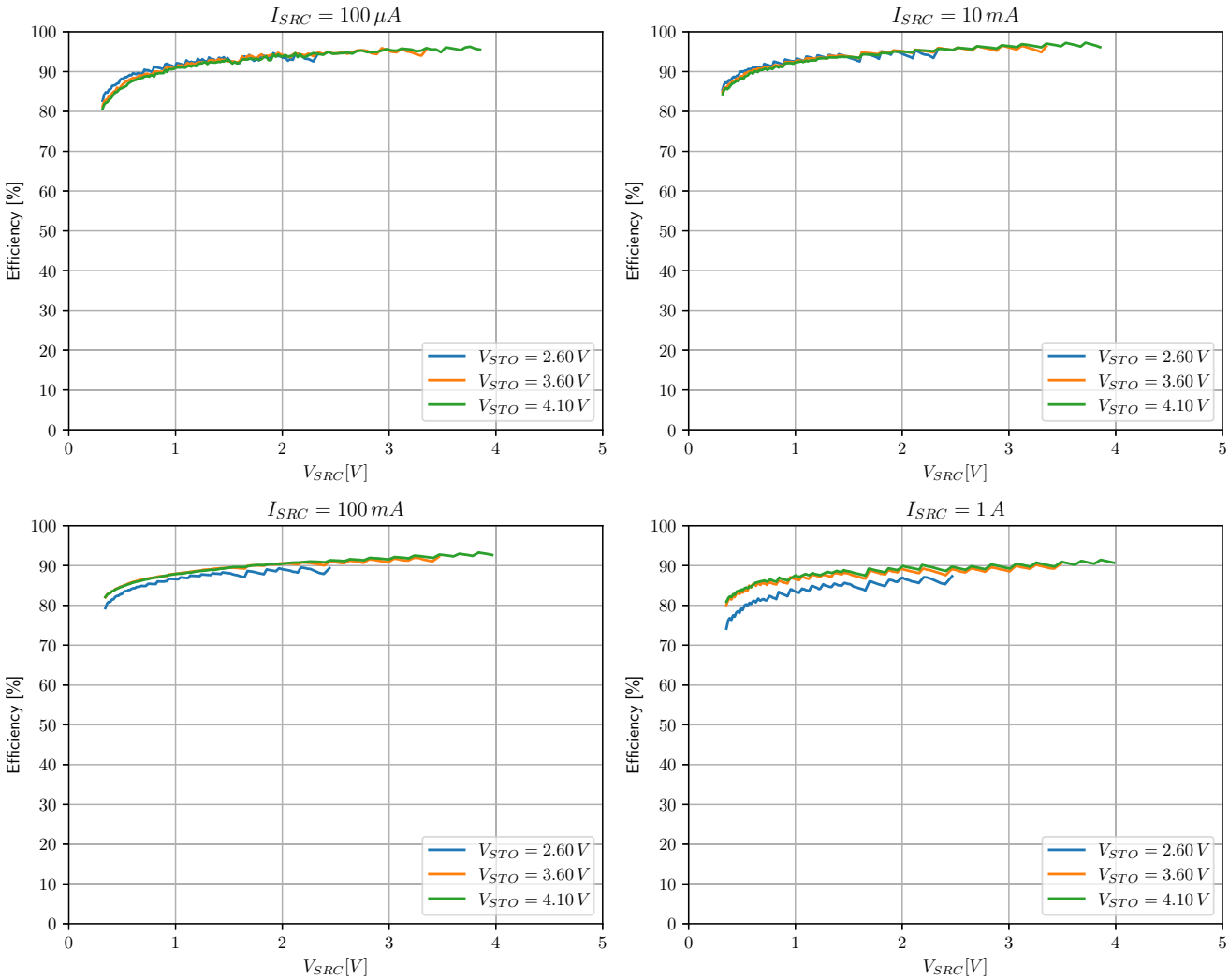



*Figure 4: SRC to STO efficiency vs. $V_{SRC}$ with $L_{BOOST\_LP}$ = 33 µH (TMULT x3) and $L_{BOOST\_HP}$ = 3.3 µH (TMULT x6)*

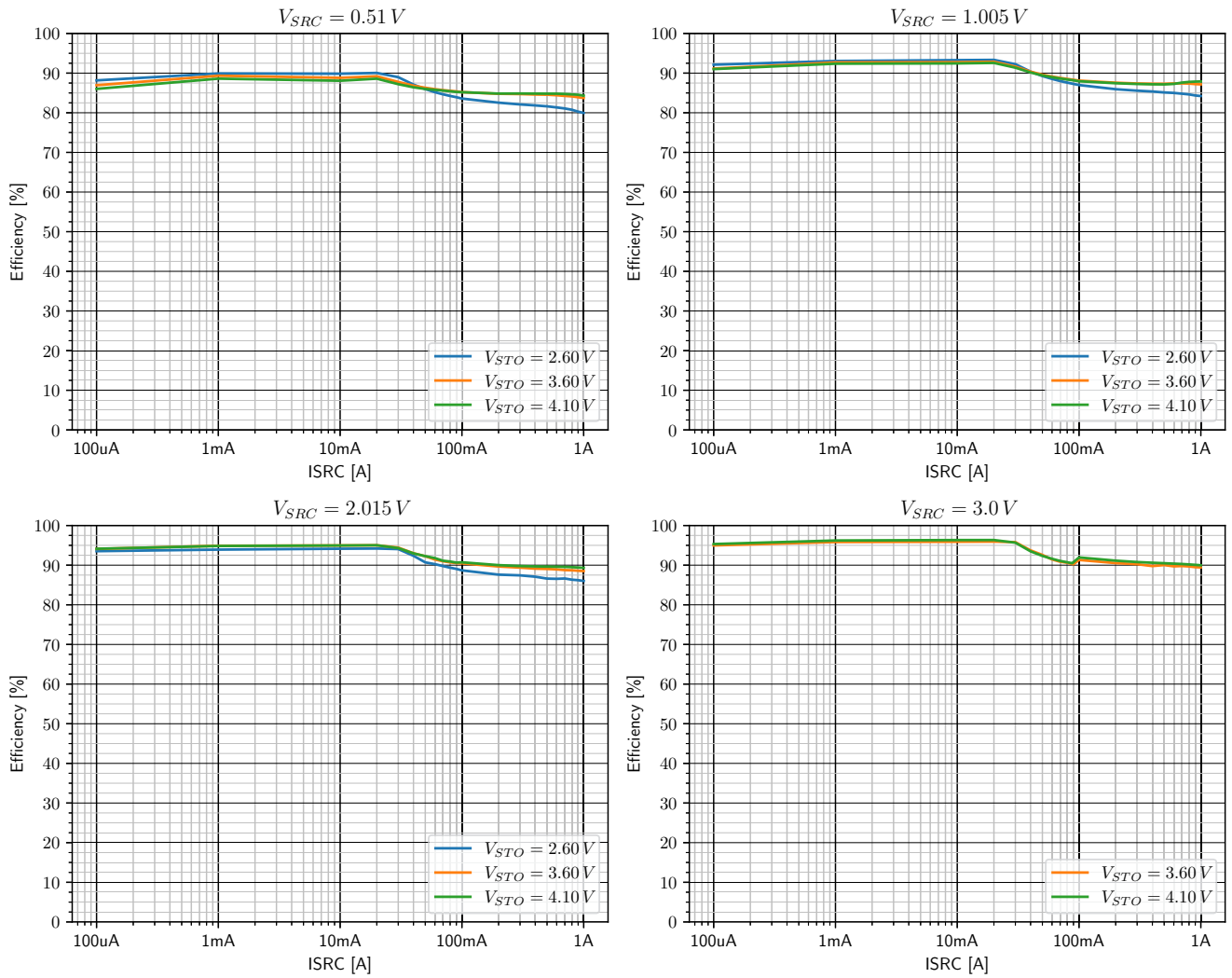



*Figure 5: SRC to STO efficiency vs. $I_{SRC}$ with $L_{BOOST\_LP}$ = 33 µH (TMULT x3) and $L_{BOOST\_HP}$ = 3.3 µH (TMULT x6)*

*NOTE: The boost efficiency graphs presented in this section include the loss of efficiency due to the AEM15820 quiescent current.*

*NOTE: The boost efficiency graphs have been measured with the external components recommended in Section 11.*

### 3.6.2. Buck Converter Conversion Efficiency

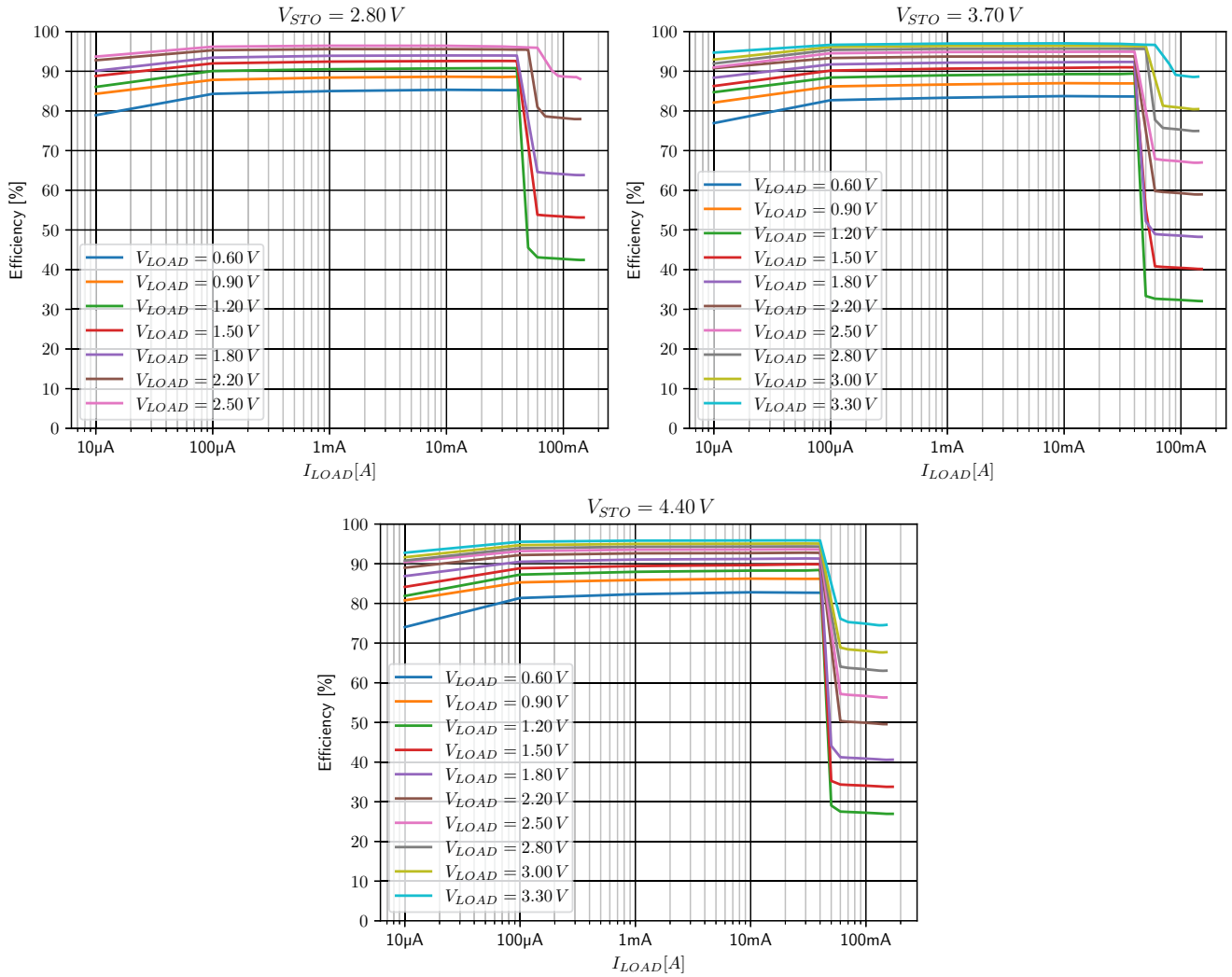



*Figure 6: STO to LOAD efficiency vs. $I_{LOAD}$ with $L_{BUCK}$ = 10 µH (TDK VLS252012CS-100M-1), BUCKCFG.TMULT = 0x01 (x2)*

*NOTE: The buck efficiency graphs presented in Figure 6 do not include the loss of efficiency due to the AEM15820 quiescent current, as it has already been included in the boost efficiency data shown in Section 3.6.1.*

*NOTE: The buck efficiency graphs have been measured with the external components recommended in Section 11.*

# 4. Functional Block Diagram

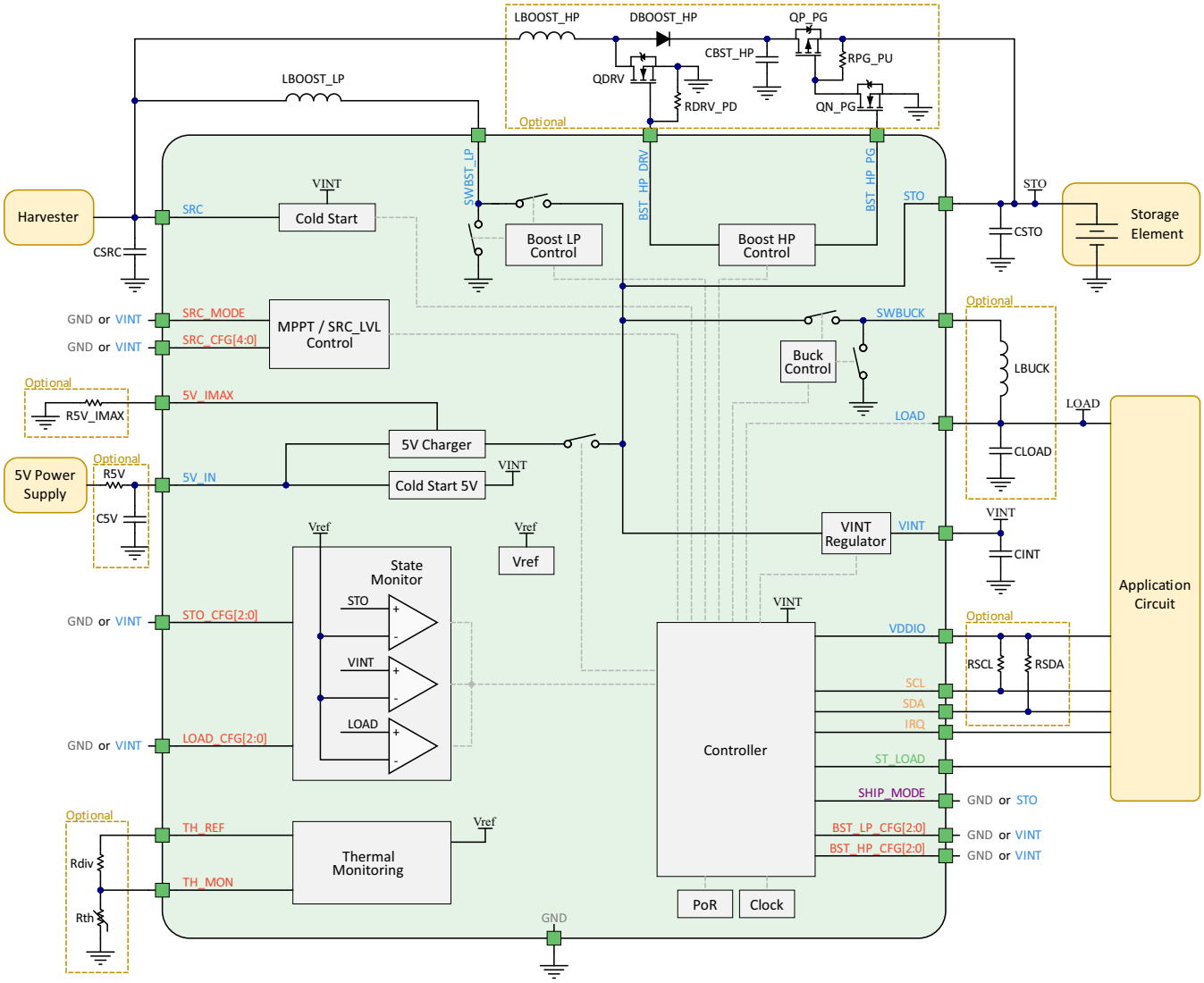



*Figure 7: Functional block diagram*

# 5. Theory of Operation

## 5.1. Cold-Start Circuits

The AEM15820 is able to coldstart from the source (SRC) or from the 5V_IN input (see Table 7 for cold-start conditions). The cold-start circuit provides energy to the AEM15820 internal supply (VINT) when the device is in RESET STATE, SENSE STO STATE or OVDIS STATE.

See Table 7 for the typical AEM15820 minimum cold-start voltage $V_{SRC,CS}$ and minimum cold-start power $P_{SRC,CS}$. Those values have been measured starting with all AEM15820 nodes discharged, except $V_{STO}$ that is charged above $V_{CHRDY}$. The cold start is considered to be finished when LOAD is supplied (buck is enabled), meaning that the AEM15820 has switched to SUPPLY STATE.

The time necessary for the AEM15820 to perform a cold start depends on multiple parameters such as:

- $I_{SRC}$: the higher the source current, the faster the cold start.
- $C_{INT}$: the higher the capacitance on VINT, the slower the cold start.

Typical cold-start time may vary between a few minutes for very low $I_{SRC}$ to a few tens of milliseconds for high $I_{SRC}$.

## 5.2. Boost Converters

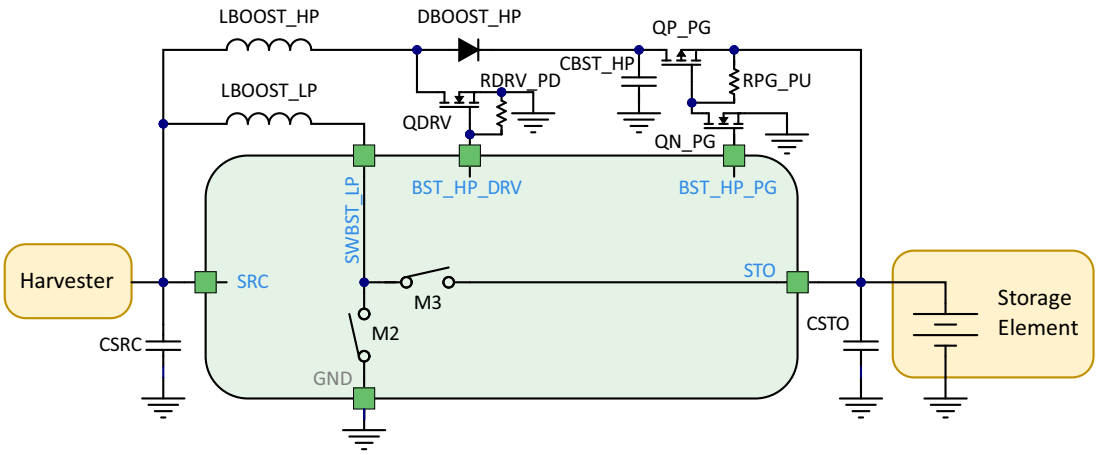



*Figure 8: Simplified schematic view of the boost converters*

### 5.2.1. Operation Principle

The boost (step-up) converters raise the voltage available at SRC to a level suitable for charging the storage element, in the range of 2.40 V to 4.59 V, according to the system configuration.

The internal switching transistors of the low-power boost converter are M2 and M3. While these transistors are replaced with $Q_{DRV}$ and $D_{BOOST\_HP}$ for the high-power boost converter. $Q_{P\_PG}$ and $Q_{N\_PG}$ are used to power gate the external high-power boost converter. The reactive power components for the low-power and the high-power boost converters are respectively $L_{BOOST\_LP}$ and $L_{BOOST\_HP}$.

Target source regulation voltage can be determined by:

- The MPPT module (ratio of open-circuit voltage) when SRC_MODE is HIGH (see Section 5.2.2).
- The constant voltage regulation setting when SRC_MODE is LOW (see Section 5.2.3).

SRC is decoupled by the capacitor $C_{SRC}$, which smooths the voltage against the current pulses induced by the boost converters.

When the power available on the SRC pin is low, the AEM15820 only uses its low-power boost converter to harvest energy from SRC. When the AEM15820 detects that the energy available on SRC is high enough, the BST_HP_PG pin is set HIGH and the high-power boost converter is automatically switched on, in addition to the low-power boost converter, to harvest the available energy.

The storage element is connected to the STO pin. This node is linked to the output of the boost converters.

The maximum current supplied to the STO pin depends on the value of both $L_{BOOST\_LP}$ and $L_{BOOST\_HP}$ and the boost converters timings for charging and discharging $L_{BOOST\_LP}$ and $L_{BOOST\_HP}$, and thus, the peak current $I_{LBOOST,PEAK}$. The boost timings can be configured thanks to the BST_LP_CFG[2:0] and BST_HP_CFG[2:0] pins or through the I²C register fields BSTLPCFG[4:2] and BSTHPCFG[4:2]. See Section 6.5 for boost timings multiplier configuration by GPIO and Section 9.6 for configuration by I²C, as well as typical combinations of $L_{BOOST\_LP}$ inductor value and boost converter timings.

While using an energy source is mandatory, using both boost converters is not: the user might use the low-power boost converter only or even use the AEM15820 only with the 5 V charger as energy source.

**CAUTION: Always ensure the high-power boost is disabled when disabling the low-power boost (e.g., when using the 5V_IN as only energy source).**

### 5.2.2. Maximum Power Point Tracking

This section describes the AEM15820 behavior when the source regulation mode is MPPT ratio. Switching to this mode is done by setting the SRC_MODE pin HIGH or by setting SRCREGU0.MODE I²C register field bit HIGH (see Sections 6.3 and 9.3).

The MPPT module is active during START STATE, OVDIS STATE and SUPPLY STATE.

In MPPT ratio mode, the AEM15820 MPPT relies on the fact that, for several models of harvesters (typ. solar cells), the ratio between the maximum power point voltage ($V_{MPP}$) and the open-circuit voltage ($V_{OC}$) is constant for a wide range of harvesting conditions. For a solar cell, this means that $V_{MPP}$ / $V_{OC}$ is constant for any lighting conditions, even though both voltages increase when luminosity increases. Please note that this is valid for a large variety of harvesters, not only solar cells.

The Maximum Power Point tracking (MPPT) ratio $V_{MPP}$ / $V_{OC}$ differs from one harvester model to another. The user must set the MPPT ratio ($R_{MPPT}$) to match the specifications of the harvester model used to maximize power extraction. This ratio is set through the configuration pins SRC_CFG[2:0] (see Section 6.3) or through the I²C interface register field SRCREGU0.CFG0 (see Section 9.3).

The MPPT module evaluates periodically with the following sequence the open-circuit voltage ($V_{OC}$) to ensure optimal power extraction at any time.

- The AEM15820 stops extracting power from the SRC during $T_{MPPT,WAIT}$ to allow the SRC voltage to rise to $V_{OC}$.
- Once this delay elapses, the AEM15820 performs the measurement of $V_{OC}$ during $T_{MPPT,MEASURE}$.
- After the measurement, the AEM15820 resumes extracting power by regulating the SRC voltage to the newly determined $V_{MPP}$.
- This MPPT evaluation is repeated every $T_{MPPT,PERIOD}$.

$T_{MPPT,WAIT}$ and $T_{MPPT,PERIOD}$ are set through the configuration pins SRC_CFG[4:3] (see Section 6.3) or by configuring the SRCREGU1 register (see Section 9.3) while $T_{MPPT,MEASURE}$ is constant for any configuration (see Table 8).

The total time during which the AEM15820 does not extract power correspond to the sum of $T_{MPPT,WAIT}$ and $T_{MPPT,MEASURE}$ (as shown in Figure 9).

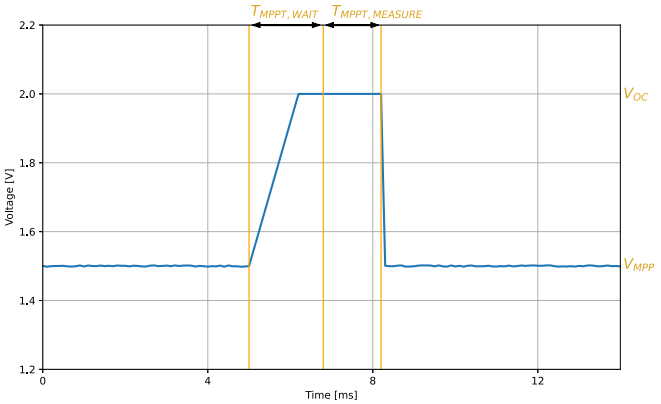



*Figure 9: MPPT evaluation behavior (with $T_{MPPT,WAIT}$ of 1.8 ms)*

### 5.2.3. Source Constant Voltage Regulation

This section describes the AEM15820 behavior when the source regulation mode is set to constant voltage. Switching to this mode is done by setting the SRC_MODE to LOW or by setting SRCREGU0.MODE I²C register field bit to LOW (see Sections 6.2 and 9.3).

During START STATE, OVDIS STATE and SUPPLY STATE, the voltage on SRC is regulated to a fixed voltage configured through the SRC_CFG[4:0] pins (see Section 6.2) or through the SRCREGUx registers (see Section 9.3).

In constant voltage regulation mode, the AEM15820 behaves as follows:

- If the open-circuit voltage $V_{OC}$ of the harvester is lower than $V_{SRC,REG}$, the AEM15820 does not extract power from the source.
- If $V_{OC}$ is higher than $V_{SRC,REG}$, the AEM15820 regulates $V_{SRC}$ to $V_{SRC,REG}$ and thus, extracts power from the source.
- If $V_{SRC,REG}$ is configured by I²C below $V_{SRCLOW}$ thanks to SRCREGUx and SRCLOW registers, the AEM15820 enters SLEEP STATE (see Section 5.9.6 and Section 9.4).

## 5.3. Buck Converter

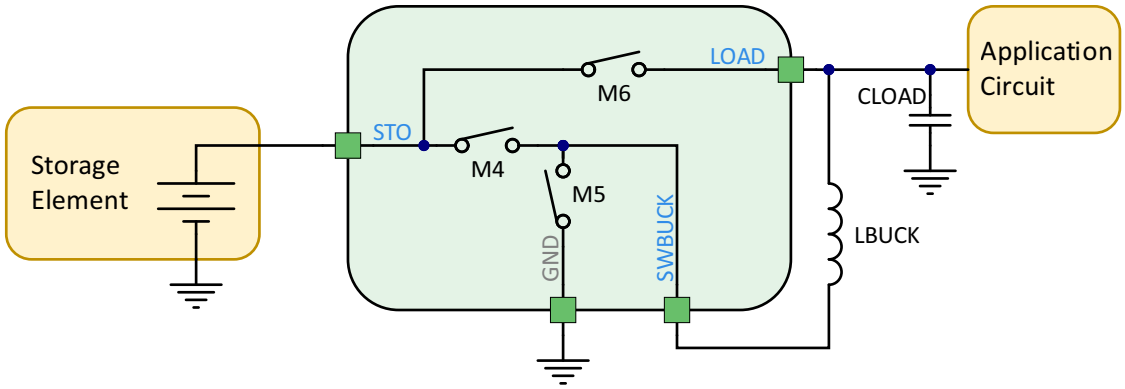



*Figure 10: Simplified schematic view of the buck converter*

The buck (step-down) converter transfers energy from the storage element connected to STO to the regulated LOAD output. The switching transistors of the buck converter are M4 and M5. The reactive power component of this converter is the external inductor $L_{BUCK}$. LOAD is decoupled by the capacitor $C_{LOAD}$, which smooths the voltage against the current pulses from the buck converter and the consumption of the external circuit connected to LOAD.

Setting the LOAD regulation voltage $V_{LOAD}$ or disabling the buck converter is done through the LOAD_CFG[2:0] pins (see Section 6.6) or the I²C register BUCKCFG (see Section 9.7).

After cold start, if the buck converter is enabled and if the temperature is within the range, the buck converter starts:

- When $V_{STO}$ is higher than $V_{CHRDY,BUCK}$ if the 5 V charger is not connected, or
- When $V_{STO}$ is higher than $V_{OVDIS,BUCK}$ if the 5 V charger is connected.

*NOTE: When using the 5 V charger, make sure that the configured $I_{5V,CC}$ is high enough to supply the circuit connected on LOAD. If not, once $V_{STO}$ rises above $V_{OVDIS,BUCK}$, LOAD is directly enabled, and the current drained on the storage element will directly discharge $V_{STO}$ below $V_{OVDIS,BUCK}$, thus, disabling the LOAD output.*

When $V_{STO}$ drops below $V_{OVDIS,BUCK}$, the AEM15820 waits for $T_{CRIT,ST}$ to set the ST_LOAD pin LOW, to set STATUS0.OVDIS register field HIGH and to schedule to disable the buck converter. The LOAD output remains enabled until the end of $T_{CRIT}$.

When the temperature gets out of the storage element discharge temperature range (TEMPCOLDDIS and TEMPHOTDIS), the AEM15820 rises the IRQFLG0.TEMPDIS and waits for $T_{CRIT,ST}$. If the temperature is still out of range after $T_{CRIT,ST}$, the ST_LOAD pin is set LOW and the AEM15820 schedules to disable the buck converter. The LOAD output remains enabled until the end of $T_{CRIT}$.

The maximum current supplied to the LOAD pin depends on both the value of $L_{BUCK}$ and the buck converter timings for charging and discharging $L_{BUCK}$, and thus, its peak current $I_{LBUCK,PEAK}$. The buck timings can be configured thanks to the I²C register field BUCKCFG.TMULT. See Section 6.6.2 for default buck timing values and Section 9.7 for further information and typical combinations of $L_{BUCK}$ inductor value and buck converter timings.

Using the buck converter is not mandatory. If not used, the user must do the following:

- Connect all LOAD_CFG[2:0] to GND (LOW) to disable the buck converter.
- Leave SWBUCK and LOAD floating.

When the difference between $V_{STO}$ and $V_{LOAD}$ is too small for the buck converter to keep working properly, it switches to "bang-bang" controlled converter mode:

- When $V_{LOAD}$ is too low, the switch M6 connects STO directly to LOAD, making $V_{LOAD}$ rise.
- When $V_{LOAD}$ is too high, M6 disconnects STO and LOAD so that $V_{LOAD}$ decreases.

This happens when the following condition is satisfied:

$$V_{STO} - V_{LOAD} < 0.25V$$

In that case, efficiency is lower than in buck mode.

## 5.4. Thermal Monitoring

The AEM15820 thermal monitoring allows for protecting the storage element from cold and hot temperatures by monitoring the ambient temperature and comparing it to the configured charge and discharge protection thresholds.

The charge minimum (cold) and maximum (hot) temperature thresholds are used to disable the boost converters in order to stop charging the storage element if the temperature is out of range.

The discharge minimum (cold) and maximum (hot) temperature thresholds are used to disable the buck converter in order to stop discharging the storage element through the LOAD if the temperature is out of range. Please note that in this case, VINT will continue to be supplied from STO.

To use the thermal monitoring feature, a resistor ($R_{DIV}$) and a NTC thermistor ($R_{TH}$) are required in order to form a resistive divider (see Figure 13). The TH_REF terminal allows for applying a reference voltage to the resistive divider while TH_MON is the measuring point. The temperature evaluation is done periodically every $T_{TEMP,MON}$ (see Table 8). To spare power, the divider is biased only during this evaluation.

See Section 6.7 for thermal monitoring configuration.

Thermal monitoring is optional, if not used, connect TH_MON to VINT and leave TH_REF floating.

## 5.5. Average Power Monitoring

The AEM15820 implements four different Average Power Monitoring (APM) modules:

- APMBSTLP: power transferred to STO from SRC through the low-power boost converter.
- APMBSTHP: count of energy pulses transferred to STO from SRC through the high-power boost converter.
- APMLOAD: power transferred from STO to LOAD (buck power converter).
- APMCHG5V: Percentage of APM window during which the 5V_IN input has been charging the storage element (5 V charger).

Please note that all APM measures are related to STO (energy provided to/from the storage) as shown on Figure 11.

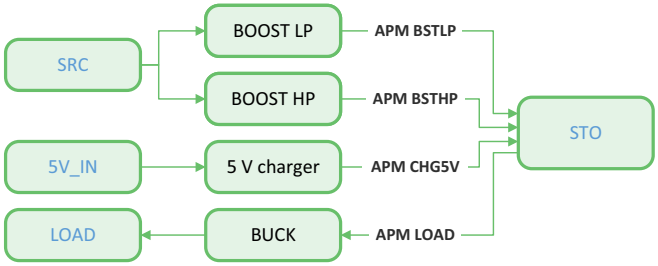



*Figure 11: Average Power Monitoring in the power chain*

### 5.5.1. BOOST and LOAD APM

The BSTLP, BSTHP, and LOAD APM modules work the same, so for these APM module explanations, the following is defined:

- APM_IN as the input node measured by the APM module.
- APM_OUT as the output node measured by the APM module.

Those APM modules are able to determine the transferred energy by counting the number of current pulses transferred from APM_IN to APM_OUT by the DCDC converter over a configurable time window, and thus, evaluates the corresponding energy.

Two modes are available:

- **Pulse Counter mode**: The APM modules count the number or DCDC pulses happening during the APM window.
- **Power Meter mode**: The APM modules integrate the energy transferred from APM_IN to APM_OUT during the APM window.

Refer to Section 9.17 for further details about how to set the modes and the window, and how to convert registers value to Joule.

*NOTE: the high-power boost APM (APMBSTHP) operates exclusively in pulse counter mode as the result in energy will mainly depend on the external components.*

### 5.5.2. 5 V Charger APM

The 5 V charger APM module (APMCHG5V) provides the percentage of the APM window during which the 5 V charger has been charging the storage element.

Refer to Section 9.17.2 for further details about how to interpret the 5 V charger APM register.

### 5.5.3. APM IRQ

If the IRQEN1.APMDONE field has been set to 1 (see Section 9.14), a rising edge on the IRQ pin along with the IRQFLG1.APMDONE field indicates the end of an APM window and thus, that new APM values are available and ready to be read in the APM data register (see Section 9.17).

Please note that all four APM modules operate synchronously with the same configured APM window.

When the IRQ pin rises due to the IRQFLG1.APMDONE, new APM data is available for all enabled APM modules. The APM data register should be read before the end of the next APM window, after which the APM data will be overwritten.

### 5.5.4. APM Accumulator

In order to get the APM data without waking up the application/MCU too often, the APM accumulator can be used.

This feature enables accumulation of APM data from the enabled APM modules over multiple consecutive APM windows. Instead of triggering the IRQ pin after each individual APM window, the AEM15820 sums the APM data from a configured number of consecutive windows. The IRQ pin is set by the IRQFLG1.APMDONE register only after the specified number of windows has been completed.

Please note that when the APM accumulator is used, the IRQ pin will be raised only after multiple APM windows, but the APM data register is still updated after each APM window.

Once the IRQ pin rises due to the IRQFLG1.APMDONE, the APM data register should be read before the end of the next APM window, after which the APM data will be overwritten.

Refer to Section 9.13 for further details about how to configure the APM accumulator feature.

## 5.6. IRQ Pin

The IRQ pin allows the application circuit to be notified of various events occurring in the AEM15820 (rising edge on the IRQ pin). At startup, the only event that is enabled is I2CRDY, signaling that the AEM15820 has finished to coldstart and thus, that it is out from RESET STATE. Other events can be enabled by writing the IRQEN0 and IRQEN1 registers (see Section 9.14).

When the IRQ pin shows a rising edge, the event that triggered it can be determined by reading the IRQFLG0 and IRQFLG1 registers (see Section 9.15). The IRQ pin is reset when the corresponding IRQFLGx register is read.

## 5.7. 5 V Charger

The AEM15820 is equipped with a 5 V charger (5V_IN) that can be used for fast charging of the storage element (STO) when the following conditions are met:

- $V_{5V\_IN} \geq 3.60$ V.
- $V_{5V\_IN} \geq V_{STO} + 200$ mV.
- The temperature is within the configured operating range.
- The AEM15820 is either in START STATE, SUPPLY STATE, or OVDIS STATE.

When the 5 V charger is connected, both boost converters are automatically disabled.

The 5 V charger operates in CC mode (see Section 5.7.1) or in CC/CV mode (see Section 5.7.2).

Using the 5 V charger is not mandatory. When not used, leave both 5V_IN and 5V_IMAX pins floating.

### 5.7.1. CC Mode

By default, the 5 V charger operates in constant current (CC) mode only. In this mode, the storage element is charged from the 5V_IN input with the configured maximum charging current ($I_{5V,CC}$). As $V_{STO}$ approaches $V_{OVCH}$, the AEM15820 gradually reduces the charging duty cycle to zero, progressively lowering the effective charging current through pulse-charging operation.

The maximum charging current is configurable in a range from 13.5 mA to 135 mA thanks to $R_{5V\_IMAX}$ resistor connected to the 5V_IMAX pin (see Section 6.8 for further details about $R_{5V\_IMAX}$ configuration).

*NOTE: When the storage element is over-discharged ($V_{STO} < V_{OVDIS}$), the charging current is limited to $I_{5V,OVDIS,CC}$ (see Table 7).*

### 5.7.2. CC/CV Mode

If enabled, the optional constant voltage (CV) mode allows the user to define a configurable end-of-charge voltage ($V_{5V,STOP}$) for the storage element. The 5 V charger operates in constant current (CC) mode during the main charging phase and maintains the configured maximum charging current until the storage element voltage approaches $V_{5V,STOP}$. The AEM15820 then switches to CV mode and reduces the charge current smoothly down to zero as $V_{STO}$ reaches $V_{5V,STOP}$.

If $V_{5V,STOP}$ is configured above $V_{OVCH}$, the CV mode has no effect and the charger behaves as if the feature was disabled. For proper operation, $V_{5V,STOP}$ must be set below $V_{OVCH}$.

See Section 6.8 for further details about how to configure the 5 V charger and Section 9.8 for CV mode enabling and $V_{5V,STOP}$ configuration.

## 5.8. Shipping Mode

The shipping mode feature allows to force the AEM15820 in RESET STATE (see Figure 12 and Section 5.9.1), thus, disabling all AEM15820 functionalities including both boost converters, the buck converter, the 5 V charger, and the I²C interface. Only VINT is charged if energy is available from SRC. The storage element is no longer charged or discharged.

See Section 6.9 for shipping mode configuration.

## 5.9. State Machine Description

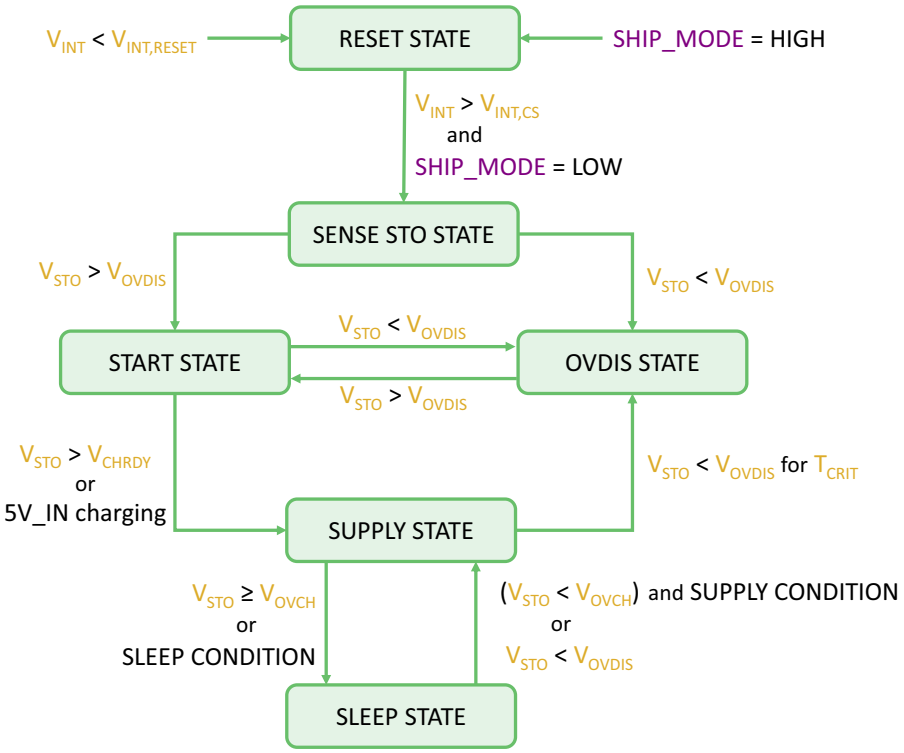



*Figure 12: State machine*

### 5.9.1. RESET STATE

The AEM15820 enters RESET STATE if one of the following is true:

- $V_{INT}$ is below $V_{INT,RESET}$ (see Table 9).
- Shipping mode is enabled (SHIP_MODE is HIGH).

In RESET STATE, the AEM15820 behaves as follows:

- Both boost converters and the buck converter are disabled.
- The AEM15820 internal supply (VINT) energy is provided by SRC or 5V_IN.
- Only $I_{Q,RESET}$ is drawn from the storage element connected to STO.

The AEM15820 stays in RESET STATE until the power available on SRC or on 5V_IN meets the cold-start requirements long enough to make $V_{INT}$ reach $V_{INT,CS}$ (see Table 7 and Table 9). Then:

- If shipping mode is disabled (SHIP_MODE is LOW), the AEM15820 reads the value on all configuration pins and switches to SENSE STO STATE.
- If shipping mode is enabled (SHIP_MODE is HIGH), the AEM15820 stays in RESET STATE until shipping mode is disabled by setting SHIP_MODE LOW. Please note that SHIP_MODE is read every $T_{GPIO,MON}$.

Please note that, from any state, the AEM15820 will switch to RESET STATE if $V_{INT}$ drops below $V_{INT,RESET}$.

### 5.9.2. SENSE STO STATE

In SENSE STO STATE, the AEM15820 behaves as follows:

- A first measure of $V_{STO}$ is performed by the AEM15820.
- The levels of SDA and SCL pins are evaluated to decide whether the I²C should be enabled (see Section 6.1.2)
- None of the DCDC converters are running.

The SENSE STO STATE lasts for about 2 ms.

From SENSE STO STATE, the AEM15820 switches to:

- START STATE if $V_{STO} > V_{OVDIS}$.
- OVDIS STATE if $V_{STO} < V_{OVDIS}$.

From this point, the I²C interface is available (see Section 6.1.2).

### 5.9.3. START STATE

When in SENSE STO STATE, the AEM15820 switches to START STATE if $V_{STO}$ is above $V_{OVDIS}$.

In START STATE, the AEM15820 behaves as follows:

- The storage element connected to STO is charged by the boost converters until $V_{STO}$ reaches $V_{CHRDY}$.
- VINT internal supply energy is provided by the storage element regardless of the power available on SRC and 5V_IN.
- The buck converter (LOAD) is disabled.

From START STATE, the AEM15820 switches to:

- SUPPLY STATE if $V_{STO} > V_{CHRDY}$ or if the 5 V charger is charging.
- OVDIS STATE if $V_{STO} < V_{OVDIS}$.

### 5.9.4. SUPPLY STATE

When in START STATE, the AEM15820 switches to SUPPLY STATE if $V_{STO}$ is above $V_{CHRDY}$ or if the 5 V charger is charging.

In SUPPLY STATE, the AEM15820 behaves the same as when in START STATE, but with the following differences:

- The LOAD is supplied by the buck converter and ST_LOAD pin is set HIGH if all of the following conditions are true:
  - The buck converter has been enabled by the user (see Section 6.6.1).
  - $V_{STO}$ is above $V_{OVDIS,BUCK}$ (if the 5 V charger is charging) or above $V_{CHRDY,BUCK}$ (if the 5 V charger is not charging).
  - The temperature is within the configured storage element discharge temperature range (TEMPCOLDDIS and TEMPHOTDIS, see Section 9.10).

From SUPPLY STATE, the AEM15820:

- Switches to SLEEP STATE if one of the following conditions is met:
  - $V_{STO} \geq V_{OVCH}$.
  - SLEEP CONDITION (see Section 5.9.6).
- Schedules to switch to OVDIS STATE if $V_{STO} < V_{OVDIS}$ for $T_{CRIT,ST}$, and waits for the end of $T_{CRIT}$ to actually switch to OVDIS STATE. If $V_{STO}$ recovers above $V_{OVDIS}$ after $T_{CRIT,ST}$ but before the end of $T_{CRIT}$, the AEM15820 will still enter OVDIS STATE at the end of $T_{CRIT}$.

### 5.9.5. OVDIS STATE

The AEM15820 switches to OVDIS STATE if:

- $V_{STO}$ is below $V_{OVDIS}$ when in SENSE STO STATE or START STATE.
- $V_{STO}$ remains below $V_{OVDIS}$ for more than $T_{CRIT,ST}$ when in SUPPLY STATE (waiting for the end of $T_{CRIT}$ to actually switch).

In OVDIS STATE, the AEM15820 behaves as follows:

- The storage element connected to STO is charged by the boost converters and/or by the 5 V charger, until $V_{STO}$ rises above $V_{OVDIS}$.
- VINT internal supply energy is provided by SRC or 5V_IN.
- The buck converter (LOAD) is disabled.

From OVDIS STATE, the AEM15820 switches to:

- START STATE if $V_{STO}$ rises above $V_{OVDIS}$.
- RESET STATE if not enough power is available on SRC and on 5V_IN to maintain $V_{INT}$ above $V_{INT,RESET}$. In this case, the STO pin is set to high impedance, so that virtually no current is drawn from the storage element connected to STO ($I_{Q,RESET}$ as defined in Section 3.4).

### 5.9.6. SLEEP STATE

SLEEP STATE allows for reducing the AEM15820 internal circuit consumption when SRC does not provide enough power or when the storage element is fully charged. Thus, storage element discharging is kept minimal. SLEEP STATE is also reached when charging is not allowed (temperature outside range, boost converters disabled, $V_{SRC}$ below the $V_{SRCLOW}$ threshold).

The following conditions are defined:

- SLEEP CONDITION is true if one of the following conditions is true:
  - Temperature outside of the range (see Section 6.7).
  - All boost converters are disabled through I²C (see Section 9.6).
  - Voltage on SRC is below the $V_{SRCLOW}$ threshold (see Section 9.4).

- SUPPLY CONDITION is true if all the following conditions are true:
  - Temperature within the range (see Section 6.7).
  - At least one boost converter is enabled (see Section 9.6).
  - Target voltage on SRC (i.e., $V_{MPP}$) is above the $V_{SRCLOW}$ threshold (see Section 9.4).

In SLEEP STATE, the AEM15820 behaves as follows:

- The storage element connected to STO is not charged by SRC, allowing for reducing the quiescent current on VINT and thus, on STO.
- If $V_{STO}$ is below $V_{OVCH}$, the storage element connected to STO can be charged from the 5 V charger by connecting a power source on 5V_IN.
- VINT internal supply energy is provided by the storage element regardless of the power available on SRC and 5V_IN.
- The buck converter (LOAD) is enabled (if the buck converter enabling conditions are true, see Section 5.9.4).

From SLEEP STATE, the AEM15820 switches back to SUPPLY STATE if one of the following conditions is met:

- SUPPLY CONDITION and $V_{STO} < V_{OVCH}$.
- $V_{STO} < V_{OVDIS}$.

# 6. System Configuration

## 6.1. Configuration Pins and I²C

### 6.1.1. Configuration Pins

After a cold start, the AEM15820 reads the configuration pins. Those are then read periodically every $T_{GPIO,MON}$. The configuration pins can be changed on-the-fly. The floating configuration pins are read as HIGH.

*NOTE: all the read-only registers (with addresses from IRQFLG0/0x18) can be read and contain valid data even if the AEM15820 is configured through the GPIO. The only exception is the APM-related registers that are no longer updated when using the GPIO configuration.*

### 6.1.2. Configuration by I²C

To configure the AEM15820 through the I²C interface after a cold start, the user must wait for the IRQ pin to rise, showing that the AEM15820 is out of RESET STATE and is ready to communicate with I²C. Please note that the IRQ pin is always low during RESET STATE. See Section 5.6 for further informations about the IRQ pin.

Once the above procedure is done, the user can write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored (except the SHIP_MODE pin) and all configurations are set by the register values. All registers have a default value that can be found in Table 20.

Registers are stored in a volatile memory, so their value is lost when VINT drops below the reset voltage $V_{INT,RESET}$, making the AEM15820 switch to RESET STATE. VDDIO is only for I²C communication bus reference voltage, so register values are kept whether VDDIO is supplied or not once registers are written.

*NOTE: It is important to note that if both SDA and SCL pins are read LOW (GND) during SENSE STO STATE, the I²C interface will be disabled. In this case, the IRQ pin will remain LOW, even if the AEM15820 is out of RESET STATE. To enable the I²C after this point, the master must first send an I²C message (START + DATA) to the AEM15820, such as the address of the AEM15820. Once the I²C interface is enabled, the IRQ pin is set HIGH along with the IRQFLG0.I2CRDY field to indicate that the I²C interface is ready.*

## 6.2. Source Constant Voltage Regulation

The following configurations apply when SRC_MODE is LOW, so that the boost converter is in constant voltage mode. The user can set the regulation voltage with SRC_CFG[4:0] (see Table 11), or through the SRCREGUx registers (see Section 9.3.3).

**CAUTION: The source regulation target voltage ($V_{SRC,REG}$) must never be configured below half of the source's open-circuit voltage ($V_{OC}$/2).**

**CAUTION: Do not reduce the source regulation target voltage ($V_{SRC,REG}$) on-the-fly by more than a factor of 2 while the boost converters are enabled. If such change is required, the boost converters must be disabled before updating the configuration.**

| Configuration pins | | | | | Voltage [V] |
|---|---|---|---|---|---|
| SRC_CFG[4:0] | | | | | $V_{SRC,REG}$ |
| L | L | L | L | L | Reserved[1] |
| L | L | L | L | H | 0.30 |
| L | L | L | H | L | 0.35 |
| L | L | L | H | H | 0.41 |
| L | L | H | L | L | 0.45 |
| L | L | H | L | H | 0.50 |
| L | L | H | H | L | 0.56 |
| L | L | H | H | H | 0.60 |
| L | H | L | L | L | 0.65 |
| L | H | L | L | H | 0.71 |
| L | H | L | H | L | 0.75 |
| L | H | L | H | H | 0.80 |
| L | H | H | L | L | 0.86 |
| L | H | H | L | H | 0.90 |
| L | H | H | H | L | 0.95 |
| L | H | H | H | H | 1.01 |

| Configuration pins | | | | | Voltage [V] |
|---|---|---|---|---|---|
| SRC_CFG[4:0] | | | | | $V_{SRC,REG}$ |
| H | L | L | L | L | 1.10 |
| H | L | L | L | H | 1.20 |
| H | L | L | H | L | 1.31 |
| H | L | L | H | H | 1.40 |
| H | L | H | L | L | 1.50 |
| H | L | H | L | H | 1.59 |
| H | L | H | H | L | 1.70 |
| H | L | H | H | H | 1.79 |
| H | H | L | L | L | 1.90 |
| H | H | L | L | H | 1.99 |
| H | H | L | H | L | 2.19 |
| H | H | L | H | H | 2.41 |
| H | H | H | L | L | 2.59 |
| H | H | H | L | H | 2.82 |
| H | H | H | H | L | 3.00 |
| H | H | H | H | H | 3.18 |

Table 11: Configuration of the source constant voltage regulation with SRC_CFG[4:0] pins

*1. This reserved configuration must not be used.*

## 6.3. Maximum Power Point Tracking

The following configurations apply when SRC_MODE is HIGH, so that the boost converter is in MPPT ratio mode. When configuring the MPPT module, the user can set the MPPT ratio and timings with SRC_CFG[4:0] (see Tables 12 and 13), or through the SRCREGUx registers (see Section 9.3).

**CAUTION: When using the source MPPT ratio mode, the source low threshold must be configured through I²C to a value higher or equal to 300 mV. See SRCLOW register in Section 9.4.**

| Configuration pins | | | MPPT Ratio |
|---|---|---|---|
| SRC_CFG[2:0] | | | $R_{MPPT}$ |
| L | L | L | Reserved[1] |
| L | L | H | 50 % |
| L | H | L | 65 % |
| L | H | H | 70 % |
| H | L | L | 75 % |
| H | L | H | 80 % |
| H | H | L | 85 % |
| H | H | H | Reserved[1] |

Table 12: MPPT ratio configuration with SRC_CFG[2:0] pins

*1. Those reserved configurations must not be used.*

| Configuration pins | | MPPT wait time [ms] | MPPT Period [ms] |
|---|---|---|---|
| SRC_CFG[4:3] | | $T_{MPPT,WAIT}$[1] | $T_{MPPT,PERIOD}$ |
| L | L | 1.8 | 116[2] |
| L | H | 7.3 | 465 |
| H | L | 29 | 1862 |
| H | H | 233 | 14895 |

Table 13: MPPT timing configuration with SRC_CFG[4:3] pins

*1. The total time spent in open-circuit is the sum of $T_{MPPT,WAIT}$ (configurable, see table above) and $T_{MPPT,MEASURE}$ (fixed, see Table 8).*
*2. If $T_{MPPT,PERIOD}$ is set to 116 ms for SRC, the APM WINDOW will automatically be set to 116 ms by the AEM15820 for the two boost converters, the buck converter, and the 5 V charger APM modules.*

When using the MPPT ratio regulation mode (SRC_MODE = H), the total capacitance connected to the SRC of the AEM15820 should be selected based on the characteristics of the energy harvester and on the available source power. The source capacitor charging time up to the open-circuit voltage ($V_{OC}$) during the Maximum Power Point (MPP) evaluations, must remain shorter than the configured $T_{MPPT,WAIT}$. This will ensure an accurate measurement of the open-circuit voltage and thus, an accurate source voltage regulation.

The selected $C_{SRC}$ must be big enough to stabilize the source voltage with high-power input, but small enough to reach the open-circuit voltage during $T_{MPPT,WAIT}$ with low-power input.

## 6.4. Storage Element Thresholds

The storage element protection thresholds, the storage element buck charge ready threshold, and the temperature thresholds are configurable to match various storage element types through the STO_CFG[2:0] pins (see Tables 14, 15, and 16), or through the following I²C registers:

- VOVDIS, VCHRDY, and VOVCH: to configure the storage element protection voltage thresholds $V_{OVDIS}$, $V_{CHRDY}$, and $V_{OVCH}$ (see Section 9.5).
- VCHRDYBUCK: to configure the buck charge ready voltage threshold $V_{CHRDY,BUCK}$ (see Section 9.5.3).
- TEMPCOLDCH, TEMPHOTCH, TEMPCOLDDIS, and TEMPHOTDIS: to configure the storage element protection temperature thresholds (see Sections 9.9 and 9.10).

For the configuration of $V_{OVDIS}$, $V_{CHRDY}$, $V_{OVCH}$, and $V_{CHRDY,BUCK}$ via I²C, ensure that the following conditions are respected:

$$V_{OVDIS} < V_{CHRDY} < V_{OVCH}$$

$$V_{OVDIS,BUCK} < V_{CHRDY,BUCK}$$

*NOTE: It is recommended to provide a minimum margin of 100 mV between $V_{OVDIS}$, $V_{CHRDY}$, and $V_{OVCH}$, and between $V_{OVDIS,BUCK}$ and $V_{CHRDY,BUCK}$ to avoid unintended state switching, or buck enabling due to small storage element voltage variations.*

The storage element buck overdischarge threshold $V_{OVDIS,BUCK}$ is not configurable. This voltage threshold is defined with the following formula:

$$V_{OVDIS,BUCK} = MAX(V_{OVDIS}, V_{LOAD})$$

| Configuration pins | | | Overdischarge voltage [V] | Charge ready voltage [V] | Overcharge voltage [V] | Storage element type |
|---|---|---|---|---|---|---|
| STO_CFG[2:0] | | | $V_{OVDIS}$ | $V_{CHRDY}$ | $V_{OVCH}$ | |
| L | L | L | 2.51 | 2.61 | 3.79 | Lithium-ion Super Capacitor (LiC) |
| L | L | H | 2.51 | 2.61 | 3.49 | Lithium-ion Super Capacitor 85 °C (LiC) |
| L | H | L | 3.00 | 3.21 | 4.13 | Lithium-ion |
| L | H | H | 3.00 | 3.21 | 3.90 | Lithium-ion (long life) |
| H | L | L | 3.51 | 3.60 | 3.90 | Lithium-ion (super long life) |
| H | L | H | 3.00 | 3.60 | 4.35 | Lithium Polymer (LiPo), NiMH |
| H | H | L | 2.81 | 3.11 | 3.62 | Lithium Iron Phosphate (LiFePO4) |
| H | H | H | 2.61 | 2.70 | 3.90 | Tadiran HLC1020 |

Table 14: Storage element thresholds configuration with STO_CFG[2:0] pins

| Configuration pins | | | Buck charge ready voltage [V] | | | | Storage element type |
|---|---|---|---|---|---|---|---|
| STO_CFG[2:0] | | | $V_{CHRDY,BUCK}$ for $V_{LOAD} \leq 2.5$ V | $V_{CHRDY,BUCK}$ for $V_{LOAD} = 2.8$ V | $V_{CHRDY,BUCK}$ for $V_{LOAD} = 3.0$ V | $V_{CHRDY,BUCK}$ for $V_{LOAD} = 3.3$ V | |
| L | L | L | 2.61 | 2.91 | 3.11 | 3.41 | Lithium-ion Super Capacitor (LiC) |
| L | L | H | 2.61 | 2.91 | 3.11 | 3.41 | Lithium-ion Super Capacitor 85 °C (LiC) |
| L | H | L | 3.21 | 3.21 | 3.21 | 3.51 | Lithium-ion |
| L | H | H | 3.21 | 3.21 | 3.21 | 3.51 | Lithium-ion (long life) |
| H | L | L | 3.60 | 3.60 | 3.60 | 3.60 | Lithium-ion (super long life) |
| H | L | H | 3.60 | 3.60 | 3.60 | 3.60 | Lithium Polymer (LiPo), NiMH |
| H | H | L | 3.11 | 3.11 | 3.21 | 3.41 | Lithium Iron Phosphate (LiFePO4) |
| H | H | H | 2.70 | 2.91 | 3.11 | 3.41 | Tadiran HLC1020 |

Table 15: Buck thresholds with STO_CFG[2:0] pins configuration depending on LOAD voltage

| Configuration pins | | | Minimum charging temperature [°C] | Maximum charging temperature [°C] | Minimum discharging temperature [°C] | Maximum discharging temperature [°C] | Storage element type |
|---|---|---|---|---|---|---|---|
| STO_CFG[2:0] | | | TEMPCOLDCH | TEMPHOTCH | TEMPCOLDDIS | TEMPHOTDIS | |
| L | L | L | -15 | 60 | -15 | 60 | Lithium-ion Super Capacitor (LiC) |
| L | L | H | -25 | 85 | -25 | 85 | Lithium-ion Super Capacitor 85 °C (LiC) |
| L | H | L | 0 | 45 | 0 | 45 | Lithium-ion |
| L | H | H | 0 | 45 | 0 | 45 | Lithium-ion (long life) |
| H | L | L | 0 | 45 | 0 | 45 | Lithium-ion (super long life) |
| H | L | H | 0 | 45 | 0 | 45 | Lithium Polymer (LiPo), NiMH |
| H | H | L | 0 | 45 | 0 | 45 | Lithium Iron Phosphate (LiFePO4) |
| H | H | H | -40 | 85 | -40 | 85 | Tadiran HLC1020 |

Table 16: Default temperature thresholds depending on STO_CFG[2:0] configuration with the recommended RDIV and RTH

**DISCLAIMER: Storage element protection thresholds and temperature thresholds provided for each storage element type in the table above are indicative to support a wide range of storage element variants. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.**

## 6.5. Boost Converter Timings

The user can configure different boost timing multiplier values, and thus, configure the peak current for the low-power and the high-power boost converters, with the BST_LP_CFG[2:0] and BST_HP_CFG[2:0], or through the BSTLPCFG and BSTHPCFG registers (see Section 9.6).

| Configuration pins | | | Boost timing multiplier |
|---|---|---|---|
| BST_LP_CFG[2:0] BST_HP_CFG[2:0] | | | $T_{MULT}$ |
| L | L | L | x1 |
| L | L | H | x2 |
| L | H | L | x3 |
| L | H | H | x4 |
| H | L | L | x6 |
| H | L | H | x8 |
| H | H | L | x12 |
| H | H | H | x16 |

Table 17: Configuration of $T_{MULT}$ with BST_LP_CFG[2:0] and BST_HP_CFG[2:0]

Please refer to Table 41 for the different minimum and recommended $L_{BOOST\_LP}$ values for each timing multiplier value. For $L_{BOOST\_HP}$, the limitations will depend on the selected high-power boost external components.

## 6.6. Buck Converter

### 6.6.1. Load Voltage

The regulated voltage on LOAD output can be configured with the LOAD_CFG[2:0] pins (see Table 18), or through the BUCKCFG register (see Section 9.7).

| Configuration pins | | | LOAD voltage [V] |
|---|---|---|---|
| LOAD_CFG[2:0] | | | $V_{LOAD}$ |
| L | L | L | Buck disabled |
| L | L | H | 1.2 |
| L | H | L | 1.8 |
| L | H | H | 2.2 |
| H | L | L | 2.5 |
| H | L | H | 2.8 |
| H | H | L | 3.0 |
| H | H | H | 3.3 |

Table 18: Configuration of LOAD voltage with LOAD_CFG[2:0]

*NOTE: the configuration of LOAD_CFG[2:0] can only be changed when the AEM15820 is in RESET STATE (see Section 5.9.1 for more information).*

### 6.6.2. Buck Converter Timings

The buck converter timing multiplier ($T_{MULT}$) default value when the I²C is not used is x2.

A different buck timing multiplier value can be configured through the BUCKCFG register (see Section 9.7), thus configuring the peak current of the buck converter inductor (available by I²C register only).

Please refer to Table 43 for the different $L_{BUCK}$ values for each timing multiplier value.

## 6.7. Thermal Monitoring

Once the thermal monitoring has been enabled by connecting $R_{DIV}$ and $R_{TH}$ as shown in Figure 13, the thermal protection can be used.

The typical values of $R_{DIV}$ and $R_{TH}$, found in Table 10, allow for having the default temperature thresholds depending on STO_CFG[2:0] configuration as shown in Table 16.

To use different temperature protection thresholds for storage element charge (see Section 9.9) and for storage element discharge (see Section 9.10), the TEMPCOLDCH, TEMPHOTCH, TEMPCOLDDIS, and TEMPHOTDIS registers can be used along with the following equations:

$$THRESH(T) = \frac{256 \cdot R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

$$R_{TH}(T) = R0 \cdot e^{B \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

$$T = \frac{B}{\ln\left(\frac{R_{TH}(T)}{R0}\right) + \frac{B}{T_0}}$$

- THRESH is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R0 [Ω] is the resistance of the NTC thermistor at ambient temperature $T_0$ = 298.15 K (25 °C).
- $R_{TH}(T)$ [Ω] is the resistance of the thermistor at temperature T [K].
- $T_0$ [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

Please note that the thermistor must be of the NTC (Negative Temperature Coefficient) type.

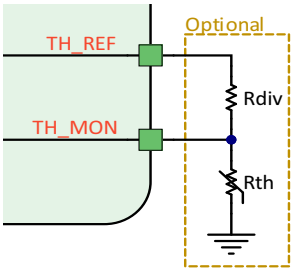



*Figure 13: TH_REF and TH_MON connections*

If thermal protection is not needed, it can be disabled through TEMPPROTECT register (see Section 9.11). In that case:

- If $R_{DIV}$ and $R_{TH}$ are connected, the temperature will continue to be measured periodically every $T_{TEMP,MON}$ but the protection thresholds will be ignored. The temperature data can be read through the TEMP register.
- If TH_MON is connected to VINT and TH_REF left floating, the thermal monitoring will be disabled.

## 6.8. 5 V Charger

As explained in the Section 5.7, the 5 V charger implements a constant current (CC) mode and a constant voltage (CV) mode.

When in constant current mode, the maximum charging current $I_{5V,CC}$ can be set by connecting a resistor $R_{5V\_IMAX}$ between 5V_IMAX and GND:

$$I_{5V,CC} = \frac{50}{R_{5V\_IMAX}}$$

$R_{5V\_IMAX}$ must be chosen so that $I_{5V,CC}$ complies with the range defined in Table 7. Example values can be found in Table 19:

| Resistor [Ω] | Maximum Charging Current [mA] |
|---|---|
| $R_{5V\_IMAX}$ | $I_{5V,CC}$ |
| 370 | 135.0 |
| 680 | 73.5 |
| 1500 | 33.3 |
| 3700 | 13.5 |

Table 19: Typical resistor values for setting 5 V charger max. current

If $V_{STO} < V_{OVDIS}$, the charging current is limited to $I_{5V,OVDIS,CC}$.

To use the CV mode (disabled by default), the user must enable CV operation mode and configure the 5 V charger stop voltage $V_{5V,STOP}$ by I²C (see Section 9.8).

Please note that, regardless of the operating mode, the rise time of the voltage applied on the 5V_IN pin must not be too short. Thus, it is recommended to add an RC circuit in series with the 5V_IN pin which matches the following, with $R_{5V}$ in series and $C_{5V}$ between 5V_IN and GND:

$$R_{5V} \cdot C_{5V} > T_{5V,RISE}$$

- $T_{5V,RISE}$ is the minimum rise time from 0 V to 5 V on the 5V_IN pin (see Table 8). Comparing this to the RC constant adds a margin as the RC constant defines 63 % of the final voltage.
- $R_{5V}$ must be determined so that, for the configured $I_{5V,CC}$, the voltage on the 5V_IN pin is:
  - above 3.60 V.
  - above $V_{STO}$ + 200 mV.
- $C_{5V}$ is determined from the value of $R_{5V}$ using the equation above. A low charging current allows for high $R_{5V}$ value and thus, for a low $C_{5V}$ value.

## 6.9. Shipping Mode

The shipping mode, described in Section 5.8, is configured as follows:

- Shipping mode enabled by connecting the SHIP_MODE pin to STO.
- Shipping mode disabled by connecting the SHIP_MODE pin to GND or by leaving it floating.

# 7. I²C Serial Interface Protocol

The AEM15820 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

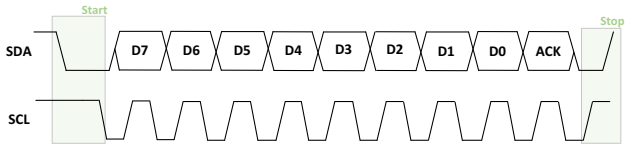



*Figure 14: I²C transmission frame*

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM15820 is a slave that will receive configuration data or send the informations requested by the master.

The AEM15820 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data is sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x61 for the AEM15820.
- Bit [0] is the communication mode: 1 for 'read mode' (used when the master reads informations from the slave) and 0 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

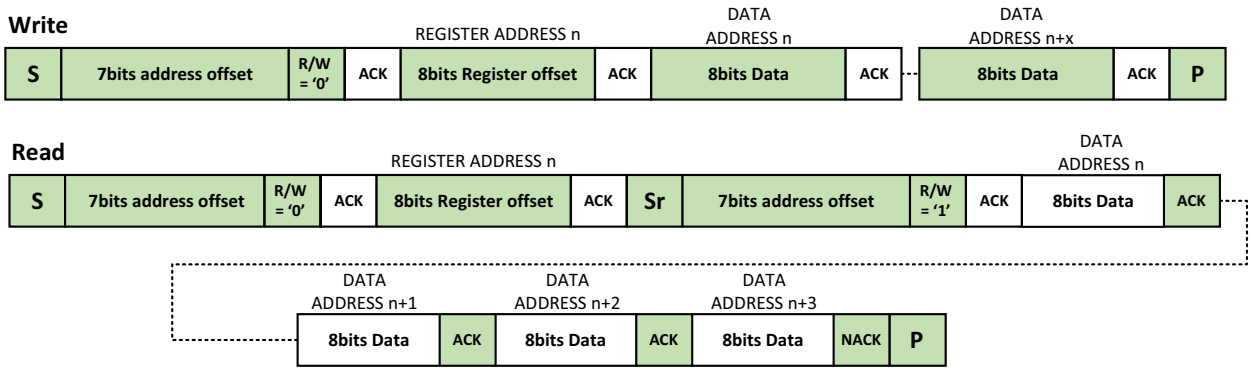
Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCOLDCH register, the master sends the value 0x0D;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMPHOTCH in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the APM0LOAD register, the master sends the value 0x22;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (APM1LOAD in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for reading several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in Figure 15. Refer to Table 20 for all register addresses.




S = START
ACK = ACKNOWLEDGE
P = STOP
R/W = READ/WRITE
NACK = NOT ACKNOWLEGDE
Sr = RESTART

*Figure 15: Read and write transmission*

# 8. Register Map

Please note that the AEM15820 device address is 0x61.

| Address | Name | Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|---|---|
| 0x00 | VERSION | [7:0] | VERSION | R | - | AEM15820 version number. |
| 0x01 | SRCREGU0 | [0:0] | MODE | R/W | 0x01 | SRC regulation mode. |
| | | [3:1] | CFG0 | R/W | Reserved | SRC regulation mechanism configuration. SRCREGU0.CFG0 default value is reserved, this field must be set by the user. |
| 0x02 | SRCREGU1 | [2:0] | CFG1 | R/W | 0x00 | |
| | | [5:3] | CFG2 | R/W | 0x00 | |
| 0x03 | RSVD_WI | [7:0] | - | R/W | - | Reserved (write-ignore). |
| 0x04 | RSVD_WI | [7:0] | - | R/W | - | Reserved (write-ignore). |
| 0x05 | VOVDIS | [5:0] | THRESH | R/W | 0x06 | Storage element overdischarge threshold. |
| 0x06 | VCHRDY | [6:0] | THRESH | R/W | 0x05 | Storage element charge ready threshold. |
| 0x07 | VOVCH | [6:0] | THRESH | R/W | 0x3A | Storage element overcharge threshold. |
| 0x08 | BSTLPCFG | [0:0] | EN | R/W | 0x01 | Boost low-power enable. |
| | | [1:1] | - | R/W | 0x01 | Reserved (write-ignored). |
| | | [4:2] | TMULT | R/W | 0x01 | Boost low-power current configuration. |
| 0x09 | BSTHPCFG | [0:0] | EN | R/W | 0x01 | Boost high-power enable. |
| | | [1:1] | - | R/W | 0x01 | Reserved (write-ignored). |
| | | [4:2] | TMULT | R/W | 0x01 | Boost high-power current configuration. |
| 0x0A | BUCKCFG | [3:0] | VLOAD | R/W | 0x00 | Buck output voltage configuration. |
| | | [6:4] | TMULT | R/W | 0x03 | Buck current configuration. |
| 0x0B | VCHRDYBUCK | [6:0] | THRESH | R/W | 0x05 | Storage element charge ready buck threshold. |
| 0x0C | CHG5V | [0:0] | EN | R/W | 0x01 | 5 V charger enable. |
| | | [1:1] | CVEN | R/W | 0x00 | Constant voltage (CV) mode enable. |
| | | [6:2] | THRESH | R/W | 0x00 | 5 V charger stop voltage threshold. |
| 0x0D | TEMPCOLDCH | [7:0] | THRESH | R/W | 0xD1 | Cold temperature threshold for storage element charging. |
| 0x0E | TEMPHOTCH | [7:0] | THRESH | R/W | 0x18 | Hot temperature threshold for storage element charging. |
| 0x0F | TEMPCOLDDIS | [7:0] | THRESH | R/W | 0xD1 | Cold temperature threshold for storage element discharging. |
| 0x10 | TEMPHOTDIS | [7:0] | THRESH | R/W | 0x18 | Hot temperature threshold for storage element discharging. |
| 0x11 | TEMPPROTECT | [0:0] | EN | R/W | 0x01 | Thermal protection enable. |
| 0x12 | SRCLOW | [2:0] | SRCTHRESH | R/W | Reserved | $V_{SRCLOW}$ threshold. |
| 0x13 | APM | [0:0] | BSTLPEN | R/W | 0x00 | APM BSTLP enable. |
| | | [1:1] | BSTHPEN | R/W | 0x00 | APM BSTHP enable. |
| | | [2:2] | LOADEN | R/W | 0x00 | APM LOAD enable. |
| | | [3:3] | CHG5VEN | R/W | 0x00 | APM 5 V charger enable. |
| | | [4:4] | MODE | R/W | 0x00 | APM mode. |
| | | [5:5] | WINDOW | R/W | 0x00 | APM window. |
| 0x14 | APMACC | [7:0] | CFG | R/W | 0x00 | Number of APM window accumulations. |

Table 20: Register map (part 1)

| Address | Name | Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|---|---|
| 0x15 | IRQEN0 | [0:0] | I2CRDY | R/W | 0x01 | IRQ serial interface ready enable. |
| | | [1:1] | VOVDIS | R/W | 0x00 | IRQ VOVDIS enable. |
| | | [2:2] | VCHRDY | R/W | 0x00 | IRQ VCHRDY enable. |
| | | [3:3] | VOVCH | R/W | 0x00 | IRQ VOVCH enable. |
| | | [4:4] | SRCLOW | R/W | 0x00 | IRQ source low threshold enable. |
| | | [5:5] | TEMPCH | R/W | 0x00 | IRQ temperature charge enable. |
| | | [6:6] | TEMPDIS | R/W | 0x00 | IRQ temperature discharge enable. |
| | | [7:7] | CHG5VCONN | R/W | 0x00 | IRQ 5 V charger connected enable. |
| 0x16 | IRQEN1 | [0:0] | SRCMPPTSTART | R/W | 0x00 | IRQ MPPT start enable. |
| | | [1:1] | SRCMPPTDONE | R/W | 0x00 | IRQ MPPT done enable. |
| | | [2:2] | - | R/W | 0x00 | Reserved (write-ignored). |
| | | [3:3] | - | R/W | 0x00 | Reserved (write-ignored). |
| | | [4:4] | STODONE | R/W | 0x00 | IRQ STO measurement done enable. |
| | | [5:5] | TEMPDONE | R/W | 0x00 | IRQ temperature measurement done enable. |
| | | [6:6] | APMDONE | R/W | 0x00 | IRQ APM done enable. |
| | | [7:7] | APMERR | R/W | 0x00 | IRQ APM error enable. |
| 0x17 | CTRL | [0:0] | UPDATE | R/W | 0x00 | Load I²C registers configuration. |
| | | [1:1] | - | R | - | Reserved. |
| | | [2:2] | SYNCBUSY | R | 0x00 | Synchronization busy flag. |
| 0x18 | IRQFLG0 | [0:0] | I2CRDY | R | 0x00 | IRQ serial interface ready flag. |
| | | [1:1] | VOVDIS | R | 0x00 | IRQ VOVDIS flag. |
| | | [2:2] | VCHRDY | R | 0x00 | IRQ VCHRDY flag. |
| | | [3:3] | VOVCH | R | 0x00 | IRQ VOVCH flag. |
| | | [4:4] | SRCLOW | R | 0x00 | IRQ source low threshold flag. |
| | | [5:5] | TEMPCH | R | 0x00 | IRQ temperature (charge) flag. |
| | | [6:6] | TEMPDIS | R | 0x00 | IRQ temperature (discharge) flag. |
| | | [7:7] | CHG5VCONN | R | 0x00 | IRQ 5 V charger connected flag. |
| 0x19 | IRQFLG1 | [0:0] | SRCMPPTSTART | R | 0x00 | IRQ MPPT start flag. |
| | | [1:1] | SRCMPPTDONE | R | 0x00 | IRQ MPPT done flag. |
| | | [2:2] | - | R | - | Reserved. |
| | | [3:3] | - | R | - | Reserved. |
| | | [4:4] | STODONE | R | 0x00 | IRQ STO measurement done flag. |
| | | [5:5] | TEMPDONE | R | 0x00 | IRQ temperature measurement done flag. |
| | | [6:6] | APMDONE | R | 0x00 | IRQ APM done flag. |
| | | [7:7] | APMERR | R | 0x00 | IRQ APM error flag. |
| 0x1A | STATUS0 | [0:0] | OVDIS | R | 0x00 | Status overdischarge. |
| | | [1:1] | CHRDY | R | 0x00 | Status charge ready. |
| | | [2:2] | OVCH | R | 0x00 | Status overcharge. |
| | | [3:3] | SRCLOW | R | 0x00 | Status source low threshold. |
| | | [4:4] | - | R | - | Reserved. |
| | | [5:5] | CHG5VCONN | R | 0x00 | Status 5 V charger connected. |

Table 20: Register map (part 2)

| Address | Name | Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|---|---|
| 0x1B | STATUS1 | [0:0] | TEMPCOLDCH | R | 0x00 | Status cold temperature (charge). |
| | | [1:1] | TEMPHOTCH | R | 0x00 | Status hot temperature (charge). |
| | | [2:2] | TEMPCOLDDIS | R | 0x00 | Status cold temperature (discharge). |
| | | [3:3] | TEMPHOTDIS | R | 0x00 | Status hot temperature (discharge). |
| 0x1C | APM0BSTLP | [7:0] | DATA | R | 0x00 | APM data 0 (BSTLP). |
| 0x1D | APM1BSTLP | [7:0] | DATA | R | 0x00 | APM data 1 (BSTLP). |
| 0x1E | APM2BSTLP | [7:0] | DATA | R | 0x00 | APM data 2 (BSTLP). |
| 0x1F | APM0BSTHP | [7:0] | DATA | R | 0x00 | APM data 0 (BSTHP). |
| 0x20 | APM1BSTHP | [7:0] | DATA | R | 0x00 | APM data 1 (BSTHP). |
| 0x21 | APM2BSTHP | [7:0] | DATA | R | 0x00 | APM data 2 (BSTHP). |
| 0x22 | APM0LOAD | [7:0] | DATA | R | 0x00 | APM data 0 (LOAD). |
| 0x23 | APM1LOAD | [7:0] | DATA | R | 0x00 | APM data 1 (LOAD). |
| 0x24 | APM2LOAD | [7:0] | DATA | R | 0x00 | APM data 2 (LOAD). |
| 0x25 | APM0CHG5V | [7:0] | DATA | R | 0x00 | APM data 0 (CHG5V). |
| 0x26 | APM1CHG5V | [7:0] | DATA | R | 0x00 | APM data 1 (CHG5V). |
| 0x27 | APMERR | [0:0] | BSTLPOV | R | 0x00 | APM counter overflow BSTLP. |
| | | [1:1] | BSTLPNVLD | R | 0x00 | APM counter corrupted BSTLP. |
| | | [2:2] | BSTHPOV | R | 0x00 | APM counter overflow BSTHP. |
| | | [3:3] | - | R | - | Reserved. |
| | | [4:4] | LOADOV | R | 0x00 | APM counter overflow LOAD. |
| | | [5:5] | LOADNVLD | R | 0x00 | APM counter corrupted LOAD. |
| | | [6:6] | CHG5VLIM | R | 0x00 | 5 V charger current limited due to overdischarged storage element. |
| 0x28 | TEMP | [7:0] | DATA | R | 0x00 | Temperature monitoring value. |
| 0x29 | STO | [7:0] | DATA | R | 0x00 | STO monitoring value. |
| 0x2A | SRC | [7:0] | DATA | R | 0x00 | SRC monitoring value. |
| ... | RSVD | - | - | R | - | Reserved. |
| 0xE0 | PN0 | [7:0] | DATA | R | 0x30 | Part number 0 data. |
| 0xE1 | PN1 | [7:0] | DATA | R | 0x32 | Part number 1 data. |
| 0xE2 | PN2 | [7:0] | DATA | R | 0x38 | Part number 2 data. |
| 0xE3 | PN3 | [7:0] | DATA | R | 0x35 | Part number 3 data. |
| 0xE4 | PN4 | [7:0] | DATA | R | 0x31 | Part number 4 data. |

Table 20: Register map (part 3)

*NOTE: Reserved registers marked as "write-ignore" can safely be written with any value and has no effect on the AEM15820 behavior, allowing the user to write all the registers at once.*

# 9. Registers Configuration

## 9.1. I²C Control (CTRL)

The CTRL register allows for updating the AEM15820 configurations and checking registers synchronization status.

| CTRL register | 0x17 | R/W | |
|---|---|---|---|
| Bit [7:3] | Bit [2] | Bit [1] | Bit [0] |
| RESERVED | SYNCBUSY | RESERVED | UPDATE |
| 0x00 | 0x00 | 0x00 | 0x00 |

Table 21: CTRL register

**Bit [2]: system registers synchronization (CTRL.SYNCBUSY)**

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not.

- 0: CTRL register not synchronizing.
- 1: CTRL register synchronizing.

**Bit [0]: system registers update (CTRL.UPDATE)**

This field is used to control the source of the AEM15820 configurations (GPIO or I²C) and to update the configurations with the current I²C register values or GPIO states.

- 0: GPIO
  - W: load configurations from the GPIO.
  - R: configurations from the GPIO is currently used if read as 0.
- 1: I2C
  - W: load configurations from the I²C registers.
  - R: configurations from the I²C registers is currently used if read as 1.

*NOTE: if the AEM15820 is already configured through the I²C registers, writing any register does not have any effect until 1 is written to the CTRL.UPDATE field, leading to the AEM15820 to read the new register values and apply them.*

*NOTE: when using I²C register configuration, the user can switch back to GPIO configuration by writing 0 to the CTRL.UPDATE field. In that case, the settings previously written to the IRQEN registers are still valid even when using GPIO configuration, as well as the data in IRQFLG register.*

## 9.2. Version Register (VERSION)

The VERSION register holds the version of the AEM15820.

| VERSION register | 0x00 | R |
|---|---|---|
| Bit [7:0] | | |
| VERSION | | |
| - | | |

Table 22: VERSION register

**Bit [7:0]: version number (VERSION.VERSION)**

## 9.3. Source Regulation (SRCREGUx)

The SRCREGUx registers allow the configuration of the SRC regulation mechanism.

Table 23 shows the use of SRCREGUx registers according to the source regulation mode.

- **SRCREGU0.MODE = 0**: constant voltage regulation mode, as described in Section 9.3.3.
  - LVL [7:0] - defines the constant regulation voltage.
- **SRCREGU0.MODE = 1**: MPPT ratio regulation mode, as described in Section 9.3.4.
  - MPPT_RATIO [2:0] - defines the MPPT ratio.
  - MPPT_WAIT [2:0] - defines the MPPT wait time.
  - MPPT_PERIOD [2:0] - defines the MPPT period.

| | SRCREGU1 | | | | | | | | SRCREGU0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| **Register Field** | | | CFG2 | | | CFG1 | | | | | | | CFG0 | | | MODE |
| **Mode 0: Constant Voltage** | | | | LVL[7:6] | | LVL[5:3] | | | | | | | LVL [2:0] | | | MODE |
| **Mode 1: MPPT** | | | MPPT_PERIOD [2:0] | | | MPPT_WAIT [2:0] | | | | | | | MPPT_RATIO [2:0] | | | MODE |

Table 23: Summary of SRCREGUx register fields

### 9.3.1. SRCREGU0

The SRCREGU0 is the first register for configuring the SRC regulation mechanism.

| SRCREGU0 register | 0x01 | R/W |
|---|---|---|
| Bit [7:4] | Bit [3:1] | Bit [0] |
| RESERVED | CFG0 | MODE |
| 0x00 | Reserved | 0x01 |

Table 24: SRCREGU0 register

**Bit [3:1]: SRC configuration 0 (SRCREGU0.CFG0)**

This fields is used to configure the following SRC regulation mechanism parameters:

- **If MODE = 0:** SRCREGU0.CFG0 configures the SRC regulation constant voltage, along with the other SRCREGU1.CFGx register fields (see Section 9.3.3).
- **If MODE = 1:** SRCREGU0.CFG0 configures the MPPT ratio (see Table 27).

**CAUTION: SRCREGU0.CFG0 default value is reserved and cannot be used. This field must be configured by the user.**

**Bit [0]: SRC regulation mode (SRCREGU0.MODE)**

This fields is used to configure the SRC regulation mode:

- 0: constant voltage regulation mode.
- 1: MPPT ratio ($V_{MPP}/V_{OC}$) regulation mode.

### 9.3.2. SRCREGU1

The SRCREGU1 is the second register for configuring the SRC regulation mechanism.

| | SRCREGU1 register | | | 0x02 | | R/W |
|---|---|---|---|---|---|---|
| | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2:0] |
| **Mode 0: Constant Voltage** | RESERVED | | | CFG2 | | CFG1 |
| | 0x00 | | | 0x00 | | 0x00 |
| **Mode 1: MPPT** | RESERVED | CFG2 | | | | CFG1 |
| | 0x00 | 0x00 | | | | 0x00 |

Table 25: SRCREGU1 register

**Bit [5:3]: SRC configuration 2 (SRCREGU1.CFG2)**

This fields is used to configure the following SRC regulation mechanism parameters:

- **If MODE = 0:** SRCREGU1.CFG2 configures the SRC constant regulation voltage, along with the other SRCREGUx.CFGx register fields (see Section 9.3.3).
- **If MODE = 1:** SRCREGU1.CFG2 configures the SRC MPPT period $T_{MPPT,PERIOD}$ (see Table 29).

*NOTE: When SRCREGU0.MODE = 0 (constant voltage mode) the SRCREGU1.CFG2 field uses bits [4:3] of the SRCREGU1 register, instead of bits [5:3] when MODE = 1 as shown in Table 25.*

**Bit [2:0]: SRC configuration 1 (SRCREGU1.CFG1)**

This fields is used to configure the following SRC regulation mechanism parameters:

- **If MODE = 0:** SRCREGU1.CFG1 configures the SRC constant regulation voltage, along with the other SRCREGUx.CFGx register fields (see Section 9.3.3).
- **If MODE = 1:** SRCREGU1.CFG1 configures the SRC MPPT wait time $T_{MPPT,WAIT}$ (see Table 28).

### 9.3.3. Constant Voltage Configuration

Table 26 describes how to configure SRCREGUx registers when the AEM15820 source regulation mode is set to constant voltage (SRCREGU0.MODE = 0).

See Table 23 for a description of how LVL[7:0] is distributed across SRCREGUx registers.

**CAUTION: The source regulation target voltage ($V_{SRC,REG}$) must never be configured below half of the source's open-circuit voltage ($V_{OC}$/2).**

**CAUTION: Do not reduce the source regulation target voltage ($V_{SRC,REG}$) on-the-fly by more than a factor of 2 while the boost converters are enabled. If such change is required, the boost converters must be disabled before updating the configuration.**

| LVL [7:0] | $V_{SRC,REG}$ [V] | LVL [7:0] | $V_{SRC,REG}$ [V] | LVL [7:0] | $V_{SRC,REG}$ [V] | LVL [7:0] | $V_{SRC,REG}$ [V] | LVL [7:0] | $V_{SRC,REG}$ [V] | LVL [7:0] | $V_{SRC,REG}$ [V] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Source Low[1] | 0x3C | 0.645 | 0x59 | 1.080 | 0x76 | 1.522 | 0x93 | 2.172 | 0xB0 | 3.455 |
| ... | | 0x3D | 0.660 | 0x5A | 1.095 | 0x77 | 1.545 | 0x94 | 2.194 | 0xB1 | 3.500 |
| 0x0C | | 0x3E | 0.675 | 0x5B | 1.110 | 0x78 | 1.567 | 0x95 | 2.227 | 0xB2 | 3.545 |
| 0x0D | Reserved[2] | 0x3F | 0.690 | 0x5C | 1.125 | 0x79 | 1.590 | 0x96 | 2.273 | 0xB3 | 3.591 |
| ... | | 0x40 | 0.705 | 0x5D | 1.140 | 0x7A | 1.612 | 0x97 | 2.318 | 0xB4 | 3.636 |
| 0x24 | | 0x41 | 0.720 | 0x5E | 1.155 | 0x7B | 1.634 | 0x98 | 2.364 | 0xB5 | 3.682 |
| 0x25 | 0.300 | 0x42 | 0.735 | 0x5F | 1.170 | 0x7C | 1.657 | 0x99 | 2.409 | 0xB6 | 3.727 |
| 0x26 | 0.315 | 0x43 | 0.750 | 0x60 | 1.185 | 0x7D | 1.679 | 0x9A | 2.455 | 0xB7 | 3.773 |
| 0x27 | 0.330 | 0x44 | 0.765 | 0x61 | 1.200 | 0x7E | 1.701 | 0x9B | 2.500 | 0xB8 | 3.818 |
| 0x28 | 0.345 | 0x45 | 0.780 | 0x62 | 1.215 | 0x7F | 1.724 | 0x9C | 2.545 | 0xB9 | 3.864 |
| 0x29 | 0.360 | 0x46 | 0.795 | 0x63 | 1.230 | 0x80 | 1.746 | 0x9D | 2.591 | 0xBA | 3.909 |
| 0x2A | 0.375 | 0x47 | 0.810 | 0x64 | 1.245 | 0x81 | 1.769 | 0x9E | 2.636 | 0xBB | 3.955 |
| 0x2B | 0.390 | 0x48 | 0.825 | 0x65 | 1.260 | 0x82 | 1.791 | 0x9F | 2.682 | 0xBC | 4.000 |
| 0x2C | 0.405 | 0x49 | 0.840 | 0x66 | 1.275 | 0x83 | 1.813 | 0xA0 | 2.727 | 0xBD | 4.045 |
| 0x2D | 0.420 | 0x4A | 0.855 | 0x67 | 1.290 | 0x84 | 1.836 | 0xA1 | 2.773 | 0xBE | 4.091 |
| 0x2E | 0.435 | 0x4B | 0.870 | 0x68 | 1.305 | 0x85 | 1.858 | 0xA2 | 2.818 | 0xBF | 4.136 |
| 0x2F | 0.450 | 0x4C | 0.885 | 0x69 | 1.320 | 0x86 | 1.881 | 0xA3 | 2.864 | 0xC0 | 4.182 |
| 0x30 | 0.465 | 0x4D | 0.900 | 0x6A | 1.335 | 0x87 | 1.903 | 0xA4 | 2.909 | 0xC1 | 4.227 |
| 0x31 | 0.480 | 0x4E | 0.915 | 0x6B | 1.350 | 0x88 | 1.925 | 0xA5 | 2.955 | 0xC2 | 4.273 |
| 0x32 | 0.495 | 0x4F | 0.930 | 0x6C | 1.365 | 0x89 | 1.948 | 0xA6 | 3.000 | 0xC3 | 4.318 |
| 0x33 | 0.510 | 0x50 | 0.945 | 0x6D | 1.380 | 0x8A | 1.970 | 0xA7 | 3.045 | 0xC4 | Reserved[2] |
| 0x34 | 0.525 | 0x51 | 0.960 | 0x6E | 1.395 | 0x8B | 1.993 | 0xA8 | 3.091 | ... | |
| 0x35 | 0.540 | 0x52 | 0.975 | 0x6F | 1.410 | 0x8C | 2.015 | 0xA9 | 3.136 | 0xFF | |
| 0x36 | 0.555 | 0x53 | 0.990 | 0x70 | 1.425 | 0x8D | 2.037 | 0xAA | 3.182 | | |
| 0x37 | 0.570 | 0x54 | 1.005 | 0x71 | 1.440 | 0x8E | 2.060 | 0xAB | 3.227 | | |
| 0x38 | 0.585 | 0x55 | 1.020 | 0x72 | 1.455 | 0x8F | 2.082 | 0xAC | 3.273 | | |
| 0x39 | 0.600 | 0x56 | 1.035 | 0x73 | 1.470 | 0x90 | 2.104 | 0xAD | 3.318 | | |
| 0x3A | 0.615 | 0x57 | 1.050 | 0x74 | 1.478 | 0x91 | 2.127 | 0xAE | 3.364 | | |
| 0x3B | 0.630 | 0x58 | 1.065 | 0x75 | 1.500 | 0x92 | 2.149 | 0xAF | 3.409 | | |

Table 26: SRC constant voltage values configured by SRCREGUx (SRCREGU0.MODE = 0)

*1. Setting SRCREGUx.LVL lower or equal to 0x0C causes the AEM15820 to consider the SRC voltage to be lower than $V_{SRCLOW}$, regardless of the SRCLOW register value, which causes the AEM15820 to enter SLEEP STATE.*

*2. Those reserved configurations must not be used.*

### 9.3.4. MPPT Configuration

This section describes how to configure the MPPT module through the SRCREGUx registers when the AEM15820 source regulation mode is set to MPPT ratio (SRCREGU0.MODE = 1).

See Table 23 for the distribution of MPPT_RATIO [2:0], MPPT_WAIT [2:0], MPPT_PERIOD [2:0] values across SRCREGUx registers.

- Table 27 shows the configuration of SRCREGU0.CFG0 register field to set the MPPT ratio.
- Table 28 shows the configuration of SRCREGU1.CFG1 register field to set the MPPT wait time before open-circuit voltage measure.
- Table 29 shows the configuration of SRCREGU1.CFG2 register field to set the MPPT period.

| SRCREGU0.CFG0 MPPT_RATIO [2:0] | | | $R_{MPPT}$ |
|---|---|---|---|
| 0 | 0 | 0 | Reserved[1] |
| 0 | 0 | 1 | 50 % |
| 0 | 1 | 0 | 65 % |
| 0 | 1 | 1 | 70 % |
| 1 | 0 | 0 | 75 % |
| 1 | 0 | 1 | 80 % |
| 1 | 1 | 0 | 85 % |
| 1 | 1 | 1 | Reserved[1] |

Table 27: SRC MPPT ratio configured by SRCREGUx (SRCREGU0.MODE = 1)

*1. Those reserved configurations must not be used.*

| SRCREGU1.CFG1 MPPT_WAIT [2:0] | | | $T_{MPPT,WAIT}$[1] [ms] |
|---|---|---|---|
| 0 | 0 | 0 | 1.8 |
| 0 | 0 | 1 | 3.6 |
| 0 | 1 | 0 | 7.3 |
| 0 | 1 | 1 | 15 |
| 1 | 0 | 0 | 29 |
| 1 | 0 | 1 | 116 |
| 1 | 1 | 0 | 233 |
| 1 | 1 | 1 | 465 |

Table 28: SRC MPPT wait time configured by SRCREGUx (SRCREGU0.MODE = 1)

*1. The total time spent in open-circuit is the sum of $T_{MPPT,WAIT}$ (configurable, see table above) and $T_{MPPT,MEASURE}$ (fixed, see Table 8).*

| SRCREGU1.CFG2 MPPT_PERIOD [2:0] | | | $T_{MPPT,PERIOD}$ [ms] |
|---|---|---|---|
| 0 | 0 | 0 | 116[1] |
| 0 | 0 | 1 | 233 |
| 0 | 1 | 0 | 465 |
| 0 | 1 | 1 | 931 |
| 1 | 0 | 0 | 1862 |
| 1 | 0 | 1 | 3724 |
| 1 | 1 | 0 | 7447 |
| 1 | 1 | 1 | 14895 |

Table 29: SRC MPPT period configured by SRCREGUx (SRCREGU0.MODE = 1)

*1. If $T_{MPPT,PERIOD}$ is set to 116 ms for the SRC, the APM WINDOW will automatically be set to 116 ms by the AEM15820 for all the APM modules.*

**CAUTION: When using the source MPPT ratio mode, the source low threshold must be configured through I²C to a value higher or equal to 300 mV. See SRCLOW register in Section 9.4.**

## 9.4. Source Low Threshold (SRCLOW)

The SRCLOW register allows the configuration of the SRC voltage threshold ($V_{SRCLOW}$) below which the AEM15820 switches to SLEEP STATE. When $V_{MPP}$ is higher than $V_{SRCLOW}$, the source is considered available.

*NOTE: The source low threshold is mainly useful in MPPT ratio mode. When using the constant voltage mode, leave the SRCLOW register at its default value unless forcing the reset state is desired.*

| SRCLOW register | 0x12 | R/W |
|---|---|---|
| Bit [7:3] | | Bit [2:0] |
| RESERVED | | SRCTHRESH |
| 0x00 | | Reserved |

Table 30: SRCLOW register

**Bit [2:0]: source low threshold (SRCLOW.SRCTHRESH)**

This field allows the configuration of the $V_{SRCLOW}$ threshold of the SRC.

Table 31 shows the threshold voltages $V_{SRCLOW}$ according to the configuration of SRCLOW.SRCTHRESH fields.

**CAUTION: SRCLOW.SRCTHRESH default value is reserved and must be overwritten by the user to a non-reserved value when using the source MPPT ratio mode. When using the source constant voltage mode, the default (reserved) value is acceptable and has no impact on the AEM15820 behavior.**

| SRCLOW. SRCTHRESH | Source low voltage threshold $V_{SRCLOW}$ [V] |
|---|---|
| 0x00 | Reserved |
| 0x01 | |
| 0x02 | |
| 0x03 | 0.300 |
| 0x04 | 0.360 |
| 0x05 | 0.405 |
| 0x06 | 0.510 |
| 0x07 | 0.600 |

Table 31: $V_{SRCLOW}$ thresholds as configured by SRCLOW register

## 9.5. Storage Element Threshold Voltages (VOVDIS / VCHRDY / VCHRDYBUCK / VOVCH)

The storage element protection thresholds, described in Section 6.4, can be set independently by the registers VOVDIS, VCHRDY, VCHRDYBUCK and VOVCH.

### 9.5.1. Overdischarge Voltage (VOVDIS)

The VOVDIS register allows the configuration of the storage element voltage below which the storage element is considered to be fully depleted, and must not be discharged any further ($V_{OVDIS}$).

| VOVDIS register | 0x05 | R/W |
|---|---|---|
| Bit [7:6] | Bit [5:0] | |
| RESERVED | THRESH | |
| 0x00 | 0x06 | |

Table 32: VOVDIS register

**Bit [5:0]: storage element overdischarge threshold (VOVDIS.THRESH)**

This field allows the configuration of $V_{OVDIS}$ based on Table 33 values or based on the following formula:

$$V_{OVDIS} = 2.400 + \text{THRESH} \cdot 0.01875$$

*NOTE: Respect $V_{OVDIS} < V_{CHRDY} < V_{OVCH}$ and keep a 100 mV minimum margin between them to avoid false state transitions.*

| VOVDIS. THRESH | $V_{OVDIS}$ [V] | VOVDIS. THRESH | $V_{OVDIS}$ [V] | VOVDIS. THRESH | $V_{OVDIS}$ [V] | VOVDIS. THRESH | $V_{OVDIS}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 2.400 | 0x10 | 2.700 | 0x20 | 3.000 | 0x30 | 3.300 |
| 0x01 | 2.419 | 0x11 | 2.719 | 0x21 | 3.019 | 0x31 | 3.319 |
| 0x02 | 2.438 | 0x12 | 2.738 | 0x22 | 3.038 | 0x32 | 3.338 |
| 0x03 | 2.456 | 0x13 | 2.756 | 0x23 | 3.056 | 0x33 | 3.356 |
| 0x04 | 2.475 | 0x14 | 2.775 | 0x24 | 3.075 | 0x34 | 3.375 |
| 0x05 | 2.494 | 0x15 | 2.794 | 0x25 | 3.094 | 0x35 | 3.394 |
| 0x06 | 2.513 | 0x16 | 2.813 | 0x26 | 3.113 | 0x36 | 3.413 |
| 0x07 | 2.531 | 0x17 | 2.831 | 0x27 | 3.131 | 0x37 | 3.431 |
| 0x08 | 2.550 | 0x18 | 2.850 | 0x28 | 3.150 | 0x38 | 3.450 |
| 0x09 | 2.569 | 0x19 | 2.869 | 0x29 | 3.169 | 0x39 | 3.469 |
| 0x0A | 2.588 | 0x1A | 2.888 | 0x2A | 3.188 | 0x3A | 3.488 |
| 0x0B | 2.606 | 0x1B | 2.906 | 0x2B | 3.206 | 0x3B | 3.506 |
| 0x0C | 2.625 | 0x1C | 2.925 | 0x2C | 3.225 | 0x3C | 3.525 |
| 0x0D | 2.644 | 0x1D | 2.944 | 0x2D | 3.244 | 0x3D | 3.544 |
| 0x0E | 2.663 | 0x1E | 2.963 | 0x2E | 3.263 | 0x3E | 3.563 |
| 0x0F | 2.681 | 0x1F | 2.981 | 0x2F | 3.281 | 0x3F | 3.581 |

Table 33: Storage element $V_{OVDIS}$ configuration by VOVDIS register

### 9.5.2. Charge Ready Voltage (VCHRDY)

The VCHRDY register allows the configuration of the storage element voltage required to switch to SUPPLY STATE ($V_{CHRDY}$).

| VCHRDY register | 0x06 | R/W |
|---|---|---|
| Bit [7] | Bit [6:0] | |
| RESERVED | THRESH | |
| 0x00 | 0x05 | |

Table 34: VCHRDY register

**Bit [6:0]: storage element charge ready threshold (VCHRDY.THRESH)**

This field allows the configuration of $V_{CHRDY}$ based on Table 35 values or based on the following formula:

$$V_{CHRDY} = 2.456 + \text{THRESH} \cdot 0.01875$$

*NOTE: Respect $V_{OVDIS}$ < $V_{CHRDY}$ < $V_{OVCH}$ and keep a 100 mV minimum margin between them to avoid false state transitions.*

| VCHRDY. THRESH | $V_{CHRDY}$ [V] | VCHRDY. THRESH | $V_{CHRDY}$ [V] | VCHRDY. THRESH | $V_{CHRDY}$ [V] | VCHRDY. THRESH | $V_{CHRDY}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 2.456 | 0x19 | 2.925 | 0x32 | 3.394 | 0x4B | 3.862 |
| 0x01 | 2.475 | 0x1A | 2.944 | 0x33 | 3.413 | 0x4C | 3.881 |
| 0x02 | 2.494 | 0x1B | 2.963 | 0x34 | 3.431 | 0x4D | 3.900 |
| 0x03 | 2.513 | 0x1C | 2.981 | 0x35 | 3.450 | 0x4E | 3.918 |
| 0x04 | 2.531 | 0x1D | 3.000 | 0x36 | 3.469 | 0x4F | 3.937 |
| 0x05 | 2.550 | 0x1E | 3.019 | 0x37 | 3.488 | 0x50 | 3.956 |
| 0x06 | 2.569 | 0x1F | 3.038 | 0x38 | 3.506 | 0x51 | 3.975 |
| 0x07 | 2.588 | 0x20 | 3.056 | 0x39 | 3.525 | 0x52 | 3.993 |
| 0x08 | 2.606 | 0x21 | 3.075 | 0x3A | 3.544 | 0x53 | 4.012 |
| 0x09 | 2.625 | 0x22 | 3.094 | 0x3B | 3.563 | 0x54 | 4.031 |
| 0x0A | 2.644 | 0x23 | 3.113 | 0x3C | 3.581 | 0x55 | 4.050 |
| 0x0B | 2.663 | 0x24 | 3.131 | 0x3D | 3.600 | 0x56 | 4.068 |
| 0x0C | 2.681 | 0x25 | 3.150 | 0x3E | 3.619 | 0x57 | 4.087 |
| 0x0D | 2.700 | 0x26 | 3.169 | 0x3F | 3.638 | 0x58 | 4.106 |
| 0x0E | 2.719 | 0x27 | 3.188 | 0x40 | 3.656 | 0x59 | 4.125 |
| 0x0F | 2.738 | 0x28 | 3.206 | 0x41 | 3.675 | 0x5A | 4.143 |
| 0x10 | 2.756 | 0x29 | 3.225 | 0x42 | 3.693 | 0x5B | 4.162 |
| 0x11 | 2.775 | 0x2A | 3.244 | 0x43 | 3.712 | 0x5C | 4.181 |
| 0x12 | 2.794 | 0x2B | 3.263 | 0x44 | 3.731 | 0x5D | 4.200 |
| 0x13 | 2.813 | 0x2C | 3.281 | 0x45 | 3.750 | 0x5E | 4.218 |
| 0x14 | 2.831 | 0x2D | 3.300 | 0x46 | 3.768 | 0x5F | 4.237 |
| 0x15 | 2.850 | 0x2E | 3.319 | 0x47 | 3.787 | 0x60 | 4.256 |
| 0x16 | 2.869 | 0x2F | 3.338 | 0x48 | 3.806 | 0x61 | 4.275 |
| 0x17 | 2.888 | 0x30 | 3.356 | 0x49 | 3.825 | 0x62 | 4.293 |
| 0x18 | 2.906 | 0x31 | 3.375 | 0x4A | 3.843 | 0x63 | 4.312 |

Table 35: Storage element $V_{CHRDY}$ configuration by VCHRDY register

### 9.5.3. Buck Charge Ready Voltage (VCHRDYBUCK)

The VCHRDYBUCK register allows the configuration of the storage element voltage ($V_{CHRDY,BUCK}$) at which the buck converter can be enabled when the 5 V charger is not used (see Section 5.3).

| VCHRDYBUCK register | 0x0B | R/W |
|---|---|---|
| Bit [7] | Bit [6:0] | |
| RESERVED | THRESH | |
| 0x00 | 0x05 | |

Table 36: VCHRDYBUCK register

**Bit [6:0]: storage element buck charge ready threshold (VCHRDYBUCK.THRESH)**

This field allows the configuration of the storage element buck charge ready threshold. This voltage threshold is then used to check if the buck converter can be enabled or if the storage element voltage is still too low.

The buck charge ready voltage can be determined based on Table 37 or on the following formula:

$$V_{CHRDY,BUCK} = 2.456 + \text{THRESH} \cdot 0.01875$$

| VCHRDYBUCK.THRESH | $V_{CHRDY,BUCK}$ [V] | VCHRDYBUCK.THRESH | $V_{CHRDY,BUCK}$ [V] | VCHRDYBUCK.THRESH | $V_{CHRDY,BUCK}$ [V] | VCHRDYBUCK.THRESH | $V_{CHRDY,BUCK}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 2.456 | 0x19 | 2.925 | 0x32 | 3.394 | 0x4B | 3.862 |
| 0x01 | 2.475 | 0x1A | 2.944 | 0x33 | 3.413 | 0x4C | 3.881 |
| 0x02 | 2.494 | 0x1B | 2.963 | 0x34 | 3.431 | 0x4D | 3.900 |
| 0x03 | 2.513 | 0x1C | 2.981 | 0x35 | 3.450 | 0x4E | 3.918 |
| 0x04 | 2.531 | 0x1D | 3.000 | 0x36 | 3.469 | 0x4F | 3.937 |
| 0x05 | 2.550 | 0x1E | 3.019 | 0x37 | 3.488 | 0x50 | 3.956 |
| 0x06 | 2.569 | 0x1F | 3.038 | 0x38 | 3.506 | 0x51 | 3.975 |
| 0x07 | 2.588 | 0x20 | 3.056 | 0x39 | 3.525 | 0x52 | 3.993 |
| 0x08 | 2.606 | 0x21 | 3.075 | 0x3A | 3.544 | 0x53 | 4.012 |
| 0x09 | 2.625 | 0x22 | 3.094 | 0x3B | 3.563 | 0x54 | 4.031 |
| 0x0A | 2.644 | 0x23 | 3.113 | 0x3C | 3.581 | 0x55 | 4.050 |
| 0x0B | 2.663 | 0x24 | 3.131 | 0x3D | 3.600 | 0x56 | 4.068 |
| 0x0C | 2.681 | 0x25 | 3.150 | 0x3E | 3.619 | 0x57 | 4.087 |
| 0x0D | 2.700 | 0x26 | 3.169 | 0x3F | 3.638 | 0x58 | 4.106 |
| 0x0E | 2.719 | 0x27 | 3.188 | 0x40 | 3.656 | 0x59 | 4.125 |
| 0x0F | 2.738 | 0x28 | 3.206 | 0x41 | 3.675 | 0x5A | 4.143 |
| 0x10 | 2.756 | 0x29 | 3.225 | 0x42 | 3.693 | 0x5B | 4.162 |
| 0x11 | 2.775 | 0x2A | 3.244 | 0x43 | 3.712 | 0x5C | 4.181 |
| 0x12 | 2.794 | 0x2B | 3.263 | 0x44 | 3.731 | 0x5D | 4.200 |
| 0x13 | 2.813 | 0x2C | 3.281 | 0x45 | 3.750 | 0x5E | 4.218 |
| 0x14 | 2.831 | 0x2D | 3.300 | 0x46 | 3.768 | 0x5F | 4.237 |
| 0x15 | 2.850 | 0x2E | 3.319 | 0x47 | 3.787 | 0x60 | 4.256 |
| 0x16 | 2.869 | 0x2F | 3.338 | 0x48 | 3.806 | 0x61 | 4.275 |
| 0x17 | 2.888 | 0x30 | 3.356 | 0x49 | 3.825 | 0x62 | 4.293 |
| 0x18 | 2.906 | 0x31 | 3.375 | 0x4A | 3.843 | 0x63 | 4.312 |

Table 37: Storage element $V_{CHRDY,BUCK}$ configuration by VCHRDYBUCK register

### 9.5.4. Overcharge Voltage (VOVCH)

The VOVCH register allows the configuration of the storage element maximum voltage before disabling its charging ($V_{OVCH}$).

| VOVCH register | 0x07 | R/W |
|---|---|---|
| Bit [7] | Bit [6:0] | |
| RESERVED | THRESH | |
| 0x00 | 0x3A | |

Table 38: VOVCH register

**Bit [6:0]: storage element overcharge threshold (VOVCH.THRESH)**

This field allows the configuration of $V_{OVCH}$ based on Table 39 values or based on the following:

- 0x00 ≤ VOVCH.THRESH ≤ 0x65:

  $V_{OVCH} = 2.700 + THRESH \cdot 0.01875$

- VOVCH.THRESH ≥ 0x66:

  $V_{OVCH} = 4.594V$

*NOTE: Respect $V_{OVDIS} < V_{CHRDY} < V_{OVCH}$ and keep a 100 mV minimum margin between them to avoid false state transitions.*

| VOVCH. THRESH | $V_{OVCH}$ [V] | VOVCH. THRESH | $V_{OVCH}$ [V] | VOVCH. THRESH | $V_{OVCH}$ [V] | VOVCH. THRESH | $V_{OVCH}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 2.700 | 0x1B | 3.206 | 0x36 | 3.713 | 0x51 | 4.219 |
| 0x01 | 2.719 | 0x1C | 3.225 | 0x37 | 3.731 | 0x52 | 4.238 |
| 0x02 | 2.738 | 0x1D | 3.244 | 0x38 | 3.750 | 0x53 | 4.256 |
| 0x03 | 2.756 | 0x1E | 3.263 | 0x39 | 3.769 | 0x54 | 4.275 |
| 0x04 | 2.775 | 0x1F | 3.281 | 0x3A | 3.788 | 0x55 | 4.294 |
| 0x05 | 2.794 | 0x20 | 3.300 | 0x3B | 3.806 | 0x56 | 4.313 |
| 0x06 | 2.813 | 0x21 | 3.319 | 0x3C | 3.825 | 0x57 | 4.331 |
| 0x07 | 2.831 | 0x22 | 3.338 | 0x3D | 3.844 | 0x58 | 4.350 |
| 0x08 | 2.850 | 0x23 | 3.356 | 0x3E | 3.863 | 0x59 | 4.369 |
| 0x09 | 2.869 | 0x24 | 3.375 | 0x3F | 3.881 | 0x5A | 4.388 |
| 0x0A | 2.888 | 0x25 | 3.394 | 0x40 | 3.900 | 0x5B | 4.406 |
| 0x0B | 2.906 | 0x26 | 3.413 | 0x41 | 3.919 | 0x5C | 4.425 |
| 0x0C | 2.925 | 0x27 | 3.431 | 0x42 | 3.938 | 0x5D | 4.444 |
| 0x0D | 2.944 | 0x28 | 3.450 | 0x43 | 3.956 | 0x5E | 4.463 |
| 0x0E | 2.963 | 0x29 | 3.469 | 0x44 | 3.975 | 0x5F | 4.481 |
| 0x0F | 2.981 | 0x2A | 3.488 | 0x45 | 3.994 | 0x60 | 4.500 |
| 0x10 | 3.000 | 0x2B | 3.506 | 0x46 | 4.013 | 0x61 | 4.519 |
| 0x11 | 3.019 | 0x2C | 3.525 | 0x47 | 4.031 | 0x62 | 4.538 |
| 0x12 | 3.038 | 0x2D | 3.544 | 0x48 | 4.050 | 0x63 | 4.556 |
| 0x13 | 3.056 | 0x2E | 3.563 | 0x49 | 4.069 | 0x64 | 4.575 |
| 0x14 | 3.075 | 0x2F | 3.581 | 0x4A | 4.088 | 0x65 | 4.594 |
| 0x15 | 3.094 | 0x30 | 3.600 | 0x4B | 4.106 | ... | |
| 0x16 | 3.113 | 0x31 | 3.619 | 0x4C | 4.125 | 0x7F | |
| 0x17 | 3.131 | 0x32 | 3.638 | 0x4D | 4.144 | | |
| 0x18 | 3.150 | 0x33 | 3.656 | 0x4E | 4.163 | | |
| 0x19 | 3.169 | 0x34 | 3.675 | 0x4F | 4.181 | | |
| 0x1A | 3.188 | 0x35 | 3.694 | 0x50 | 4.200 | | |

Table 39: Storage element $V_{OVCH}$ configuration by VOVCH register

## 9.6. Boost Converters (BSTLPCFG and BSTHPCFG)

The BSTLPCFG and BSTHPCFG registers allow the configuration of the boost converters.

| **BSTLPCFG register** **BSTHPCFG register** | **0x08** **0x09** | **R/W** **R/W** | |
|---|---|---|---|
| Bit [7:5] | Bit [4:2] | Bit [1] | Bit [0] |
| RESERVED | TMULT | RESERVED | EN |
| 0x00 | 0x01 | 0x01 | 0x01 |

Table 40: BSTLPCFG and BSTHPCFG registers

**Bit [4:2]: boost converter timing multiplier (BSTLPCFG.TMULT / BSTHPCFG.TMULT)**

This field allows the modification of the peak current of each boost inductor by increasing/decreasing the on/off timings of the corresponding boost converter. The higher the timing multiplier, the higher the boost inductor peak current, and thus the higher the average source current pulled from SRC to STO.

The peak current in the inductor also depends on the value of the inductor (see Table 41).

**Bit [1]: reserved (write-ignore)**

This field is reserved. It can safely be written with any value and has no effect on the AEM15820.

**Bit [0]: boost converter enable (BSTLPCFG.EN / BSTHPCFG.EN)**

This field allows enabling or disabling each boost converter.

- 0: disable the boost converter.
- 1: enable the boost converter.

**CAUTION: the high-power boost can be enabled or disabled at any time (BSTHPCFG.EN). However, the low-power boost (BSTLPCFG.EN) must not be disabled unless the external boost is also disabled. Always ensure the high-power boost is disabled when disabling the low-power one.**

| **BSTLPCFG/ BSTHPCFG. TMULT** | **Timing Multiplier** | **Minimum[1] $L_{BOOST\_LP}$ [µH]** | **Recommended[2] $L_{BOOST\_LP}$ [µH]** |
|---|---|---|---|
| 0x00 | x1 | 3.3 | 10 |
| 0x01 | x2 | 6.6 | 15 |
| 0x02 | x3 | 9.9 | 33 |
| 0x03 | x4 | 13.2 | 47 |
| 0x04 | x6 | 19.8 | 68 |
| 0x05 | x8 | 26.4 | 100 |
| 0x06 | x12 | 39.6 | 120 |
| 0x07 | x16 | 52.8 | 180 |

Table 41: Timing multiplier configured by TMULT field with corresponding low-power boost inductor value

*1. Never install a low-power boost inductor with an inductance (effective value including tolerance, derating, etc.) lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM15820.*
*2. Those values provide the best efficiency/current capability trade-off for the low-power boost converter according to the tests carried out in the e-peas laboratory.*

*NOTE: The inductor values in Table 41 apply only to $L_{BOOST\_LP}$. For $L_{BOOST\_HP}$, the limitations depend on the high-power boost external components.*

## 9.7. Buck Converter (BUCKCFG)

The BUCK register allows the configuration of the buck converter, which output is the LOAD pin.

*NOTE: the configuration of the BUCKCFG.VLOAD field must not be set to "OFF" (0x00 or any value above 0x0A) if the buck converter was previously enabled, whether it was through the LOAD_CFG[2:0] pins or using the BUCKCFG register.*

| BUCKCFG register | | 0x0A | R/W |
|---|---|---|---|
| Bit [7] | Bit [6:4] | Bit [3:0] | |
| RESERVED | TMULT | VLOAD | |
| 0x00 | 0x03[1] | 0x00 | |

Table 42: BUCKCFG register

*1. The buck converter timing multiplier default value is different depending on whether the AEM15820 is configured by I²C or not. See Section 6.6.2 for the default values of each configuration method.*

**Bit [6:4]: buck converter timing multiplier (BUCKCFG.TMULT)**

This field allows the modification of the peak current of the buck inductor by increasing/decreasing the on/off timings of the buck converter. The higher the timing multiplier, the higher the buck inductor peak current, and thus the higher the average current pulled from STO to LOAD.

The peak current in the inductor depends also on the value of the inductor (see Table 43).

**Bit [3:0]: buck converter output regulation voltage (BUCKCFG.VLOAD)**

This field allows the configuration of the buck converter regulation output voltage ($V_{LOAD}$). The available configurations can be found in Table 44. To switch off the buck converter, set BUCK.VLOAD to 0x00, or from 0x0B to 0x0F.

| BUCKCFG. TMULT | Timing Multiplier | Minimum[1] $L_{BUCK}$ [µH] | Recommended[2] $L_{BUCK}$ [µH] |
|---|---|---|---|
| 0x00 | x1 | 1.7 | 6.8 |
| 0x01 | x2 | 3.3 | 10 |
| 0x02 | x3 | 5.0 | 15 |
| 0x03 | x4 | 6.6 | 22 |
| 0x04 | x6 | 9.9 | 33 |
| 0x05 | x8 | 13.2 | 47 |
| 0x06 | x12 | 19.8 | 68 |
| 0x07 | x16 | 26.4 | 100 |

Table 43: Buck inductor values according to buck timing

*1. Never install an inductor with an inductance (real value including tolerance, derating, etc.) lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM15820.*
*2. Those values provide the best efficiency/current capability trade-off according to the tests carried out in the e-peas laboratory.*

| BUCKCFG.VLOAD | $V_{LOAD}$ [V] |
|---|---|
| 0x00 | OFF |
| 0x01 | 0.6 |
| 0x02 | 0.9 |
| 0x03 | 1.2 |
| 0x04 | 1.5 |
| 0x05 | 1.8 |
| 0x06 | 2.2 |
| 0x07 | 2.5 |
| 0x08 | 2.8 |
| 0x09 | 3.0 |
| 0x0A | 3.3 |
| 0x0B | OFF |
| ... | |
| 0x0F | |

Table 44: $V_{LOAD}$ settings by BUCKCFG.VLOAD register

## 9.8. 5 V Charger (CHG5V)

The CHG5V register allows the configuration of the 5 V charger (as explained in Section 5.7).

| CHG5V register | 0x0C | R/W | |
|---|---|---|---|
| Bit [7] | Bit [6:2] | Bit [1] | Bit [0] |
| RESERVED | THRESH | CVEN | EN |
| 0x00 | 0x00 | 0x00 | 0x01 |

Table 45: CHG5V register

**Bit [6:2]: 5 V charger stop voltage threshold (CHG5V.THRESH)**

This field allows the configuration of the 5 V charger stop voltage threshold ($V_{5V,STOP}$), which is the storage element voltage at which the 5 V charger will stop to charge the storage element when the constant voltage (CV) mode is enabled (see Table 46).

**Bit [1]: 5 V charger constant voltage mode enable (CHG5V.CVEN)**

This field allows enabling or disabling of the constant voltage (CV) operation mode (see Section 5.7).

- 0: disable the 5 V charger CV mode.
- 1: enable the 5 V charger CV mode.

**Bit [0]: 5 V charger enable (CHG5V.EN)**

This field allows enabling or disabling of the 5 V charger.

- 0: disable the 5 V charger.
- 1: enable the 5 V charger.

| CHG5V. THRESH | $V_{5V,STOP}$ [V] | CHG5V. THRESH | $V_{5V,STOP}$ [V] | CHG5V. THRESH | $V_{5V,STOP}$ [V] | CHG5V. THRESH | $V_{5V,STOP}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 2.65 | 0x08 | 3.35 | 0x10 | 3.75 | 0x18 | 4.15 |
| 0x01 | 2.75 | 0x09 | 3.40 | 0x11 | 3.80 | 0x19 | 4.20 |
| 0x02 | 2.85 | 0x0A | 3.45 | 0x12 | 3.85 | 0x1A | 4.25 |
| 0x03 | 2.95 | 0x0B | 3.50 | 0x13 | 3.90 | 0x1B | 4.30 |
| 0x04 | 3.05 | 0x0C | 3.55 | 0x14 | 3.95 | 0x1C | 4.40 |
| 0x05 | 3.15 | 0x0D | 3.60 | 0x15 | 4.00 | 0x1D | 4.50 |
| 0x06 | 3.25 | 0x0E | 3.65 | 0x16 | 4.05 | 0x1E | 4.60 |
| 0x07 | 3.30 | 0x0F | 3.70 | 0x17 | 4.10 | 0x1F | 4.70 |

Table 46: $V_{5V,STOP}$ configuration by CHG5V register

## 9.9. STO Charge Temperature Protection (TEMPCOLDCH and TEMPHOTCH)

Those fields are used when the thermal protection monitoring (TEMPPROTECT) is enabled (see Section 9.11) to configure the minimum (cold) and maximum (hot) temperature protection thresholds for charging the storage element connected to STO.

If the temperature is out of the charge temperature range, the boost converters will be disabled to stop charging the storage element.

THRESH value is determined as follows from the desired temperature T:

- Determine the resistance of the thermo resistor $R_{TH}$ at the desired temperature.
- Calculate THRESH using the following formula:

$$THRESH(T) = \frac{256 \cdot R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

See Section 6.7 for further information about thermal monitoring configuration.

### 9.9.1. TEMPCOLDCH

The TEMPCOLDCH register allows the configuration of the minimum temperature for storage element charging.

| TEMPCOLDCH register | 0x0D | R/W |
|---|---|---|
| Bit [7:0] | | |
| THRESH | | |
| 0xD1 | | |

Table 47: TEMPCOLDCH register

**Bit [7:0]: storage element charge minimum temperature threshold (TEMPCOLDCH.THRESH)**

This field allows the configuration of the minimum temperature (cold) threshold for storage element charging.

### 9.9.2. TEMPHOTCH

The TEMPHOTCH register allows the configuration of the maximum temperature for storage element charging.

| TEMPHOTCH register | 0x0E | R/W |
|---|---|---|
| Bit [7:0] | | |
| THRESH | | |
| 0x18 | | |

Table 48: TEMPHOTCH register

**Bit [7:0]: storage element charge maximum temperature threshold (TEMPHOTCH.THRESH)**

This field allows the configuration of the maximum temperature (hot) threshold for storage element charging.

## 9.10. STO Discharge Temperature Protection (TEMPCOLDDIS and TEMPHOTDIS)

Those fields are used when the thermal protection monitoring (TEMPPROTECT) is enabled (see Section 9.11) to configure the minimum (cold) and maximum (hot) temperature protection thresholds for discharging the storage element connected to STO.

If the temperature is out of the discharge temperature range, the buck converter will be disabled to stop discharging the storage element through the LOAD. In this case, VINT will continue to be supplied from STO.

See Section 6.7 for further information about thermal monitoring configuration.

### 9.10.1. TEMPCOLDDIS

The TEMPCOLDDIS register allows the configuration of the minimum temperature (cold) for storage element discharging.

| TEMPCOLDDIS register | 0x0F | R/W |
|---|---|---|
| Bit [7:0] | | |
| THRESH | | |
| 0xD1 | | |

Table 49: TEMPCOLDDIS register

**Bit [7:0]: storage element discharge minimum temperature threshold (TEMPCOLDDIS.THRESH)**

This field allows the configuration of the minimum temperature (cold) threshold for storage element discharging.

### 9.10.2. TEMPHOTDIS

The TEMPHOTDIS register allows the configuration of the maximum temperature (hot) for storage element discharging.

| TEMPHOTDIS register | 0x10 | R/W |
|---|---|---|
| Bit [7:0] | | |
| THRESH | | |
| 0x18 | | |

Table 50: TEMPHOTDIS register

**Bit [7:0]: storage element discharge maximum temperature threshold (TEMPHOTDIS.THRESH)**

This field allows the configuration of the maximum temperature (hot) threshold for storage element discharging.

## 9.11. Thermal Protection Monitoring (TEMPPROTECT)

The TEMPPROTECT register allows enabling or disabling the thermal protection based on the protection thresholds described in Sections 9.9 and 9.10.

| TEMPPROTECT register | 0x11 | R/W |
|---|---|---|
| Bit [7:1] | | Bit [0] |
| RESERVED | | EN |
| 0x00 | | 0x01 |

Table 51: TEMPPROTECT register

**Bit [0]: thermal protection monitoring enable (TEMPPROTECT.EN)**

This field allows enabling or disabling the thermal protection monitoring:

- 0: disable the thermal protection.
- 1: enable the thermal protection.

## 9.12. Average Power Monitoring (APM)

The APM register allows the configuration of the Average Power Monitoring feature.

The configuration of this register affects the APM readings of both boost converters, as well as the readings of the buck converter and the 5 V charger.

For APM data interpretation, refer to the Section 9.17.

| APM register | | | 0x13 | | R/W | |
|---|---|---|---|---|---|---|
| Bit [7:6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| RESERVED | WINDOW | MODE | CHG5VEN | LOADEN | BSTHPEN | BSTLPEN |
| 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |

Table 52: APM register

**Bit [5]: APM window (APM.WINDOW)**

This field allows the configuration of the APM window.

- 0: select a window of 233 ms.
- 1: select a window of 116 ms.

*NOTE: if SRC is configured with an MPPT period of 116 ms, the APM window will automatically switch to 116 ms for both boost converters, for the buck converter, and for the 5 V charger, regardless of whether the corresponding converter is enabled or not. This is the case for the SRCREGU1.CFG2 default value (MPPT default period is 116 ms).*

**Bit [4]: APM mode (APM.MODE)**

This field allows the configuration of the BSTLP and LOAD APM mode (the BSTHP and CHG5V APM are always in counter mode).

- 0: set the BSTLP and LOAD APM in counter mode.
- 1: set the BSTLP and LOAD APM in power meter mode.

**Bit [3]: 5 V charger APM enable (APM.CHG5VEN)**

This field allows enabling or disabling the APM for CHG5V.

- 0: disable the 5 V charger APM.
- 1: enable the 5 V charger APM.

**Bit [2]: load output APM enable (APM.LOADEN)**

This field allows enabling or disabling the APM for LOAD.

- 0: disable the load output APM.
- 1: enable the load output APM.

**Bit [1]: high-power boost APM enable (APM.BSTHPEN)**

This field allows enabling or disabling the APM for the high-power boost converter (BSTHP).

- 0: disable the high-power boost APM.
- 1: enable the high-power boost APM.

**Bit [0]: low-power boost APM enable (APM.BSTLPEN)**

This field allows enabling or disabling the APM for the low-power boost converter (BSTLP).

- 0: disable the low-power boost APM.
- 1: enable the low-power boost APM.

## 9.13. APM Accumulator (APMACC)

The APMACC register allows the configuration of the APM accumulator feature.

| APMACC register | 0x14 | R/W |
|---|---|---|
| Bit [7:0] | | |
| CFG | | |
| 0x00 | | |

Table 53: APMACC register

**Bit [7:0]: APM accumulator configuration (APMACC.CFG)**

This field allows the configuration of the number of APM windows during which the APM data is accumulated before rising the IRQ APMDONE flag (see Section 5.5.4). The APM accumulator can be used with both APM modes (pulse counter mode and power meter mode).

APMACC.CFG must be configured to the wanted number of accumulated windows minus 1 (e.g., set APMACC.CFG to 2 to accumulate APM data over 3 APM windows).

To disable the APM accumulator, set APMACC.CFG to 0 (the IRQ pin will be raised after every APM window).

## 9.14. IRQ Enable (IRQENx)

### 9.14.1. IRQEN0

The IRQEN0 register allows the configuration of which events trigger the IRQ pin rising edge (see also the IRQEN1 register).

| IRQEN0 register | | | | 0x15 | | R/W | |
|---|---|---|---|---|---|---|---|
| Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| CHG5VCONN | TEMPDIS | TEMPCH | SRCLOW | VOVCH | VCHRDY | VOVDIS | I2CRDY |
| 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x01 |

Table 54: IRQEN0 register

**Bit [7]: 5 V charger connected (IRQEN0.CHG5VCONN)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.CHG5VCONN when the 5 V charger gets connected or disconnected (see Table 7 for $V_{5V\_IN}$ requirements).

- 0: disable the IRQ flag for 5 V charger connection.
- 1: enable the IRQ flag for 5 V charger connection.

**Bit [6]: storage element discharge temperature (IRQEN0.TEMPDIS)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.TEMPDIS when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers).

- 0: disable the IRQ flag for discharge temperature range.
- 1: enable the IRQ flag for discharge temperature range.

**Bit [5]: storage element charge temperature (IRQEN0.TEMPCH)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.TEMPCH when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers).

- 0: disable the IRQ flag for charge temperature range.
- 1: enable the IRQ flag for charger temperature range.

**Bit [4]: source low voltage (IRQEN0.SRCLOW)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.SRCLOW when the source voltage falls below $V_{SRCLOW}$ (in MPPT ratio mode) or when $V_{SRC,REG}$ target is configured below $V_{SRCLOW}$ (in constant voltage mode).

- 0: disabled the IRQ flag for source low threshold.
- 1: enable the IRQ flag for source low threshold.

**Bit [3]: storage element overcharge (IRQEN0.VOVCH)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VOVCH when the storage element voltage crosses $V_{OVCH}$ (selected through the VOVCH register).

- 0: disable the IRQ flag for $V_{OVCH}$ crossing.
- 1: enable the IRQ flag for $V_{OVCH}$ crossing.

**Bit [2]: storage element charge ready (IRQEN0.VCHRDY)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VCHRDY when the storage element voltage crosses $V_{CHRDY}$ (selected through the VCHRDY register).

- 0: disable the IRQ flag for $V_{CHRDY}$ crossing.
- 1: enable the IRQ flag for $V_{CHRDY}$ crossing.

**Bit [1]: storage element overdischarge (IRQEN0.VOVDIS)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VOVDIS after $T_{CRIT,ST}$ when the storage element voltage drops below $V_{OVDIS}$ (selected through the VOVDIS register) or directly when the storage element voltage rises above $V_{OVDIS}$.

- 0: disable the IRQ flag for $V_{OVDIS}$ crossing.
- 1: enable the IRQ flag for $V_{OVDIS}$ crossing.

**Bit [0]: I2C interface ready (IRQEN0.I2CRDY)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.I2CRDY when the serial interface ($I^2C$) is ready to communicate.

- 0: disable the IRQ flag for $I^2C$ interface readiness.
- 1: enable the IRQ flag for $I^2C$ interface readiness.

### 9.14.2. IRQEN1

The IRQEN1 register allows the configuration of which events trigger the IRQ pin rising edge (see also the IRQEN0 register).

| IRQEN1 register | | | | 0x16 | R/W | |
|---|---|---|---|---|---|---|
| Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3:2] | Bit [1] | Bit [0] |
| APMERR | APMDONE | TEMPDONE | STODONE | RESERVED | SRCMPPTDONE | SRCMPPTSTART |
| 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |

Table 55: IRQEN1 register

**Bit [7]: APM error (IRQEN1.APMERR)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.APMERR when an APM error occurs.

- 0: disable the IRQ flag for APM errors.
- 1: enable the IRQ flag for APM errors.

**Bit [6]: APM done (IRQEN1.APMDONE)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.APMDONE when APM data is available.

- 0: disable the IRQ flag for new available APM data.
- 1: enable the IRQ flag for new available APM data.

**Bit [5]: temperature measurement done (IRQEN1.TEMPDONE)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.TEMPDONE when the temperature measurement is done.

- 0: disable the IRQ flag for temperature measurement completion.
- 1: enable the IRQ flag for temperature measurement completion.

**Bit [4]: storage element voltage measurement done (IRQEN1.STODONE)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.STODONE when the storage element voltage measurement is done.

- 0: disable the IRQ flag for STO voltage measurement completion.
- 1: enable the IRQ flag for STO voltage measurement completion.

**Bit [3:2]: reserved (write-ignore)**

Those fields are reserved. They can safely be written with any value and has no effect on the AEM15820.

**Bit [1]: source MPPT done (IRQEN1.SRCMPPTDONE)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.SRCMPPTDONE when the source MPP evaluation is done.

- 0: disable the IRQ flag for source MPP evaluation completion.
- 1: enable the IRQ flag for source MPP evaluation completion.

**Bit [0]: source MPPT start (IRQEN1.SRCMPPTSTART)**

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.SRCMPPTSTART when the source MPP evaluation starts.

- 0: disable the IRQ flag for source MPP evaluation start.
- 1: enable the IRQ flag for source MPP evaluation start.

## 9.15. IRQ Flags (IRQFLGx)

The IRQFLGx registers allow the user to get a status about specific AEM15820 events. When the event happens, the IRQ pin switches HIGH and the register field bit that corresponds to the event will switch to 1, provided that the event flag has been enabled in the corresponding IRQENx register. The bit will stay to 1 and the IRQ pin will stay HIGH until the IRQFLGx register is read.

Please note that if the AEM15820 is configured through the I²C registers to enable IRQ flags, the behavior of the IRQ pin as well as the IRQFLGx register stays the same even if the AEM15820 has switched back to GPIO configuration by writing 0 to CTRL.UPDATE.

### 9.15.1. IRQFLG0

The IRQFLG0 register is the IRQ pin event flags register 0.

| IRQFLG0 register | | | | 0x18 | | R | |
|---|---|---|---|---|---|---|---|
| Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| CHG5VCONN | TEMPDIS | TEMPCH | SRCLOW | VOVCH | VCHRDY | VOVDIS | I2CRDY |
| 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |

Table 56: IRQFLG0 register

**Bit [7]: 5 V charger connected (IRQFLG0.CHG5VCONN)**

This IRQ pin event flag is set when the 5 V charger gets connected or disconnected (see Table 7 for $V_{5V\_IN}$ requirements), if the corresponding event source has been previously enabled through the IRQEN0.CHG5VCONN field.

- 0: the 5 V charger was not connected or disconnected.
- 1: the 5 V charger was connected or disconnected.

**Bit [6]: storage element discharge temperature (IRQFLG0.TEMPDIS)**

This IRQ pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers), if the corresponding event source has been previously enabled through the IRQEN0.TEMPDIS field.

- 0: the temperature did not cross the minimum or maximum temperature allowed for discharging.
- 1: the temperature crossed the minimum or maximum temperature allowed for discharging.

**Bit [5]: storage element charge temperature (IRQFLG0.TEMPCH)**

This IRQ pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers), if the corresponding event source has been previously enabled through the IRQEN0.TEMPCH field.

- 0: the temperature did not cross the minimum or maximum temperature allowed for charging.
- 1: the temperature crossed the minimum or maximum temperature allowed for charging.

**Bit [4]: source low voltage (IRQFLG0.SRCLOW)**

This IRQ pin event flag is set when the source voltage falls below $V_{SRCLOW}$ threshold (in MPPT ratio mode) or when $V_{SRC,REG}$ target is configured below $V_{SRCLOW}$ (in constant voltage mode), if the corresponding event source has been previously enabled through the IRQEN0.SRCLOW field.

- 0: the source voltage did not fall below $V_{SRCLOW}$.
- 1: the source voltage fell below $V_{SRCLOW}$.

**Bit [3]: storage element overcharge (IRQFLG0.VOVCH)**

This IRQ pin event flag is set when the storage element voltage crosses $V_{OVCH}$ (selected through the VOVCH register), if the corresponding event source has been previously enabled through the IRQEN0.VOVCH field.

- 0: the storage element voltage did not cross $V_{OVCH}$.
- 1: the storage element voltage crossed $V_{OVCH}$.

**Bit [2]: storage element charge ready (IRQFLG0.VCHRDY)**

This IRQ pin event flag is set when the storage element voltage crosses $V_{CHRDY}$ (selected through the VCHRDY register), if the corresponding event source has been previously enabled through the IRQEN0.VCHRDY field.

- 0: the storage element voltage did not cross $V_{CHRDY}$.
- 1: the storage element voltage crossed $V_{CHRDY}$.

**Bit [1]: storage element overdischarge (IRQFLG0.VOVDIS)**

This IRQ pin event flag is set after $T_{CRIT,ST}$ when the storage element voltage drops below $V_{OVDIS}$ (selected through the VOVDIS register) or directly when the storage element rises above $V_{OVDIS}$, if the corresponding event source has been previously enabled through the IRQEN0.VOVDIS field.

- 0: the storage element voltage did not cross $V_{OVDIS}$.
- 1: the storage element voltage crossed $V_{OVDIS}$.

**Bit [0]: I2C interface ready (IRQFLG0.I2CRDY)**

This IRQ pin event flag is set when the serial interface ($I^2C$) is ready to communicate, if the corresponding event source has been previously enabled through the IRQEN0.I2CRDY field.

- 0: $I^2C$ interface not yet ready to communicate.
- 1: $I^2C$ interface became ready to communicate.

### 9.15.2. IRQFLG1

The IRQFLG1 register is the IRQ pin event flags register 1.

| IRQFLG1 register | | | | 0x19 | R | |
|---|---|---|---|---|---|---|
| Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3:2] | Bit [1] | Bit [0] |
| APMERR | APMDONE | TEMPDONE | STODONE | RESERVED | SRCMPPTDONE | SRCMPPTSTART |
| 0x00 | 0x00 | 0x00 | 0x00 | - | 0x00 | 0x00 |

Table 57: IRQFLG1 register

**Bit [7]: APM error (IRQFLG1.APMERR)**

This IRQ pin event flag is set when an APM error occurs, if the corresponding event source has been previously enabled through the IRQEN1.APMERR field.

- 0: no APM error occurred.
- 1: an APM error occurred.

**Bit [6]: APM done (IRQFLG1.APMDONE)**

This IRQ pin event flag is set when APM data is available, if the corresponding event source has been previously enabled through the IRQEN1.APMDONE field.

- 0: no new APM data available.
- 1: new APM data available.

**Bit [5]: temperature measurement done (IRQFLG1.TEMPDONE)**

This IRQ pin event flag is set when the temperature measurement is done, if the corresponding event source has been previously enabled through the IRQEN1.TEMPDONE field.

- 0: temperature measurement not completed.
- 1: temperature measurement completed.

**Bit [4]: storage element voltage measurement done (IRQFLG1.STODONE)**

This IRQ pin event flag is set when the storage element voltage measurement is done, if the corresponding event source has been previously enabled through the IRQEN1.STODONE field.

- 0: storage element voltage measurement not completed.
- 1: storage element voltage measurement completed.

**Bit [3:2]: reserved**

Those fields are reserved.

**Bit [1]: source MPPT done (IRQFLG1.SRCMPPTDONE)**

This IRQ pin event flag is set when the source MPP evaluation is done, if the corresponding event source has been previously enabled through the IRQEN1.SRCMPPTDONE field.

- 0: source MPP evaluation not completed.
- 1: source MPP evaluation completed.

**Bit [0]: source MPPT start (IRQFLG1.SRCMPPTSTART)**

This IRQ pin event flag is set when the source MPP evaluation starts, if the corresponding event source has been previously enabled through the IRQEN1.SRCMPPTSTART field.

- 0: source MPP evaluation not started.
- 1: source MPP evaluation started.

## 9.16. Status (STATUSx)

### 9.16.1. STATUS0

The STATUS0 register is the AEM15820 status register 0.

| STATUS0 register | | | 0x1A | | R | |
|---|---|---|---|---|---|---|
| Bit [7:6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| RESERVED | CHG5VCONN | RESERVED | SRCLOW | OVCH | CHRDY | OVDIS |
| 0x00 | 0x00 | - | 0x00 | 0x00 | 0x00 | 0x00 |

Table 58: STATUS0 register

**Bit [5]: 5 V charger connected (STATUS0.CHG5VCONN)**

This status indicates whether the 5 V charger is considered connected or not (see Table 7 for $V_{5V\_IN}$ requirements).

- 0: the 5 V charger is disconnected.
- 1: the 5 V charger is connected.

**Bit [4]: reserved**

This field is reserved.

**Bit [3]: source low voltage (STATUS0.SRCLOW)**

This status indicates whether the source voltage is higher than $V_{SRCLOW}$ or not.

- 0: the source is higher than $V_{SRCLOW}$.
- 1: the source is equal or lower than $V_{SRCLOW}$.

**Bit [2]: storage element overcharge (STATUS0.OVCH)**

This status indicates whether the storage element voltage is higher than $V_{OVCH}$ or not.

- 0: the storage element voltage is lower than the overcharge threshold.
- 1: the storage element voltage is equal or higher than the overcharge threshold.

**Bit [1]: storage element charge ready (STATUS0.CHRDY)**

This status indicates whether the storage element voltage is higher than $V_{CHRDY}$ or not.

- 0: the storage element voltage is lower than the charge ready threshold.
- 1: the storage element voltage is equal or higher than the charge ready threshold.

**Bit [0]: storage element overdischarge (STATUS0.OVDIS)**

This status indicates whether the storage element voltage has been lower than $V_{OVDIS}$ for more than $T_{CRIT,ST}$ or not.

- 0: the storage element voltage has not been equal or lower than the overdischarge threshold for more than $T_{CRIT,ST}$.
- 1: the storage element voltage has been equal or lower than the overdischarge threshold for more than $T_{CRIT,ST}$.

### 9.16.2. STATUS1

The STATUS1 register is the AEM15820 status register 1.

| STATUS1 register | 0x1B | | R | |
|---|---|---|---|---|
| Bit [7:4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| RESERVED | TEMPHOTDIS | TEMPCOLDDIS | TEMPHOTCH | TEMPCOLDCH |
| 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |

Table 59: STATUS1 register

**Bit [3]: storage element discharge maximum temperature (STATUS1.TEMPHOTDIS)**

This status indicates whether the temperature is higher than the hot threshold (for storage element discharging) or not.

- 0: the temperature is below the hot threshold.
- 1: the temperature is equal or above the hot threshold.

**Bit [2]: storage element discharge minimum temperature (STATUS1.TEMPCOLDDIS)**

This status indicates whether the temperature is higher than the cold threshold (for storage element discharging) or not.

- 0: the temperature is above the cold threshold.
- 1: the temperature is equal or below the cold threshold.

**Bit [1]: storage element charge maximum temperature (STATUS1.TEMPHOTCH)**

This status indicates whether the temperature is higher than the hot threshold (for storage element charging) or not.

- 0: the temperature is below the hot threshold.
- 1: the temperature is equal or above the hot threshold.

**Bit [0]: storage element charge minimum temperature (STATUS1.TEMPCOLDCH)**

This status indicates whether the temperature is higher than the cold threshold (for storage element charging) or not.

- 0: the temperature is above the cold threshold.
- 1: the temperature is equal or below the cold threshold.

## 9.17. APM Data Summary (APMxBSTLP, APMxBSTHP, APMxCHG5V and APMxLOAD)

### 9.17.1. APMxBSTLP, APMxBSTHP, and APMxLOAD Summary

The APM data registers for both boost converters and for the buck converter all share the same field structure, depending of the configured APM mode, as described in Table 60.

**Pulse Counter Mode**: in this mode, the value in the APM data registers is the number of pulses drawn by the DCDC converter during the APM window (see Section 5.5). The APM data in pulse counter mode depends on the APM accumulator configuration:

- If the APM accumulator is not used (APMACC.CFG set to 0), the APM data can be accessed directly in the COUNTER fields (see Table 60).
- If the APM accumulator is used, the APM data can be computed by left bit-shifting (OFFSET bits) the value in the COUNTER fields (see Table 60).

**Power Meter mode**: in this mode, the value in the APM data registers (POWER fields) can be computed by left bit-shifting by the value in the OFFSET field to obtain the measured APM power ($P_{APM}$) and energy ($E_{APM}$) provided to/from the storage element during the previous APM window or sum of accumulated APM windows (see Section 5.5):

$$P_{APM} = \frac{(\text{POWER} \ll \text{OFFSET}) \cdot \alpha}{\text{APMACC.CFG} + 1}$$

$$E_{APM} = P_{APM} \cdot \text{APM window}$$

Where:

$P_{APM}$ is the average power (W) provided to/from the storage element during the previous APM window.

$\alpha$ is the correction factor used to convert the APM values from the APMxBSTLP and APMxLOAD registers into power. This alpha factor takes into account the configured APM window and $T_{MULT}$, the variability between devices, the board layout, and the effective value of $L_{DCDC}$, as well as several other parameters that affect the APM conversion. The alpha factor can be determined by calibrating the complete system to take all these parameters into account. Please contact e-peas support for more details about alpha calibration.

(APMACC.CFG + 1) is the number of accumulated windows. Equal to 1 if the APM accumulator is not used.

$E_{APM}$ is the energy (J) provided to/from the storage element during the previous APM window.

APM window is the duration (s) used to calculate $E_{APM}$. It must match the actual APM window duration, which may slightly deviate from the nominal datasheet values (116/233 ms). If the APM accumulator is used, this APM window represent the sum of the accumulated APM windows duration.

*NOTE: the high-power boost APM (APMxBSTHP registers) operates exclusively in pulse counter mode.*

| | APM2BSTLP APM2BSTHP APM2LOAD | | | | | | | | APM1BSTLP APM1BSTHP APM1LOAD | | | | | | | | APM0BSTLP APM0BSTHP APM0LOAD | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| Register fields | APM2BSTLP.DATA[7:0] APM2BSTHP.DATA[7:0] APM2LOAD.DATA[7:0] | | | | | | | | APM1BSTLP.DATA[7:0] APM1BSTHP.DATA[7:0] APM1LOAD.DATA[7:0] | | | | | | | | APM0BSTLP.DATA[7:0] APM0BSTHP.DATA[7:0] APM0LOAD.DATA[7:0] | | | | | | | |
| Global APM Field | APM DATA [23:0] | | | | | | | | | | | | | | | | | | | | | | | |
| Pulse Counter Mode (no accumulator) | | COUNTER [22:16] | | | | | | | COUNTER [15:8] | | | | | | | | COUNTER [7:0] | | | | | | | |
| Pulse Counter Mode (with accumulator) | OFFSET [4:0] | | | | | COUNTER [18:16] | | | COUNTER [15:8] | | | | | | | | COUNTER [7:0] | | | | | | | |
| Power Meter Mode (with or without accumulator) | OFFSET [4:0] | | | | | POWER [18:16] | | | POWER [15:8] | | | | | | | | POWER [7:0] | | | | | | | |

Table 60: Summary of APMxBSTLP, APMxBSTHP, and APMxLOAD register fields

### 9.17.2. APMxCHG5V Summary

The APM data registers for the 5 V charger are exclusively used in counter mode to provide the percentage of time during which the 5 V charger has been charging the storage element over the APM window, as described in Table 61.

The charging duty cycle ($D_{CHG}$) over the previous window, or accumulated windows, is obtained thanks to the following formulas:

$$D_{CHG} = \frac{\text{COUNTER}}{\text{MAX COUNTER} - 1}$$

Where MAX COUNTER depends on the configured APM window and APM accumulator:

- For APM window set to 116 ms:

$$\text{MAX COUNTER} = 64 \cdot (\text{APMACC.CFG} + 1)$$

- For APM window set to 233 ms:

$$\text{MAX COUNTER} = 128 \cdot (\text{APMACC.CFG} + 1)$$

Once the charging duty cycle has been defined, the average power and the energy transferred to the storage element from the 5V_IN pin during the previous APM window can be computed with the following formulas:

$$P_{APM} = I_{5V,CC} \cdot V_{STO} \cdot D_{CHG}$$

$$E_{APM} = P_{APM} \cdot \text{APM window}$$

Where:

$P_{APM}$ is the average power (W) provided to the storage element during the previous APM window.

$I_{5V,CC}$ is the 5 V charger current (A) in constant current operation. For higher accuracy, the actual charging current delivered to the storage element must be used, which may slightly deviate from the configured $I_{5V,CC}$.

$V_{STO}$ is the average storage element voltage (V) over the previous APM window.

$D_{CHG}$ is the charging duty cycle of the 5 V charger.

$E_{APM}$ is the energy (J) provided to the storage element during the previous APM window.

APM window is the duration (s) used to calculate $E_{APM}$. It must match the actual APM window duration, which may slightly deviate from the nominal datasheet values (116/233 ms). If the APM accumulator is used, this APM window represent the sum of the accumulated APM windows.

*NOTE: When $V_{STO}$ is below $V_{OVDIS}$, the 5 V charger current $I_{5V,CC}$ must be replaced by $I_{5V,OVDIS,CC}$.*

*NOTE: When the 5 V charger constant voltage (CV) mode is enabled, the 5 V charger current will decrease from the configured $I_{5V,CC}$ as $V_{STO}$ approaches the configured $V_{5V,STOP}$ (see Section 5.7), thus, making the above formulas incorrect.*

| | APM1CHG5V | | | | | | | | APM0CHG5V | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| Pulse Counter Mode | COUNTER [15:8] | | | | | | | | COUNTER [7:0] | | | | | | | |

Table 61: Summary of APMxCHG5V register fields

## 9.18. Boost Converters APM Data (APMxBSTLP and APMxBSTHP)

### 9.18.1. APM0BSTLP and APM0BSTHP

The APM0BSTLP and APM0BSTHP are the first set of registers providing the boost converters APM data.

| APM0BSTLP register | 0x1C | R |
|---|---|---|
| APM0BSTHP register | 0x1F | R |
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 62: APM0BSTLP and APM0BSTHP registers

**Bit [7:0]: boost converters APM data (APM0BSTLP.DATA / APM0BSTHP.DATA)**

This field contains the bits [7:0] of the boost converters APM data (see Table 60 for detailed fields according to APM mode).

### 9.18.2. APM1BSTLP and APM1BSTHP

The APM1BSTLP and APM1BSTHP are the second set of registers providing the boost converters APM data.

| APM1BSTLP register | 0x1D | R |
|---|---|---|
| APM1BSTHP register | 0x20 | R |
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 63: APM1BSTLP and APM1BSTHP registers

**Bit [7:0]: boost converters APM data (APM1BSTLP.DATA / APM1BSTHP.DATA)**

This register contains the bits [15:8] of the boost converters APM data (see Table 60 for detailed fields according to APM mode).

### 9.18.3. APM2BSTLP and APM2BSTHP

The APM2BSTLP and APM2BSTHP are the third set of registers providing the boost converters APM data.

| APM2BSTLP register | 0x1E | R |
|---|---|---|
| APM2BSTHP register | 0x21 | R |
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 64: APM2BSTLP and APM2BSTHP registers

**Bit [7:0]: boost converters APM data (APM2BSTLP.DATA / APM2BSTHP.DATA)**

This register contains the bits [23:16] of the boost converters APM data (see Table 60 for detailed fields according to APM mode).

## 9.19. LOAD APM Data (APMxLOAD)

### 9.19.1. APM0LOAD

The APM0LOAD is the first register providing the LOAD APM data.

| APM0LOAD register | 0x22 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 65: APM0LOAD register

**Bit [7:0]: LOAD APM data (APM0LOAD.DATA)**

This register contains the bits [7:0] of the LOAD APM data (see Table 60 for detailed fields according to APM mode).

### 9.19.2. APM1LOAD

The APM1LOAD is the second register providing the LOAD APM data.

| APM1LOAD register | 0x23 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 66: APM1LOAD register

**Bit [7:0]: LOAD APM data (APM1LOAD.DATA)**

This register contains the bits [15:8] of the LOAD APM data (see Table 60 for detailed fields according to APM mode).

### 9.19.3. APM2LOAD

The APM2LOAD is the third register providing the LOAD APM data.

| APM2LOAD register | 0x24 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 67: APM2LOAD register

**Bit [7:0]: LOAD APM data (APM2LOAD.DATA)**

This register contains the bits [23:16] of the LOAD APM data (see Table 60 for detailed fields according to APM mode).

## 9.20. CHG5V APM Data (APMxCHG5V)

### 9.20.1. APM0CHG5V

The APM0CHG5V is the first register providing the 5 V charger APM data.

| APM0CHG5V register | 0x25 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 68: APM0CHG5V register

**Bit [7:0]: 5 V charger APM data (APM0CHG5V.DATA)**

This register contains the bits [7:0] of the CHG5V APM data (see Table 61 for detailed fields).

### 9.20.2. APM1CHG5V

The APM1CHG5V is the second register providing the 5 V charger APM data.

| APM1CHG5V register | 0x26 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 69: APM1CHG5V register

**Bit [7:0]: 5 V charger APM data (APM1CHG5V.DATA)**

This register contains the bits [15:8] of the CHG5V APM data (see Table 61 for detailed fields).

## 9.21. APM Error (APMERR)

The APMERR register provides the APM errors status.

*NOTE: When the APM accumulator is used (see Section 5.5.4), if an APM error occurs, the corresponding APMERR field will remain high during the whole accumulation window. The IRQFLG1.APMERR will be raised after the end of the total accumulation window.*

| APMERR register | | | | 0x27 | | R | |
|---|---|---|---|---|---|---|---|
| Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | Bit [0] |
| RESERVED | CHG5VLIM | LOADNVLD | LOADOV | RESERVED | BSTHPOV | BSTLPNVLD | BSTLPOV |
| 0x00 | 0x00 | 0x00 | 0x00 | - | 0x00 | 0x00 | 0x00 |

Table 70: APMERR register

**Bit [6]: 5 V charger current limited (APMERR.CHG5VLIM)**

This field warns the user that the 5 V charging current $I_{5V,CC}$ is limited to $I_{5V,OVDIS,CC}$ because $V_{STO}$ is below $V_{OVDIS}$.

- 0: $I_{5V,CC}$ is not limited due to $V_{OVDIS}$.
- 1: $I_{5V,CC}$ is limited to $I_{5V,OVDIS,CC}$.

**Bit [5]: LOAD APM data invalid (APMERR.LOADNVLD)**

This field indicates whether the LOAD APM data is corrupted or not, which occurs when the buck converter runs in "bang-bang" controlled converter mode (see Section 5.3), when:.

$$V_{STO} - V_{LOAD} < 0.25V$$

This field is updated both in pulse counter mode and in power meter mode.

- 0: the LOAD APM data is valid.
- 1: the LOAD APM data is corrupted.

**Bit [4]: LOAD APM counter overflow (APMERR.LOADOV)**

This field indicates whether a LOAD APM counter overflow error occurred or not.

This field is updated both in pulse counter mode and in power meter mode.

- 0: no LOAD APM counter overflow error occurred.
- 1: a LOAD APM counter overflow error occurred

**Bit [3]: reserved**

This field is reserved.

**Bit [2]: high-power boost APM counter overflow (APMERR.BSTHPOV)**

This field indicates whether a BSTHP APM counter overflow error occurred or not.

- 0: no BSTHP APM counter overflow error occurred.
- 1: a BSTHP APM counter overflow error occurred.

**Bit [1]: low-power boost APM data invalid (APMERR.BSTLPNVLD)**

This field indicates whether the BSTLP APM data is corrupted or not. This occurs when $V_{SRC} > V_{STO}$ and the low-power boost converter runs in diode conduction mode.

This field is updated only if the APM is configured in power meter mode.

- 0: the BSTLP APM data is valid.
- 1: the BSTLP APM data is corrupted.

**Bit [0]: low-power boost APM counter overflow (APMERR.BSTLPOV)**

This field indicates whether a BSTLP APM counter overflow error occurred or not.

This field is updated both in pulse counter mode and in power meter mode.

- 0: no BSTLP APM counter overflow error occurred.
- 1: a BSTLP APM counter overflow error occurred.

## 9.22. Temperature Monitoring Data (TEMP)

The TEMP register allows providing the temperature monitoring data as long as $R_{DIV}$ and $R_{TH}$ are connected (see Figure 13).

| TEMP register | 0x28 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 71: TEMP register

**Bit [7:0]: temperature monitoring data (TEMP.DATA)**

This field gives the code that results from the temperature monitoring.

$R_{TH}$ can be determined using the following equation:

$$R_{TH} = \frac{R_{DIV} \cdot DATA}{256 - DATA}$$

Thus the temperature T in Kelvin can be obtained with the following formula.

$$T = \frac{B}{\ln\left(\frac{R_{TH}}{R0}\right) + \frac{B}{T_0}}$$

See Section 5.4 for further information.

## 9.23. Storage Element Voltage Data (STO)

The STO register allows providing the storage element monitoring data.

| STO register | 0x29 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 72: STO register

**Bit [7:0]: storage element monitoring data (STO.DATA)**

This field contains the code that results from the storage element monitoring.

$V_{STO}$ can be determined using the following formula:

$$V_{STO} = \frac{4.8 \cdot DATA}{256}$$

## 9.24. Source Voltage Data (SRC)

The SRC register is the source data register for the SRC voltage.

| SRC register | 0x2A | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x00 | | |

Table 73: SRC register

**Bit [7:0]: source voltage data (SRC.DATA)**

This field contains the code that results from the source voltage measurement for the MPPT regulation. Maximum value is 0xB9.

To convert data from the register to Volts, use either the formulas from Table 74 or the values from Table 75 used as a lookup table. Please note the value in register SRC.DATA are always within the ranges given in those two tables.

| SRC.DATA Range | Formula [V] |
|---|---|
| 0x00 - 0x06 | 0.113 |
| 0x07 - 0x12 | $0.09 + (2 \cdot DATA - 9) \cdot 0.0075$ |
| 0x13 - 0x39 | $0.3 + (2 \cdot DATA - 37) \cdot 0.015$ |
| 0x68 - 0x79 | $\frac{0.3 + (2 \cdot DATA - 165) \cdot 0.015}{0.67}$ |
| 0x9F - 0xB9 | $\frac{0.3 + (2 \cdot DATA - 293) \cdot 0.015}{0.33}$ |

Table 74: Source voltage $V_{SRC}$ from SRC.DATA register value (formula)

| SRC.DATA | $V_{SRC}$ [V] | SRC.DATA | $V_{SRC}$ [V] | SRC.DATA | $V_{SRC}$ [V] | SRC.DATA | $V_{SRC}$ [V] |
|---|---|---|---|---|---|---|---|
| 0x00 | 0.113 | 0x1D | 0.615 | 0x36 | 1.365 | 0xA2 | 2.318 |
| ... | ... | 0x1E | 0.645 | 0x37 | 1.395 | 0xA3 | 2.409 |
| 0x06 | 0.113 | 0x1F | 0.675 | 0x38 | 1.425 | 0xA4 | 2.500 |
| 0x07 | 0.128 | 0x20 | 0.705 | 0x39 | 1.455 | 0xA5 | 2.591 |
| 0x08 | 0.143 | 0x21 | 0.735 | 0x68 | 1.410 | 0xA6 | 2.682 |
| 0x09 | 0.158 | 0x22 | 0.765 | 0x69 | 1.455 | 0xA7 | 2.773 |
| 0x0A | 0.173 | 0x23 | 0.795 | 0x6A | 1.500 | 0xA8 | 2.864 |
| 0x0B | 0.188 | 0x24 | 0.825 | 0x6B | 1.545 | 0xA9 | 2.955 |
| 0x0C | 0.203 | 0x25 | 0.855 | 0x6C | 1.590 | 0xAA | 3.045 |
| 0x0D | 0.218 | 0x26 | 0.885 | 0x6D | 1.634 | 0xAB | 3.136 |
| 0x0E | 0.233 | 0x27 | 0.915 | 0x6E | 1.679 | 0xAC | 3.227 |
| 0x0F | 0.248 | 0x28 | 0.945 | 0x6F | 1.724 | 0xAD | 3.318 |
| 0x10 | 0.263 | 0x29 | 0.975 | 0x70 | 1.769 | 0xAE | 3.409 |
| 0x11 | 0.278 | 0x2A | 1.005 | 0x71 | 1.813 | 0xAF | 3.500 |
| 0x12 | 0.293 | 0x2B | 1.035 | 0x72 | 1.858 | 0xB0 | 3.591 |
| 0x13 | 0.315 | 0x2C | 1.065 | 0x73 | 1.903 | 0xB1 | 3.682 |
| 0x14 | 0.345 | 0x2D | 1.095 | 0x74 | 1.948 | 0xB2 | 3.773 |
| 0x15 | 0.375 | 0x2E | 1.125 | 0x75 | 1.993 | 0xB3 | 3.864 |
| 0x16 | 0.405 | 0x2F | 1.155 | 0x76 | 2.037 | 0xB4 | 3.955 |
| 0x17 | 0.435 | 0x30 | 1.185 | 0x77 | 2.082 | 0xB5 | 4.045 |
| 0x18 | 0.465 | 0x31 | 1.215 | 0x78 | 2.127 | 0xB6 | 4.136 |
| 0x19 | 0.495 | 0x32 | 1.245 | 0x79 | 2.172 | 0xB7 | 4.227 |
| 0x1A | 0.525 | 0x33 | 1.275 | 0x9F | 2.045 | 0xB8 | 4.318 |
| 0x1B | 0.555 | 0x34 | 1.305 | 0xA0 | 2.136 | 0xB9 | 4.409 |
| 0x1C | 0.585 | 0x35 | 1.335 | 0xA1 | 2.227 | | |

Table 75: Source voltage $V_{SRC}$ from SRC.DATA register value (lookup table)

## 9.25. Part Number (PNx)

| PN0 register | 0xE0 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x30 | | |

Table 76: PN0 register

| PN1 register | 0xE1 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x32 | | |

Table 77: PN1 register

| PN2 register | 0xE2 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x38 | | |

Table 78: PN2 register

| PN3 register | 0xE3 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x35 | | |

Table 79: PN3 register

| PN4 register | 0xE4 | R |
|---|---|---|
| Bit [7:0] | | |
| DATA | | |
| 0x31 | | |

Table 80: PN4 register

# 10. Typical Application Circuits

## 10.1. Example Circuit 1

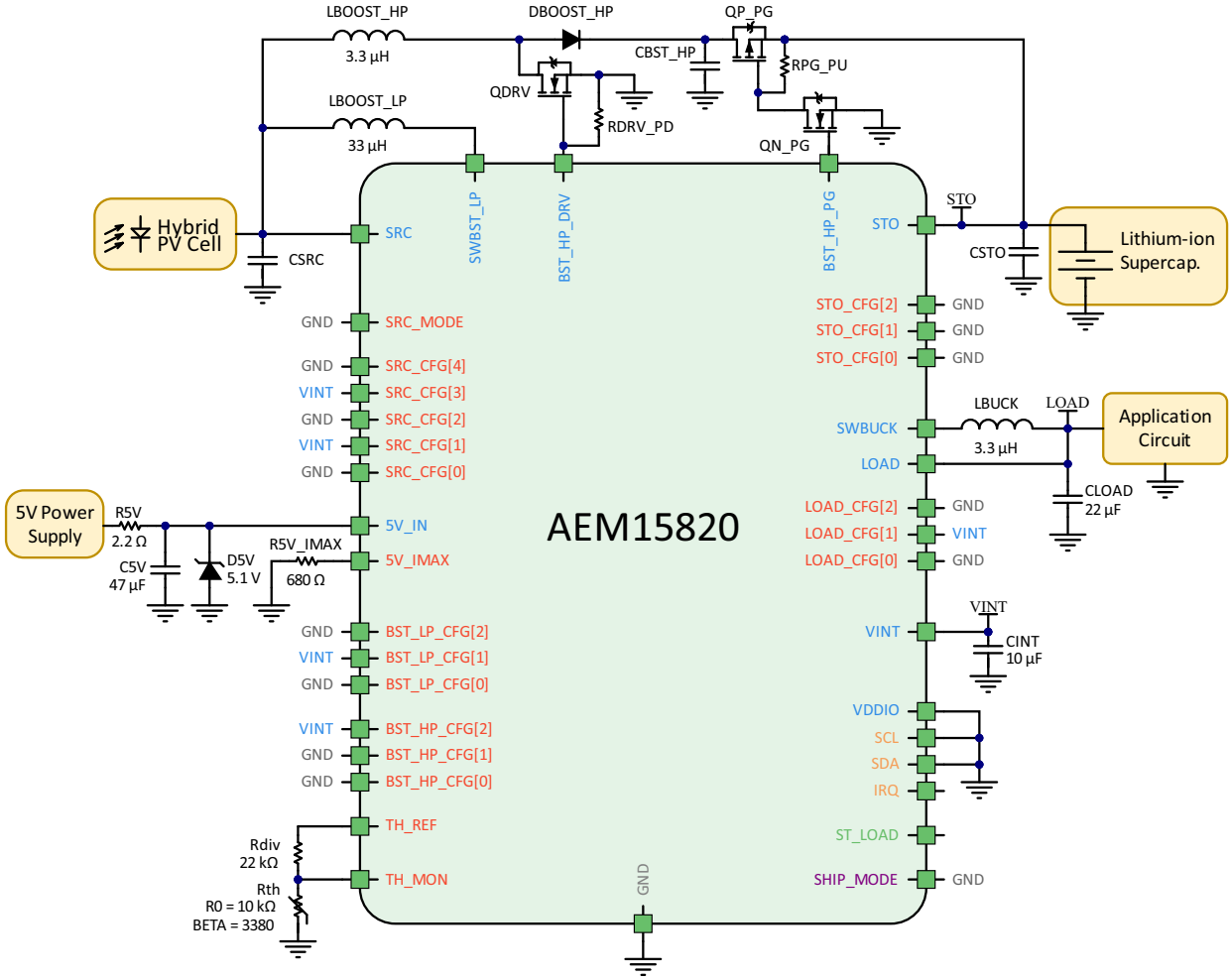



*Figure 16: Typical application circuit 1*

Figure 16 shows a typical application circuit of the AEM15820.

**Configuration of SRC**

The energy source is a hybrid PV cell which has a constant 0.75 V MPP voltage, to harvest both indoor and outdoor using both the low-power and the high-power boost converters. The SRC is configured as follows:

- SRC_MODE = L (constant voltage mode).
- SRC_CFG[4:0] = LHLHL (0.75 V regulation).
- $L_{BOOST\_LP}$ = 33 µH for best efficiency/current capability trade-off with the configured boost timings multiplier.
- BST_LP_CFG[2:0] = LHL (low-power boost timings x3).
- $L_{BOOST\_HP}$ = 3.3 µH.
- BST_HP_CFG[2:0] = HLL (high-power boost timings x6).

**Configuration of STO**

The storage element is a Lithium-ion supercapacitor, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = LLL:
  - $V_{OVDIS}$ = 2.51 V.
  - $V_{CHRDY}$ = 2.61 V.
  - $V_{OVCH}$ = 3.79 V.

**Configuration of LOAD**

The application circuit is supplied with 1.8 V with current peaks up to 100 mA. The buck converter is configured as follows:

- LOAD_CFG[2:0] = LHL (1.8 V).
  - $V_{CHRDY,BUCK} = V_{CHRDY} = 2.61$ V.
- $L_{BUCK}$ = 3.3 µH for high current capability with default buck timings when I²C is not used (see Sections 6.6.2 and 9.7).

**Configuration of 5V_IN**

The maximum allowed current to charge the storage element is 75 mA. Closest standard series resistor is 680 Ω, which leads to a 73.5 mA maximum current.

- $R_{5V\_IMAX}$ = 680 Ω.
- $I_{5V,CC}$ = 73.5 mA.

The RC filter, which role is to slow down the rise time of the 5 V source, can be determined with the following steps.

$R_{5V}$ is calculated so that the voltage drop across it ensures a $V_{5V\_IN}$ higher than the maximum value between $V_{OVCH}$ + 200 mV and 3.60 V:

$$V_{OVCH} + 0.2\,V > 3.60\,V$$

$$I_{5V,CC} \cdot R_{5V} < 5V - V_{OVCH} - 0.2V$$

$$R_{5V} < \frac{5V - V_{OVCH} - 0.2V}{I_{5V,CC}} \Leftrightarrow R_{5V} < \frac{5V - 3.79V - 0.2V}{73.5 \times 10^{-3}}$$

$$R_{5V} < 13.74\Omega$$

$C_{5V}$ is calculated so that the 5V_IN voltage rise time remains below $T_{5V,RISE}$:

$$R_{5V} \cdot C_{5V} > T_{5V,RISE}$$

$$R_{5V} \cdot C_{5V} > 50\mu s$$

To meet these two conditions, the following component values have been selected:

- $R_{5V}$ = 2.2 Ω
- $C_{5V}$ = 47 µF

The 5 V source is expected to have ripple and/or over voltages up to 5.5 V, so a 5.1 V zener diode $D_{5V}$ is added to prevent those to damage the AEM15820.

The minimum required power rating of $D_{5V}$ is computed as follows, from its maximum reverse current $I_{D5V}$, its voltage $V_{D5V}$ and the resistor $R_{5V}$:

$$P_{D5V} \geq I_{D5V} \cdot V_{D5V} \Leftrightarrow P_{D5V} \geq \frac{5.5V - 5.1V}{R_{5V}} \cdot 5.1V$$

$$P_{D5V} \geq \frac{5.5V - 5.1V}{2.2} \cdot 5.1V \Leftrightarrow P_{D5V} \geq 927mW$$

$R_{5V}$ dissipated power $P_{R5V,idle}$ when the 5 V charger does not pull any current to charge the storage element is determined as follows:

$$P_{R5V,idle} = \frac{(5.5V - 5.1V)^2}{R_{5V}} \Leftrightarrow P_{R5V,idle} = \frac{(5.5V - 5.1V)^2}{2.2}$$

$$P_{R5V,idle} = 73mW$$

Furthermore, $R_{5V}$ dissipated power $P_{R5V,CC}$ at $I_{5V,CC}$ current (73.5 mA) is determined as follows:

$$P_{R5V,CC} = R_{5V} \cdot I_{5V,CC}^{\ 2} = 2.2\Omega \cdot (73.5mA)^2 = 12mW$$

The minimum required power rating of $R_{5V}$ is the maximum of $P_{R5V,idle}$ and $P_{R5V,CC}$, thus, 73 mW.

**I²C configuration**

I²C is not used:

- VDDIO, SDA, and SCL are tied to GND.
- IRQ is left floating.

**Temperature monitoring**

Temperature monitoring is used to protect the storage element from being charged and discharged when temperature is outside the range:

- $R_{TH}$:
  - R0 = 10 kΩ.
  - BETA = 3380.
- $R_{DIV}$ = 22 kΩ.
- STO_CFG[2:0] = LLL:
  - TEMPCOLDCH = -15 °C.
  - TEMPHOTCH = 60 °C.
  - TEMPCOLDDIS = -15 °C.
  - TEMPHOTDIS = 60 °C.

**Shipping mode**

Shipping mode is not used.

- SHIP_MODE is connected to GND.

## 10.2. Example Circuit 2

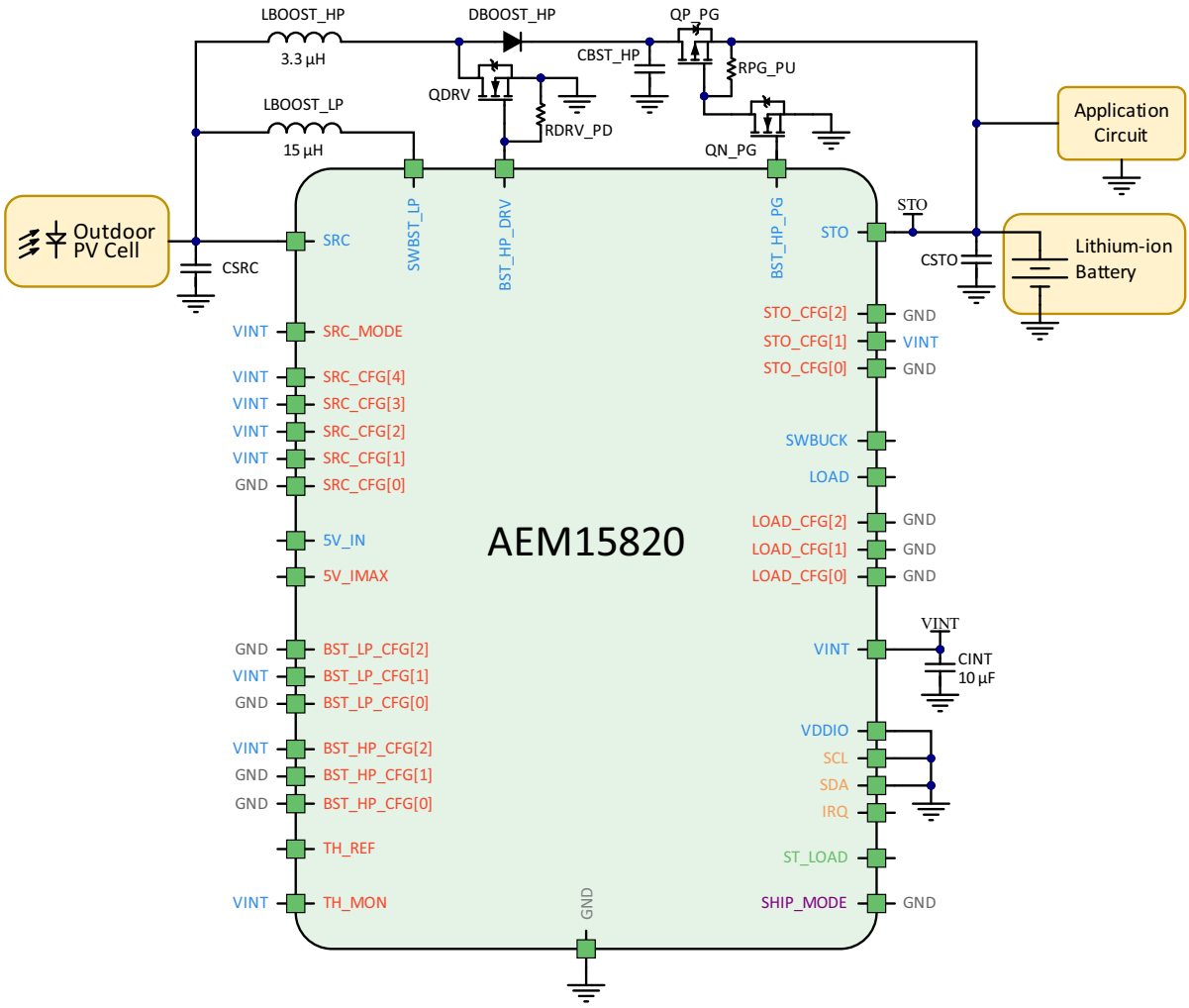



*Figure 17: Typical application circuit 2*

Figure 17 shows a typical application circuit of the AEM15820.

**Configuration of SRC**

The energy source is an outdoor PV cell. Both the low-power and the high-power boost converters are used. The MPPT is used with a 85 % ratio. Long MPPT wait/period are set to ensure that the PV cell has enough time to reach its open circuit voltage during the $V_{OC}$ evaluation (see Section 6.3).

- SRC_MODE = H (MPPT mode).
- SRC_CFG[2:0] = HHL (85%).
- SRC_CFG[4:3] = HH.
  - $T_{MPPT,WAIT}$ = 233 ms.
  - $T_{MPPT,PERIOD}$ = 14895 ms.
- $L_{BOOST\_LP}$ = 15 µH for high current capability with the configured boost timings multiplier.
- BST_LP_CFG[2:0] = LHL (low-power boost timings x3).
- $L_{BOOST\_HP}$ = 3.3 µF.
- BST_HP_CFG[2:0] = HLL (high-power boost timings x6).

**Configuration of STO**

The storage element is a Lithium-ion battery, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = LHL.
  - $V_{OVDIS}$ = 3.00 V.
  - $V_{CHRDY}$ = 3.21 V.
  - $V_{OVCH}$ = 4.13 V.

**Configuration of LOAD**

The application circuit is supplied from the storage element, so the LOAD output is not used:

- LOAD_CFG[2:0] = LLL: buck converter is disabled.
- SWBUCK and LOAD are left floating.

**Configuration of 5V_IN**

The 5 V charger is not used:

- 5V_IN and 5V_IMAX are left floating.

**I²C configuration**

I²C is not used:

- VDDIO, SDA, and SCL are tied to GND.
- IRQ is left floating.

**Temperature monitoring**

Temperature monitoring is not used:

- TH_MON is connected to VINT.
- TH_REF is left floating.

**Shipping mode**

Shipping mode is not used.

- SHIP_MODE is connected to GND.

## 10.3. Example Circuit 3

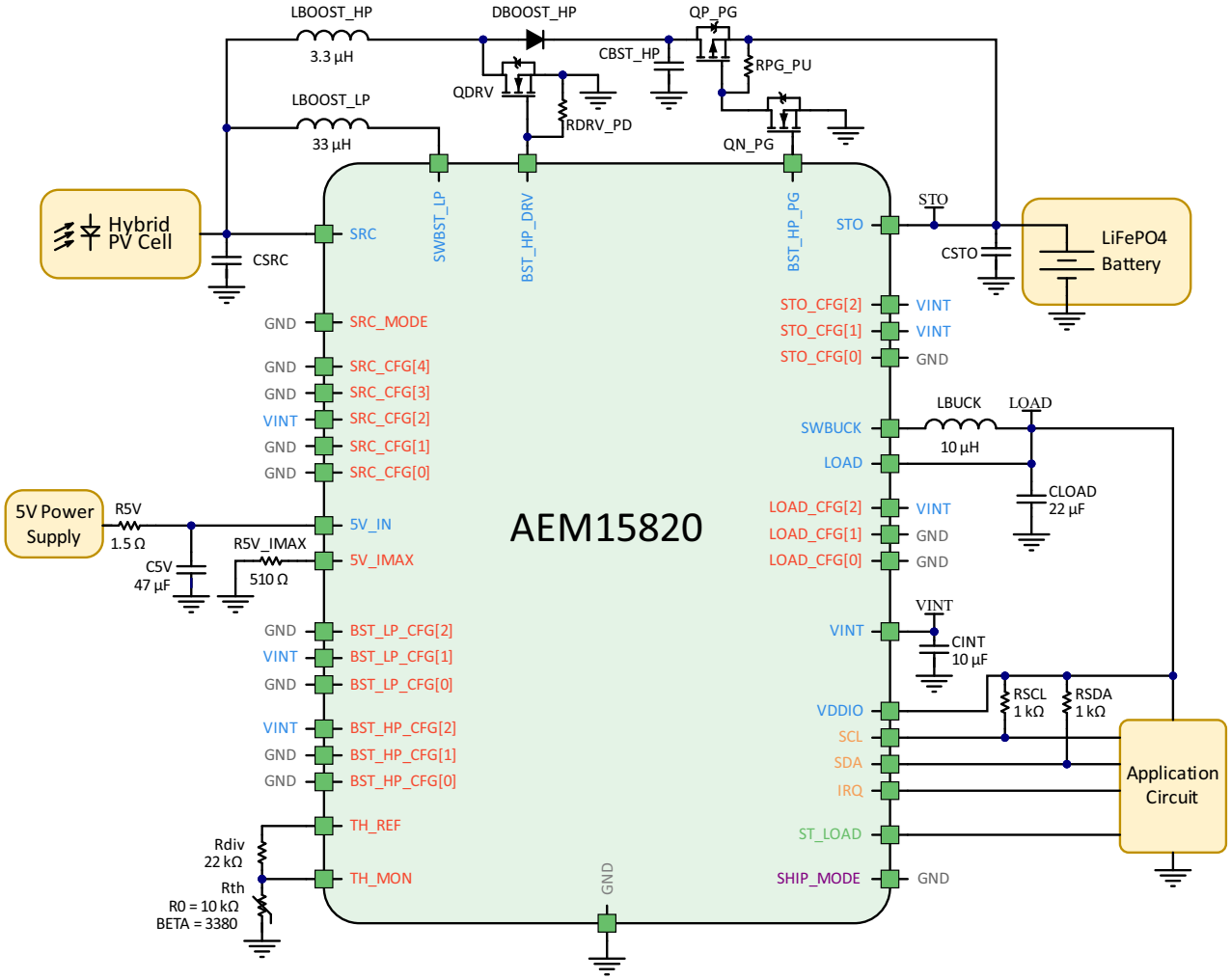



*Figure 18: Typical application circuit 3*

Figure 18 shows a typical application circuit of the AEM15820.

**Configuration of SRC**

The energy source is a hybrid PV cell with a constant 0.45 V maximum power point voltage, to harvested both indoor and outdoor using both the low-power and the high-power boost converters. The SRC is configured as follows:

- SRC_MODE = L (constant voltage mode).
- SRC_CFG[4:0] = LLHLL (0.45 V regulation).
- $L_{BOOST\_LP}$ = 33 µH for best efficiency/current capability trade-off with the configured boost timings multiplier.
- Low-power boost $T_{MULT}$ = x3 (configured through I²C register, see Table 81).
- $L_{BOOST\_HP}$ = 3.3 µH.
- High-power boost $T_{MULT}$ = x6 (configured through I²C register, see Table 81).

**Configuration of STO**

The storage element is a $LiFePO_4$ battery, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = HHL.
  - $V_{OVDIS}$ = 2.81 V.
  - $V_{CHRDY}$ = 3.11 V.
  - $V_{OVCH}$ = 3.62 V.

**Configuration of LOAD**

The application circuit is supplied with 2.5 V with current peaks up to 20 mA. The buck converter is configured as follows:

- LOAD_CFG[2:0] = HLL (2.5 V)
  - $V_{CHRDY,BUCK}$ = $V_{CHRDY}$ = 3.11 V.
- $L_{BUCK}$ = 10 µH for best efficiency/current capability trade-off with the configured buck timings multiplier.
- $T_{MULT}$ = x2 (configured through I²C register, see Table 81).

**Configuration of 5V_IN**

The maximum allowed current to charge the storage element is 100 mA. Closest standard series resistor is 510 Ω, which leads to a 98 mA maximum current.

- $R_{5V\_IMAX}$ = 510 Ω.
- $I_{5V,CC}$ = 98 mA.

The power supply connected on the 5V_IN provides a voltage from minimum 4 V to maximum 5 V. The RC filter, which role is to slow down the rise time of the 5 V source, can be selected with the following steps to ensure the 5 V charger operates properly.

$R_{5V}$ is calculated so that the voltage drop across it ensures a $V_{5V\_IN}$ higher than the maximum value between $V_{OVCH}$ + 200 mV and 3.60 V, considering the minimum voltage available from the power supply:

$$V_{OVCH} + 0.2\,V > 3.60\,V$$

$$I_{5V,CC} \cdot R_{5V} < 4V - V_{OVCH} - 0.2V$$

$$R_{5V} < \frac{4V - V_{OVCH} - 0.2V}{I_{5V,CC}} \quad \Leftrightarrow \quad R_{5V} < \frac{4V - 3.62V - 0.2V}{98 \times 10^{-3}}$$

$$R_{5V} < 1.84\Omega$$

$C_{5V}$ is calculated so that the 5V_IN voltage rise time remains below $T_{5V,RISE}$:

$$R_{5V} \cdot C_{5V} > T_{5V,RISE}$$

$$R_{5V} \cdot C_{5V} > 50\mu s$$

To meet these two conditions, the following component values have been selected:

- $R_{5V}$ = 1.5 Ω
- $C_{5V}$ = 47 µF

$R_{5V}$ dissipated power $P_{R5V,CC}$ at $I_{5V,CC}$ (98 mA) is determined as follows:

$$P_{R5V,CC} = R_{5V} \cdot I_{5V,CC}^{\ 2} = 1.5\Omega \cdot (98mA)^2 = 14.4mW$$

**I²C configuration**

I²C is used to configure the AEM15820:

- VDDIO is connected to LOAD, which is the node supplying the application circuit that communicates with the AEM15820 through I²C.
- SDA and SCL are pulled-up to VDDIO with 1 kΩ resistors and connected to the application circuit micro controller (MCU) I²C bus.
- IRQ and ST_LOAD are connected to the application circuit MCU GPIOs.

The configuration is sent through the I²C bus. Please note that the configuration done through pins (SRC_CFG[4:0], STO_CFG[2:0], LOAD_CFG[2:0], etc.) must also be written to the registers, otherwise the default register values will be applied (see Section 9 for further details about configuring the AEM15820 with I²C registers).

See Table 81 for the whole I²C register configuration (all other registers have appropriate default values).

**Temperature monitoring**

Temperature monitoring is used to protect the storage element from being charged and discharged outside its acceptable temperature range. The following settings are applied (see Table 81 for the corresponding register values):

- $R_{TH}$:
  - R0 = 10 kΩ.
  - BETA = 3380.
- $R_{DIV}$ = 22 kΩ.
- Charging is allowed between 0°C and +45°C.
- Discharging is allowed between -20°C and +65°C.
- Thermal protection monitoring is enabled by default (see Section 9.11) so it is not mandatory to write the TEMPPROTECT register.

**Average Power Monitoring (APM)**

To set up the APM, the user must do the following:

- Enable the APM event in register IRQEN1 so that a rising edge is generated on the IRQ pin to notify the application MCU when a new APM data is ready. This is done by setting the IRQEN1.APMDONE field to 1.
- Configure the APM register:
  - APM.WINDOW = 0: APM window of 233 ms for longest integration.
  - APM.MODE = 1: power meter mode (for the BSTLP and LOAD APM modules).
  - APM.LOADEN = 1: enable power monitoring of energy from STO to LOAD.
  - APM.BSTLPEN = 1: enable APM monitoring from the low-power boost converter to STO.
  - APM.BSTHPEN = 1: enable APM monitoring from the high-power boost converter to STO.
  - APM.CHG5VEN = 1: enable APM monitoring on the 5 V charger.
- Read APM data when IRQ raises.
- Read the IRQFLG1 register to reset the IRQ pin.

**Shipping mode**

Shipping mode is not used.

- SHIP_MODE is connected to GND.

| Register Name | Value | Notes |
|---|---|---|
| SRCREGU1<br>SRCREGU0 | 0x05<br>0x0E | Constant voltage mode.<br>$V_{SRC,REG}$ = 0.450 V. |
| VOVDIS | 0x15 | $V_{OVDIS}$ = 2.794 V. |
| VCHRDY | 0x22 | $V_{CHRDY}$ = 3.094 V. |
| VOVCH | 0x32 | $V_{OVCH}$ = 3.638 V. |
| BSTLPCFG | 0x09 | Low-power boost converter enabled.<br>$T_{MULT}$ = x3. |
| BSTHPCFG | 0x11 | High-power boost converter enabled.<br>$T_{MULT}$ = x6. |
| BUCKCFG | 0x17 | $V_{LOAD}$ = 2.5 V.<br>$T_{MULT}$ = x2. |
| TEMPCOLDCH | 0x90 | Min. 0°C for charge. |
| TEMPHOTCH | 0x2E | Max. +45°C for charge. |
| TEMPCOLDDIS | 0xC6 | Min. -20°C for discharge. |
| TEMPHOTDIS | 0x1B | Max. +65°C for discharge. |
| TEMPPROTECT | 0x01 | Enable thermal protection monitoring. |
| APM | 0x1F | APM register configuration as explained above. |
| IRQEN1 | 0x40 | Enable APMDONE IRQ. |
| CTRL | 0x01 | Write this register after writing the others to load I²C register configuration. |

Table 81: Summary of I²C register configuration for typical application circuit 3

# 11. Minimum BOM

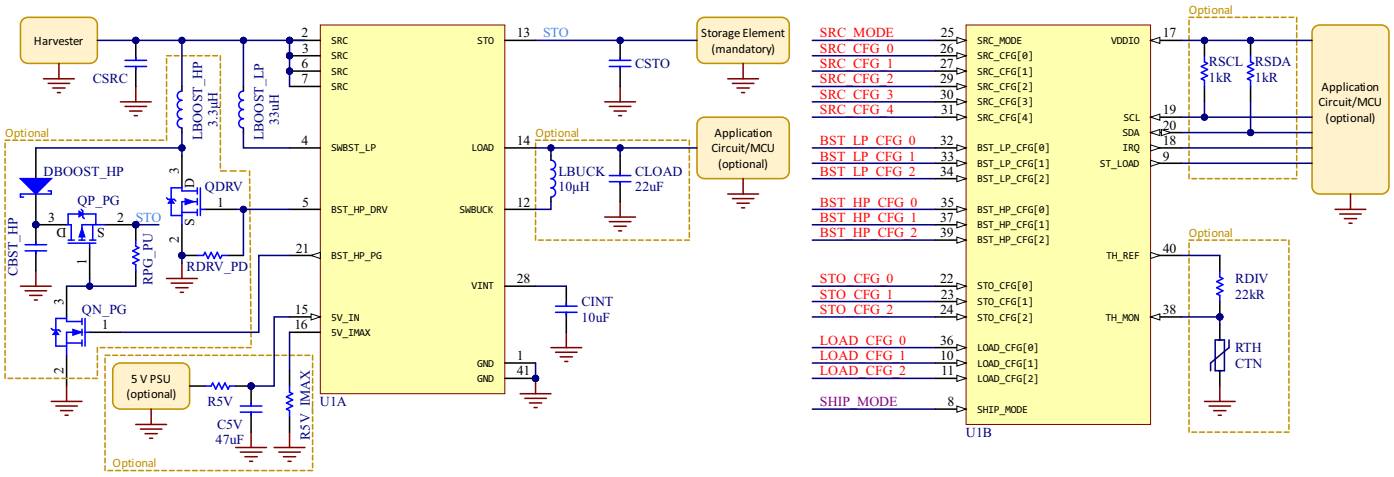



*Figure 19: Schematic*

| Designator | | Description | Quantity | Manufacturer | Part Number |
|---|---|---|---|---|---|
| Mandatory | U1 | AEM15820 | 1 | e-peas | order at sales@e-peas.com |
| | Storage Element | Min. voltage 2.4 V<br>Max. voltage 5.0 V | 1 | To be defined by user. | |
| | CINT | Ceramic capacitor 10 µF, 6.3 V, 20 %, X5R, 0402 | 1 | Murata | GRM155R60J106ME44D |
| | CSTO | Ceramic capacitor 47 µF, 6.3 V, 20 %, X5R, 0603 | 1 | Murata | GRM188R60J476ME15D |
| | CSRC | Ceramic capacitor 22 µF, 10 V, 20 %, X5R, 0603 | 2 | Murata | GRM188R61A226ME15D |
| | | Ceramic capacitor 220 µF, 6.3 V, 20 %, X5R, 1206 | 2 | Murata | GRM31CR60J227ME11L |
| | LBOOST_LP | Power Inductor 33 µH - 0.68 A | 1 | Coilcraft | LPS4018-333MRB |
| Optional | LBOOST_HP[1] | Power Inductor 3.3 µH - 7.3 A | 1 | Wurth | 74438367033 |
| | DBOOST_HP[1] | Schottky Rectifier 15 V, 1 A | 1 | Vishay | VS-10BQ015HM3/5BT |
| | QDRV[1] | Power MOSFET, N Channel, 30 V, 10 A, 0.0124 Ω | 1 | Rohm | RF4E100AJTCR |
| | QP_PG[1] | Power MOSFET, P Channel, 20 V, 89 A, 0.0035 Ω | 1 | Diodes Incorporated | DMP2005UFG-13 |
| | QN_PG[1] | Power MOSFET, N Channel, 60 V, 230 mA, 3.5 Ω | 1 | Infineon | BSS138NH6327XTSA2 |
| | RPG_PU[1] | Resistor 330 kΩ | 1 | Yageo | RC0603FR-07330KL |
| | RDRV_PD[1] | Resistor 330 kΩ | 1 | Yageo | RC0603FR-07330KL |
| | CBST_HP[1] | Ceramic capacitor 47 µF, 6.3 V, 20 %, X5R, 0603 | 1 | Murata | GRM188R60J476ME15D |
| | C5V | Ceramic capacitor 47 µF, 6.3 V, 20 %, X5R, 0603 | 1 | Murata | GRM188R60J476ME15D |
| | R5V | Resistor | 1 | To be defined by user. | |
| | R5V_IMAX | Resistor | 1 | To be defined by user. | |
| | CLOAD | Ceramic capacitor 22 µF, 10 V, 20 %, X5R, 0603 | 1 | Murata | GRM188R61A226ME15D |
| | LBUCK | Power inductor 10 µH | 1 | TDK | VLS252012CX-100M-1 |
| | RSCL | Resistor 1 kΩ | 1 | Multicomp | MCWR06X1001FTL |
| | RSDA | Resistor 1 kΩ | 1 | Multicomp | MCWR06X1001FTL |
| | RDIV | Resistor 22 kΩ | 1 | Yageo | RC0402FR-0722KL |
| | RTH | 10 kΩ NTC thermistor | 1 | Murata | NCP15XH103J03RC |

Table 82: Minimum BOM

*1. Required components if the high-power boost converter is used in addition to the low-power boost converter.*

# 12. Layout

## 12.1. Guidelines

The following guidelines must be applied for best performances:

- Make sure that ground and power signals are routed with large tracks. If an internal ground plane is used, place vias as close as possible to the components, especially for decoupling capacitors.
- Reactive components related to the low-power boost converter and the buck converter must be placed as close as possible to the corresponding pins (SWBST_LP, SWBUCK, LOAD and STO), and be routed with large tracks/polygons.
- Reactive components related to the high-power boost converter must be placed as close as possible to the high-power boost switching node, and be routed with large tracks/polygons. Use several vias for ground and power paths.
- Keep distance between inductors to avoid magnetic coupling.
- PCB track capacitance must be reduced as much as possible on the boost converters switching nodes. This is done as follows:
  - Keep the connection between the SWBST_LP / SWBUCK pins / high-power boost switching node and their corresponding inductors short.
  - Remove the ground and power planes under the SWBST_LP / SWBUCK / high-power boost switching nodes. The polygon on the opposite external layer may also be removed.
  - Increase the distance between SWBST_LP / SWBUCK / high-power boost switching node and the ground polygon on the external PCB layer where the AEM15820 is mounted.
- PCB track capacitance must be reduced as much as possible on the TH_REF node. Same principle as for SWBST_LP and the high-power boost switching node may be applied.

# 13. Package Information

## 13.1. Moisture Sensitivity Level

| Package | Moisture Sensitivity Level (MSL)[1] |
|---|---|
| QFN-40 | Level 1 |

Table 83: Moisture sensitivity level

*1. According to JEDEC 22-A113 standard.*

## 13.2. RoHS Compliance

e-peas product complies with RoHS requirement.

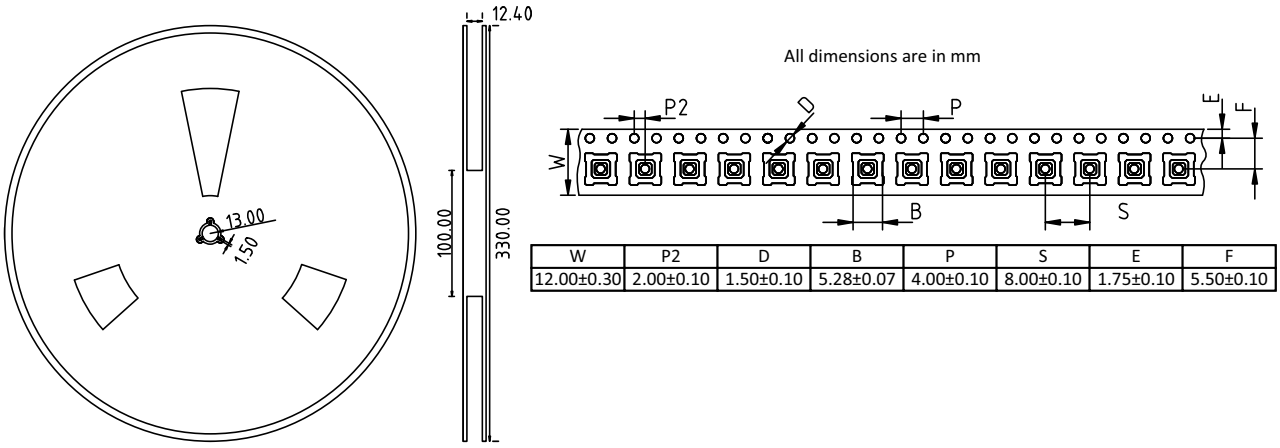
e-peas defines “RoHS” to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

## 13.3. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.

## 13.4. Tape and Reel Dimensions




| W | P2 | D | B | P | S | E | F |
|---|---|---|---|---|---|---|---|
| 12.00±0.30 | 2.00±0.10 | 1.50±0.10 | 5.28±0.07 | 4.00±0.10 | 8.00±0.10 | 1.75±0.10 | 5.50±0.10 |

*Figure 20: Tape and reel dimensions*

## 13.5. Package Dimensions

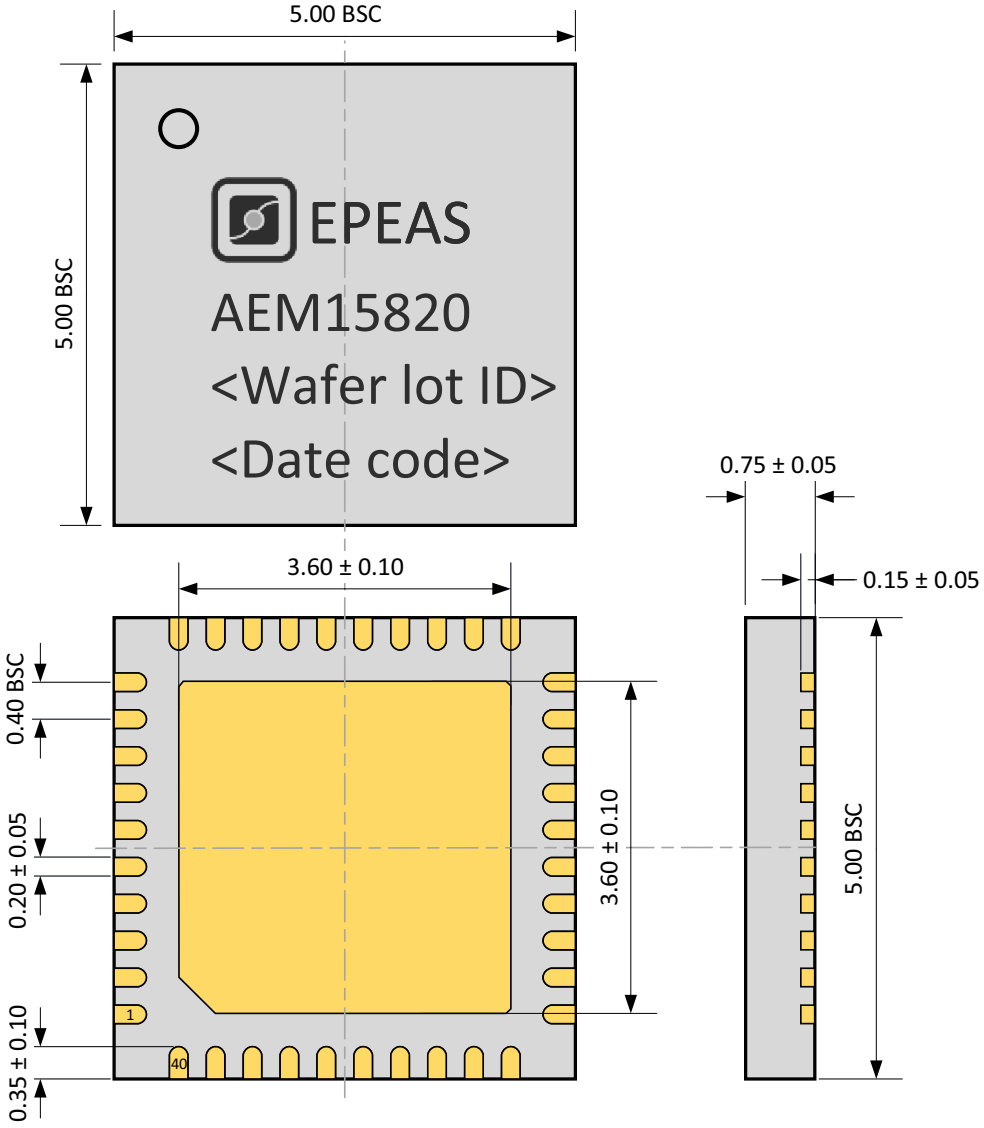



*Figure 21: QFN 40-pin 5x5mm drawing (all dimensions in mm)*

## 13.6. Board Layout

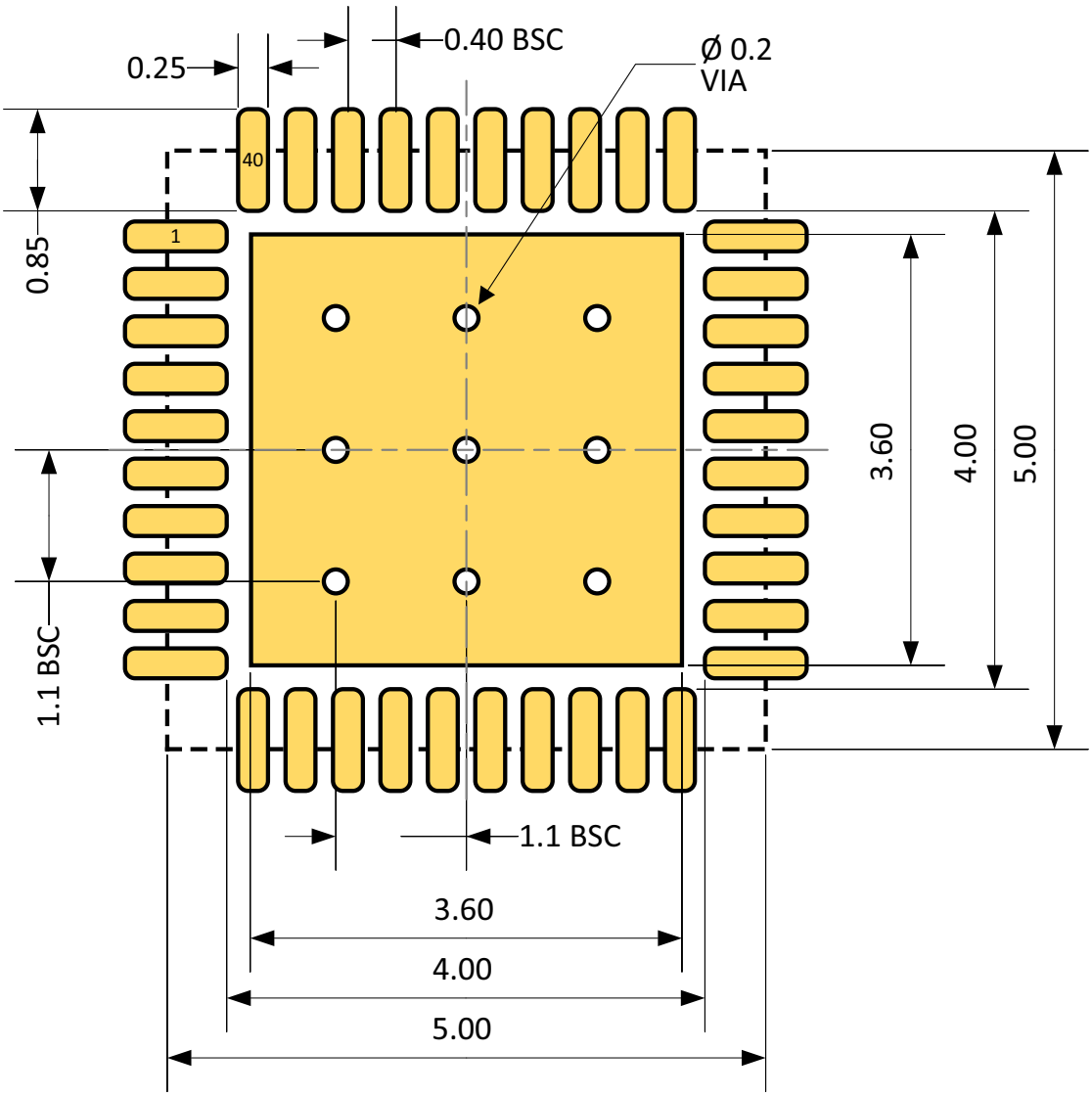



*Figure 22: Recommended board layout for QFN40 package (all dimensions in mm)*

## 14. Glossary

$C_{5V}$

Decoupling capacitor on the 5V_IN pin.

$C_{BST,HP}$

Decoupling capacitor of the high-power boost converter.

$C_{INT}$

Decoupling capacitor on the VINT pin.

$C_{LOAD}$

Decoupling capacitor on LOAD pin.

$C_{SRC}$

Decoupling capacitor on the SRC pin.

$C_{STO}$

Decoupling capacitor on the STO pin.

$D_{5V}$

Zener diode that ensures that the voltage on 5V_IN stays below 5.5 V at any time.

$D_{BOOST\_HP}$

High-power boost converter diode.

$D_{CHG}$

5 V charger APM charging duty cycle (see Section 9.17.2).

$E_{APM}$

Energy that was provided to/from the storage element during the APM window (see Section 9.17).

$I_{5V,CC}$

Current provided to the storage element by the 5V_IN when in constant current mode.

$I_{5V,OVDIS,CC}$

Charging current of the 5 V charger when in constant current (CC) mode and $V_{STO} < V_{OVDIS}$.

$I_{5V,CV}$

Current provided to the storage element by the 5V_IN when in constant voltage mode.

$I_{LBOOST,PEAK}$

Peak current in $L_{BOOST\_LP}$ or $L_{BOOST\_HP}$ when the corresponding boost converter is running.

$I_{LBUCK,PEAK}$

Peak current in $L_{BUCK}$ when the buck converter is running.

$I_{Q,SHIP}$

AEM15820 internal quiescent current on STO in shipping mode (SHIP_MODE is HIGH) with or without energy available on SRC.

$I_{Q,SLEEP}$

AEM15820 internal quiescent current drawn on STO in SLEEP STATE.

$I_{Q,SUPPLY}$

AEM15820 internal quiescent current drawn on STO in SUPPLY STATE.

$I_{Q,RESET}$

AEM15820 internal quiescent current drawn on STO in RESET STATE.

$I_{SRC}$

Current extracted from the harvester connected on SRC.

$L_{BOOST\_LP}$

Low-power boost converter inductor.

$L_{BOOST\_HP}$

High-power boost converter inductor.

$L_{BUCK}$

Buck converter inductor.

$P_{APM}$

Power provided to/from the storage element measured through the APM (see Section 9.17).

$P_{R5V,CC}$

Power dissipated by the $R_{5V}$ when the 5 V charger is in constant current (CC) mode.

$P_{R5V,idle}$

Power dissipated by $R_{5V}$ when no current is pulled by the 5 V charger (current only flowing in the zener protection diode).

$Q_{DRV}$

NMOS transistor for driving the high-power boost converter.

$Q_{N\_PG}$

NMOS transistor pulling the $Q_{P\_PG}$ gate LOW when BST_HP_PG pin is HIGH, turning the high-power boost converter on.

$Q_{P\_PG}$

PMOS transistor used to enable or disable power to the high-power boost converter.

$R_{5V}$

Resistor creating a RC filter with $C_{5V}$ on 5V_IN to limit $T_{5V,RISE}$.

$R_{5V\_IMAX}$

Resistor connected between 5V_IMAX and GND that defines the maximum current provided to the storage element by the 5 V charger (5V_IN pin).

$R_{DIV}$

Along with $R_{TH}$, resistor creating a resistive voltage divider connected to TH_MON, used for thermal monitoring.

$R_{DRV\_PD}$

Resistor pulling BST_HP_DRV pin LOW.

$R_{MPPT}$

For the boost converters, ratio between the open circuit voltage $V_{OC}$ and the voltage regulation $V_{MPP}$ determined by the MPPT (when the boost converter is in MPPT mode).

$R_{PG\_PU}$

Resistor pulling the $Q_{P\_PG}$ gate HIGH when BST_HP_PG pin is LOW, turning the high-power boost converter off.

$R_{SCL}$ / $R_{SDA}$

Pull-up resistors used for the I²C communication bus.

$R_{TH}$

Along with $R_{DIV}$, thermistor creating a resistive voltage divider connected to TH_MON, used for thermal monitoring.

$T_{5V,RISE}$

Minimum voltage rise time on the 5V_IN pin.

$T_{CRIT}$

Delay for the AEM15820 to go in OVDIS STATE and to disable the LOAD output (see Section 5.9).

$T_{CRIT,ST}$

Delay for the AEM15820 to notify the application about an overdischarged storage element, a temperature out of discharge temperature range, and to schedule to disable the LOAD output (see Section 5.3).

$T_{GPIO,MON}$

GPIO reading rate.

$T_{MPPT,MEASURE}$

Duration of $V_{OC}$ measurement during MPP evaluation.

$T_{MPPT,PERIOD}$

Time between the start of two MPP evaluations (see Table 13).

$T_{MPPT,WAIT}$

Time interval during which the AEM15820 stops extracting power and allows the source voltage to rise to the open-circuit voltage before $V_{OC}$ measurement begins (see Table 13).

$T_{MULT}$

Boost or buck converter inductor charging timings multiplier.

$T_{STO,MON}$

Storage element voltage monitoring rate.

$T_{TEMP,MON}$

Temperature monitoring rate.

$V_{5V\_IN}$

Voltage on the 5V_IN pin.

$V_{5V\_IN,MIN}$

Minimum voltage on the 5V_IN pin.

$V_{5V,STOP}$

Voltage on STO at which the 5 V charger stops charging the storage element (see Section 5.7).

$V_{CHRDY}$

In START STATE, voltage required on the storage element to switch to SUPPLY STATE (see Section 6.4).

$V_{CHRDY,BUCK}$

Minimum voltage accepted on the storage element before starting to supply the LOAD if the 5 V charger is not used.

$V_{ESD}$

Electrostatic discharge voltage.

$V_{INT}$

Voltage on the VINT pin.

$V_{INT,CS}$

Minimum voltage on VINT to allow the AEM15820 to switch from RESET STATE to SENSE STO STATE.

$V_{INT,RESET}$

Minimum voltage on VINT before switching to RESET STATE (from any other state).

$V_{LOAD}$

Voltage on the LOAD pin.

$V_{MPP}$

Target regulation voltage on SRC when extracting power (when SRC regulation mode is MPPT).

$V_{OC}$

Open circuit voltage of the harvester connected on SRC.

$V_{OVCH}$

Maximum voltage accepted on the storage element before disabling its charging (see Section 6.4).

$V_{OVDIS}$

Voltage below which the storage element is considered to be fully depleted, and must not be discharged any further (see Section 6.4).

$V_{OVDIS,BUCK}$

Minimum storage element voltage accepted before:

- Starting to supply the LOAD if the 5 V charger is used,
- Stopping to supply the LOAD when the storage element voltage is too low.

$V_{SRCLOW}$

$V_{SRC}$ threshold below which the AEM15820 switches to SLEEP STATE, as described in Section 9.4.

$V_{SRC}$

Voltage on the SRC pin.

$V_{SRC,CS}$

Minimum SRC voltage required for the AEM15820 to coldstart.

$V_{SRC,REG}$

Target regulation voltage of the source, depending on SRC_CFG[4:0] configuration or I²C register (when SRC regulation mode is constant voltage).

$V_{STO}$

Voltage on the STO pin.

$V_{VDDIO}$

Voltage on the VDDIO pin.

# 15. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | December, 2025 | Initial release. |
| 1.1 | December, 2025 | - Updated the storage element types in the “Simplified schematic view” figure.<br>- Added ESD ratings. |
| 1.2 | January, 2026 | Updated the minimum source power required for cold-start typical value. |

Table 84: Revision history