Compact PMIC with Source Voltage Level Configuration for Single/ Dual PV Cells or Pulsed Source

Features and Benefits

Cold start from 250 mV input voltage and 5 µW input power (typical)
- Fast start-up from source.

Constant input voltage regulation (0.12 V to 1.47 V)
- Optimized for single/dual elements capacitive PV cell, intermittent and pulsed power sources.

Selectable overdischarge and overcharge protection
- Supports various types of rechargeable batteries (LiC, Li-ion, LiPo, Li-ceramic pouch, etc.).

Ultra-low power idle mode
- Stored energy is preserved when no source available.

Shipping and shelf mode
- Prevents energy drain from battery when no source available (KEEP_ALIVE pin);
- Disables storage element charging (DIS_STO_CH pin).

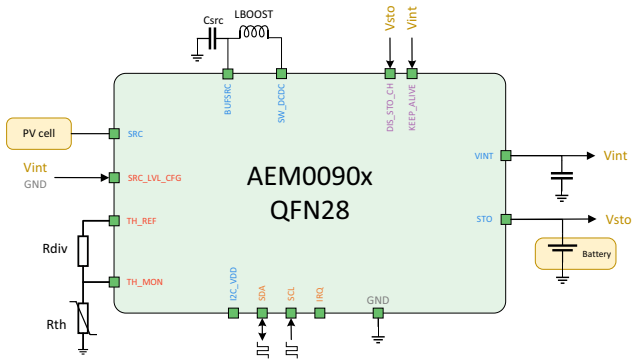
Configuration pins or I²C
- Easy setup;
- Basic settings at startup with configuration pins;
- Advanced configuration with I²C (Fast Mode Plus).

Average power monitoring
- Easy estimation of the harvested power.

Integrated thermistor conditioning circuit
- Configurable battery thermal protection.

Applications

Wearable Electronics	Keyboards
Remote Control	Electronic Shelf Labels
Smart Buildings	Indoor Sensors



Description

The AEM0090x is a compact, fully integrated battery charger that harvests DC power to store energy in rechargeable batteries. It extends battery lifetime and removes the need for primary energy storage in a large range of applications.

Selecting the operating voltage allows the user to set a constant Maximum Power Point at which the AEM0090x operates, to charge a storage element, such as a Li-ion battery or a LiC. The boost converter operates with input voltages ranging from 120 mV to 1.47 V, making AEM0090x ideal for single or dual element PV cell.

The AEM0090x has a unique cold-start circuit capable of operation with input voltages as low as 250 mV and power as minimal as 5 µW. The output voltages ranges from 2.8 V to 4.8 V, with configurable protection levels to prevent overcharging and overdischarging of the storage element. No external components are necessary to set these protection levels. Additionally, thermal monitoring safeguards the storage element, while an Average Power Monitoring system offers insights into the harvested energy for the application circuit.

Thanks to the keep-alive feature, the AEM0090x internal circuit can stay powered by the storage element even in absence of a harvesting source. When keep-alive is disabled and no harvesting source is present, the AEM0090x turns off, preserving the energy of the storage element.

A shelf-mode can be obtained by disabling the keep-alive feature, preventing the battery to be drained during device storage. Furthermore, enabling the DIS_STO_CH feature creates a shipping mode by preventing battery charging.

The AEM00900 application schematic is featuring small PCB size (51 mm²) and a global lower bill of material. The AEM00901 application schematic allows higher performance with a PCB area penalty as low as 6 mm², enabling small size and low cost implementation for single/dual element PV or pulsed sources versus other DCDC based solutions.

Device Information

Part Number	Package	Body size
10AEM00900C0000 10AEM00901C0000	QFN 28-pin	4x4mm

Evaluation Board

Part number
2AAEM00900C001
2AAEM00901C001

Table of Contents

1. Introduction 6
2. Pin Configuration and Functions 7
3. Absolute Maximum Ratings 9
4. Thermal Resistance 9
5. Material 9
5.1. RoHS Compliance 9
5.2. REACH Compliance 9
6. Typical Electrical Characteristics at 25 °C 10
7. Recommended Operation Conditions 11
8. Functional Block Diagram 12
9. Theory of Operation 13
9.1. Boost Converter 13
9.2. Source Voltage Regulation 13
9.3. Thermal Monitoring 13
9.4. Average Power Monitoring 14
9.5. Automatic High Power Mode (AEM00900 only) 14
9.6. Keep-alive 14
9.7. IRQ Pin 14
9.8. State Description 15
9.8.1. Reset State 15
9.8.2. Sense STO State 15
9.8.3. Supply State 15
9.8.4. Sleep State 15
10. System Configuration 16
10.1. Configuration Pins and I²C 16
10.1.1. Configuration Pins 16
10.1.2. Configuration by I²C 16
10.2. Source Level Configuration 17
10.3. Storage Element Thresholds Configuration 17
10.4. Disable Storage Element Charging 18
10.5. I²C Serial Interface Protocol 19
10.6. Registers Map 21
10.7. Registers Configurations 23
10.7.1. Version Register (VERSION) 23
10.7.2. Source Voltage Regulation Register (SRCREGU) 23
10.7.3. Storage Element Threshold Registers (VOVDIS, VOVCH) 25
10.7.4. Temperature Register (TEMPCOLD, TEMPHOT) 25
10.7.5. Power Register (PWR) 26
10.7.6. Sleep Register (SLEEP) 27
10.7.7. Storage Element Acquisition Rate Register (STOMON) 28
10.7.8. Average Power Monitoring Control Register (APM) 28
10.7.9. IRQ Enable Register (IRQEN) 29
10.7.10. I²C Control (CTRL) 30

10.7.11. IRQ Flag Register (IRQFLG) 30
10.7.12. Status Register (STATUS) 31
10.7.13. Average Power Monitoring Data Registers (APM) 32
10.7.14. Temperature Data Register (TEMP) 32
10.7.15. Battery Voltage Register (STO) 33
Table 27: 33
10.8. External Components 34
10.8.1. Storage Element 34
10.8.2. External Inductor Information 34
10.8.3. External Capacitors Information 34
10.8.4. Optional External Components for Thermal Monitoring 34
10.8.5. Optional Pull-up Resistors for the I²C Interface 34
11. Typical Application Circuits 35
11.1. Example Circuit 1 35
11.2. Example Circuit 2 36
12. Circuit Behavior 37
13. Performance Data 40
13.1. DCDC Conversion Efficiency 40
13.2. Quiescent Current 42
14. Package Information 43
14.1. Plastic Quad Flatpack no-lead (QFN28 4x4mm) 43
14.2. QFN28 Board Layout 43
15. Minimum BOM 44
16. Layout 45
17. Glossary 47
18. Revision History 48

List of Figures

Figure 1: Simplified schematic view 6
Figure 2: Pinout diagram QFN28 7
Figure 3: Functional block diagram 12
Figure 4: Simplified schematic view of the AEM0090x 13
Figure 5: TH_REF and TH_MON connections 13
Figure 6: Average Power Monitoring description 14
Figure 7: Diagram of the AEM0090x state machine 15
Figure 8: I²C transmission frame 19
Figure 9: Read and write transmission 20
Figure 10: Typical application circuit 1 35
Figure 11: Typical application circuit 2 36
Figure 12: Start-up State 37
Figure 13: Supply State 37
Figure 14: Behavior with the Keep Alive mode and without the source 38
Figure 15: Behavior without the Keep Alive mode and without the source 38
Figure 16: Thermal Monitoring Behavior 39
Figure 17: AEM00901 DCDC conversion efficiency (LDCDC: Coilcraft LPS4018-333MRB) 40
Figure 18: AEM00900 DCDC conversion efficiency (LDCDC: TDK VLS252012HBX-6R8M-1) 41
Figure 19: Quiescent current 42
Figure 20: QFN28 4x4 mm 43
Figure 21: QFN28 4x4 mm board layout 43
Figure 22: AEM0090x schematic 44
Figure 23: AEM00900 QFN28 layout example 45
Figure 24: AEM00901 QFN28 layout example 46

List of Tables

Table 1: Pins description QFN28 7
Table 2: Absolute maximum ratings 9
Table 3: Thermal data 9
Table 4: Electrical characteristics 10
Table 5: Recommended operating conditions 11
Table 6: Configuration of SRC_LVL_CFG[5:0] 17
Table 7: Usage of STO_CFG[2:0] 18
Table 8: Register summary 21
Table 9: VERSION register 23
Table 10: SRCREGU register (0x01) 24
Table 11: TEMPCOLD register 25
Table 12: TEMPHOT register 26
Table 13: PWR register 26
Table 14: SLEEP register 27
Table 15: Configuration of the sleep threshold 27
Table 16: Acquisition rates for STO ADC 28
Table 17: APM register 28
Table 18: Configuration of APM computation windows 28
Table 19: IRQEN register 29
Table 20: CTRL register 30
Table 21: IRQFLG register 30
Table 22: Status register 31
Table 23: APM registers in pulse counter mode 32
Table 24: APM to nano-Joule conversion factor 32
Table 25: APM register in power meter mode 32
Table 26: TEMP register 32
Table 27: STO register 33
Table 28: Typical application circuit 2 register settings 36
Table 29: AEM0090x bill of material 44
Table 30: Revision history 48

Figure 1: Simplified schematic view

1. Introduction

The AEM0090x is a full-featured energy efficient battery charger able to charge a storage element (connected to STO) from an energy source (connected to SRC).

The core of the AEM0090x is a regulated switching converter (boost) with high power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 250 mV and a sparse amount of power of at least 5 µW is available at the source (KEEP_ALIVE set to HIGH), the AEM0090x coldstarts. After the cold start, the AEM extracts the power available from the source if the input voltage is higher than $V_{SRC,REG}$.

The AEM0090x can be fully configured through the I²C or partially by configuration pins. I²C configuration is not mandatory, as the default configuration is made to fit the most common needs, along with the configuration pins for the most common settings.

Through I²C communication or through the configuration pins, the user can select a specific operating mode from a variety of modes that cover most application requirements without any dedicated external component. The battery protection thresholds (V_{OVCH} and V_{OVDIS}) can be configured with the help of the STO_CFG[2:0] pins. They can also be configured in 60 mV steps using the I²C bus.

Depending on the harvester, the source regulation voltage, $V_{SRC,REG}$, can be configured using six configuration pins (SRC_LVL_CFG[5:0]) or using I²C communication.

The AEM0090x features an optional temperature protection. It can be set through the I²C interface and allows to define a temperature range so that, when the ambient temperature is outside that range, battery charging is disabled. One additional resistor and one additional thermistor are needed for this feature.

The KEEP_ALIVE functionality sets the source from which the AEM0090x supplies its internal circuitry VINT. It can be supplied either from the harvester connected on SRC or from the battery connected to STO.

When KEEP_ALIVE is disabled, the AEM0090x internal circuitry is running as long as enough energy is available on SRC. If no energy is available on SRC, the internal voltage drops down to reset voltage and the AEM needs to go through a cold start before being able to charge the battery again. This is useful for applications with long periods without energy on SRC and when the I²C is not used. If the I²C communication is used, the AEM will need to be reconfigured after the cold-start. With this setting there is no quiescent current taken from the battery to supply the AEM0090x and the power balance is always positive.

When KEEP_ALIVE is enabled, the AEM0090x is supplied by STO, the circuit stays in SUPPLY STATE or SLEEP STATE as long as the battery connected to STO is above the overdischarge threshold. It prevents loosing the I²C configuration when energy harvesting is not occurring and offers faster reactivity as the AEM is not reset depending on the available energy on SRC.

2. Pin Configuration and Functions

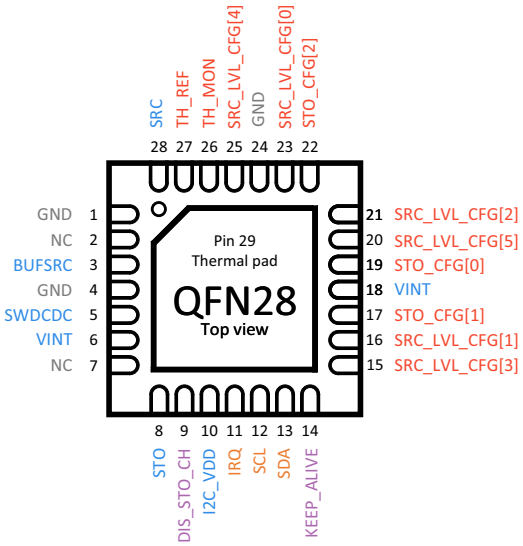


Figure 2: Pinout diagram QFN28

NAME	PIN NUMBER	Function
Power Pins		
SRC	28	Connection to the harvested energy source.
BUFSRC	3	Connection to an external capacitor buffering the boost converter input.
SWDCDC	5	Switching node of the boost converter.
VINT	6, 18	Internal supply voltage.
STO	8	Connection to the energy storage element (rechargeable battery). Cannot be left floating, voltage must always be above 2.5 V.
I2C_VDD	10	Connection to supply the I²C interface. - Connect to a 1.5 V to 5.0 V power supply if I²C is used. - Connect to GND if I²C is not used.
I²C Pins		
SDA	13	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	12	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	11	Output Interrupt request. Leave floating if not used.
Configuration Pins		
STO_CFG[0]	19	Used for the configuration of the threshold voltages for the energy storage element. Read as HIGH if left floating.
STO_CFG[1]	17	
STO_CFG[2]	22	
SRC_LVL_CFG[0]	23	Used for the configuration of the source voltage level. Read as HIGH if left floating.
SRC_LVL_CFG[1]	16	
SRC_LVL_CFG[2]	21	
SRC_LVL_CFG[3]	15	
SRC_LVL_CFG[4]	25	
SRC_LVL_CFG[5]	20	
TH_REF	27	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	26	Pin for temperature monitoring. Connect to VINT if not used.
Control Pins		
DIS_STO_CH	9	When HIGH, the AEM stops charging the battery. Read as LOW if left floating.
KEEP_ALIVE	14	When HIGH, the internal circuitry is supplied from STO. When LOW, the internal circuitry is supplied from SRC.

Table 1: Pins description QFN28

NAME	PIN NUMBER	Function
Other pins		
GND	1, 4, 24, 29 (thermal pad)	Ground connection, each terminal should be strongly tied to the PCB ground plane, pin 29 (thermal pad) being the main GND connection of the AEM0090x.
NC	2, 7	Not connected pins, leave floating.

Table 1: Pins description QFN28

3. Absolute Maximum Ratings

Parameter	Value
Voltage on SRC	2.0 V
Voltage on BUFSRC, SWDCDC, STO, I2C_VDD, SDA, SCL, IRQ, KEEP_ALIVE	5.5 V
Voltage on VINT, DIS_STO_CH, STO_CFG[2:0], SRC_LVL_CFG[5:0], TH_REF, TH_MON	2.75 V
Operating junction temperature	-40°C to 125°C
ESD HBM voltage	TBD
ESD CDM voltage	TBD

Table 2: Absolute maximum ratings

4. Thermal Resistance

Package	θJA	θJC	Unit
QFN28	TBD	TBD	°C/W

Table 3: Thermal data

ESD CAUTION

ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE
These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

5. Material

5.1. RoHS Compliance

e-peas product complies with RoHS requirement.

e-peas defines “RoHS” to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

5.2. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.

6. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Minimum source power required for cold start[1]	During cold start KEEP_ALIVE = VINT		5		µW
		During cold start KEEP_ALIVE = GND		14		µW
$V_{SRC,CS}$	Minimum source voltage required for cold start[1]			0.25		V
$V_{SRC,REG}$	Target regulation voltage of the source (depending on SRC_LVL_CFG[5:0] configuration or I²C register)		0.12		1.47	V
V_{OC}	Open-circuit voltage of the source				2.0	V
Storage Element						
V_{STO}	Voltage on the storage element		2.5		4.8	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging		3	See section 10.3	4.8	V
V_{OVDIS}	Minimum voltage accepted on the storage element before stopping to supply VINT if Keep-alive is enabled.		2.8		4.05	V
Internal supply & Quiescent Current						
V_{INT}	Internal supply voltage			2.2		V
$I_{QSUPPLY}$	Quiescent current on VINT in SUPPLY STATE	V_{STO} = 3.7 V		300		nA
I_{QSLEEP}	Quiescent current on VINT in SLEEP STATE	V_{STO} = 3.7 V		150		nA
I_{QSTO}	Quiescent current on STO when Keep-alive functionality is disabled			1		nA
$T_{RESET,SLEEP}$	Delay before V_{INT} crossing reset voltage when no energy on SRC and Keep-alive functionality disabled, or if Keep-alive is enabled but the battery voltage dropped below V_{OVDIS}	C_{INT} = 3.3 µF (leakage neglected), AEM in SLEEP STATE, no I²C communication		2.2		s
$T_{RESET,SUPPLY}$		C_{INT} = 3.3 µF (leakage neglected), AEM in SUPPLY STATE, no I²C communication		1.1		s
I²C interface						
Bus frequency				400	1000	kHz
I2C_VDD	I²C interface supply pin		1.5		5.0	V
SCL	I²C interface communication pins		Pull-up to I2C_VDD with resistors			
SDA						

Table 4: Electrical characteristics

1.These values are valid with the recommended BOM components (see Section 15)

7. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External Components						
L_{DCDC}	Inductor of the boost converter	AEM00900	3.3	6.8		µH
		AEM00901		33	47	
C_{SRC}	Capacitor decoupling the BUFSRC terminal		10			µF
C_{INT}	Capacitor decoupling V_{INT}		3.3			µF
C_{STO}	Capacitor decoupling the STO terminal[1]		5	22		µF
R_{DIV}	Optional - pull-up resistor for the thermal monitoring		5k	22k	33k	Ω
R_{TH}	Optional - NTC thermistor for the thermal monitoring	R0		10k		Ω
		Beta		3380		K
R_{SCL} / R_{SDA}	Optional - pull-up resistors for the I²C interface			1k		Ω
Logic input Pins						
SRC_LVL_CFG[5:0]	Configuration pins for the SRC voltage level	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
STO_CFG[2:0]	Configuration pins for the storage element thresholds	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
KEEP_ALIVE	Configuration for the “Keep alive” functionality	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
DIS_STO_CH	Configuration for disabling the charging of the battery	Logic HIGH	Connect to STO			
		Logic LOW	Connect to GND			

Table 5: Recommended operating conditions

1.Decoupling capacitor of at least 5µF is required to avoid damaging the AEM. The decoupling capacitor is to be sized according to the storage element internal resistance (ESR) to ensure optimal efficiency of the DCDC converter. It is recommended to use a capacitor of at least 22 µF when measuring the AEM0090x efficiency with laboratory equipment such as source measurement units (SMU). A battery must be connected to STO when a harvester is connected to the AEM to avoid damaging it.

8. Functional Block Diagram

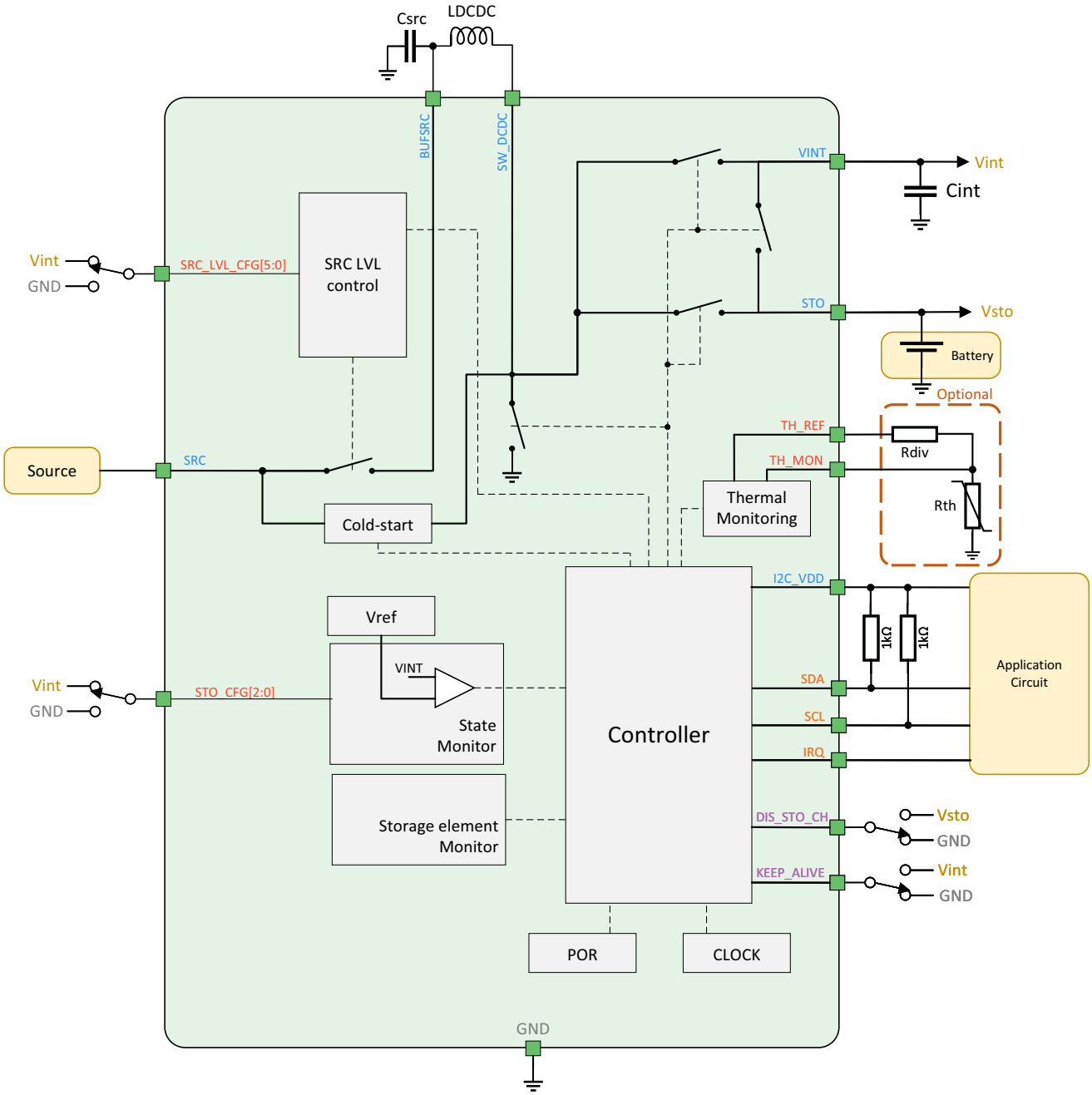


Figure 3: Functional block diagram

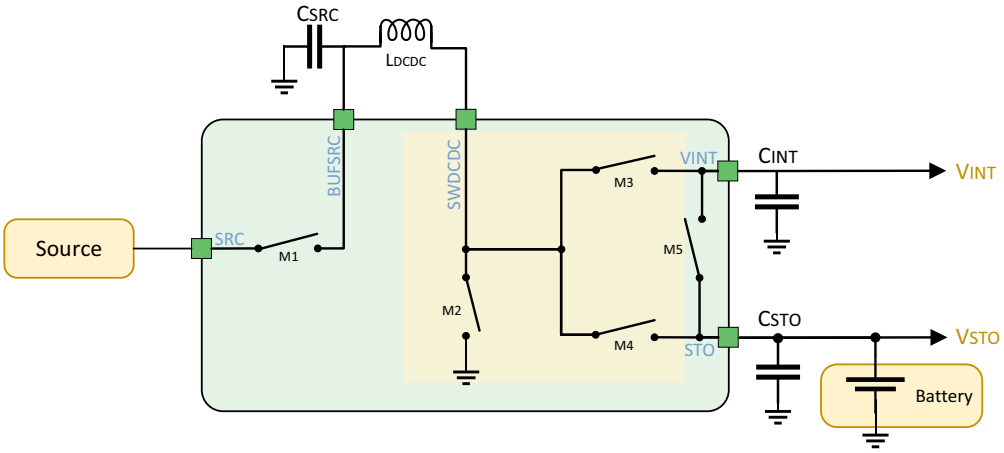


Figure 4: Simplified schematic view of the AEM0090x

9. Theory of Operation

9.1. Boost Converter

The boost (step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.8 V to 4.8 V, according to the system configuration. The switching transistors of the boost converter are M2, M3 and M4. The reactive power component of this converter is the external inductor L_{DCDC}.

When the boost converter is extracting energy from SRC, M1 is closed. BUFSRC is decoupled by the capacitor C_{SRC}, which smoothens the voltage against the current pulses induced by the boost converter.

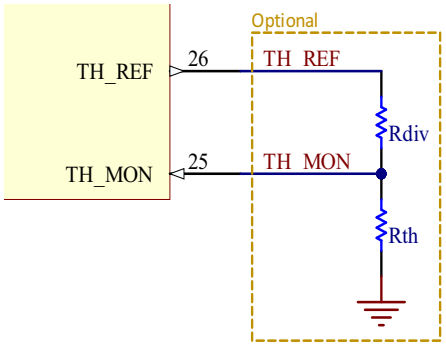
The storage element is connected to the STO pin, which voltage is V_{STO}. This node is linked to the output of the boost converter through transistor M4. When energy harvesting is occurring, the boost converter charges the battery. M4 disconnects the storage element when V_{STO} reaches V_{OVCH}. If VINT drops below its regulation value and if Keep-alive functionality is disabled, the AEM switches its output by enabling M3 instead of M4 until VINT reaches its target plus a small hysteresis. If the Keep-alive functionality is enabled, VINT is instead supplied from STO by modulating the gate of M5. In this case M3 is never activated.

9.2. Source Voltage Regulation

During SUPPLY STATE, the voltage on SRC is regulated to a voltage configured by the user. The AEM0090x offers a choice of one hundred and three values for the source voltage. If the open-circuit voltage of the harvester is lower than $V_{SRC,REG}$, the AEM0090x does not extract the power from the source. If the SRC voltage is higher, the AEM0090x regulates V_{SRC} to $V_{SRC,REG}$ and extracts power.

9.3. Thermal Monitoring

Thermal monitoring allows to protect the storage element by disabling the charge of the storage element and setting the STATUS.TEMP register when the temperature is outside of the defined temperature range. Enabling this functionality requires the use of a resistor (R_{DIV}) and a thermistor (R_{TH}). See Figure 5 for external components connections. The TH_REF terminal allows a reference voltage to be applied to the resistive divider while TH_MON is the measuring point. An ADC is measuring the voltage on TH_MON between 0 and 1 V. The temperature evaluation is done periodically (typ. every 8 s) to spare power. Information for the thermal monitoring is described in section 10.7.4. Thermal monitoring is optional, if not used connect TH_MON to VINT and leave TH_REF floating.



9.4. Average Power Monitoring

The Average Power Monitoring (APM) allows to evaluate the energy transfer from SRC to STO. The APM is able to determine the transferred energy by counting the number of current pulses transferred to STO by the boost converter over a configurable time window, and thus, evaluate the corresponding energy.

Two modes are available: Pulse Counter Mode and Power Meter Mode.

The APM behavior is described in Figure 6:

- **Phase A**:
  - **Pulse Counter Mode**: APM counts the number of DCDC pulses happening during T_A
  - **Power Meter Mode**: APM integrates the energy transferred from SRC to STO during T_A
- **Phase B**: APM waits during $T_B = T_A$
- **IRQ**: a rising edge is triggered on the IRQ pin, if IRQEN.APMDONE field is set to 1 (see Section 10.7.9 and Section 10.7.11). A rising edge on IRQ along with the IRQFLAG.APMDONE field set to 1 indicates to the user that a new value is available and ready to be read in the APM Data Register (Section 10.7.13).

Refer to Sections 10.7.8. and 10.7.13 for further details about how to set modes, how to convert registers value to Joule and how to set T_A.

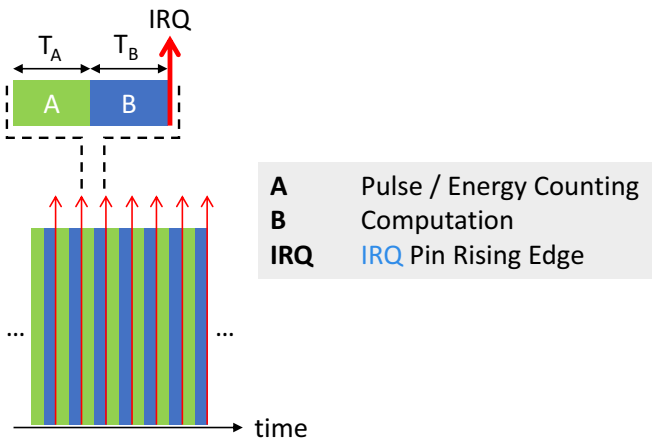


Figure 6: Average Power Monitoring description

9.5. Automatic High Power Mode (AEM00900 only)

When the AEM detects that the energy available on SRC is high enough, the boost converter automatically switches to high-power mode, increasing the harvesting current capability at the price of a slight efficiency degradation.

Preventing the AEM to switch to high-power mode may allow to use an inductor with half peak current rating for L_{DCDC} (see Section 10.8.2). On the other hand, allowing the AEM to switch to high-power mode increases the maximum current that the AEM can harvest from SRC to STO.

Automatic high-power mode is enabled by default and can be disabled by setting the PWR.HPEN to 0 through the I²C interface.

NOTE: this feature is not available on the AEM010901, that is always in high power mode.

9.6. Keep-alive

The internal circuitry connected to VINT can be supplied either by SRC through the boost converter (keep-alive disabled), or by the battery STO (keep-alive enabled).

When the keep-alive feature is disabled, the AEM0090x is supplied from SRC. The AEM will switch to RESET STATE if the energy on SRC is not sufficient.

When the keep-alive feature is enabled, the AEM0090x is supplied from STO. VINT is regulated as long as enough energy is available from the storage element connected on STO. The keep-alive feature allows to maintain the I²C registers configuration. Referring to Table 4, the quiescent current is then $I_{QSUPPLY}$ or I_{QSLEEP}, depending on whether the AEM0090x is in SUPPLY STATE or in SLEEP STATE.

9.7. IRQ Pin

The IRQ pin allows user to get notified when various events happen (rising edge on IRQ pin). At startup, the only flag that is enabled is I2CRDY, allowing user to know when the AEM0090x has finished to coldstart and thus, is out of RESET STATE and is ready to be programmed through I²C. Other flags can be enabled by writing the IRQEN register (Section 10.7.9). When the IRQ pin shows a rising edge, the flags can be determined by reading the IRQFLG register (Section 10.7.11). Reading the registers will reset the IRQ pin.

9.8. State Description

9.8.1. Reset State

In RESET STATE all nodes are deeply discharged and there is no available energy to be harvested. The AEM stays in this state until the source connected to SRC meets the cold start requirements long enough to make VINT rise up to 2.2 V. Cold start requirements depend on whether the Keep-alive feature is enabled or not:

- KEEP_ALIVE = 1:
  - V_{SRC} ≥ 250 mV
  - $P_{SRC,CS}$ ≥ 5 µW
- KEEP_ALIVE = 0:
  - V_{SRC} ≥ 250 mV
  - $P_{SRC,CS}$ ≥ 14 µW

When VINT has reached 2.2 V, the AEM0090x reads the configuration pins and switches to SENSE STO STATE.

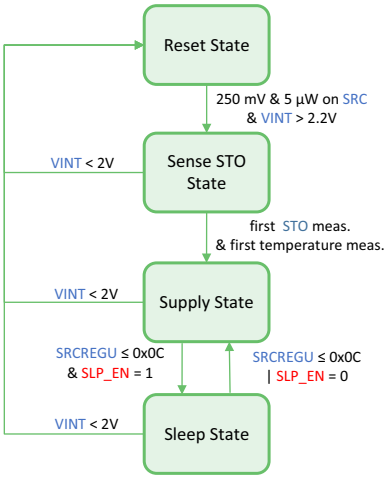


Figure 7: Diagram of the AEM0090x state machine

9.8.2. Sense STO State

In SENSE STO STATE the AEM0090x does the following measurements in order to know if the charging condition of the battery are met :

- Battery voltage on STO;
- Temperature through pins TH_MON and TH_REF (see Section 9.3. and 10.7.4.).

In this state, Once the measurements are done, AEM0090x switches to SUPPLY STATE.

9.8.3. Supply State

In SUPPLY STATE, the AEM transfers charges directly from to STO while maintaining V_{INT}.

If V_{INT} drops and the energy available on SRC is not sufficient to make V_{INT} rise again, there are two possible behaviors, depending on the 'Keep Alive' feature:

- If keep-alive is enabled, VINT is supplied by the battery through M5, so the AEM0090x stays in SUPPLY STATE while energy is available on the battery;
- If keep-alive is disabled, VINT will no longer be maintained and the AEM switches to RESET STATE.

9.8.4. Sleep State

Please note that the first condition for the AEM0090x to enter SLEEP STATE is to set the SLEEP.EN field in the SLEEP register 1, as shown on Figure 7.

In SLEEP STATE, the AEM power consumption is reduced. This mode may be used when the power available on the input is presumably low.

The AEM0090x enters sleep mode when the following conditions are met:

- Field SLEEP.EN in the SLEEP register is set to 1.
- SRCREGU register value is set to 0x0C (I^2C).

10. System Configuration

10.1. Configuration Pins and I²C

10.1.1. Configuration Pins

After a cold start, the AEM0090x reads the configuration GPIOs. Those are then read periodically every 2 s, with the exception of the DIS_STO_CH pin that is read every 1 s. The configuration pins can be changed on-the-fly and the corresponding configuration will be updated at the next IO reading. The floating configuration pins are read as HIGH, except DIS_STO_CH which is read as LOW.

10.1.2. Configuration by I²C

To configure the AEM0090x through the I²C interface after a cold start, the user must wait for the IRQ pin to rise, showing that the AEM0090x is out of RESET STATE and is ready to communicate with I²C. The interrupt is reseted by reading its register. Please note that the IRQ pin is always low during RESET STATE. See Section 10.7.11 for further informations about the IRQ pin.

Once IRQ goes HIGH, the user can then write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored and all the configurations are set by the register values. All registers have a default value, that can be found in Table 8. It is possible to go back to the GPIO configuration by resetting the CTRL.UPDATE bit. To apply any modification to the configuration, simply change the wanted registers value and set the CTRL.UPDATE bit again.

Registers are stored in a volatile memory, so their value are lost when VINT drops below the reset voltage (2 V), making the AEM0090x switch to RESET STATE. Thus, when using the I²C configuration, it is highly recommended to enable the keep-alive (see section 10.7.5.). If keep-alive functionality is disabled, register configuration is lost every time the energy available SRC is not sufficient to maintain V_{INT} above the reset voltage (2 V).

10.2. Source Level Configuration

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	L	L	H	H	L	0.12 V
L	L	L	H	H	H	0.13 V
L	L	H	L	L	L	0.15 V
L	L	H	L	L	H	0.16 V
L	L	H	L	H	L	0.18 V
L	L	H	L	H	H	0.19 V
L	L	H	H	L	L	0.21 V
L	L	H	H	L	H	0.22 V
L	L	H	H	H	L	0.24 V
L	L	H	H	H	H	0.25 V
L	H	L	L	L	L	0.27 V
L	H	L	L	L	H	0.28 V
L	H	L	L	H	L	0.30 V
L	H	L	L	H	H	0.33 V
L	H	L	H	L	L	0.36 V
L	H	L	H	L	H	0.39 V
L	H	L	H	H	L	0.42 V
L	H	L	H	H	H	0.45 V
L	H	H	L	L	L	0.48 V
L	H	H	L	L	H	0.51 V
L	H	H	L	H	L	0.54 V
L	H	H	L	H	H	0.57 V
L	H	H	H	L	L	0.60 V
L	H	H	H	L	H	0.63 V
L	H	H	H	H	L	0.66 V
L	H	H	H	H	H	0.69 V

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
H	L	L	L	L	L	0.72 V
H	L	L	L	L	H	0.75 V
H	L	L	L	H	L	0.78 V
H	L	L	L	H	H	0.81 V
H	L	L	H	L	L	0.84 V
H	L	L	H	L	H	0.87 V
H	L	L	H	H	L	0.90 V
H	L	L	H	H	H	0.93 V
H	L	H	L	L	L	0.96 V
H	L	H	L	L	H	0.99 V
H	L	H	L	H	L	1.02 V
H	L	H	L	H	H	1.05 V
H	L	H	H	L	L	1.08 V
H	L	H	H	L	H	1.11 V
H	L	H	H	H	L	1.14 V
H	L	H	H	H	H	1.17 V
H	H	L	L	L	L	1.20 V
H	H	L	L	L	H	1.23 V
H	H	L	L	H	L	1.26 V
H	H	L	L	H	H	1.29 V
H	H	L	H	L	L	1.32 V
H	H	L	H	L	H	1.35 V
H	H	L	H	H	L	1.38 V
H	H	L	H	H	H	1.41 V
H	H	H	L	L	L	1.44 V
H	H	H	L	L	H	1.47 V

Table 6: Configuration of SRC_LVL_CFG[5:0]

The source voltage regulation can be configured using GPIO or I²C communication.

Six dedicated configuration pins, SRC_LVL_CFG[5:0], allow selecting the $V_{SRC,REG}$ at which the source regulates its voltage. All configurations set below SRC_LVL_CFG[LLLHHL] will be set at 0.12 V.

The I²C communication allows more precision than the GPIO configuration (see Section 10.7.2), as SRCREGU.VALUE (0x01) is a 7-bit register.

10.3. Storage Element Thresholds Configuration

The user must set the voltage thresholds for which the storage element is considered to be discharged (V_{OVDIS}) and fully charged (V_{OVCH}).

V_{OVDIS} is configured on the VOVDIS (0x02) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\text{THRESH} = \frac{V_{OVDIS} - 0.50625}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value is 2.8 V. If the register value corresponds to V_{OVDIS} < 2.8 V, the threshold voltage is forced to 2.8 V.

V_{OVCH} is configured on the VOVCH (0x03) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\text{THRESH} = \frac{V_{OVCH} - 1.2375}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value is 3.0 V. If the register value corresponds to V_{OVCH} < 3.0 V, the threshold voltage is forced to 3.0 V.

It is also possible to configure V_{OVDIS} and V_{OVCH} with configuration pins STO_CFG[2:0] as shown in table 7.

Configuration	Storage element threshold		Battery type
STO_CFG[2:0]	V_{OVCH}	V_{OVDIS}	
LLL	4.50 V	3.30 V	NiCd 3 cells
LLH	4.00 V	2.80 V	Tadrian TLI1020A
LHL	3.63 V	2.80 V	LiFePO4
LHH	3.90 V	2.80 V	Tadrian HLC1020
HLL	3.90 V	3.50 V	Li-ion (ultra long life)
HLH	3.90 V	3.01 V	Li-ion (long life)
HHL	4.35 V	3.01 V	LiPo
HHH	4.12 V	3.01 V	Li-ion/solid-state/ NiMH

Table 7: Usage of STO_CFG[2:0]

DISCLAIMER: the provided storage element thresholds in the table above are indicative to support a wide range of storage element variants. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.

10.4. Disable Storage Element Charging

Pulling up DIS_STO_CH to STO disables the charging of the storage element connected to STO.

Please note that, if the keep-alive feature is enabled by pulling up KEEP_ALIVE to VINT, VINT is supplied by STO regardless of the setting of DIS_STO_CH. To make sure that the storage element is neither charged nor used to supply VINT, user must both tie DIS_STO_CH to STO and tie KEEP_ALIVE to GND.

10.5. I²C Serial Interface Protocol

The AEM0090x uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

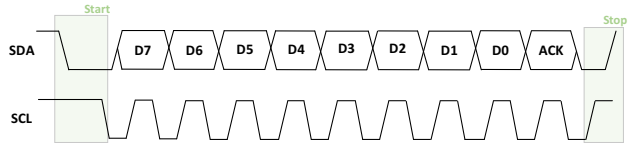


Figure 8: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM0090x is a slave that will receive configuration data or send the informations requested by the master.

The AEM0090x supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x40 or 0x41 for the AEM0090x, depending on the value of the I2C_ADDR pin. For packages where the I2C_ADDR pin is not present, the address is 0x41;
- Bit [0] is the communication mode: 1 for 'read mode' (used when the master reads informations from the slave) and 0 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCOLD register, the master sends the value 0x04;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMPHOT in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the SRC_REGU register, the master sends the value 0x18;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (STATUS.VOVDIS in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for writing several registers;

- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in the figure 9. Refer to Table 8 for all register addresses.

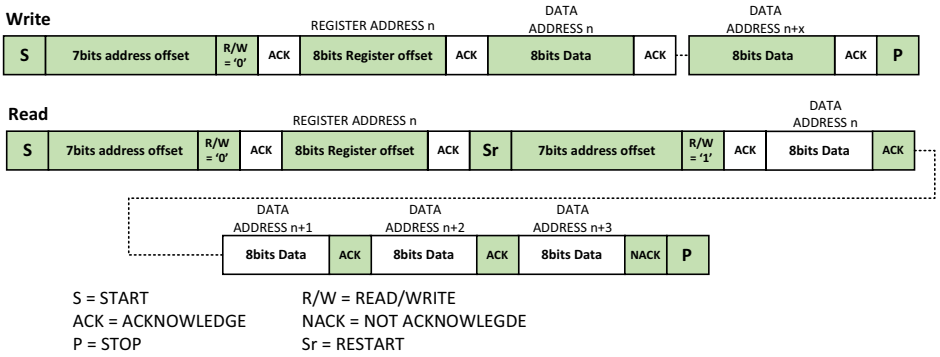


Figure 9: Read and write transmission

10.6. Registers Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	VERSION	[3:0]	MINOR	R	-	Chip ID
		[7:4]	MAJOR	R	-	
0x01	SRCREGU	[7:0]	VALUE	R/W	0x77 (1.47V)	Source voltage regulation
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.05V)	Overdischarge level of the storage element
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keepalive enable
		[1:1]	HPEN	R/W	0x01	AEM00900: High power mode enable AEM00901: Reserved
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable
		[3:3]	STOCHDIS	R/W	0x00	Battery charging disable
0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable
		[3:1]	SRCTHRESH	R/W	0x00	SRC LOW threshold
0x08	STOMON	[2:0]	RATE	R/W	0x00	ADC rate
0x09	APM	[0:0]	EN	R/W	0x00	APM enable
		[1:1]	MODE	R/W	0x00	APM mode
		[3:2]	WINDOW	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SRCTHRESH	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag
		[1:1]	VOVDIS	R	0x00	IRQ STOR OVDIS flag
		[2:2]	VOVCH	R	0x00	IRQ STOR OVCH flag
		[3:3]	SRCTHRESH	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP	R	0x00	IRQ temperature flag
		[5:5]	APMDONE	R	0x00	IRQ APM done flag
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS
		[2:2]	VOVCH	R	0x00	Status STO OVCH
		[3:3]	SRCTHRESH	R	0x00	Status SRC LOW
		[4:4]	TEMP	R	0x00	Status temperature
		[6:6]	CHARGE	R	0x00	Status STO CH
		[7:7]	BSTDIS	R	0x00	Status BST DIS GPIO
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0

Table 8: Register summary

Address	Name	Bit	Field Name	Access	RESET	Description
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data
0x12	STO	[7:0]	DATA	R	0x00	Battery voltage
0x13	RSVD	[7:0]	-	R	-	Reserved
0xE0	PN0	[7:0]	DATA	R	0X30	Part number 0 data
0xE1	PN1	[7:0]	DATA	R	0X30	Part number 1 data
0xE2	PN2	[7:0]	DATA	R	0X39	Part number 2 data
0xE3	PN3	[7:0]	DATA	R	0X30	Part number 3 data
0xE4	PN4	[7:0]	DATA	R	0X31	Part number 4 data

Table 8: Register summary

10.7. Registers Configurations

10.7.1. Version Register (VERSION)

The VERSION register holds the version of the chip, with major and minor revision numbers.

VERSION Register	0x00	R
Bit [7:4]	Bit [3:0]	
MAJOR	MINOR	
0x00	0x00	

Table 9: VERSION register

Bit [7:4]: major revision number (VERSION.MAJOR).

Bit [3:0]: minor revision number (VERSION.MINOR).

10.7.2. Source Voltage Regulation Register (SRCREGU)

The source voltage regulation can be set thanks to the I²C communication with more precision. The register is made of 7 bits. Use the table 10 to set the SRCREGU.VALUE register according the desired $V_{SRC,REG}$.

SRC .DATA [7:0]	$V_{SRC,REG}$ [V]	SRC .DATA [7:0]	$V_{SRC,REG}$ [V]	SRC .DATA [7:0]	$V_{SRC,REG}$ [V]	SRC .DATA [7:0]	$V_{SRC,REG}$ [V]
0x00	0.1125	0x25	0.3	0x40	0.705	0x5B	1.11
...	0.1125	0x26	0.315	0x41	0.72	0x5C	1.125
0x0C	0.1125	0x27	0.33	0x42	0.735	0x5D	1.14
0x0D	0.12	0x28	0.345	0x43	0.75	0x5E	1.155
0x0E	0.1275	0x29	0.36	0x44	0.765	0x5F	1.17
0x0F	0.135	0x2A	0.375	0x45	0.78	0x60	1.185
0x10	0.1425	0x2B	0.39	0x46	0.795	0x61	1.2
0x11	0.15	0x2C	0.405	0x47	0.81	0x62	1.215
0x12	0.1575	0x2D	0.42	0x48	0.825	0x63	1.23
0x13	0.165	0x2E	0.435	0x49	0.84	0x64	1.245
0x14	0.1725	0x2F	0.45	0x4A	0.855	0x65	1.26
0x15	0.18	0x30	0.465	0x4B	0.87	0x66	1.275
0x16	0.1875	0x31	0.48	0x4C	0.885	0x67	1.29
0x17	0.195	0x32	0.495	0x4D	0.9	0x68	1.305
0x18	0.2025	0x33	0.51	0x4E	0.915	0x69	1.32
0x19	0.21	0x34	0.525	0x4F	0.93	0x6A	1.335
0x1A	0.2175	0x35	0.54	0x50	0.945	0x6B	1.35
0x1B	0.225	0x36	0.555	0x51	0.96	0x6C	1.365
0x1C	0.2325	0x37	0.57	0x52	0.975	0x6D	1.38
0x1D	0.24	0x38	0.585	0x53	0.99	0x6E	1.395
0x1E	0.2475	0x39	0.6	0x54	1.005	0x6F	1.41
0x1F	0.255	0x3A	0.615	0x55	1.02	0x70	1.425
0x20	0.2625	0x3B	0.63	0x56	1.035	0x71	1.44
0x21	0.27	0x3C	0.645	0x57	1.05	0x72	1.455
0x22	0.2775	0x3D	0.66	0x58	1.065	0x73	1.47
0x23	0.285	0x3E	0.675	0x59	1.08	...	1.47
0x24	0.2925	0x3F	0.69	0x5A	1.095	0x75	1.47

Table 10: SRCREGU register (0x01)

To find the other correlations between the voltages and the values to put in the register, the user can use those formulas:

If the desired $V_{SRC,REG}$ is between 0.12V and 0.30V:

$$VALUE = \frac{V_{SRC,REG} - 0.0225}{0.0075}$$

If the desired $V_{SRC,REG}$ is between 0.30V and 1.47V:

$$VALUE = \frac{V_{SRC,REG} + 0.255}{0.015}$$

If SRCREG.VALUE is set to 0b0001100 and that SLEEP.EN is set, the AEM0090x switches to SLEEP STATE.

10.7.3. Storage Element Threshold Registers (VOVDIS, VOVCH)

The configuration of the storage element thresholds is done by setting two different registers through the I²C communication:

- The V_{OVDIS} threshold is configured in register VOVDIS (0x02);
- The V_{OVCH} threshold is configured in register VOVCH (0x03).

The information about the storage element threshold voltage is available on section 10.3.

10.7.4. Temperature Register (TEMPCOLD, TEMPHOT)

The configuration of the temperature thresholds is done by setting two registers through I²C communication:

- The low temperature threshold is configured in register TEMPCOLD (0x04);
- The high temperature threshold is configured in register TEMPHOT (0x05).

The temperature protection uses a voltage divider consisting of the resistor R_{DIV} and the thermistor $R_{TH}(T)$. Considering the specifications of the thermistor used, it is possible to determine the relationship between the temperature and the resistance of the thermistor. The following equation must therefore be applied to determine the value to be written to the register:

$$THRES = 256 \cdot \frac{R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

The equation is the same for both the high and the low thresholds. THRESH is the value to be written to the registers, $R_{TH}(T)$ is the resistance of the thermistor at the threshold temperature and R_{DIV} is the resistance that creates a resistive divider with $R_{TH}(T)$, as shown on figure 5. The AEM0090x determines if the ambient temperature is within the range previously set by measuring the voltage on pin TH_MON.

The following equations are useful to determine the temperature from the THRES register field value:

$$R_{TH}(T) = R0 \cdot e^{B \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

$$T = \frac{B}{\ln\left(\frac{R_{TH}(T)}{R0}\right) + \frac{B}{T_0}}$$

- THRESH is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R0 [Ω] is the resistance of the NTC thermistor at ambient temperature T_0 = 298.15 K (25 °C).
- $R_{TH}(T)$ [Ω] is the resistance of the thermistor at temperature T [K].
- T_0 [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

For example with a Murata NCP15XH103J03RC the default thresholds are 0°C and 45°C (see table 8), which matches the specifications of most Li-Ion batteries.

10.7.4.1. TEMPCOLD

Minimum temperature (cold) for storage element charging register.

TEMPCOLD Register	0x04	R/W
Bit [7:0]		
THRESH		
0x8F		

Table 11: TEMPCOLD register

Bit [7:0]: THRESH (TEMPCOLD.THRESH).

This fields is used to configure the minimum temperature (cold) threshold.

10.7.4.2. TEMPHOT

Maximum temperature (hot) for storage element charging register.

TEMPHOT Register	0x05	R/W
Bit [7:0]		
THRESH		
0x2F		

Table 12: TEMPHOT register

Bit [7:0]: THRESH (TEMPHOT.THRESH).

This fields is used to configure the maximum temperature (hot) threshold.

10.7.5. Power Register (PWR)

The PWR (0x06) register is dedicated to the power settings of the AEM0090x and is made of 4 bits:

PWR Register	0x06		R/W	
Bit [7:4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	STOCHDIS	TMONEN	AEM00900: HPEN AEM00901: Reserved	KEEPALEN
0x00	0	1	1	1

Table 13: PWR register

Bit [3]: Battery charging disable (PWR.STOCHDIS).

This register is allowed in read and write mode.

Setting this bit to 0 allows the charging of the battery. Setting this bit to 1 disables it.

Bit [2]: Temperature monitoring enable (PWR.TMONEN).

The temperature monitoring enable bit enables the monitoring of the ambient temperature.

Setting this bit to 1 enables the temperature monitoring. Setting this bit to 0 disables it.

Bit [1]: High-power mode enable (PWR.HPEN).

Setting this bit to 1 allows the AEM to automatically enter high-power mode if needed, allowing for more power to be harvested from SRC (see section 9.5.).

Setting this bit to 0 disables automatic high-power mode.

NOTE: the PWR.HPEN field is only available on the AEM00900 and is reserved on the AEM00901.

Bit [0]: Keep alive enable (PWR.KEEPALEN).

This field defines the energy source from which the AEM0090x supplies VINT (internal circuitry).

When PWR.KEEPALEN is set to 0, VINT is supplied by SRC through the boost converter. When PWR.KEEPALEN field is set to 1, VINT is supplied by STO. Refer to section 9.6. for more information.

NOTE: disabling the Keep alive feature is not recommended when configuring the AEM0090x with I²C registers, see Section 9.6.

10.7.6. Sleep Register (SLEEP)

The Sleep register SLEEP (0x07) enables the sleep mode and sets the conditions for entering the sleep mode.

SLEEP Register	0x07	R/W
Bit [7:4]	Bit [3:1]	Bit [0]
RESERVED	SRCTHRESH	EN
0x00	0x00	1

Table 14: SLEEP register

SLEEP.SRCTHRESH	
Configuration	SRC threshold
0x00	0.105 V
0x01	0.202 V
0x02	0.255 V
0x03	0.300 V
0x04	0.360 V
0x05	0.405 V
0x06	0.510 V
0x07	0.600 V

Table 15: Configuration of the sleep threshold

Bit [3:1]: Sleep threshold (SLEEP.SRCTHRESH)

This field sets the voltage threshold below which the AEM0090x enters SLEEP STATE. Table 15 shows the available settings.

For example, if the sleep threshold is set to 010, the AEM will go into SLEEP STATE if the source target voltage is set below 0.255 V.

Bit [0]: Sleep mode enable (SLEEP.EN)

This field enables SLEEP STATE when set to 1. When set to 0, the AEM0090x will never switch to SLEEP STATE. The SRC threshold is set by default at 0.105 mV.

10.7.7. Storage Element Acquisition Rate Register (STOMON)

This field (STOMON, 0x08) configures the acquisition rate of the ADC that measures STO voltage. Depending on the application, the source and the storage element, the user might want to increase the frequency of the acquisitions of the battery voltage, so that the acquisition rate is significantly faster than the expected voltage variation on the battery. Increasing this frequency increases the energy consumption of the AEM0090x.

STOMON Register (0x08)		
Configuration	Sampling rate	Additional consumption on storage element (typ.)
0x00	Every 1.024 s	0.4 nA
0x01	Every 512 ms	0.8 nA
0x02	Every 256 ms	1.6 nA
0x03	Every 128 ms	3.2 nA
0x04	Every 64 ms	6.4 nA

Table 16: Acquisition rates for STO ADC

10.7.8. Average Power Monitoring Control Register (APM)

Average Power Monitoring (APM; register address 0x09) allows for estimating the energy transferred from the source to the battery over a certain period of time.

APM Register	**0x09**	**R/W**	
Bit [7:4]	Bit [3:2]	Bit [1]	Bit [0]
RESERVED	WINDOW	MODE	EN
0x00	0x00	0	0

Table 17: APM register

Bit [3:2]: APM computation window (APM.WINDOW)

This field is used to select the APM computation window (noted T_A in Section 9.4). The energy transferred is integrated over this configurable time window.

APM.WINDOW		
Configuration	Computation window	APM register refresh rate
0x00	128 ms	256 ms
0x01	64 ms	128 ms
0x02	32 ms	64 ms

Table 18: Configuration of APM computation windows

Please note that, as described in Section 9.4, measurement period is twice the computation window, meaning that a new measurement is available every 2 x T_A.

Bit [1]: APM mode (APM.MODE)

The APM implements two modes:

- **Power meter mode**: the number of pulses during a period is multiplied by a value to obtain the energy that has been transferred taking into account the efficiency of the AEM0090x. This mode is enabled by setting the APM mode bit to 1.
- **Pulse counter mode**: the AEM0090x counts the number of current pulses drawn by the boost converter. This mode is enabled by setting the APM mode bit to 0.

Bit [0]: APM enable (APM.EN)

This field enables the APM feature. When the APM.EN field bit is set to 1, it is enabled. If APM.EN field is set to 0, the feature is disabled.

10.7.9. IRQ Enable Register (IRQEN)

Interrupts enable register: configures on which event the IRQ pin is set HIGH.

IRQEN Register				0x0A		R/W	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	APMERR	APMDONE	TEMP	SRCTHRESH	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 19: IRQEN register

Bit [6]: IRQ APM error enable (IRQEN.APMERR)

Setting this bit enables the IRQ pin to be asserted (HIGH) when an APM error occurs

Bit [5]: IRQ APM done enable (IRQEN.APMDONE)

Setting this bit enables the IRQ pin to be asserted (HIGH) when new APM data is available.

Bit [4]: IRQ temperature enable (IRQEN.TEMP)

Setting this bit enables the IRQ pin to be asserted (HIGH) when the temperature crosses the minimum or maximum temperature allowed to charge the battery (see section 10.7.4.).

Bit [3]: IRQ source low enable (IRQEN.SRCTHRESH)

Setting this bit enables the IRQ pin to be asserted (HIGH) when $V_{SRC,REG}$ crosses the SRC LOW threshold (112mV).

Bit [2]: IRQ storage over-charge enable (IRQEN.VOVCH)

Setting this bit enables the IRQ pin to be asserted (HIGH) when the battery voltage crosses the V_{OVCH} threshold.

Bit [1]: IRQ storage over-discharge enable (IRQEN.VOVDIS)

Setting this bit enables the IRQ pin to be asserted (HIGH) when the storage element voltage crosses the V_{OVDIS} threshold.

Bit [0]: IRQ serial interface ready enable (IRQEN.I2CRDY)

This bit is activated by default.

When the AEM0090x has coldstarted and is ready to communicate through I²C. The IRQ pin is asserted (HIGH).

10.7.10. I²C Control (CTRL)

Control register.

CTRL Register	0x0B	R/W	
Bit [7:3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	SYNCBUSY	RESERVED	UPDATE
0x00	0	0	0

Table 20: CTRL register

Bit [2]: SYNCBUSY (CTRL.SYNCBUSY).

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not.

- 0: NSYNC - R: CTRL register not synchronizing.
- 1: SYNC - R: CTRL register synchronizing.

Bit [0]: UPDATE (CTRL.UPDATE).

This field is used to control the source of the AEM0090x configuration (GPIO or I²C).

Furthermore, this field is used to update the AEM0090x configuration with the current configuration from the I²C registers.

- 0: GPIO
  - W: load configurations from the GPIO.
  - R: configurations from the GPIO is currently used if read as 0.
- 1: I2C
  - W: load configurations from the I²C registers.
  - R: configurations from the I²C is currently used if read as 1.

NOTE: if the AEM0090x is already configured through the I²C registers, writing any register does not have any effect until 1 is written to the CTRL.UPDATE field, leading to the AEM0090x to read the new register values and apply them.

NOTE: when using I²C register configuration, user can switch back to GPIO configuration by writing 0 to the CTRL.UPDATE field. In that case, the settings previously written to the IRQEN registers are still valid even when using GPIO configuration, as well as the data in IRQFLG register.

10.7.11. IRQ Flag Register (IRQFLG)

The IRQFLG (0x0C) register contains all interrupt flags, corresponding to those enabled in the IRQEN register. This register is reseted when read.

IRQFLG Register			0x0C			R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	APMERR	APMDONE	TEMP	SRCTHRESH	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 21: IRQFLG register

Bit [6]: IRQ APM error Flag (IRQFLG.APMERR)

This interrupt flag is set to 1 when an APM error occurs.

Bit [5]: IRQ APM done Flag (IRQFLG.APMDONE)

This interrupt flag is set to 1 when a new APM data is available, if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption is not triggered.

Bit [4]: IRQ temperature Flag (IRQFLG.TEMP)

This interrupt flag is set to 1 when the temperature crosses the minimum or maximum temperature (selected through the TEMPCOLD and TEMPHOT registers), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption is not triggered.

Bit [3]: IRQ source low Flag (IRQFLG.SRCTHRESH)

This interrupt flag is set to 1 when $V_{SRC,REG}$ crosses the SRC LOW voltage (112mV), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption is not triggered.

Bit [2]: IRQ storage over-charge Flag (IRQFLG.VOVCH)

This interrupt flag is set to 1 when the battery crosses the overcharge voltage (selected through the VOVCH register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption is not triggered.

Bit [1]: IRQ storage over-discharge Flag (IRQFLG.VOVDIS)

This interrupt flag is set to 1 when the battery crosses the overdischarge voltage (selected through the VOVDIS register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption is not triggered.

Bit [0]: IRQ serial interface ready Flag (IRQFLG.I2CRDY)

This interrupt flag is set to 1 when the AEM0090x has coldstarted and is ready to communicate through I²C (the corresponding interrupt source is enabled by default). If this bit is 0, this interruption has not triggered.

10.7.12. Status Register (STATUS)

The STATUS (0x0D) register contains informations about the status of the AEM0090x.

STATUS Register				0x0D		R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
BSTDIS	CHARGE	RESERVED	TEMP	SRCTHRESH	VOVCH	VOVDIS	RESERVED
0	0	0	0	0	0	0	0

Table 22: Status register

Bit [7]: Status BSTDIS (STATUS.BSTDIS)

This status indicates whether the storage charging is enabled or not via the GPIO or I²C. If this bit is set to 0, the storage element charging is enabled. If it is set to 1, the storage element charging is disabled.

Bit [6]: Status STOR CH (STATUS.CHARGE)

This status indicates whether the AEM is currently charging the battery or not. If this bit is set to 0, the storage element is charging. If it is set to 1, the storage element is not charging.

Set condition:

$$(V_{STO} < V_{OVCH}) \ \& \ \overline{\text{STATUS.TEMP}} \ \& \ \overline{\text{STATUS.BSTDIS}}$$

$$\& \ (\text{OVDIS STATE} \mid \text{SUPPLY STATE} \mid \text{SHUTDOWN STATE})$$

Bit [4]: Temperature Status (STATUS.TEMP)

This bit is set to 1 if the ambient temperature is outside the range defined by the TEMPCOLD and TEMPHOT registers. It is set to 0 is the temperature is within this range.

Bit [3]: Status SRC LOW (STATUS.SRCTHRESH)

This status indicates whether the source target voltage is higher or lower than the sleep level threshold (112mV). If the source target voltage is higher than the sleep level then the field is set to 0, else the field is set to 1.

Bit [2]: Status STOR OVCH (STATUS.VOVCH)

This status indicates whether the battery voltage is higher or lower than the overcharge level threshold. If the battery voltage rises above V_{OVCH} then the field is set to 1, else it is set to 0.

Bit [1]: Status STOR OVDIS (STATUS.VOVDIS)

This status indicates whether the battery is higher or lower than the overdischarge level threshold. If the battery voltage goes below V_{OVDIS} then the field is set to 1, else it is set to 0.

10.7.13. Average Power Monitoring Data Registers (APM)

The APM (0x0E, 0x0F, 0x10) registers contain the Average Power Monitoring data. Depending on the mode of the APM configured in the APM control register (APM), data is processed differently:

- **Pulse Counter Mode**: the number of pulses is distributed within the registers described in Table 23.

APM0 Register (0x0E)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

APM1 Register (0x0F)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

APM2 Register (0x10)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED			DATA[20:16]				

Table 23: APM registers in pulse counter mode

- **Power Meter Mode**: the energy value E_{APM} in nano-joule is determined by left bit-shifting (SHIFT bits) the value in the DATA field (see Table 25) and applying the following formula:

$$E_{APM} = (DATA \ll SHIFT) \cdot \alpha$$

Product	L_{DCDC}	V_{SRC}	α
AEM00900	3.3 µH	0.25 V to 0.70 V	0.16886
		0.70 V to 1.47 V	0.19774
	4.7 µH	0.25 V to 0.70 V	0.13658
		0.70 V to 1.47 V	0.15930
	6.8 µH	0.25 V to 0.70 V	0.08817
		0.70 V to 1.47 V	0.10166
AEM00901	33 µH	0.25 V to 0.70 V	0.04108
		0.70 V to 1.47 V	0.03607

Table 24: APM to nano-Joule conversion factor

NOTE: the conversion ratio α is proportional to the inductance of L_{DCDC}. Values from Table 24 are valid for the nominal values stated.

APM0 Register (0x0E)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

APM1 Register (0x0F)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

APM2 Register (0x10)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
SHIFT[3:0]				DATA[19:16]			

Table 25: APM register in power meter mode

10.7.14. Temperature Data Register (TEMP)

This field contains the result of the ADC acquisition for the temperature monitoring. The voltage at the terminals of the voltage divider can be derived by applying the following equation, with V_{REF} = 1 V:

$$V_{TH} = \frac{V_{REF} \cdot DATA}{256}$$

Or, in order to make a comparison with the table in the thermistor datasheet, it is possible to find the impedance of the thermistor:

$$R_{TH} = R_{DIV} \cdot \frac{DATA}{256 - DATA}$$

TEMP Register	0x11	R
Bit [7:0]		
DATA		
0x00		

Table 26: TEMP register

10.7.15. Battery Voltage Register (STO)

The STO (0x12) contains the 8 bits result from the ADC acquisition of the battery voltage. To convert the result to Volts, the following equation is applied.

$$V_{STO} = \frac{4.8V \cdot DATA}{256}$$

STO Register	0x12	R
Bit [7:0]		
DATA		
0x00		

Table 27: STO register

10.8. External Components

10.8.1. Storage Element

The storage element of the AEM0090x must be a rechargeable battery, which size should be chosen so that its voltage does not fall below V_{OVDIS} even during occasional current peak from the battery to the load connected on it. To keep the chip functionality, minimum voltage on STO pin shall never fall below 2.8V.

The monitoring of the storage element is done periodically. It is therefore possible that the storage element may be overloaded if it is incorrectly sized.

It is mandatory to buffer the battery with a capacitor C_{STO} if the internal resistance of the battery is high, to ensure that the current pulled from the battery by the application circuit does not ever make the battery voltage fall below 2.8 V.

A minimal decoupling capacitor of 22 µF is recommended to obtain optimal DCDC converter efficiency when using high ESR battery, or when measuring efficiency using laboratory equipments such as source measurement units (SMU).

10.8.2. External Inductor Information

L_{DCDC}

The AEM0090x operates with one standard miniature inductor. L_{DCDC} must comply to the following:

- Peak current rating must be at least 1 A for a 3.3 µH inductor in high-power mode and 500 mA if high-power mode is disabled. Current rating decreases linearly when inductor value increases.
- Switching frequency must be at least 10 MHz.
- ESR as low as possible as it has a strong influence on DCDC efficiency.
- The recommended values for optimal efficiency is:
  - 6.8 µH for AEM00900
  - 33 µH for AEM00901

10.8.3. External Capacitors Information

C_{SRC}

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage variations when the buck-boost converter is active. The recommended value is 10 µF.

C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The recommended value is 3.3 µF.

C_{STO}

This capacitor allows for buffering the current peaks of the boost converter output.

10.8.4. Optional External Components for Thermal Monitoring

The following components are required for the thermal monitoring:

- One resistor, typ. 22 kΩ ±20% (PNRC0402FR-0722KL)
- One NTC thermistor, typ. R0 = 10 kΩ ±5% and Beta = 3380 K ±3% (NCP15XH103J03RC)

10.8.5. Optional Pull-up Resistors for the I²C Interface

SDA and SCL must be pulled-up by resistors (1 kΩ typical) if the I²C interface is used. The value must be determined according to the I²C mode used.

11. Typical Application Circuits

11.1. Example Circuit 1

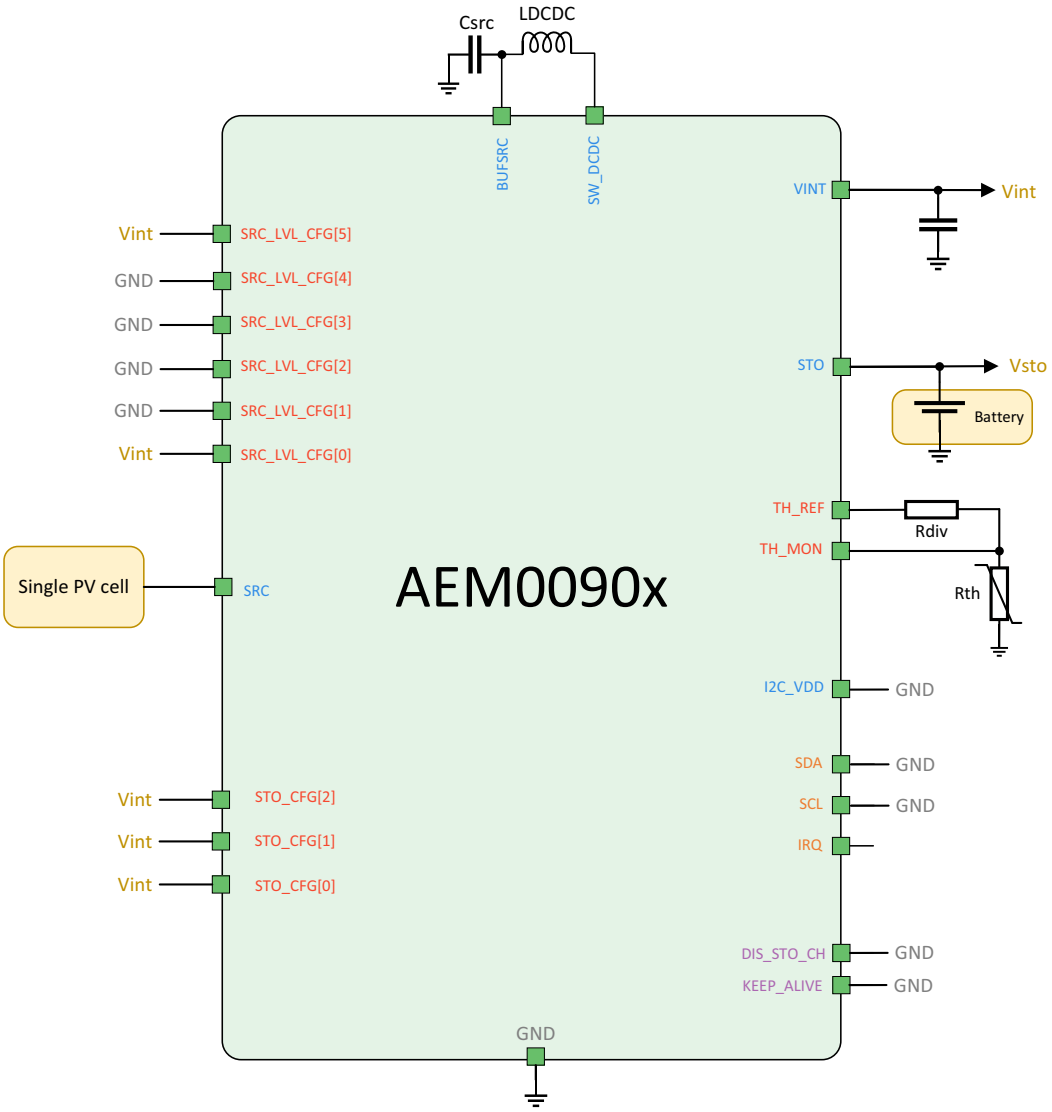


Figure 10: Typical application circuit 1

The circuit is an example of a system with solar energy harvesting with the AEM0090x. It uses a Li-ion rechargeable battery as energy storage.

- Energy source: PV cell.
- SRC_LVL_CFG[5:0] = HLLLLH: The source voltage regulation is set to 0.75V to extract the maximum power of the PV cell.
- STO_CFG[2:0] = HHH: The storage element is a Li-ion battery.
- V_{OVCH} = 4.12 V
- V_{OVDIS} = 3.01 V
- The thermal monitoring is used with a default threshold value (TEMPCOLD = 0°C, TEMPHOT = 45°C) with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC.
- The I²C communication is not used.
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled.

11.2. Example Circuit 2

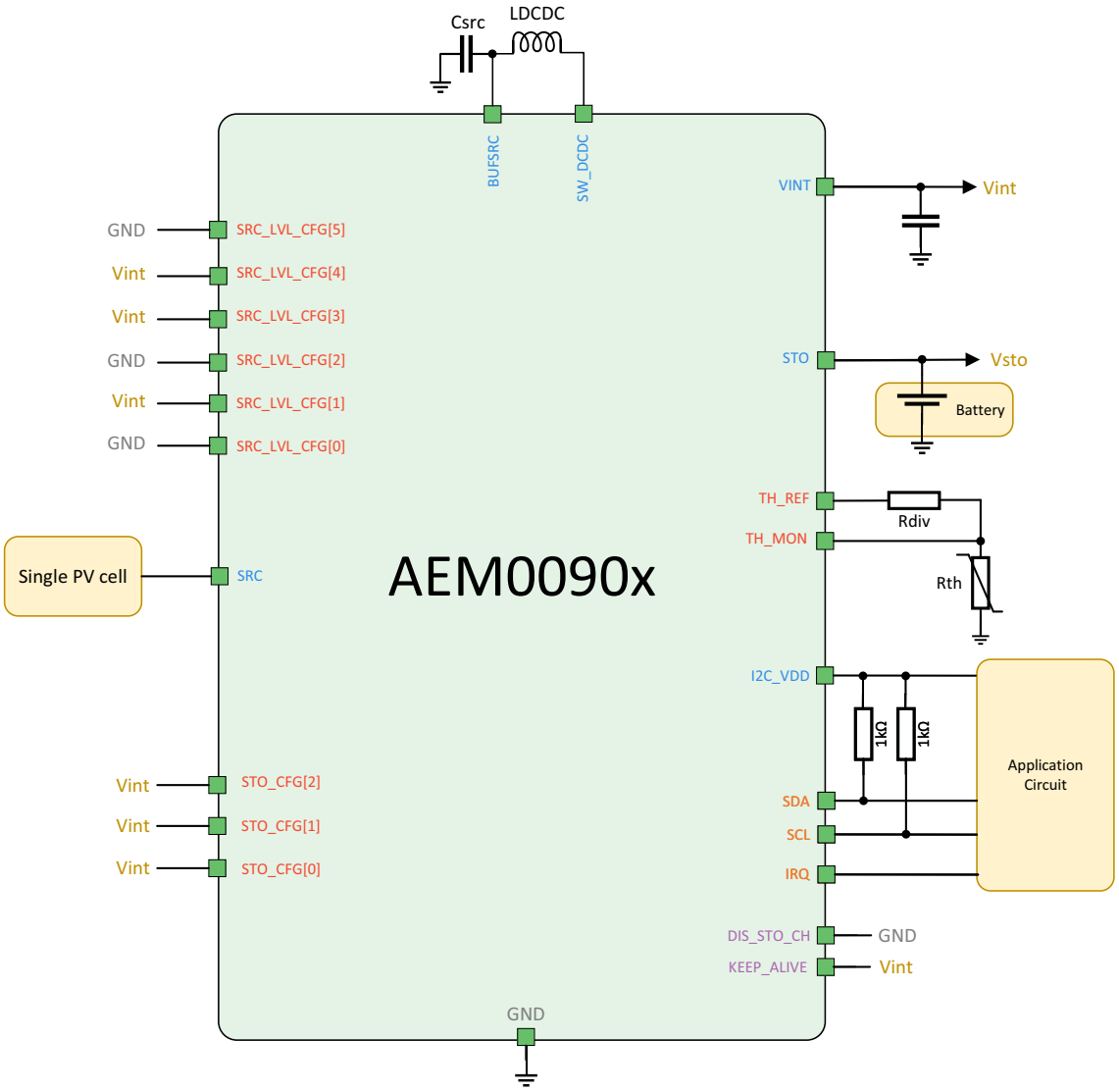


Figure 11: Typical application circuit 2

The circuit is a example of a system with solar energy harvesting with the AEM0090x. It uses a NiCd 3 cells battery as storage element.

- Energy source: PV cell
- SRC_LVL_CFG[5:0]: Configured through the I²C communication (0.555 V)
- STO_CFG[2:0]: Configured through the I²C communication
  - V_{OVCH} = 4.12 V
  - V_{OVDIS} = 3.30 V
- The thermal monitoring is used and the thresholds are configured through the I²C communication (Cold threshold = 10°C, Hot threshold = 60°C with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC).
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled.

Register Address	Register Name	Value
0x01	SRCREGU	0011 0110
0x02	VOVDIS	0011 0010
0x03	VOVCH	0011 0011
0x04	TEMPCOLD	0111 0100
0x05	TEMPHOT	0001 1111

Table 28: Typical application circuit 2 register settings

NOTE: a configuration tool is available on e-peas website. It helps the user to read and write registers.

12. Circuit Behavior

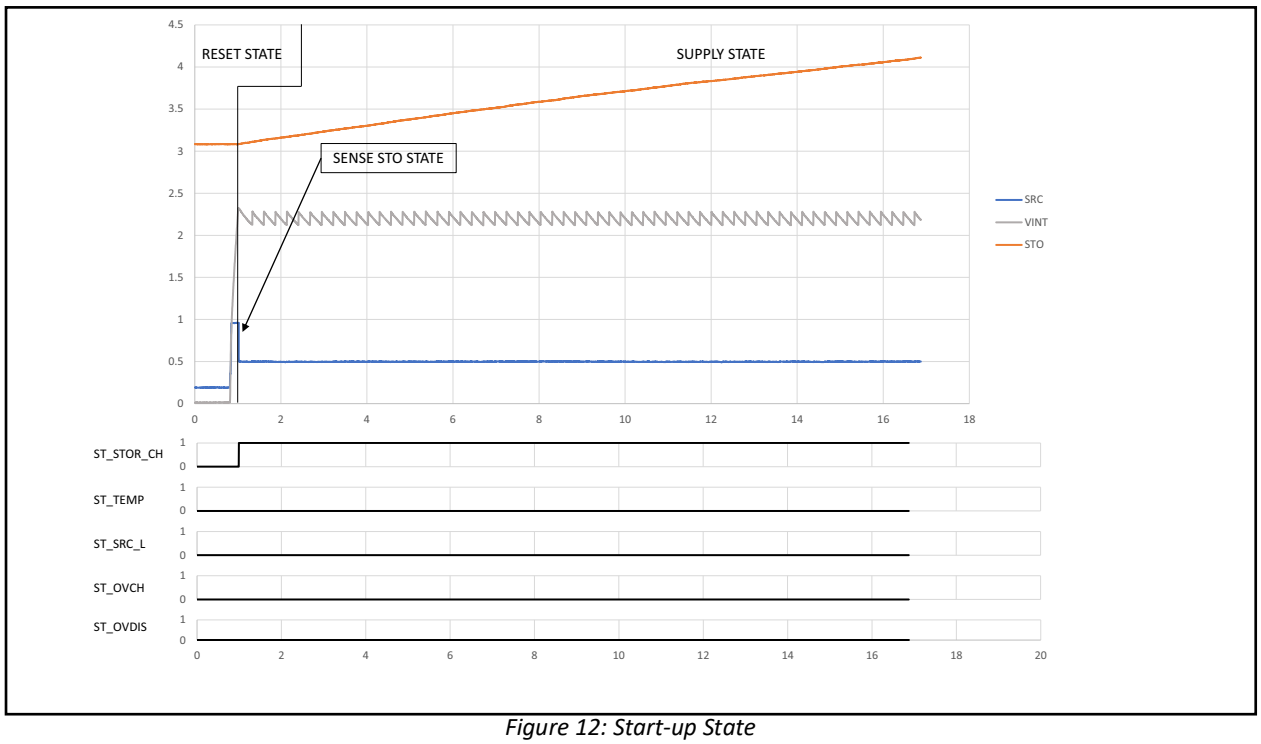


Figure 12: Start-up State

STO_CFG[2:0] = HHH, SRC_LVL_CFG[5:0] = LHHLLH, storage element: capacitor (10 mF) pre-charged to 3V, SRC: current source 5 mA with voltage compliance (1.0 V), DIS_STO_CH = GND, KEEP_ALIVE = H.

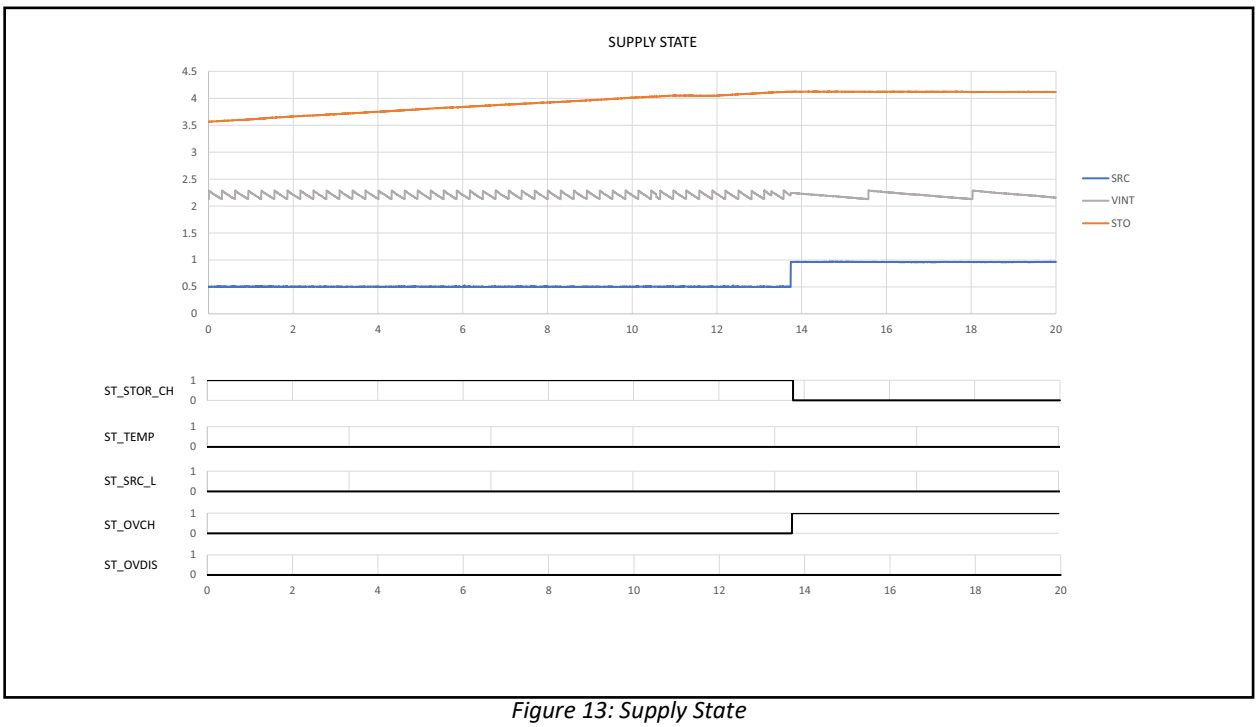


Figure 13: Supply State

STO_CFG[2:0] = HHH, SRC_LVL_CFG[5:0] = LHHLLH, storage element: capacitor (10 mF) pre-charged to 3 V, SRC: current source 5 mA with voltage compliance (0.8 V), DIS_STO_CH = GND, KEEP_ALIVE = H.

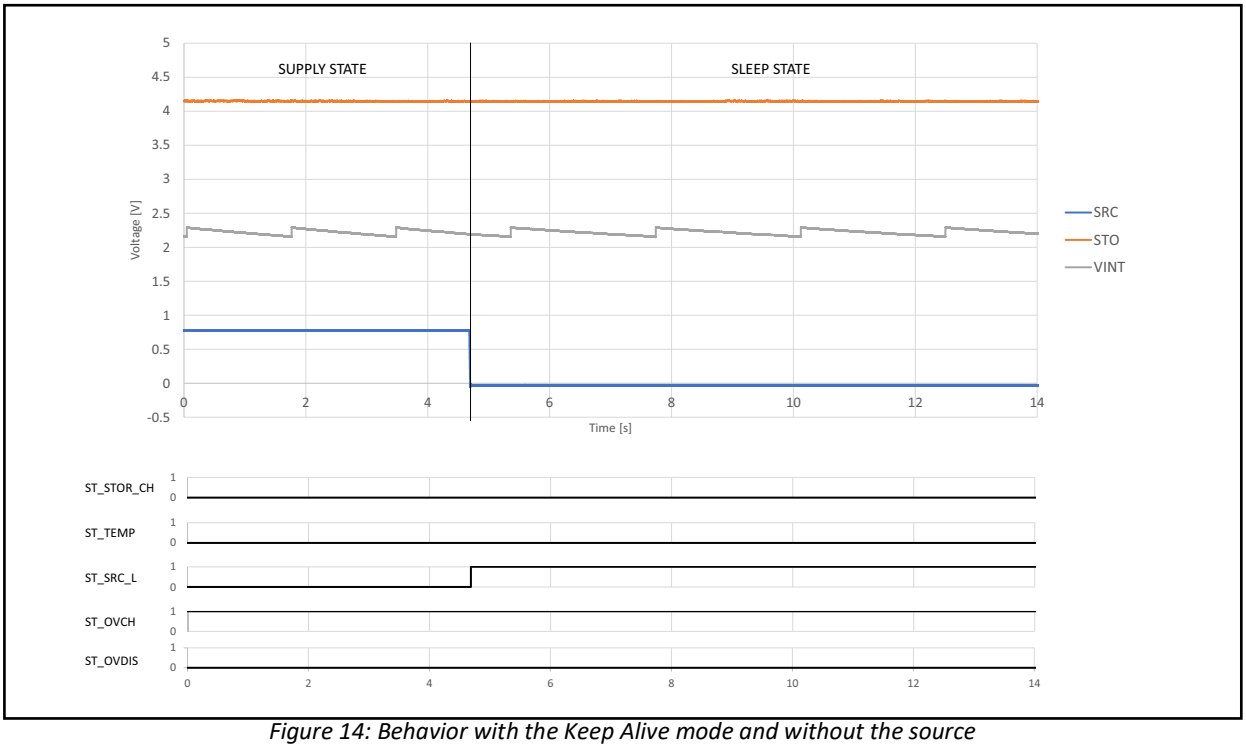


Figure 14: Behavior with the Keep Alive mode and without the source

STO_CFG[2:0] = HHH, SRC_LVL_CFG[5:0] = LHHLLH, storage element: capacitor (10 mF) pre-charged to 3 V, SRC: current source 5 mA with voltage compliance (0.8 V)(stop after ~4.5 sec), DIS_STO_CH = GND, KEEP_ALIVE = H.

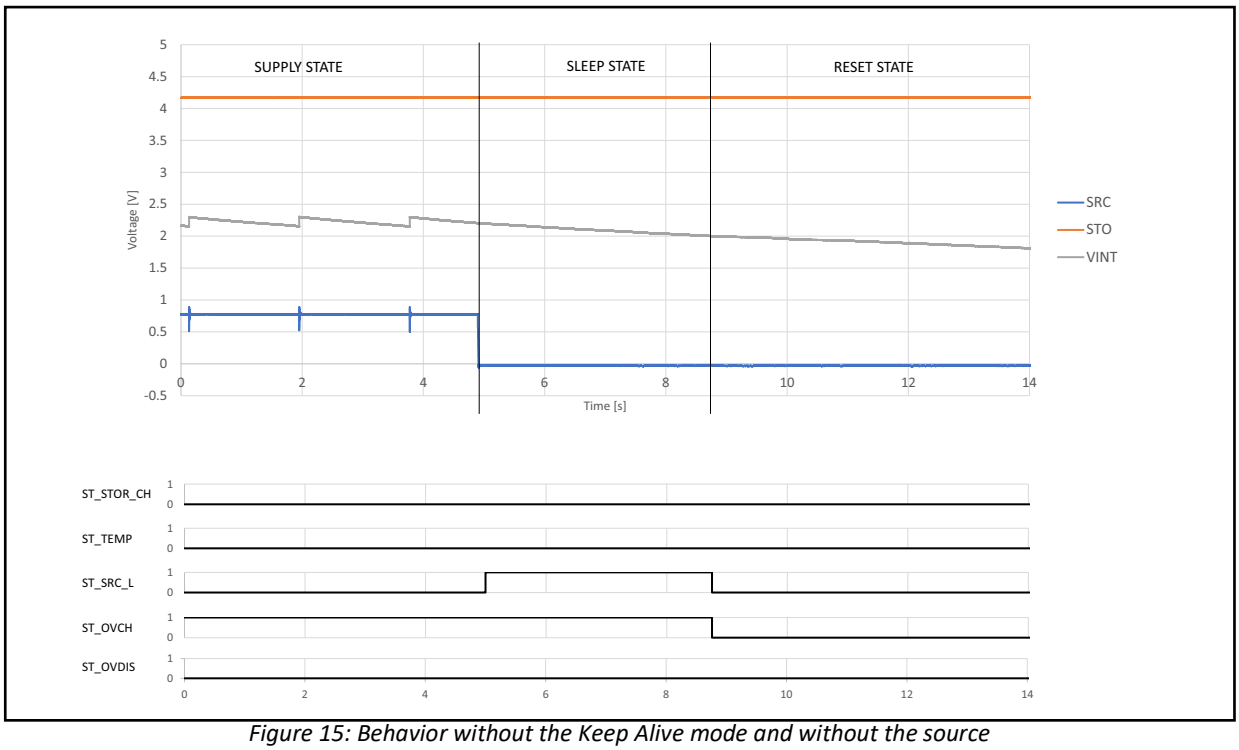


Figure 15: Behavior without the Keep Alive mode and without the source

STO_CFG[2:0] = HHH, SRC_LVL_CFG[5:0] = LHHLLH, storage element: capacitor (10 mF) pre-charged to 3 V, SRC: current source 5 mA with voltage compliance (0.8 V)(stop after ~5 sec), DIS_STO_CH = GND, KEEP_ALIVE = L.

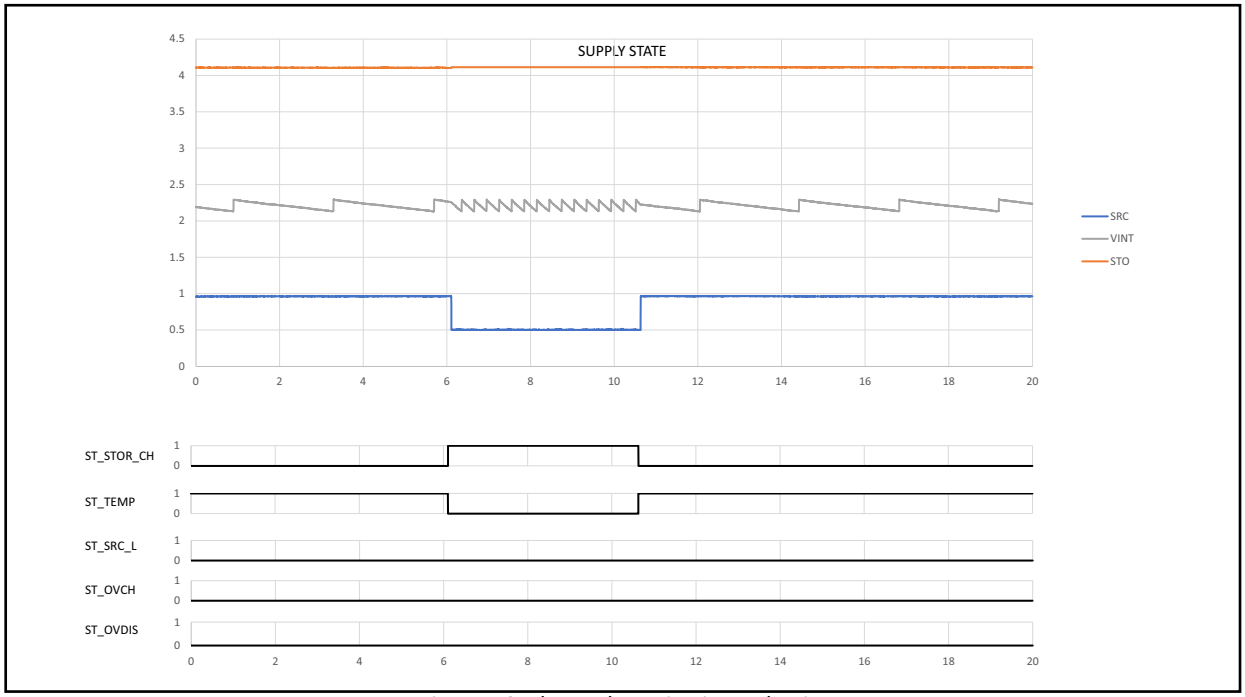


Figure 16: Thermal Monitoring Behavior

STO_CFG[2:0] = HHH, SRC_LVL_CFG[5:0] = LHHLLH, storage element: capacitor (10 mF) pre-charged to 3 V, SRC: current source 5 mA with voltage compliance (0.8 V)(stop after ~5 sec), DIS_STO_CH = GND, KEEP_ALIVE = H. The temperature is lower than 0 °C before 6.5 s and after 13.2 s.

13. Performance Data

13.1. DCDC Conversion Efficiency

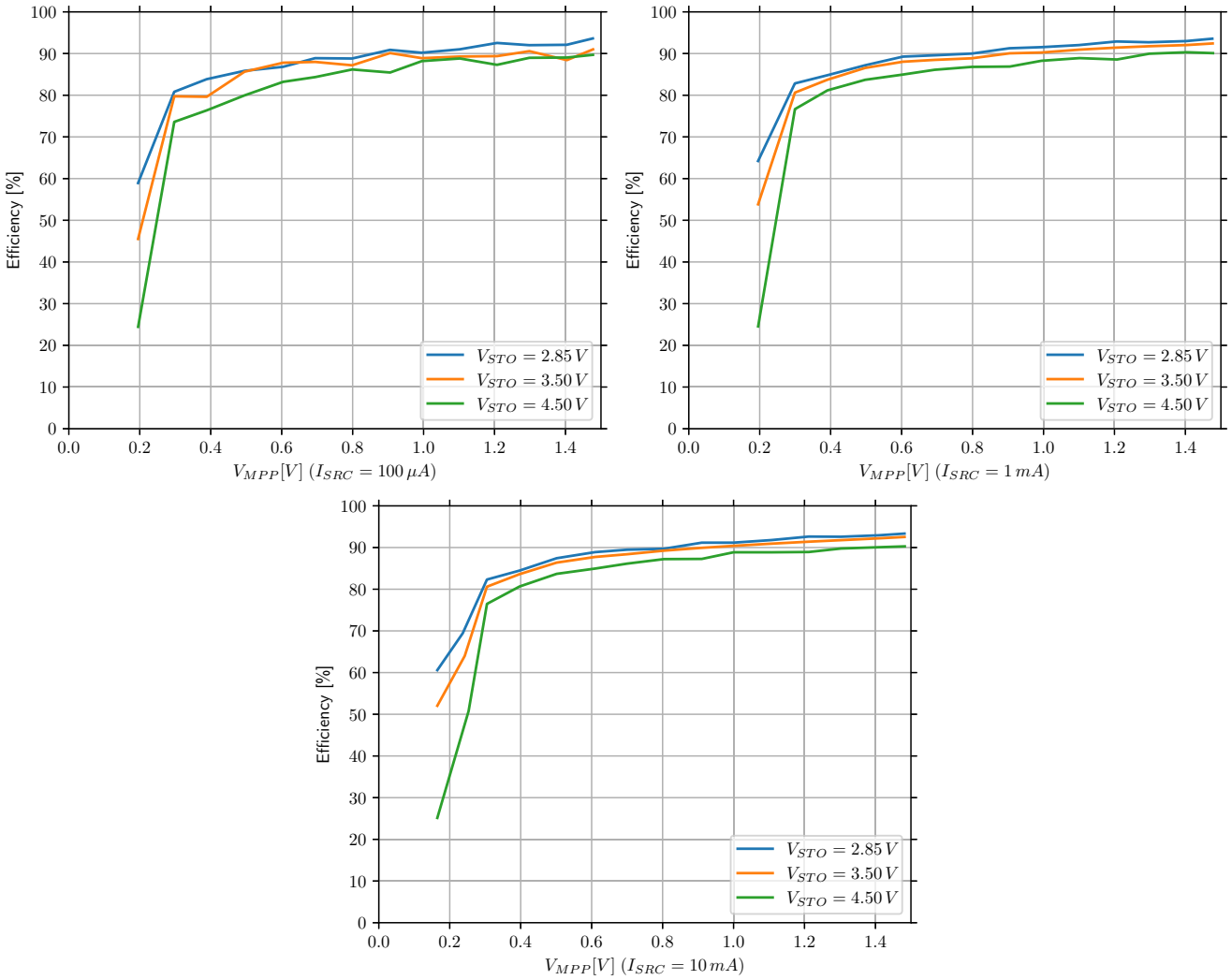


Figure 17: AEM00901 DCDC conversion efficiency (LDCDC: Coilcraft LPS4018-333MRB)

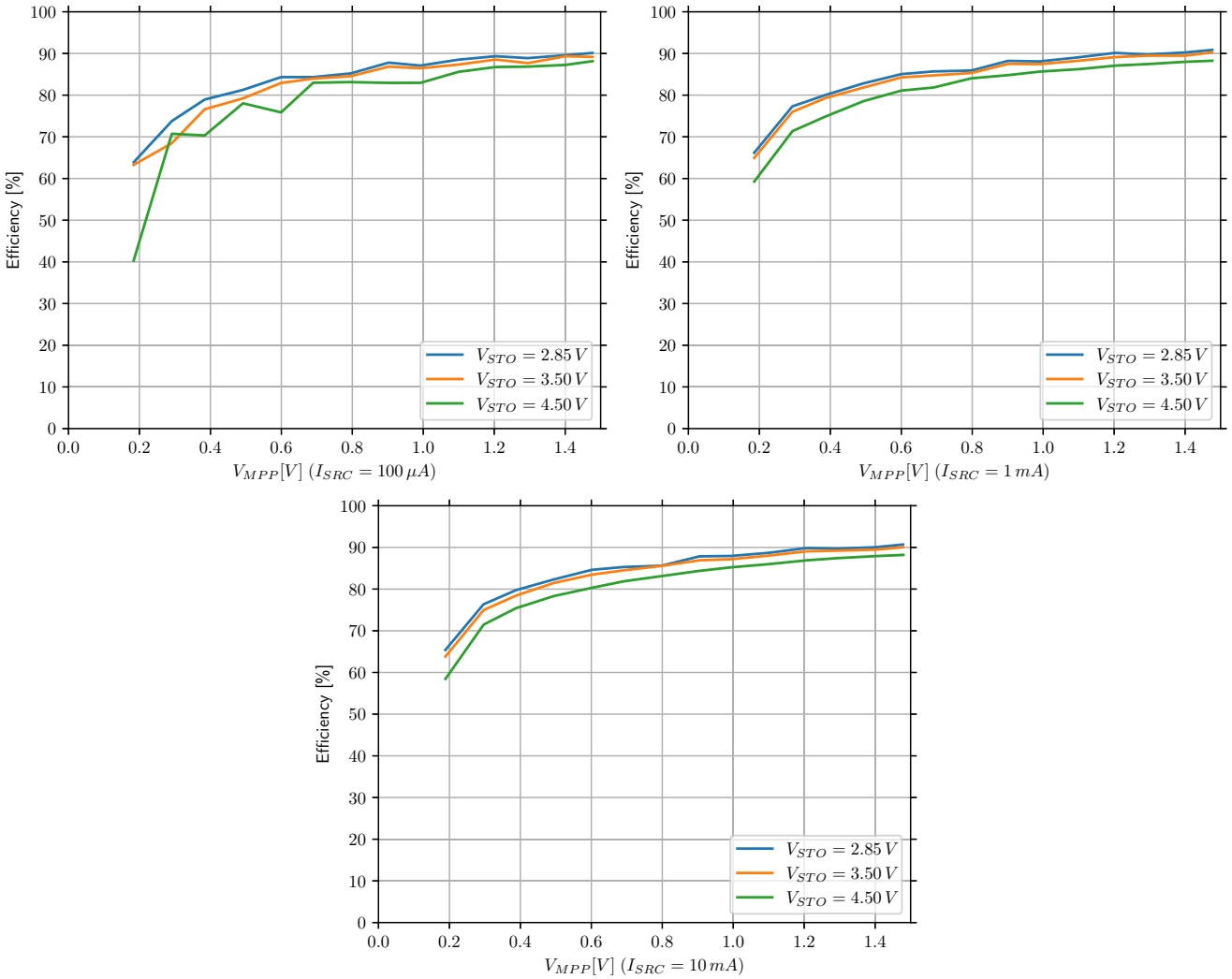


Figure 18: AEM00900 DCDC conversion efficiency (LDCDC: TDK VLS252012HBX-6R8M-1)

13.2. Quiescent Current

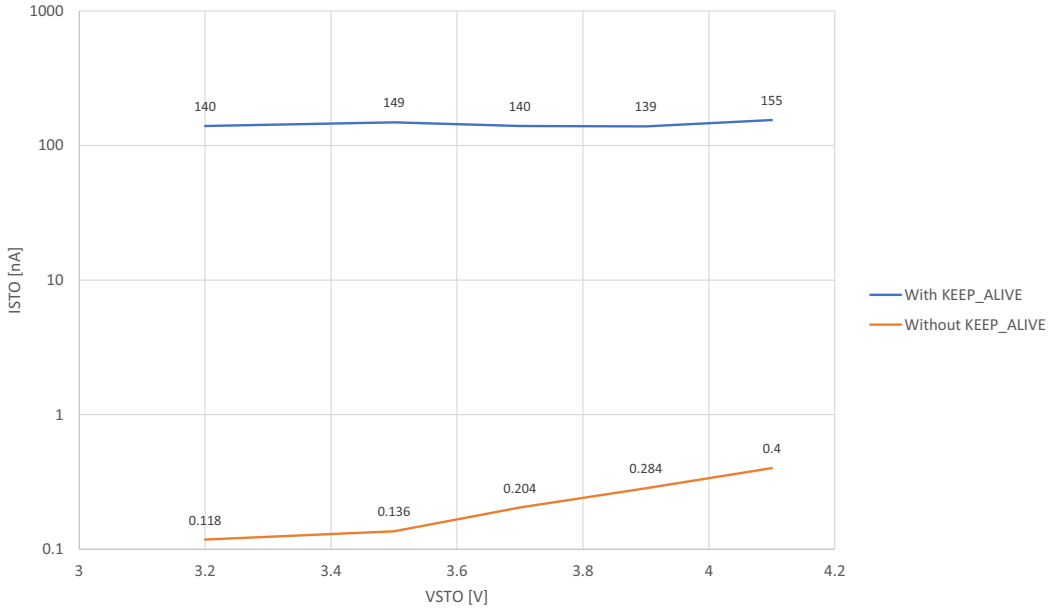


Figure 19: Quiescent current

14. Package Information

14.1. Plastic Quad Flatpack no-lead (QFN28 4x4mm)

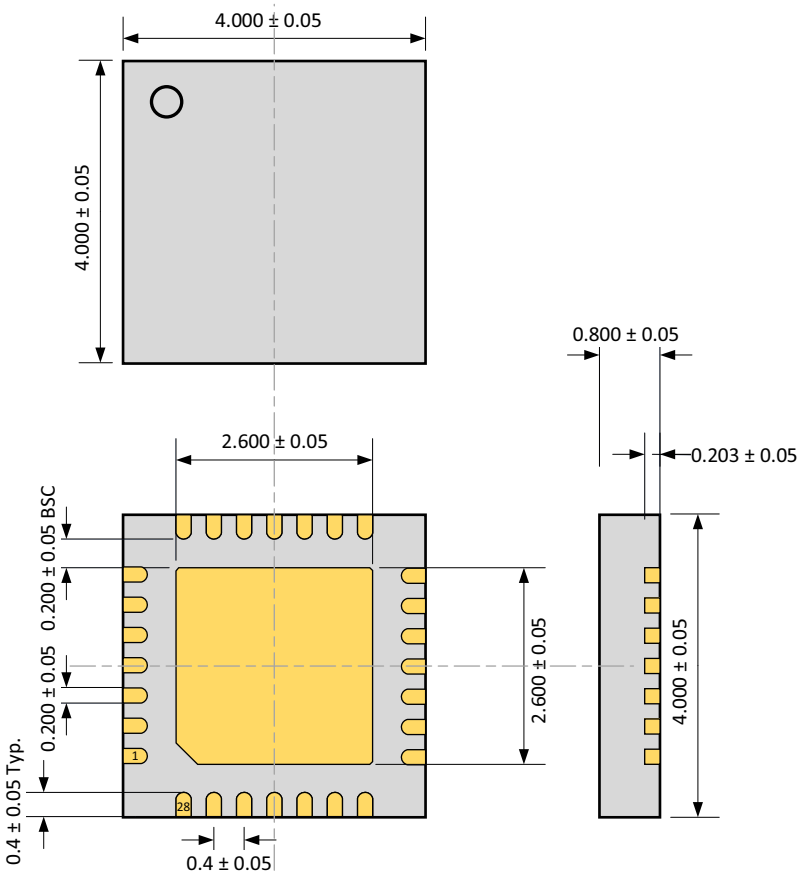


Figure 20: QFN28 4x4 mm

14.2. QFN28 Board Layout

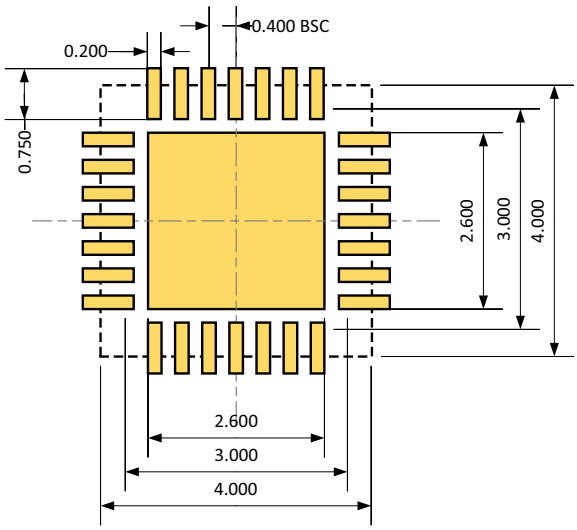


Figure 21: QFN28 4x4 mm board layout

15. Minimum BOM

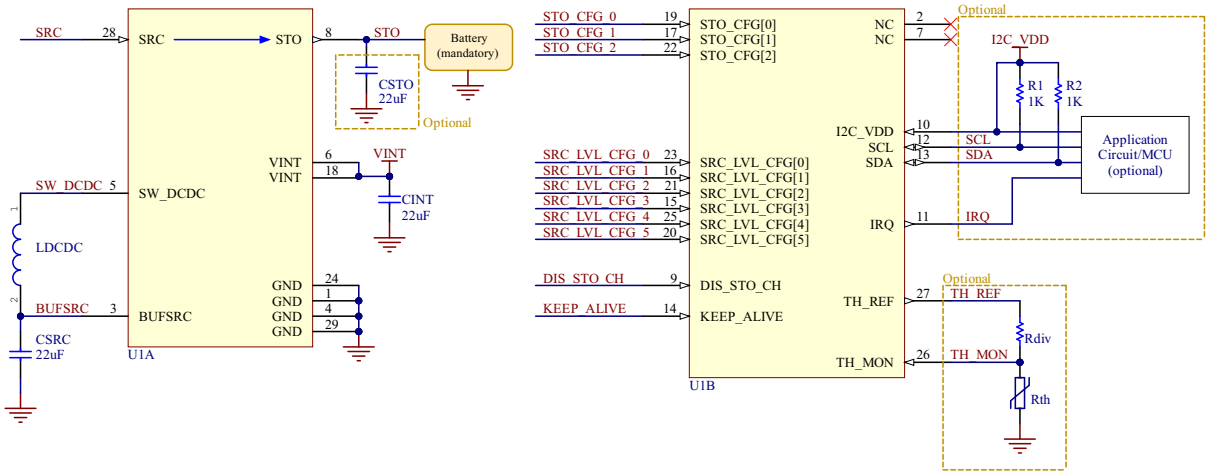


Figure 22: AEM0090x schematic

	Designator	Description	Quantity	Manufacturer	Part number
Mandatory	U1	AEM0090x	1	e-peas	order at sales@e-peas.com
	Battery	Battery with 2.8 V min. voltage	1	To be defined by the user	
	LDCDC (AEM00900)	Power inductor 6.8 µH 1.15A 1008	1	TDK	VLS252012HBX-6R8M-1
	LDCDC (AEM00901)	Power inductor 33 µH 680 mA 1515	1	Coilcraft	LPS4018-333MRB
	CSRC	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CINT	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CSTO	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
Optional	R1, R2	Pull-up 1kΩ Resistors for I²C interface	2	Yageo	AC0603FR-071KL
	Rth	10kΩ NTC thermistor for temperature monitoring	1	Murata	NCP15XH103J03RC
	Rdiv	Resistor 22kΩ 1%	1	Yageo	PNRC0402FR-0722KL

Table 29: AEM0090x bill of material

16. Layout

The following figures are showcasing layout examples of the AEM0090x.

The following guidelines must be applied for best performances:

- Make sure that ground and power signals are routed with large tracks. If an internal ground plane is used, place via as close as possible to the components, especially for decoupling capacitors.
- Reactive components related to the boost converter must be placed as close as possible to the corresponding pins (SWDCDC, BUFSRC and STO), and be routed with large tracks/polygons.
- PCB track capacitance must be reduced as much as possible on the boost converter switching node SWDCDC. This is done as follows:
  - Keep the connection between the SWDCDC pin and the inductor short.
  - Remove the ground and power planes under the SWDCDC node. The polygon on the opposite external layer may also be removed.
  - Increase the distance between SWDCDC and the ground polygon on the external PCB layer where the AEM0090x is mounted.
- PCB track capacitance must be reduced as much as possible on the TH_REF node. Same principle as for SWDCDC may be applied.

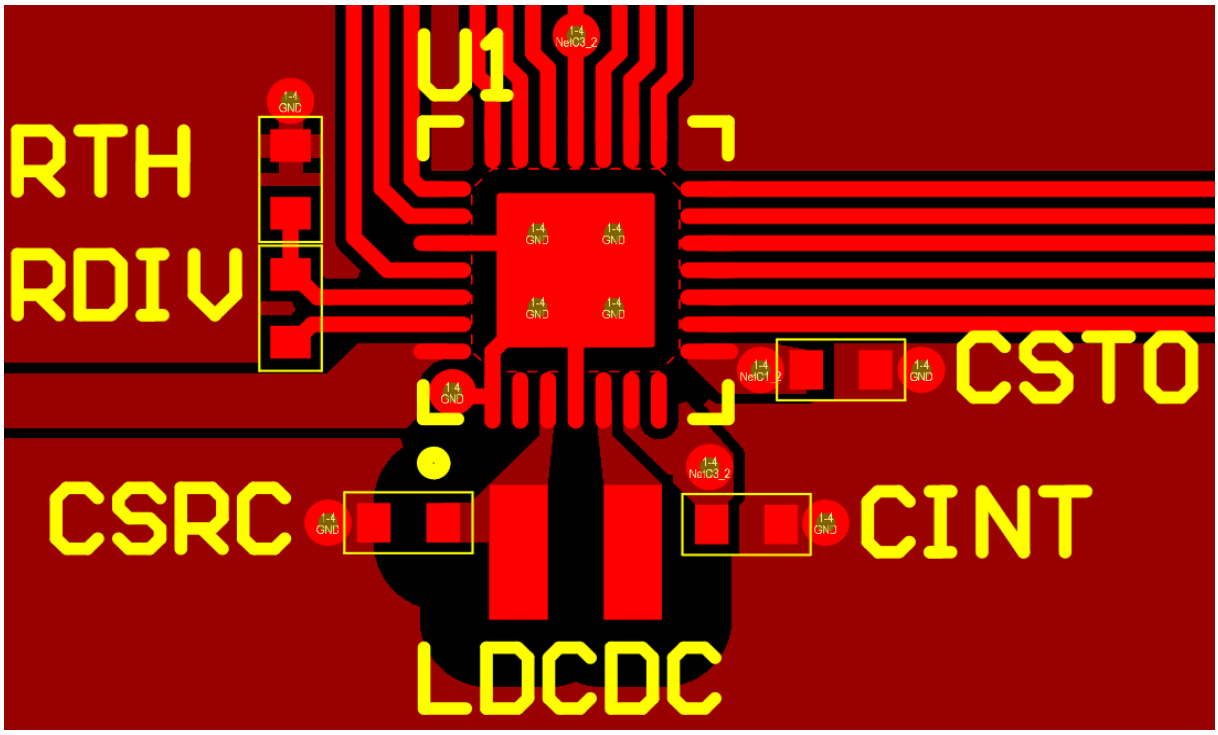


Figure 23: AEM00900 QFN28 layout example

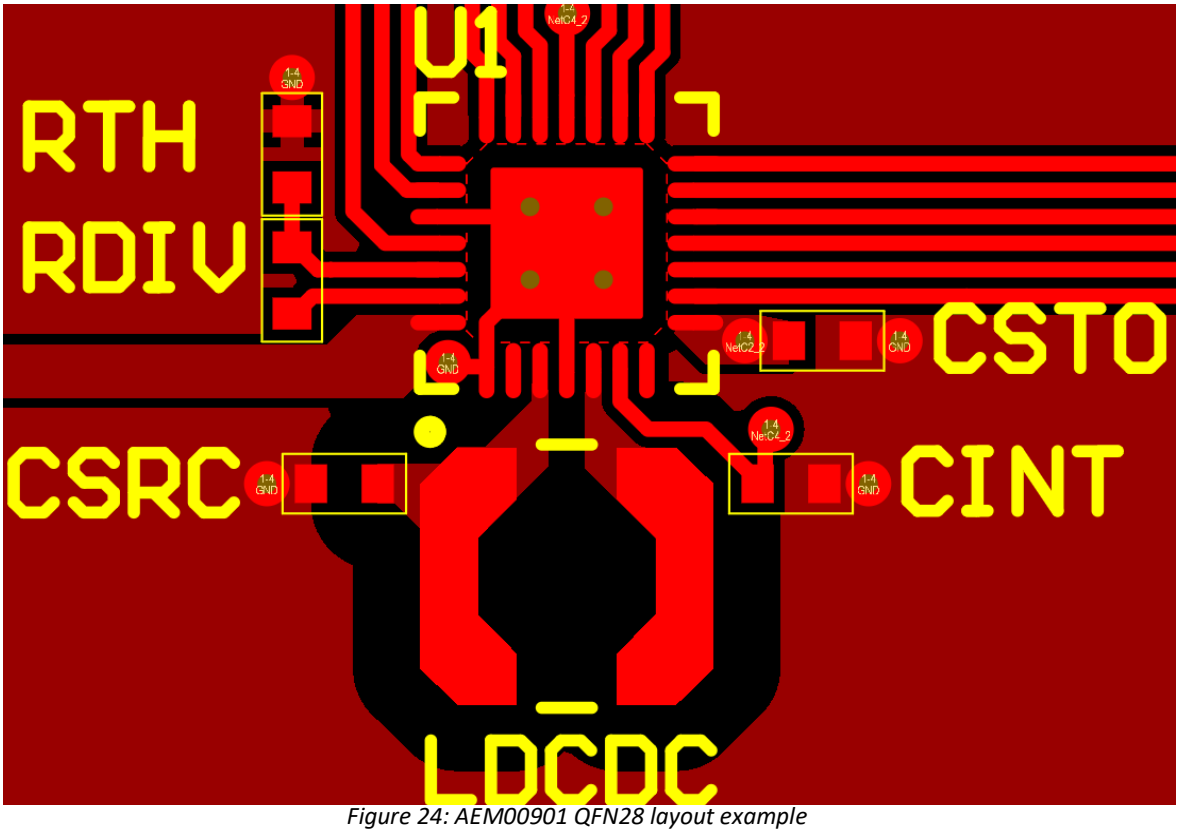


Figure 24: AEM00901 QFN28 layout example

17. Glossary

V_{STO}

Voltage at STO pin.

$V_{SRC,REG}$

Target regulation voltage at the SRC pin.

$V_{SRC,CS}$

Minimum source voltage required for cold start.

V_{SRC}

Voltage at SRC pin.

V_{OVDIS}

Over-discharge voltage at STO pin.

V_{OVCH}

Over-charge voltage at STO pin.

V_{OC}

Open-circuit voltage of the harvester connected to the SRC pin.

V_{INT}

AEM0090x internal circuit voltage supply.

$V_{INT,CS}$

Minimum voltage on VINT to allow the AEM0090x to switch from RESET STATE to SENSE STO STATE.

$T_{RESET,SUPPLY}$

From SUPPLY STATE: delay before reset when no energy on SRC and Keep-alive functionality disabled, or if Keep-alive is enabled but the battery voltage dropped below V_{OVDIS}.

$T_{RESET,SLEEP}$

Same as $T_{RESET,SUPPLY}$ from SLEEP STATE.

$P_{SRC,CS}$

Minimum power available on SRC for the AEM0090x to coldstart.

$I_{QSUPPLY}$

Quiescent current on VINT when the AEM0090x is in SUPPLY STATE.

I_{QSLEEP}

Quiescent current on VINT when the AEM0090x is in SLEEP STATE.

I_{QSTO}

Quiescent current on STO when Keep-alive functionality is disabled.

R_{TH}

Thermistor used for the AEM0090x thermal monitoring feature.

R_{DIV}

Resistor that creates a resistive voltage divider with R_{TH}.

C_{INT}

VINT pin decoupling capacitor.

C_{SRC}

BUFSRC pin decoupling capacitor.

L_{DCDC}

DCDC converter inductor.

R_{SCL} / R_{SDA}

Respectively, I^2C SCL and SDA pin pull-up resistors.

18. Revision History

Revision	Date	Description
1.0	January, 2022	Creation of the document.
1.1	February, 2023	- APM register conversion to energy: replaced formula by Table 24. - I2C_VDD: max. voltage to 2.2 V. - I2C_VDD: more explanation about pin use when using I²C and not using I²C. - Added component part number. - LDCDC from 4.7 µH to 6.8 µH in typical application circuits and in efficiency graphs (AEM00900). - Explanations about CSTO influence on efficiency.
1.2	February, 2024	- Thermal pad (back plane) renamed as pin 29.
1.3	August, 2024	- Small fixes. - Modified $V_{SRC,REG}$ register format - Removed register 0x13

Table 30: Revision history