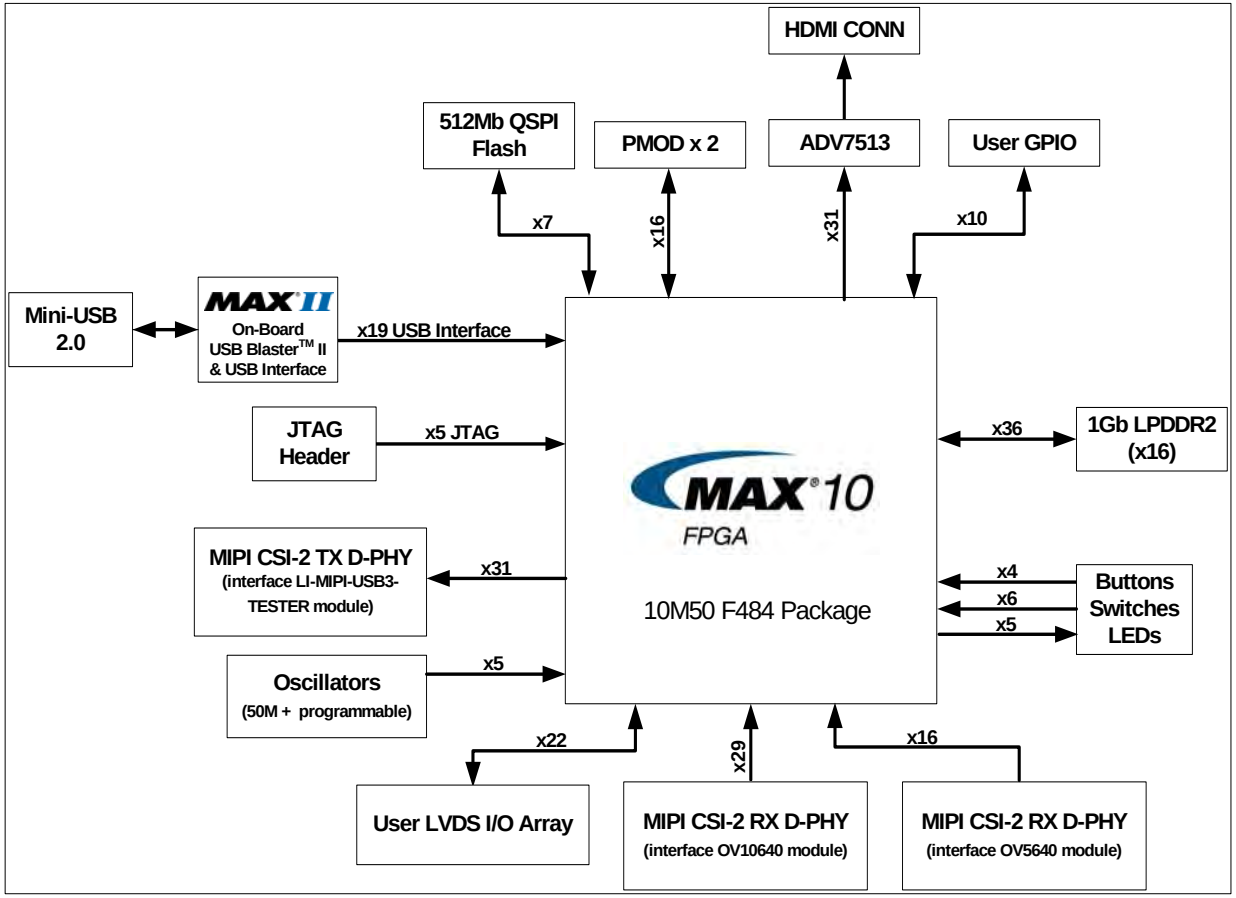
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321404-A1.1
Gerber Files	110-0321404-A1.1
PCB Design Files	120-0321404-A1.1
Assembly Drawing	130-0321404-A1.1
Fab Drawing	140-0321404-A1.1
Schematic Drawing	150-0321404-A1.1
PCB Film	160-0321404-A1.1
Bill of Materials	170-0321404-A1.1
Schematic Design Files	180-0321404-A1.2
Functional Specification	210-0321404-A1.1
PCB Layout Guidelines	220-0321404-A1.1
Assembly Rework	320-0321404-A1.1

REV	DATE	PAGES	DESCRIPTION
A1	Jun 19 2015	All	Initial Revision A Release.
A1.1	Sep 15 2015	1	Update block diagram.
		2	Update power tree.
		10	Delete C12.
		18	Add note for SW2.4 MAX10_BYPASSn.
		22	Change the value of C219 from DNI to 47uF.
		23	Add R315 to 1.2V_VCCIO.
		25	Change the value of C232 from 100uF to DNI.
A1.2	Dec 23 2015	10	Change LPDDR2_IS43LD16640A-3BL(333MHz part) to IS43LD16640A-25BL (400MHz part) due to Altera IP recommendation.

MAX 10 FPGA 10M50 Evaluation Kit Board



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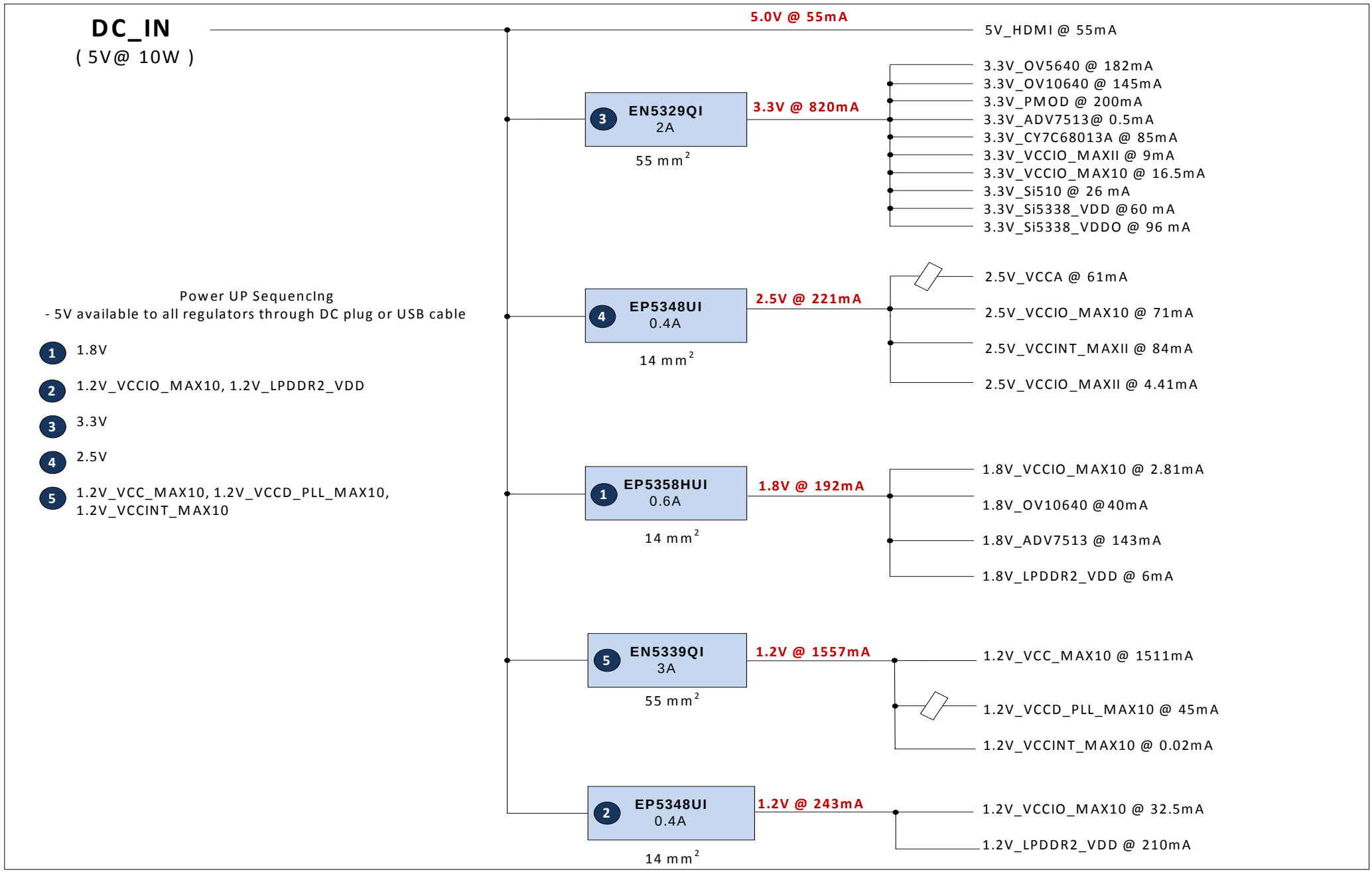
POWER TREE



Power UP Sequencing
- 5V available to all regulators through DC plug or USB cable

1. 1.8V
2. 1.2V_VCCIO_MAX10, 1.2V_LPDDR2_VDD
3. 3.3V
4. 2.5V
5. 1.2V_VCC_MAX10, 1.2V_VCCD_PLL_MAX10, 1.2V_VCCINT_MAX10

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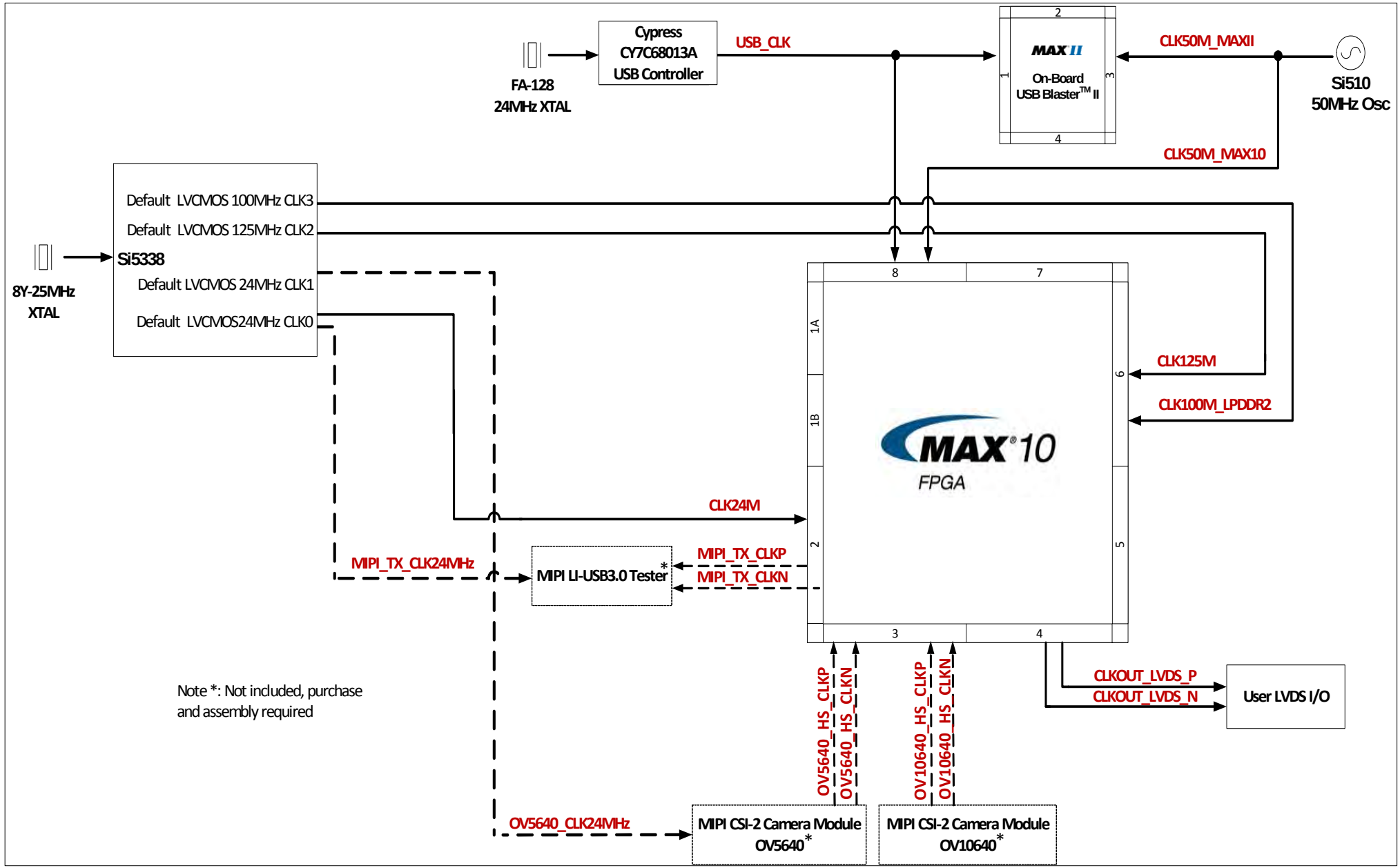
CLOCK TREE



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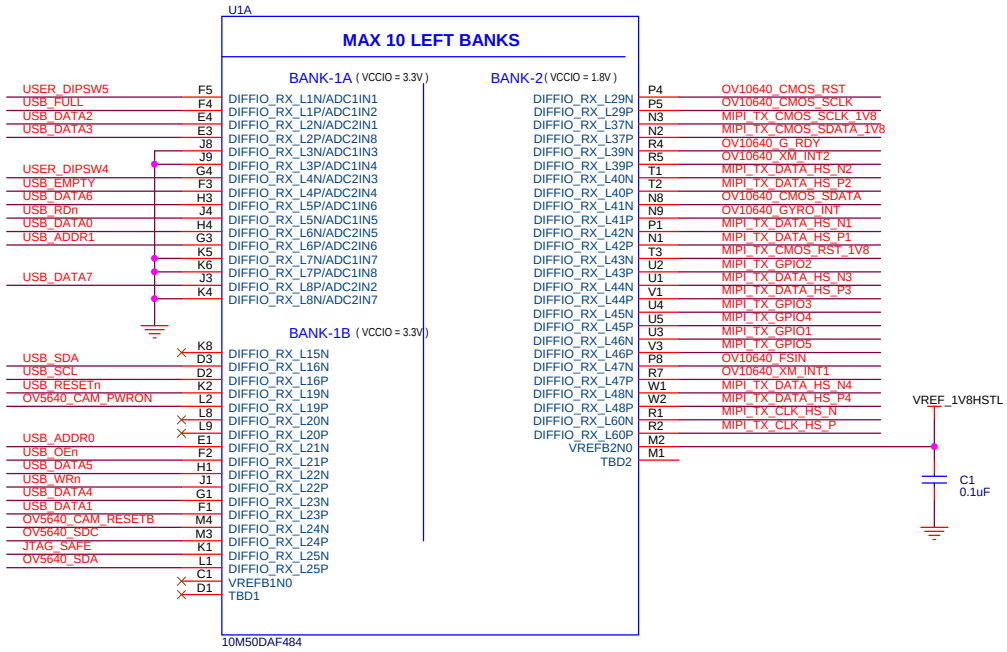
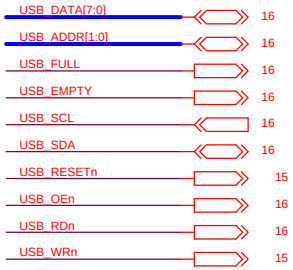
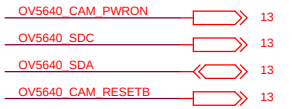
MAX10 BANKS 1 & 2



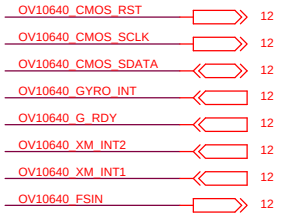
MAX10 USB Interface



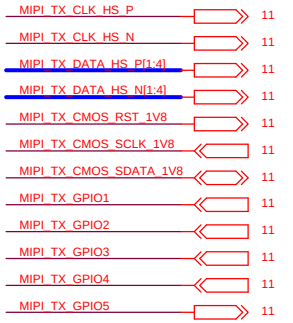
OV5640 CSI-2 RX Interface



OV10640 CSI-2 RX Interface



LI-USB3 CSI-2 TX Interface



Misc

User DIP Switch

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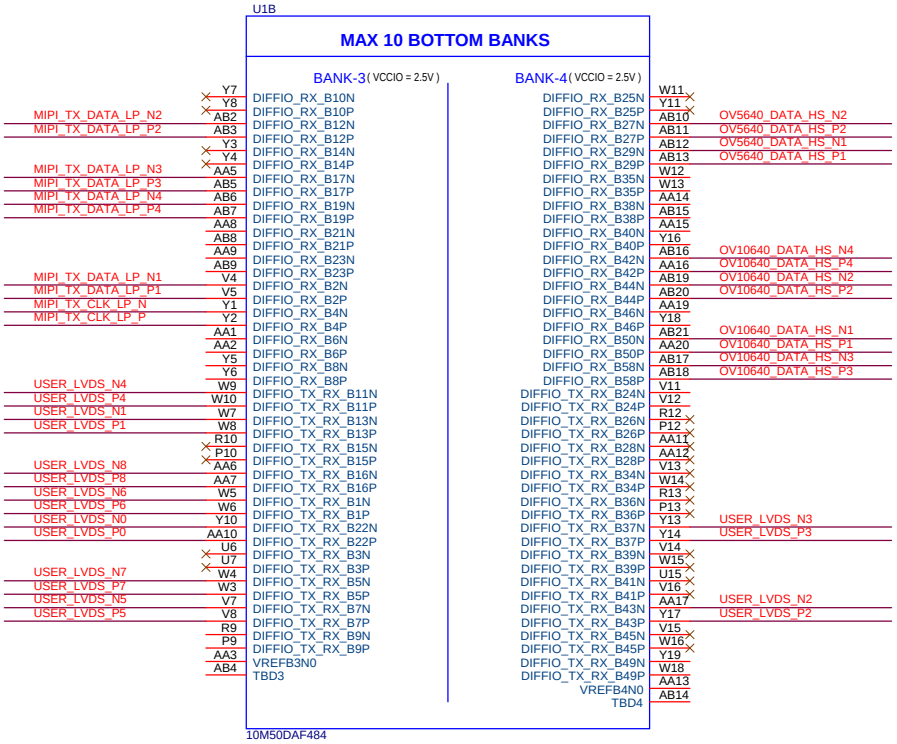
MAX10 BANKS 3 & 4



User LVDS IO

USER_LVDS_P[0:8] 17
USER_LVDS_N[0:8] 17

OV10640 Interface

OV10640_DATA_HS_P[1:4] 12
OV10640_DATA_HS_N[1:4] 12

OV5640 Interface

OV5640_DATA_HS_P[1:2] 13
OV5640_DATA_HS_N[1:2] 13

LI-USB3 CSI-2 TX Interface

MIPI_TX_CLK_LP_P 11
MIPI_TX_CLK_LP_N 11
MIPI_TX_DATA_LP_P[1:4] 11
MIPI_TX_DATA_LP_N[1:4] 11

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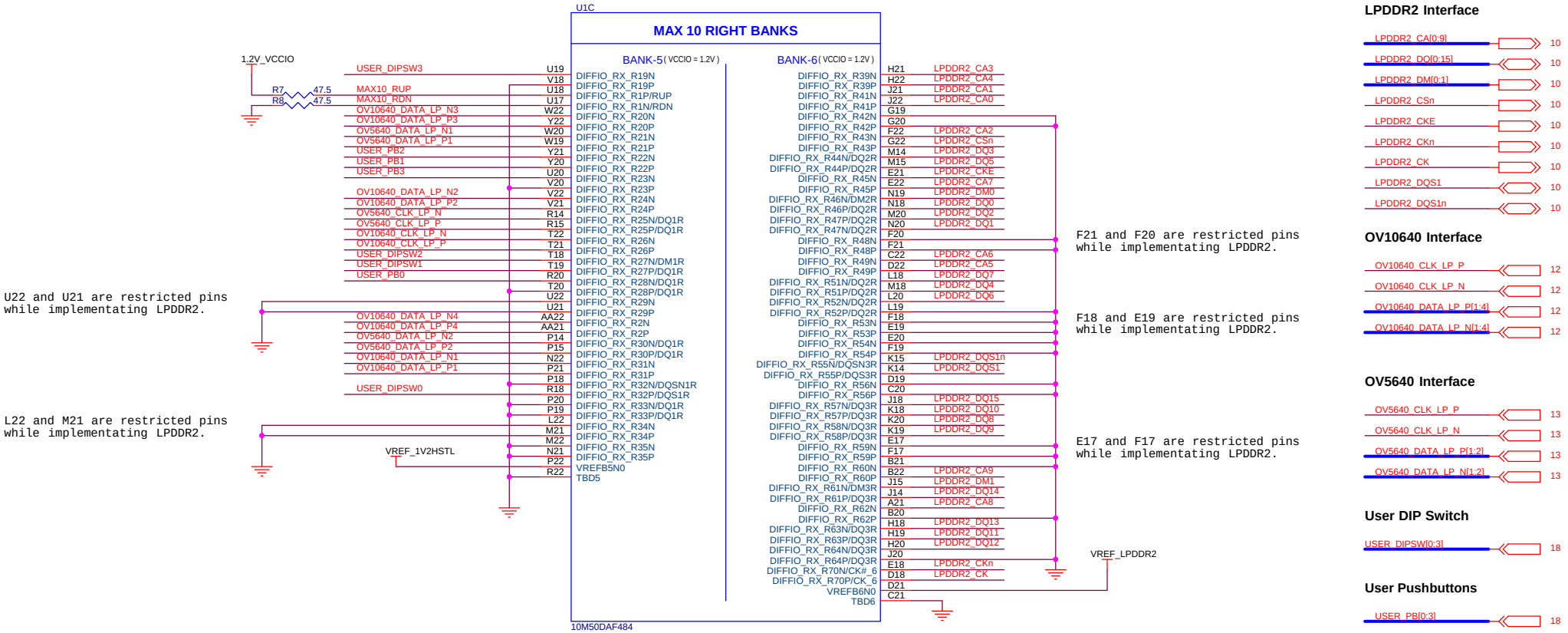
MAX10 BANKS 5 & 6



LPDDR2 Interface

LPDDR2_CA[0:9] 10
LPDDR2_DQ[0:15] 10
LPDDR2_DM[0:1] 10
LPDDR2_CSn 10
LPDDR2_CKE 10
LPDDR2_CKn 10
LPDDR2_CK 10
LPDDR2_DQS1 10
LPDDR2_DQS1n 10

OV10640 Interface

OV10640_CLK_LP_P 12
OV10640_CLK_LP_N 12
OV10640_DATA_LP_P[1:4] 12
OV10640_DATA_LP_N[1:4] 12

OV5640 Interface

OV5640_CLK_LP_P 13
OV5640_CLK_LP_N 13
OV5640_DATA_LP_P[1:2] 13
OV5640_DATA_LP_N[1:2] 13

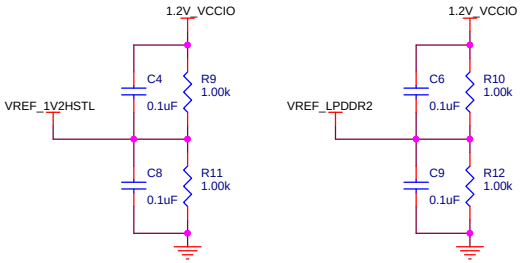
User DIP Switch

USER_DIPSW[0:3] 18

User Pushbuttons

USER_PB[0:3] 18

Reference Voltages of 1.2V HSTL and LPDDR2



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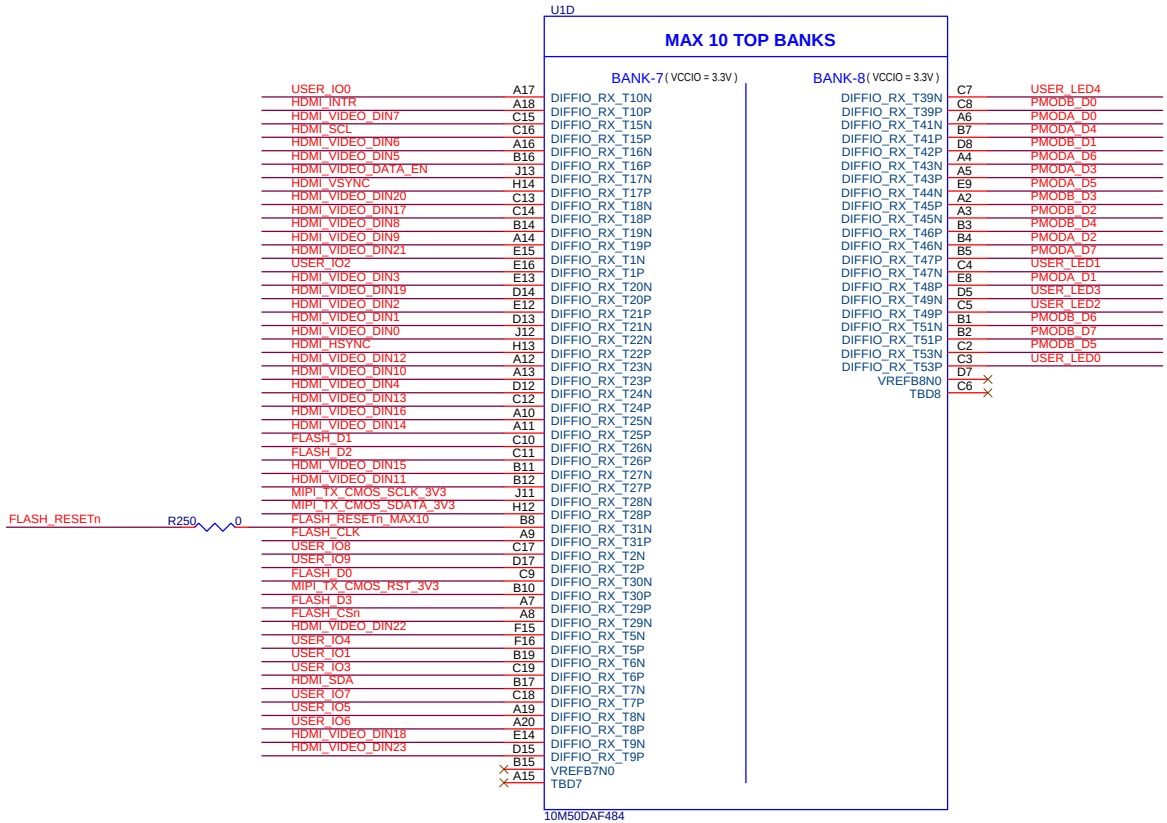
MAX10 BANKS 7 & 8



User IO

USER_IO[0:9] — 17

PMOD

PMODA_D[7:0] — 17

PMODB_D[7:0] — 17

HDMI TX

HDMI_VIDEO_DIN[23:0] — 14

HDMI_HSYNC — 14

HDMI_VSYNC — 14

HDMI_VIDEO_DATA_EN — 14

HDMI_INTR — 14

HDMI_SDA — 14

HDMI_SCL — 14

Flash

FLASH_RESETn — 15,25

FLASH_CSn — 25

FLASH_CLK — 25

FLASH_D[0:3] — 25

LI-USB3 CSI-2 TX Interface

MIPI_TX_CMOS_SCLK_3V3 — 11

MIPI_TX_CMOS_SDATA_3V3 — 11

MIPI_TX_CMOS_RST_3V3 — 11

User LED

USER_LED[0:4] — 18

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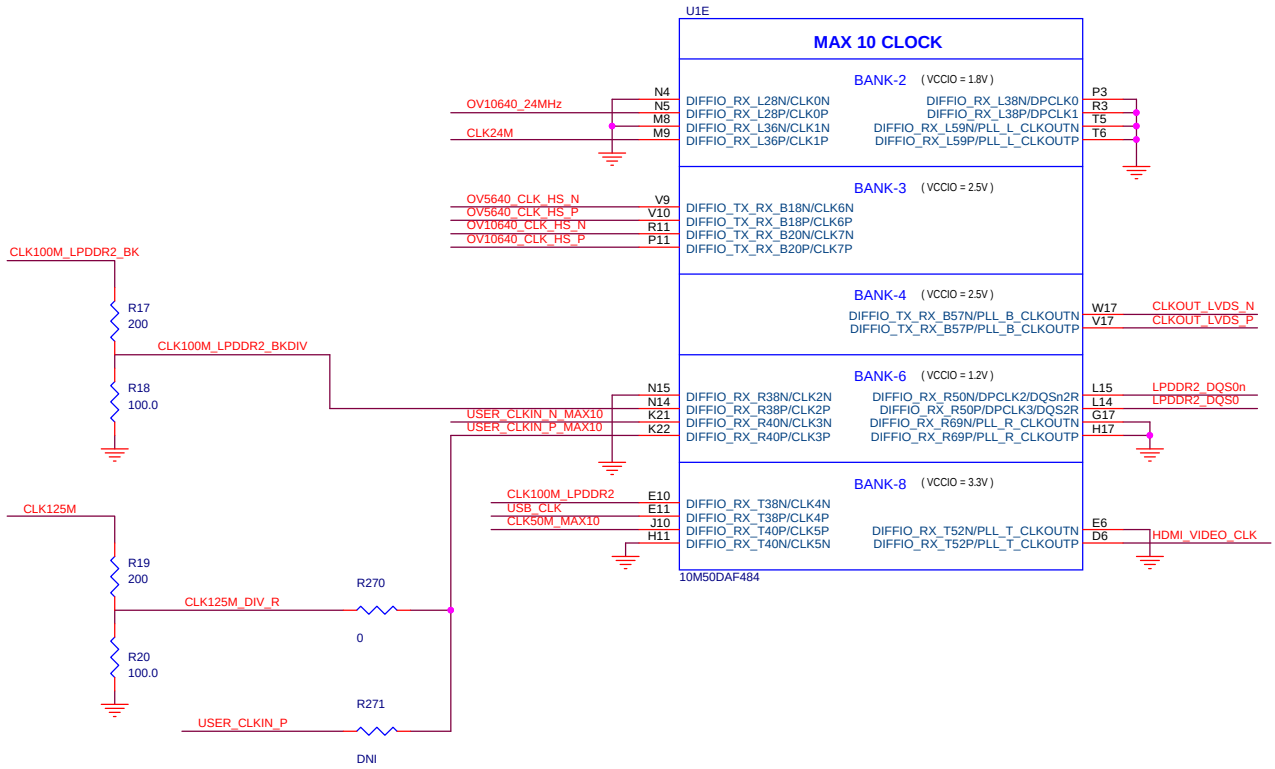
MAX10 CLOCKS



Note: CLK125M_LVDS is the clock source provided to external LVDS user interface.
USER_CLKIN_P is used for external sigle-ended clock input.
USER_CLKIN_P/N is used for external differential clock input.

LPDDR2 Interface
- LPDDR2_DQS0 — 10
- LPDDR2_DQS0n — 10

OV5640 Interface
- OV5640_CLK_HS_P — 13
- OV5640_CLK_HS_N — 13

OV10640 Interface
- OV10640_CLK_HS_P — 12
- OV10640_CLK_HS_N — 12
- OV10640_24MHz — 12

Si5338
- CLK50M_MAX10 — 19
- CLK24M — 19
- CLK125M — 19
- CLK100M_LPDDR2 — 19
- CLK100M_LPDDR2_BK — 19

USB Blaster II
- USB_CLK — 15

User LVDS
- USER_CLKIN_P — 17
- USER_CLKIN_N_MAX10 — 17
- CLKOUT_LVDS_P — 17
- CLKOUT_LVDS_N — 17

HDMI
- HDMI_VIDEO_CLK — 14

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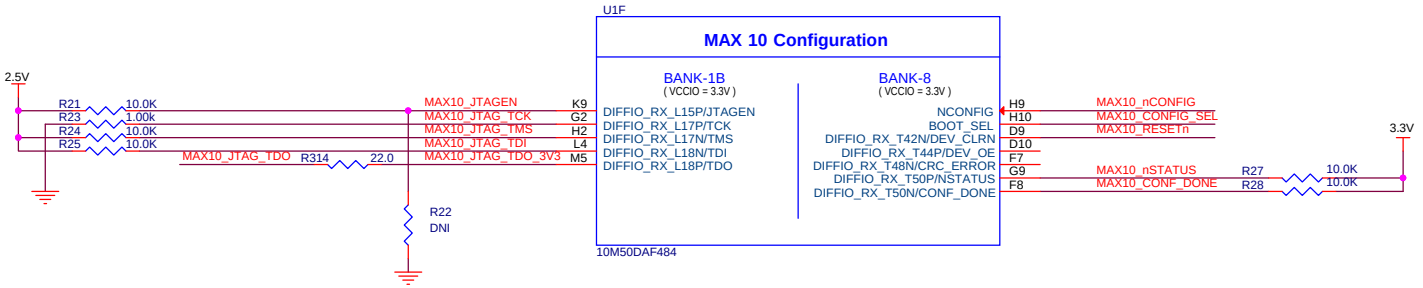
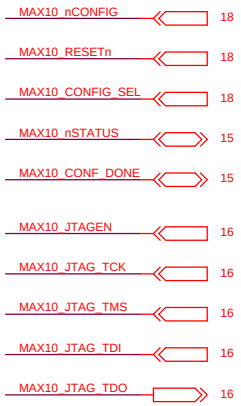
MAX10 CONFIGURATION



Configuration



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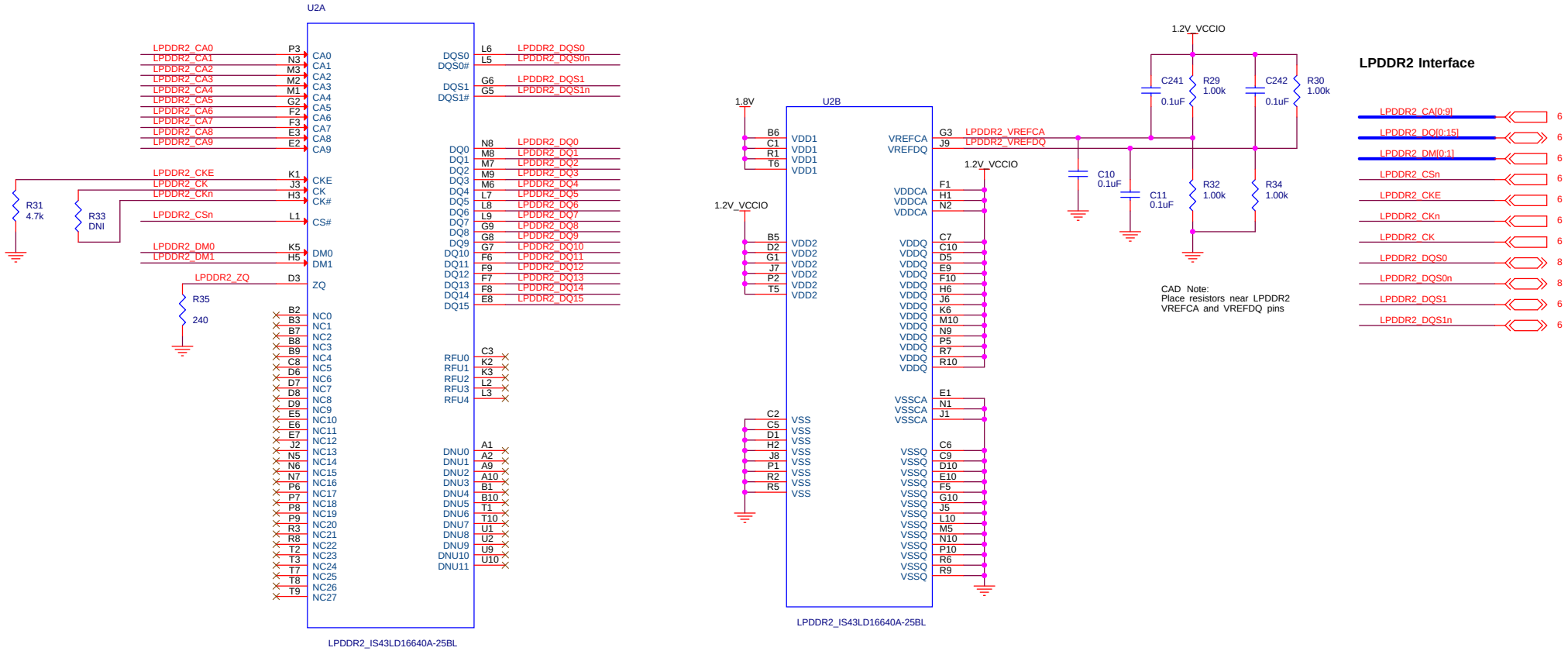
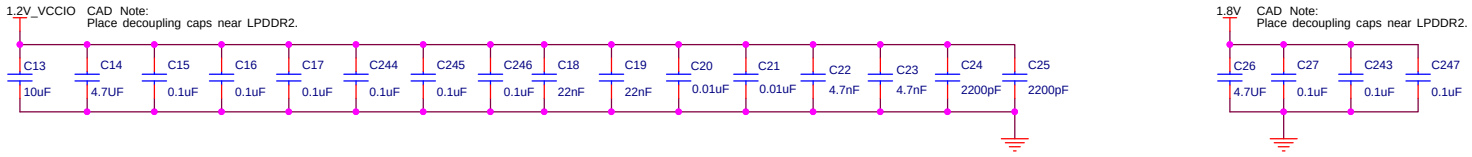
LPDDR2 SDRAM x 16



LPDDR2 Power Decoupling



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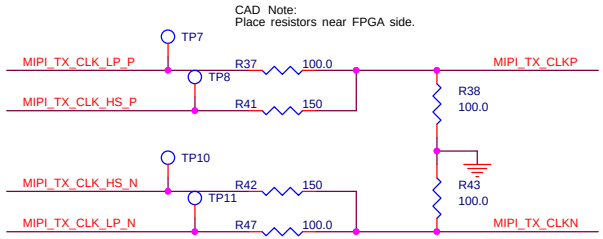
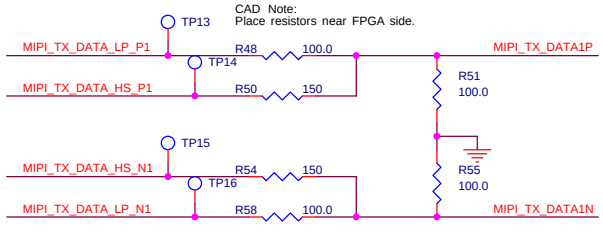
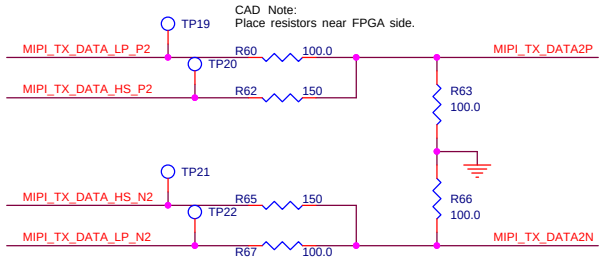
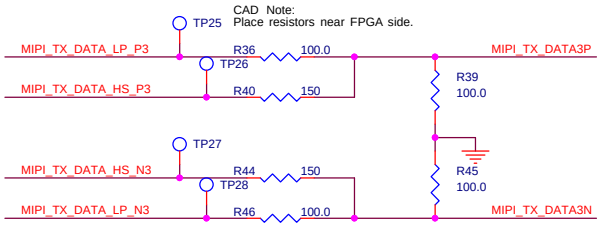
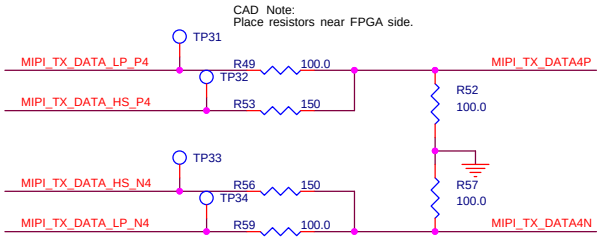
MIPI CSI-2 TX D-PHY

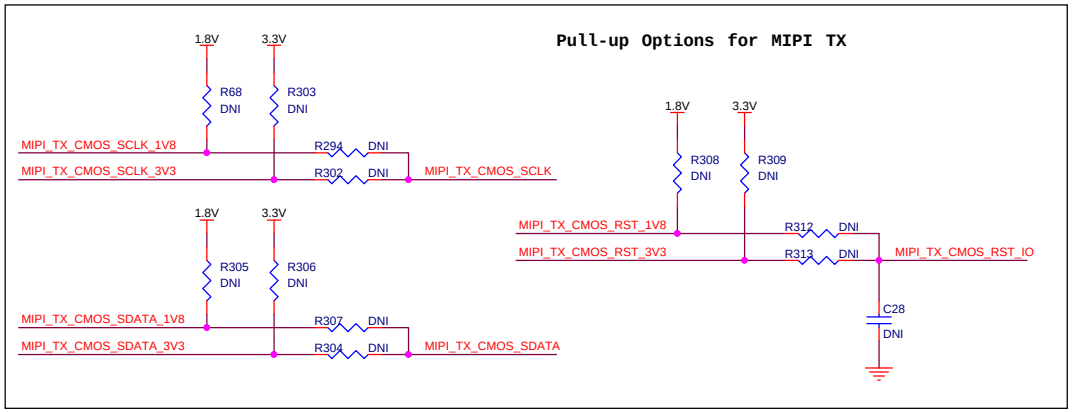


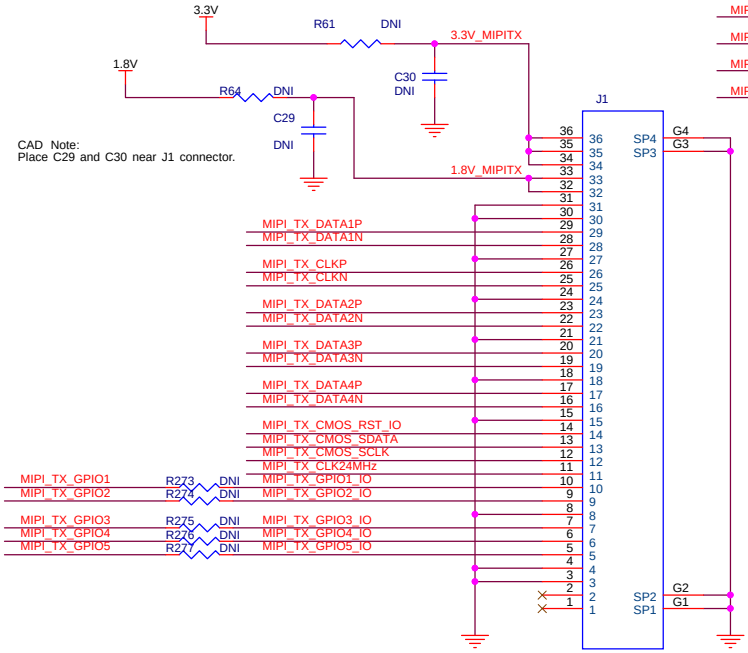


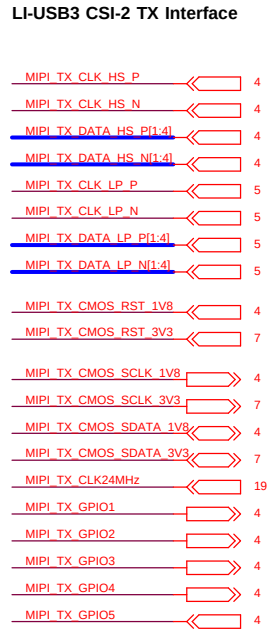












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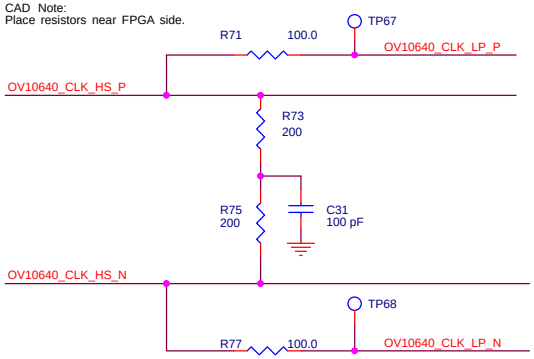
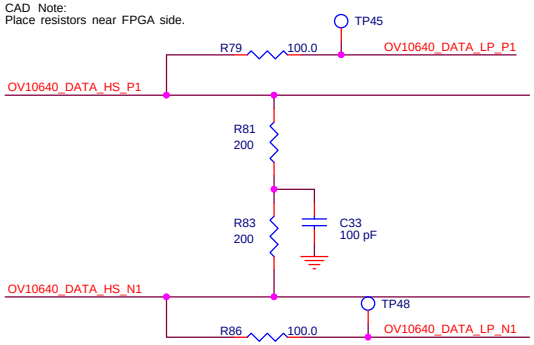
MIPI CSI-2 RX D-PHY OV10640

CAD Note:
Place resistors near FPGA side.



CAD Note:
Place resistors near FPGA side.



CAD Note:
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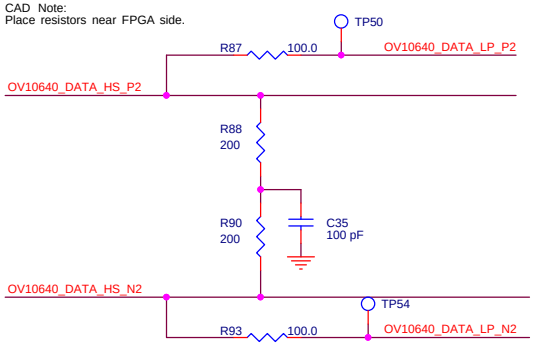
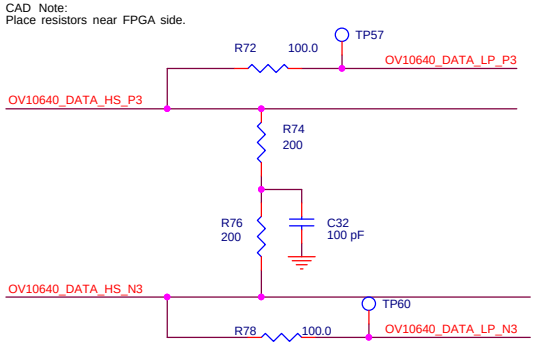
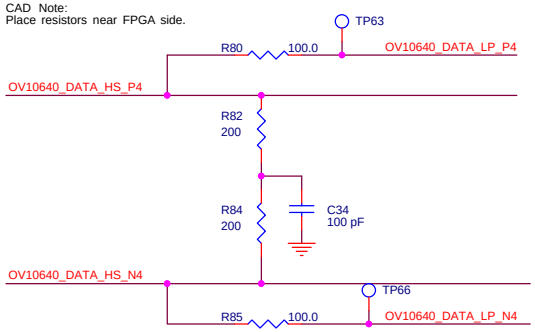
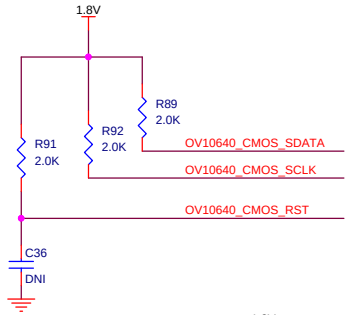


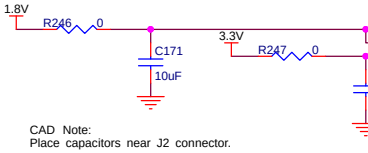
CAD Note:
Place resistors near FPGA side.



CAD Note:
Place resistors near FPGA side.

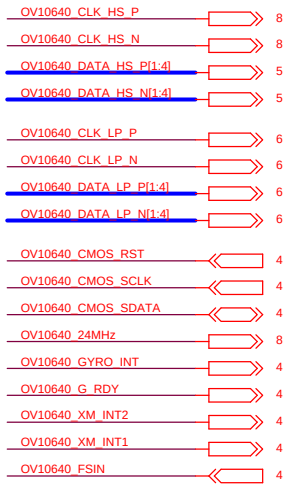






CAD Note:
Place capacitors near J2 connector.

OV10640 CSI-2 RX Interface



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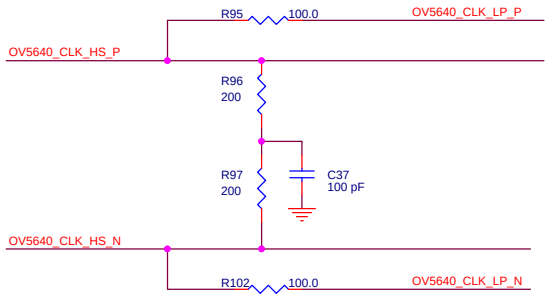
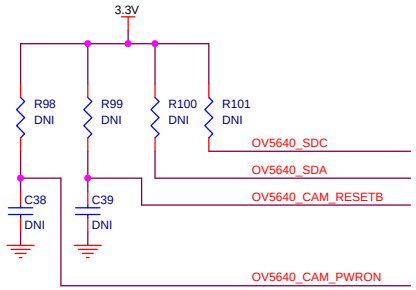
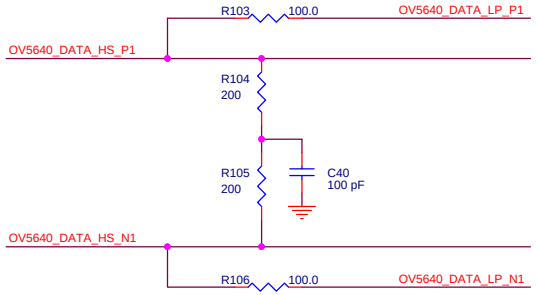
MIPI CSI-2 RX D-PHY OV5640

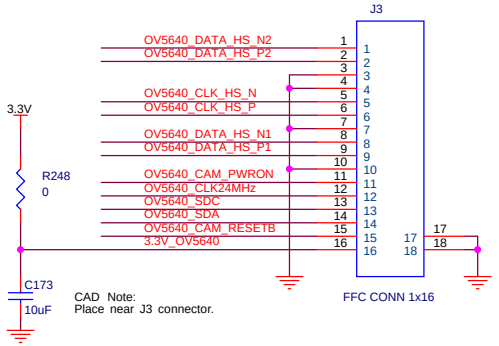
CAD Note:
Place resistors near FPGA side.





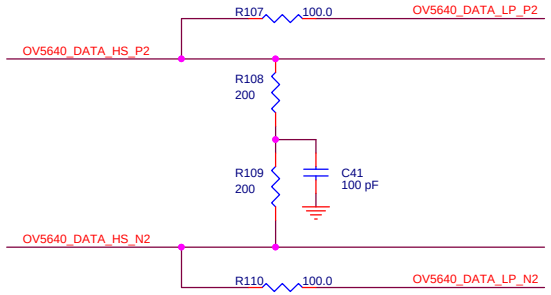
CAD Note:
Place resistors near FPGA side.



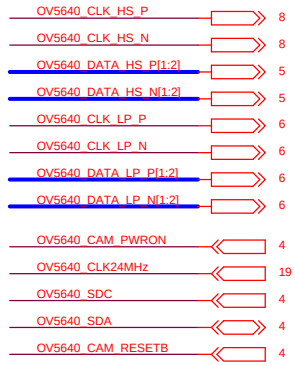


CAD Note:
Place near J3 connector.

CAD Note:
Place resistors near FPGA side.



OV5640 CSI-2 RX Interface



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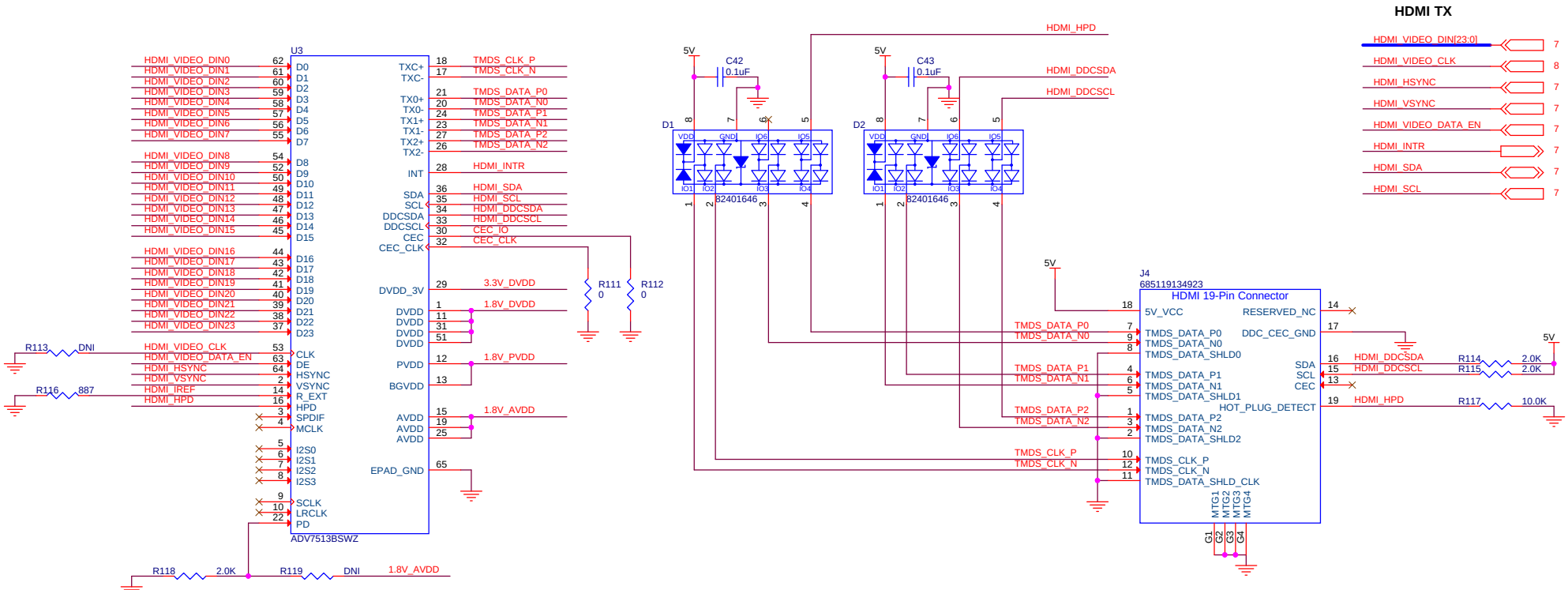
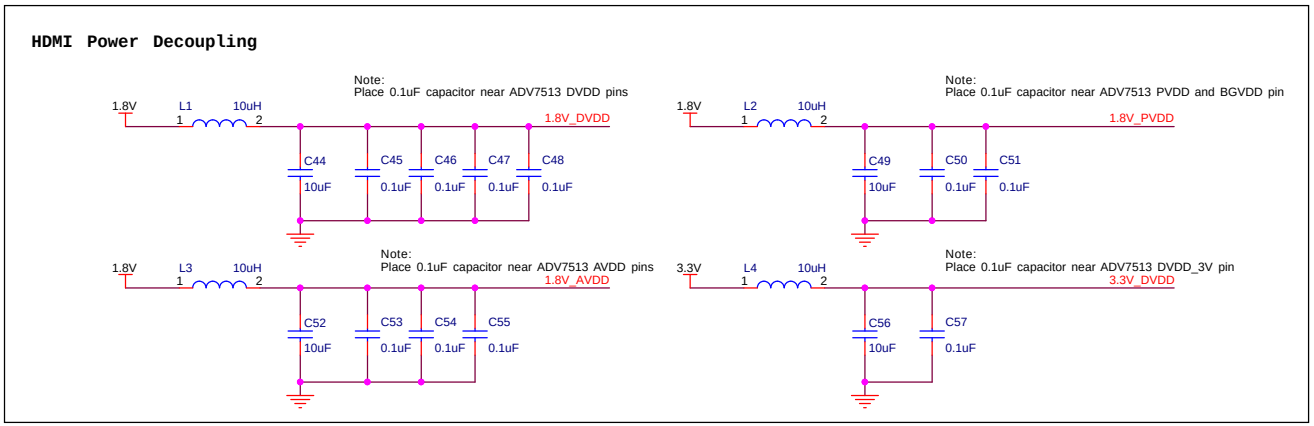
HDMI (VIDEO ONLY)



HDMI Power Decoupling



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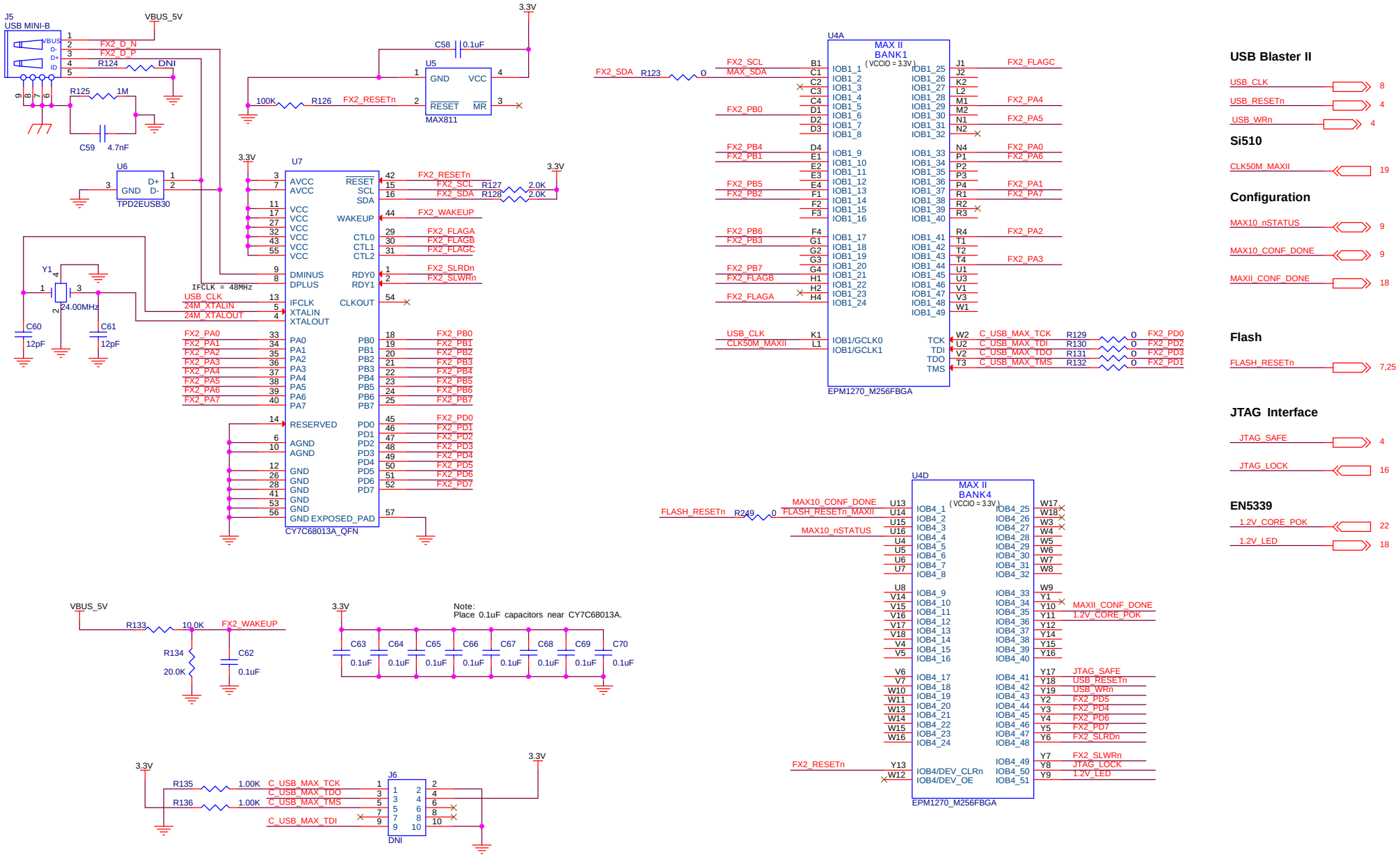
ON-BOARD USB BLASTER II-1



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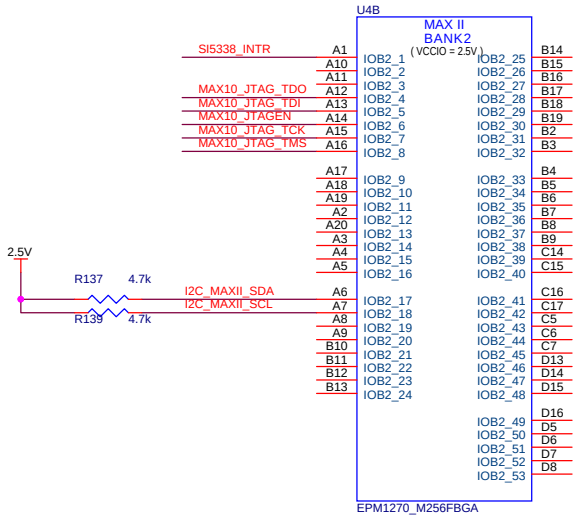
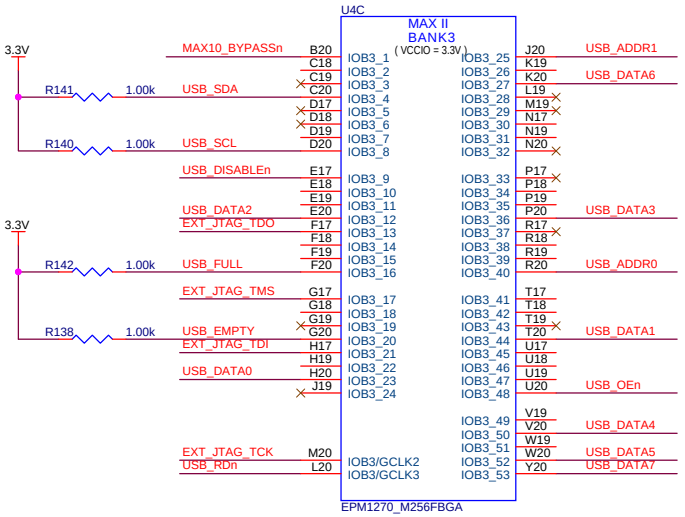
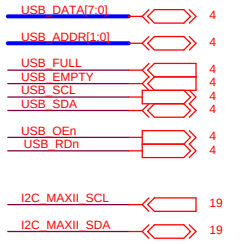
ON-BOARD USB BLASTER II-2

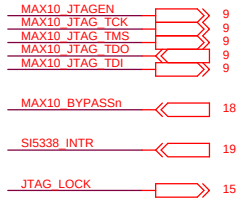


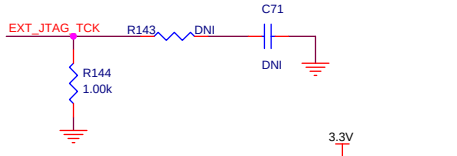


MAX10 USB Interface

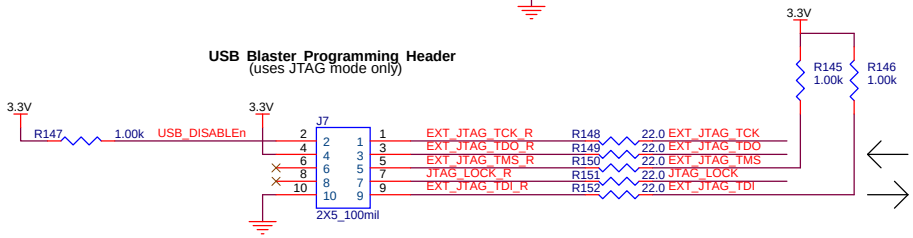


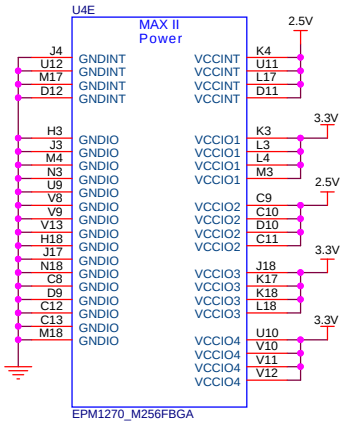
JTAG Interface



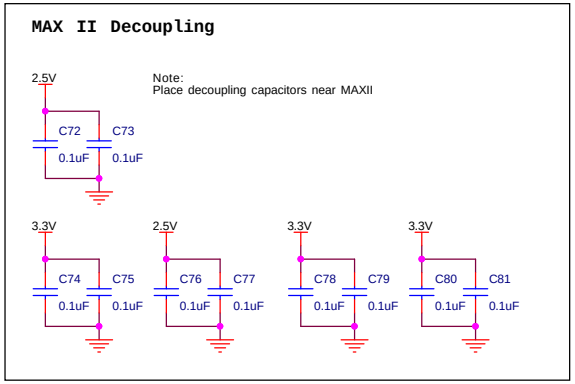


USB Blaster Programming Header
(uses JTAG mode only)





MAX II Decoupling



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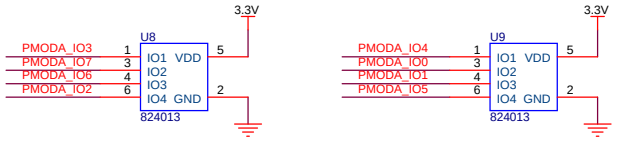
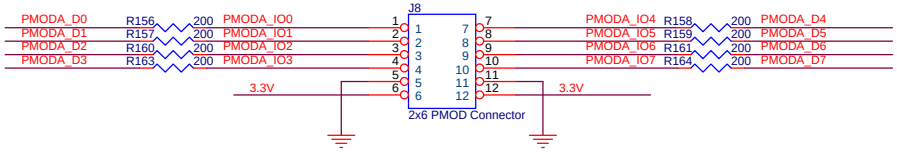
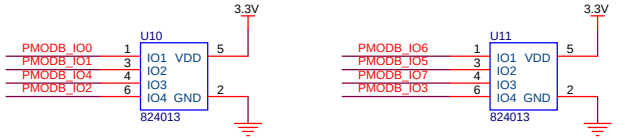
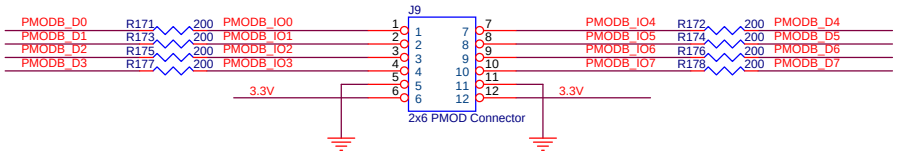
PMOD, GPIO, LVDS USER IO

PMOD

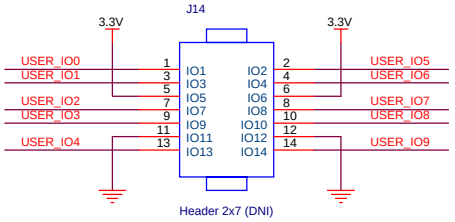






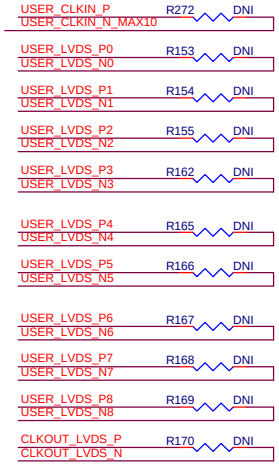


User GPIO

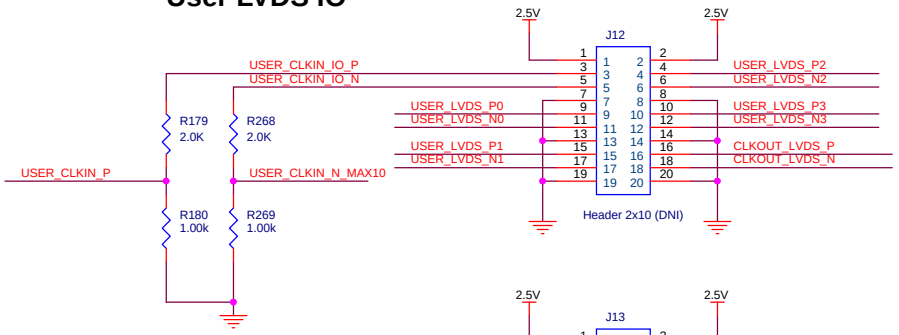


LVDS Termination

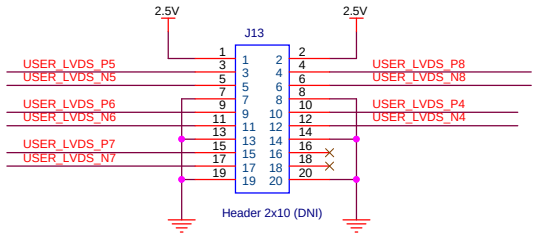
Note: Place near MAX 10 side.

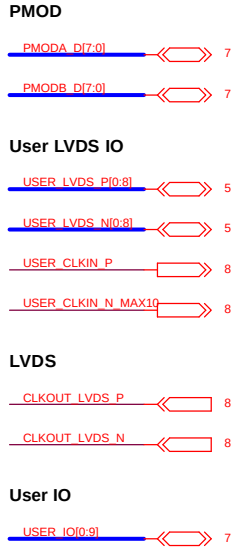


User LVDS IO



Note: USER_CLKIN_IO_P is used if external single-ended clk needs to use on-chip PLL resource. USER_CLKIN_IO_P/N is used for external differential clk input. Values of R179,R180,R268, and R269 might be adjusted according to user input voltage.





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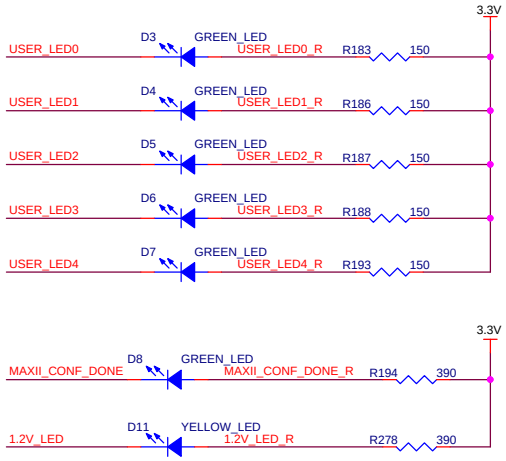
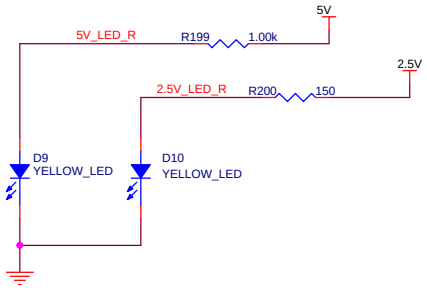
PUSHBUTTON, SWITCH, LED

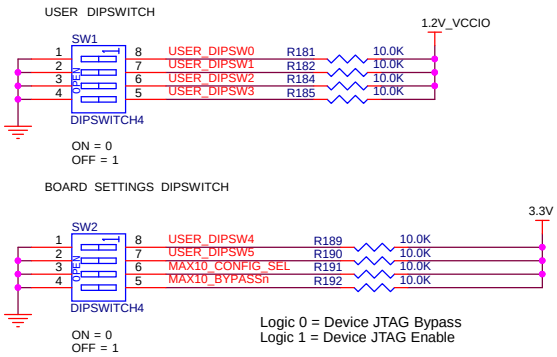
User LED



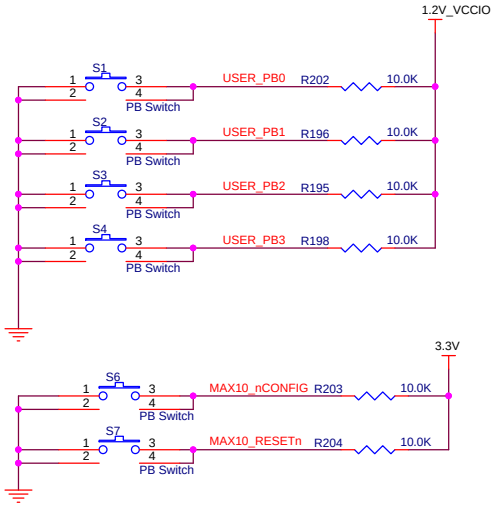
Power LED



User DIP Switch



User Pushbutton



MAXII

MAXII_CONF_DONE — 15

1.2V_LED — 15

User LED

USER_LED[0:4] — 7

User Pushbutton

USER_PB[0:3] — 6

MAX10_nCONFIG — 9

MAX10_RESETn — 9

User DIP Switch

USER_DIPSW[0:3] — 6

USER_DIPSW[4:5] — 4

MAX10_CONFIG_SEL — 9

MAX10_BYPASSn — 16

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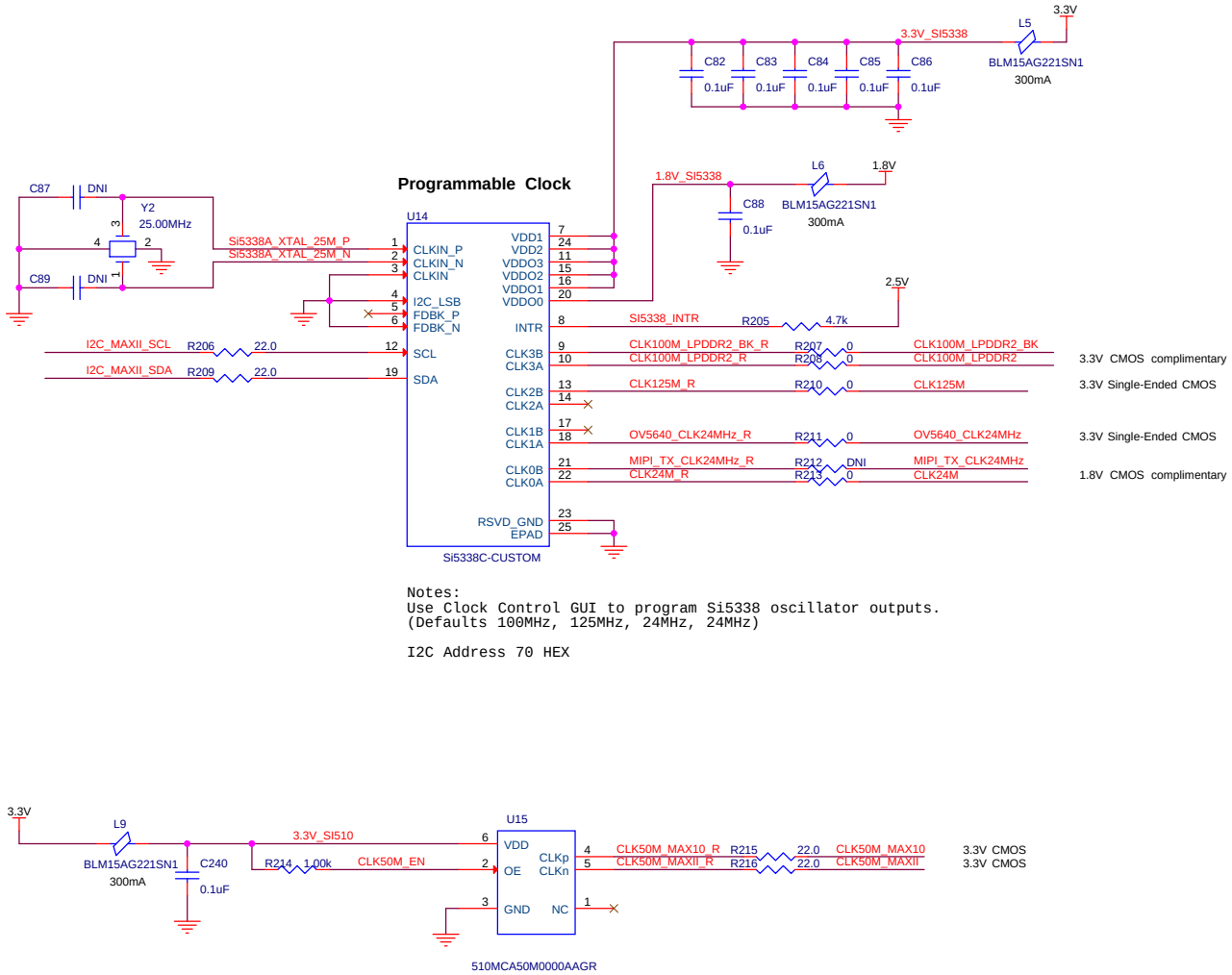
CLOCKING



Notes:
Use Clock Control GUI to program Si5338 oscillator outputs.
(Defaults 100MHz, 125MHz, 24MHz, 24MHz)

I2C Address 70 HEX

MAX 10

CLK50M_MAX10 8
CLK24M 8
CLK125M 8
CLK100M_LPDDR2 8
CLK100M_LPDDR2_BK 8
SI5338_INTR 16

MAXII

CLK50M_MAXII 15
I2C_MAXII_SCL 16
I2C_MAXII_SDA 16

DM385 CSI-2 TX Interface

OV5640_CLK24MHz 13
MIPI_TX_CLK24MHz 11

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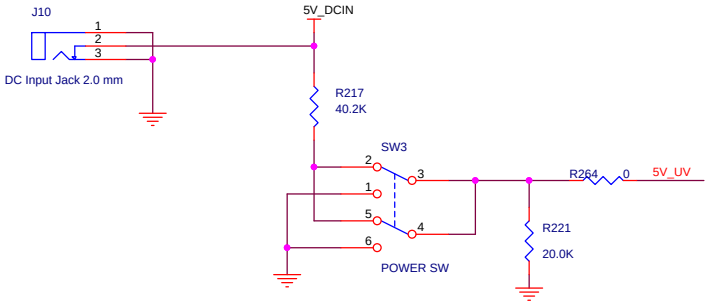
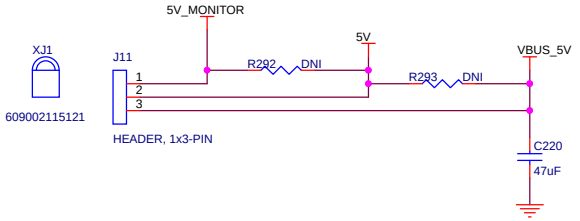
HOT SWAP and POWER 3.3V

5V
DC Input

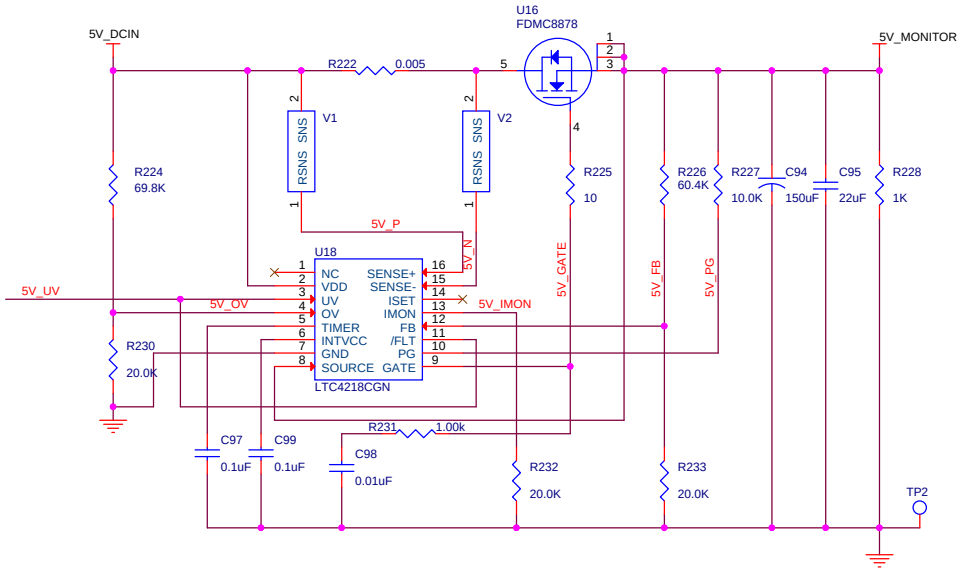




CAUTION:
When NOT using jumpers,
solder R292 for power input from DC Jack,
or solder R293 for USB power.
SOLDER ONLY ONE POWER OPTION,
AND SUGGEST NOT TO USE WITH JUMPER.

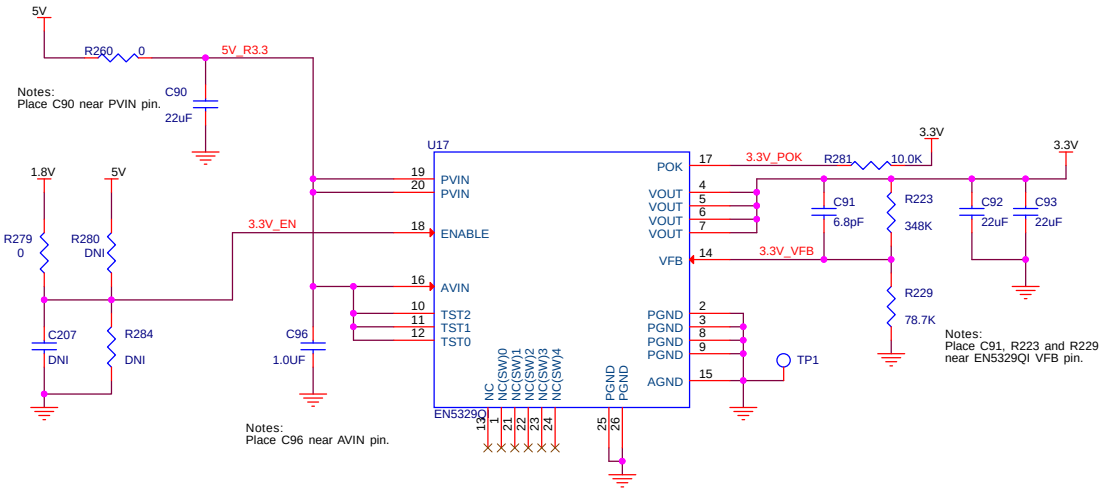
EN5329

Hot Swap for DC Plug



Hot Swap Controller Circuit

POWER 3.3V



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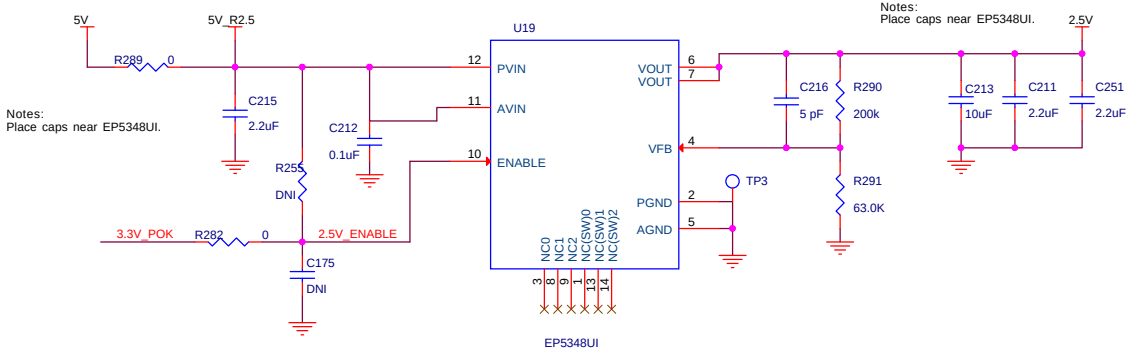
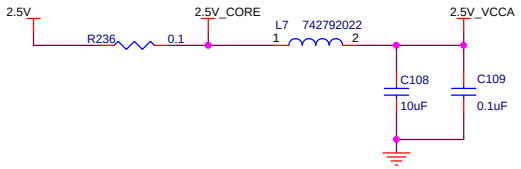
POWER 2.5V & 1.8V

POWER 2.5V

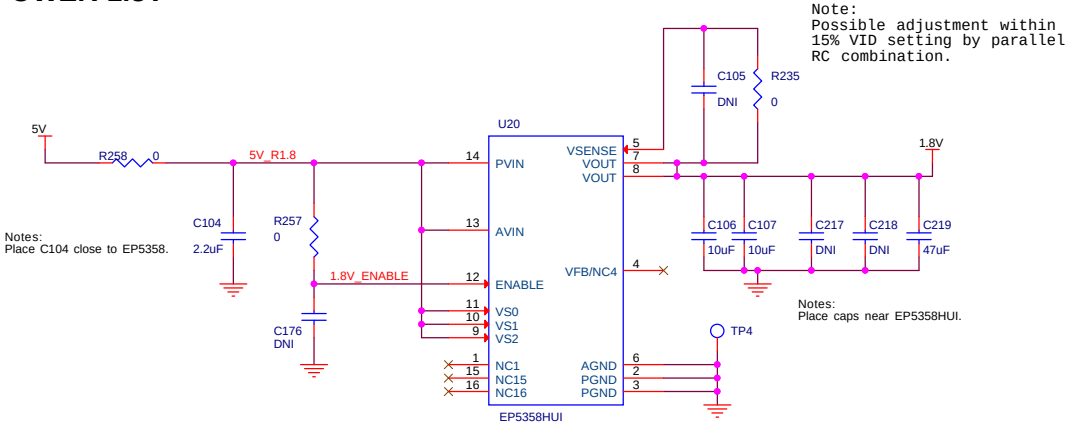


EN5329

POWER 2.5V_VCCA



POWER 1.8V



Note:
Possible adjustment within 15% VID setting by parallel RC combination.

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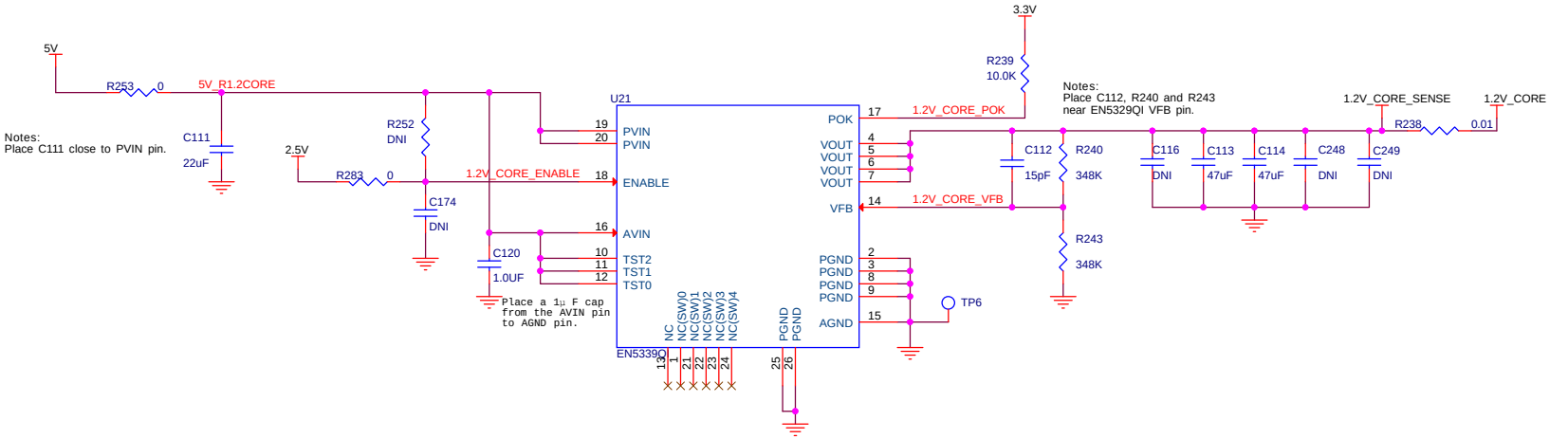
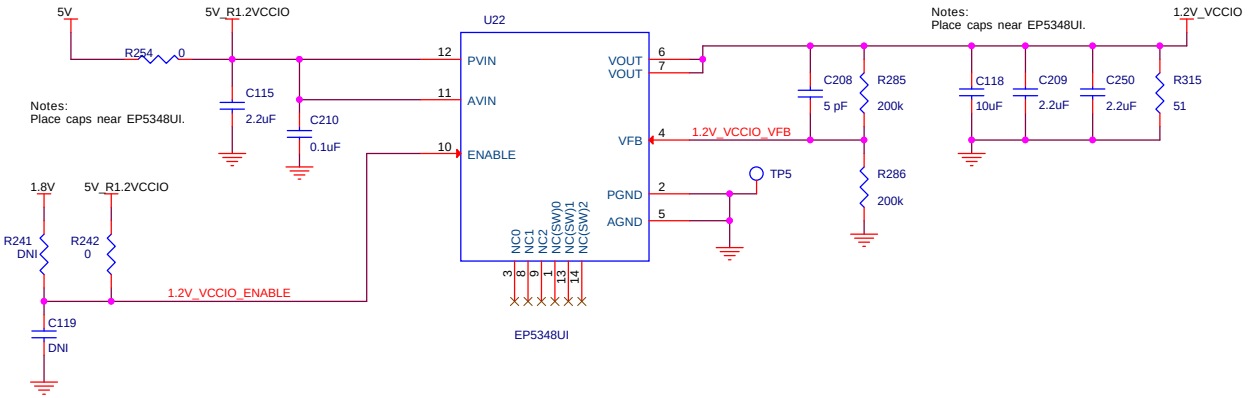
POWER 1.2V

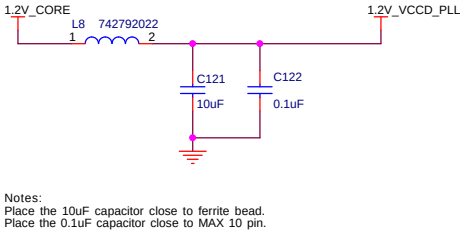
POWER 1.2V_CORE



POWER 1.2V_VCCIO



POWER 1.2V_VCCD_PLL



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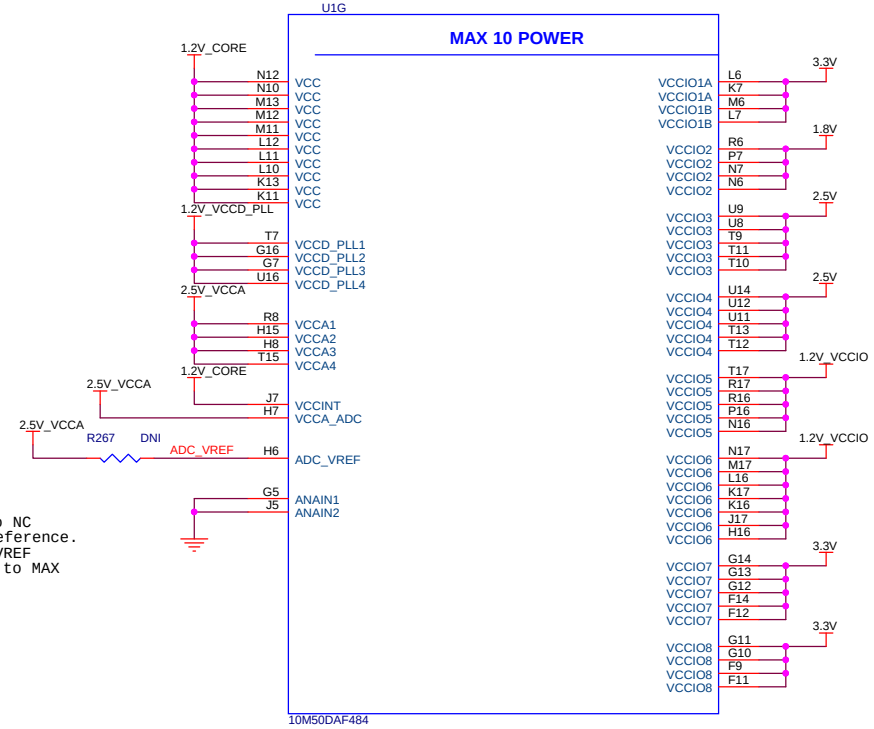
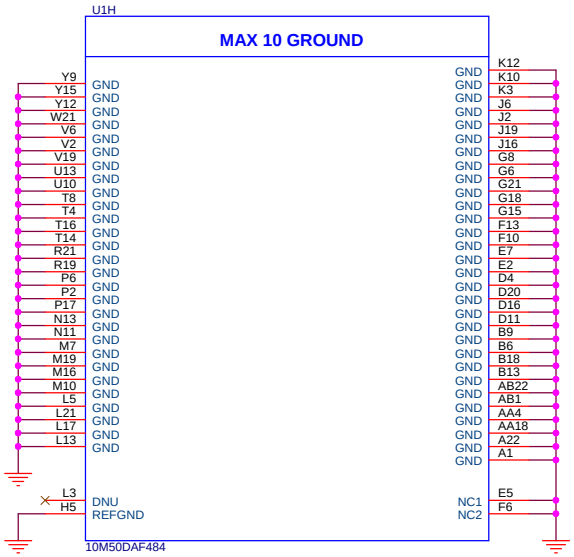
MAX 10 POWER & GROUND

Note:
According to MAX 10 pin connection guideline PCG-01018-1.2, "Tie the VCCINT pin to any 1.2V power domain if you are not using ADC." Therefore, connect VCCINT to 1.2V_CORE for DC or DF production device migration.

Note:
According to MAX 10 pin connection guideline PCG-01018-1.2, "Tie the VCCA_ADC pin to any 2.5V power domain if you are not using ADC, and do not tie the VCCA_ADC pin to GND." Therefore, connect VCCA_ADC to 2.5V_CORE for DC or DF production device migration.

Note:
For ES device, connect ADC_VREF to NC when not using external voltage reference. For DC/DF production device, ADC_VREF pin is migrated to VCCA according to MAX 10 Errata.





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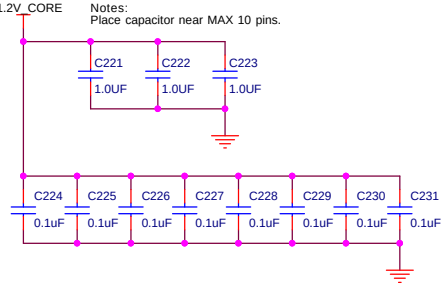
DECOUPLING

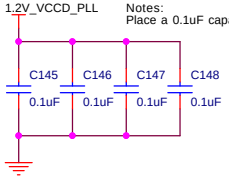
1.2V_CORE

Notes:
Place capacitor near MAX 10 pins.



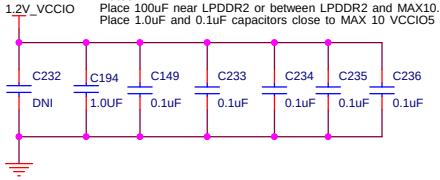
1.2V_VCCD_PLL

Notes:
Place a 0.1uF capacitor close to each MAX 10 VCCD pin.



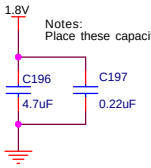
1.2V_VCCIO

Notes:
Place 100uF near LPDDR2 or between LPDDR2 and MAX10.
Place 1.0uF and 0.1uF capacitors close to MAX 10 VCCIO5 and VCCIO6 pins.



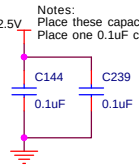
1.8V

Notes:
Place these capacitors close to MAX 10 VCCIO2.



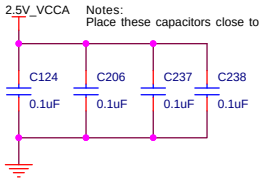
2.5V

Notes:
Place these capacitors close to MAX 10 VCCIO3 and VCCIO4 pins.
Place one 0.1uF close to MAX 10 VCCA_ADC pin.



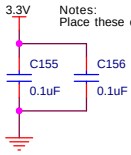
2.5V_VCCA

Notes:
Place these capacitors close to each MAX 10 VCCA pin.



3.3V

Notes:
Place these capacitors close to MAX 10 VCCIO7 and VCCIO8 pins.



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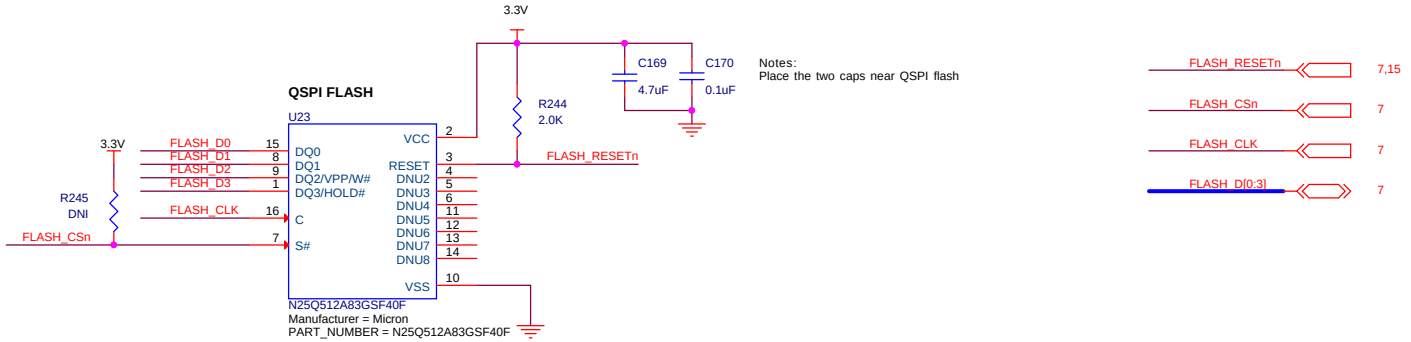
QSPI FLASH



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