

**Schematic modified for
CY8CKIT-064S0S2-4343W PSoC 64 Wi-Fi BT Secure Boot Pioneer Kit**

CYW9-BASE-01 Pioneer Baseboard

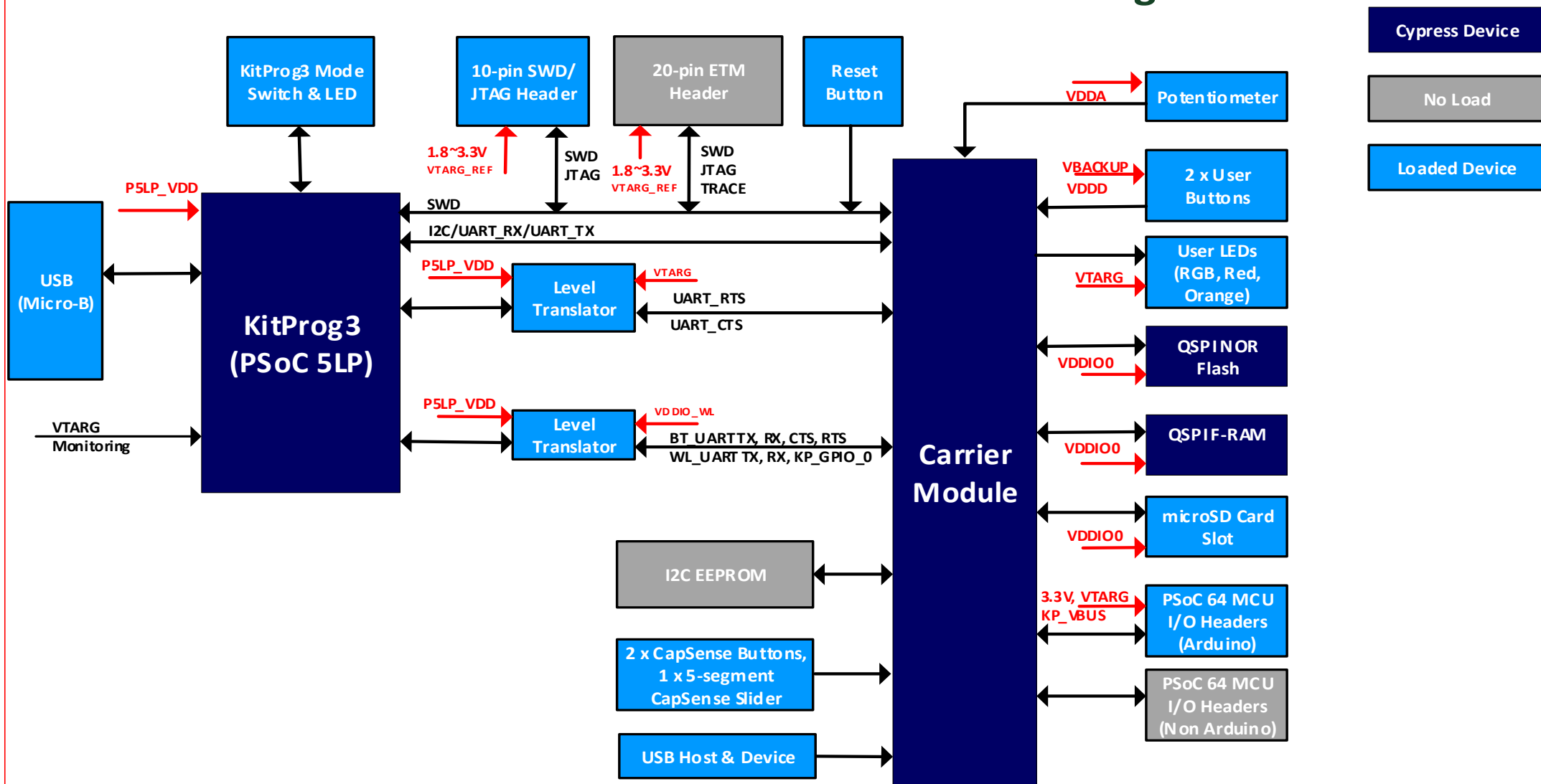
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01	Title Page
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03	Power Supply Block Diagram
04	Power Supply (1)
05	Power Supply (2)
06	KitProg3 Controller
07	KitProg3 Power and Headers
08	Carrier Module Power
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Drawing Numbers

PCBA	121-60579-01
PCB	600-60552-01
FAB DRW	610-60552-01
ASSY DRW	620-60552-01
SCH DRW	630-60552-01

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SCH Title : CYW9-BASE-01 Pioneer Baseboard							
Page Title : Title Page							
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CYW9-BASE-01 Architecture Block Diagram



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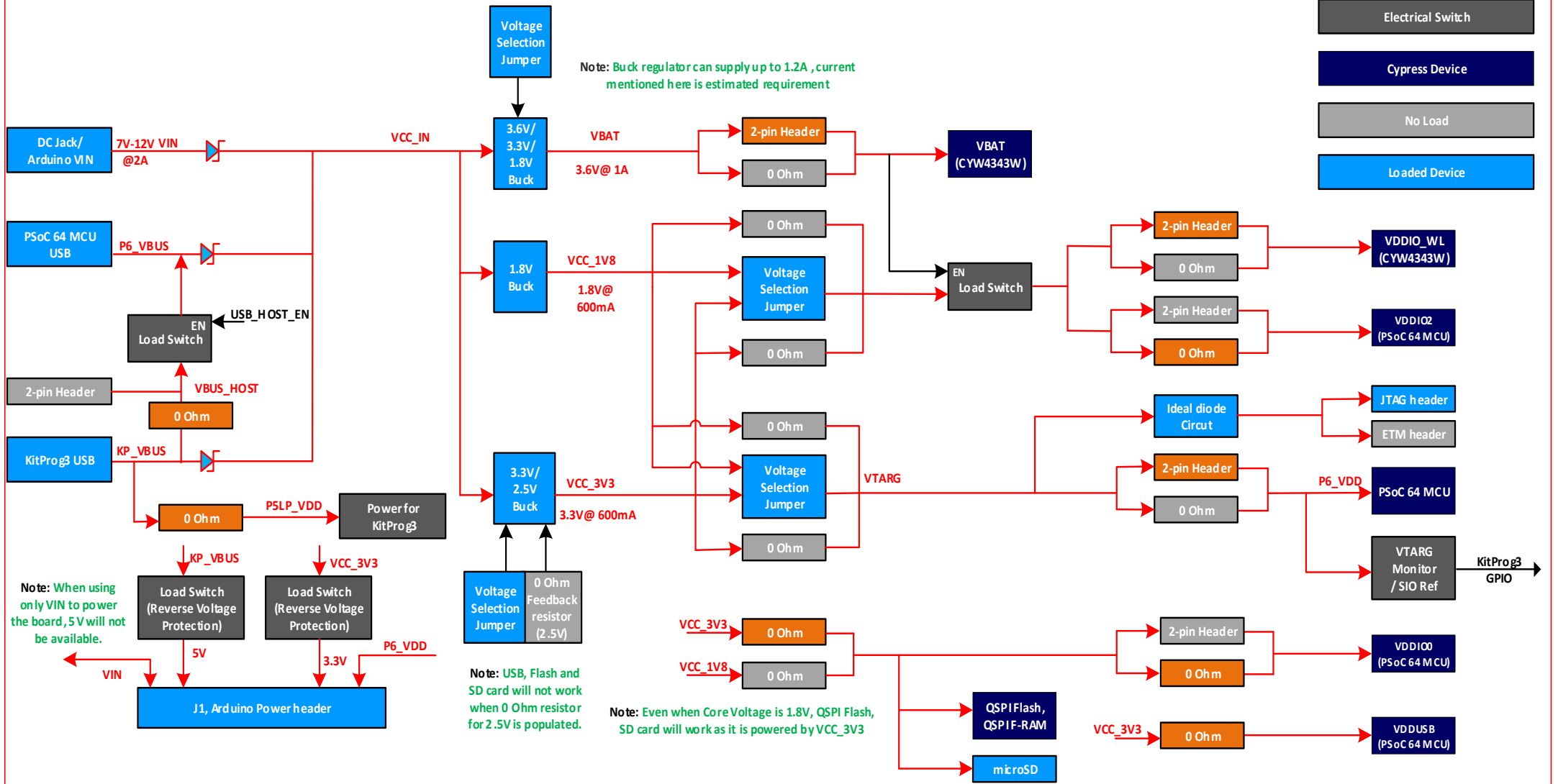
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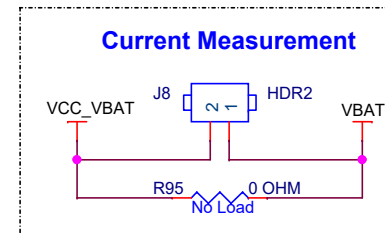
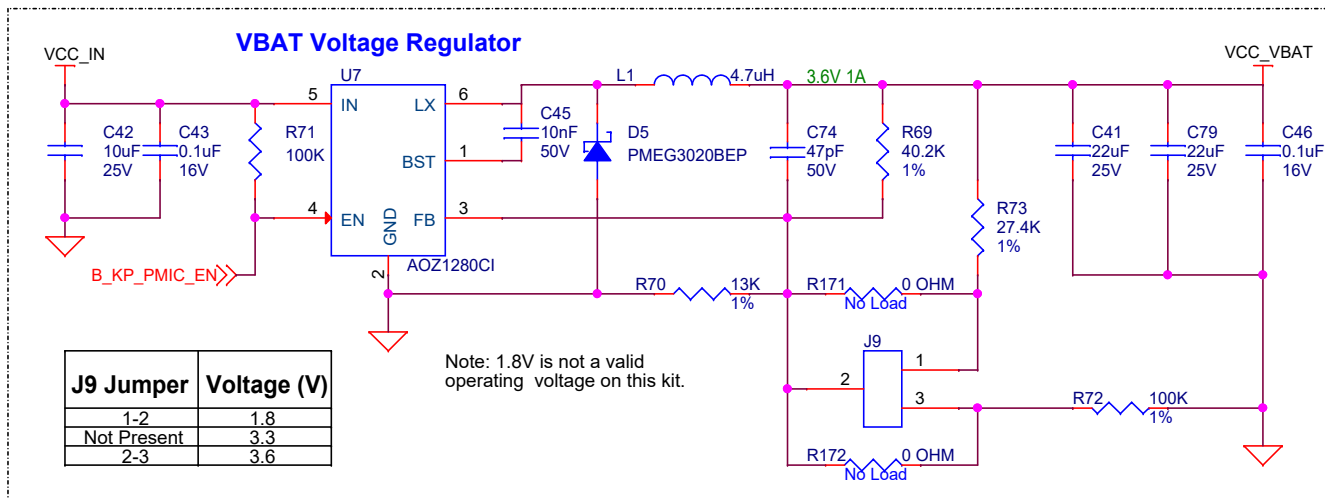
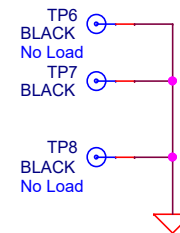
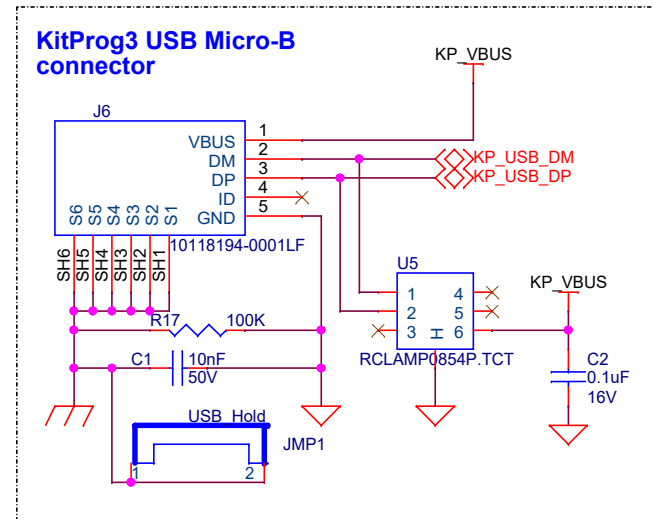
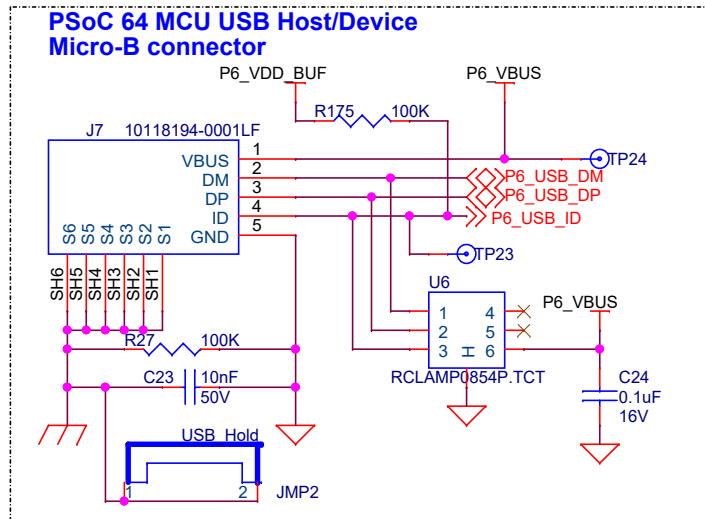
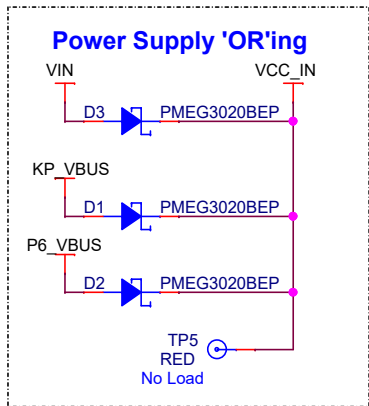
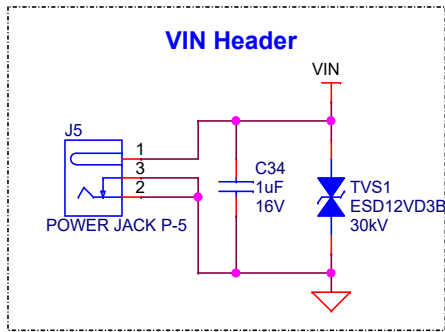
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Page Title : Functional Block Diagram

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Power Supply Section





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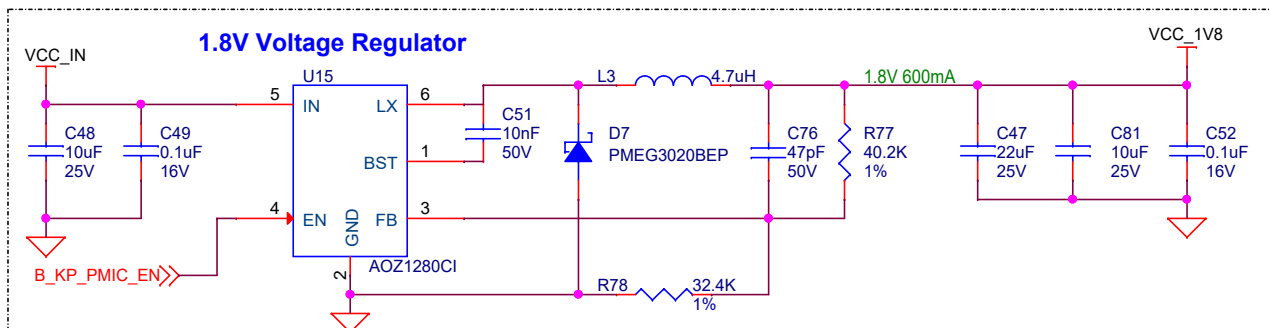
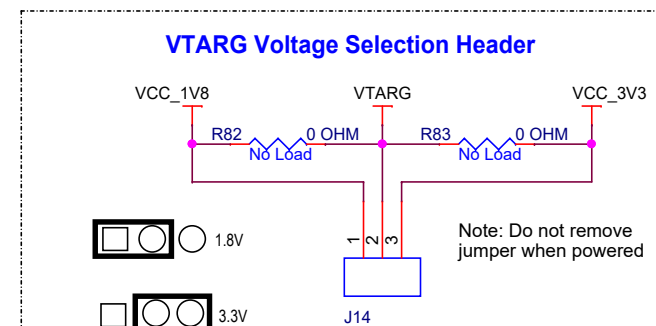
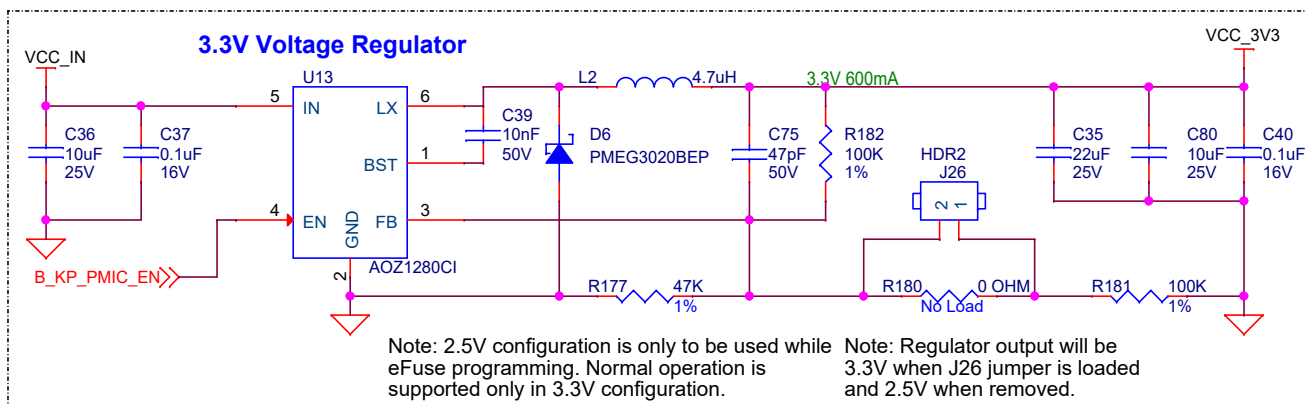
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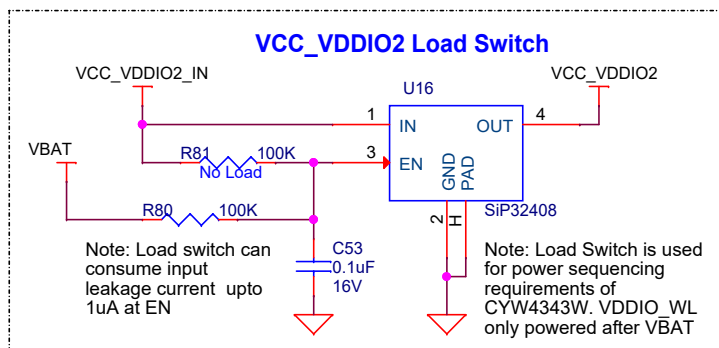
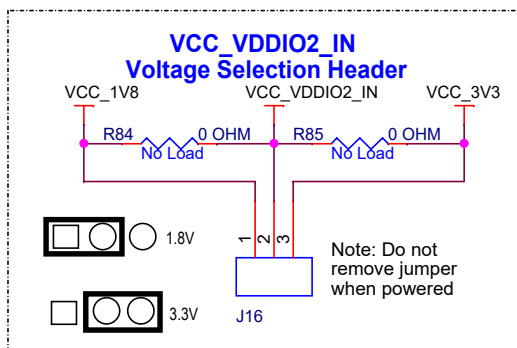
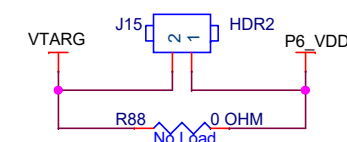
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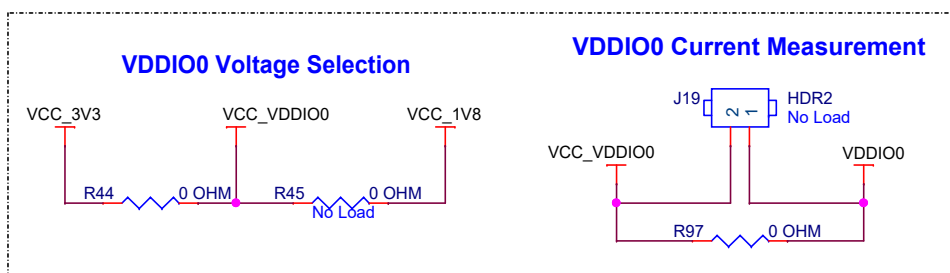
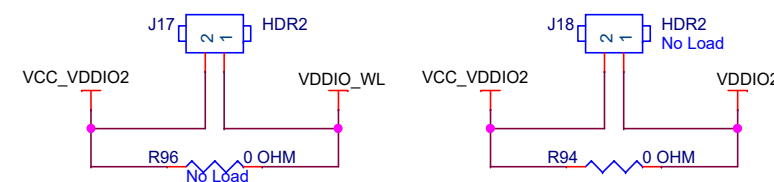
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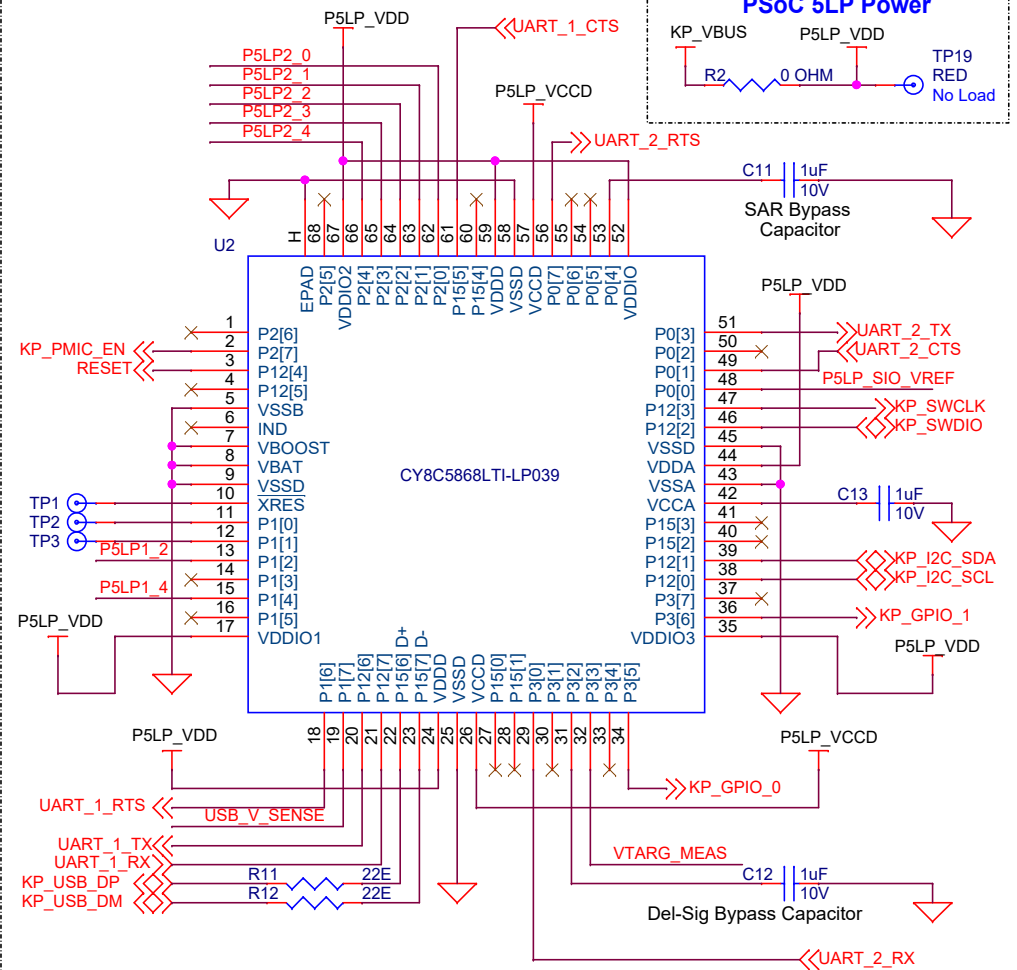
P6_VDD Current Measurement



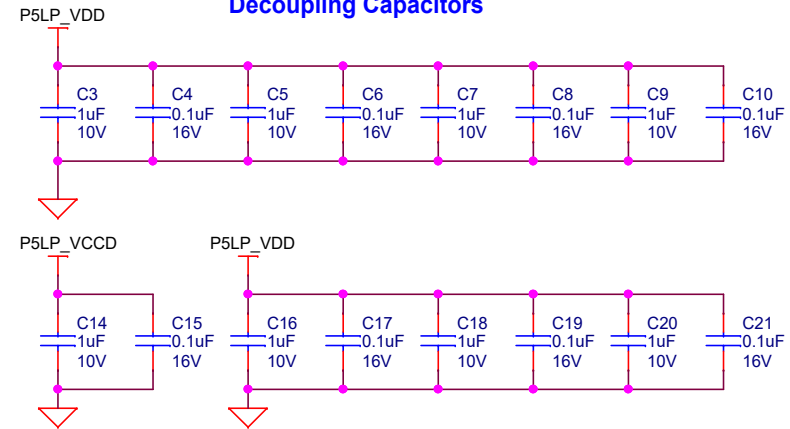
VDDIO_WL & VDDIO2 Current Measurement



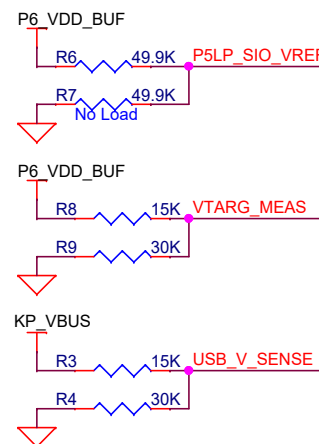
PSoC 5LP based KitProg3



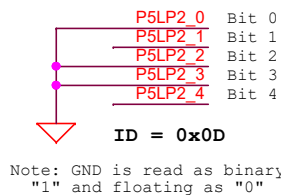
Decoupling Capacitors



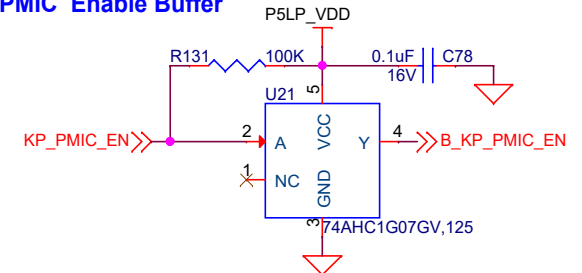
Voltage Monitoring



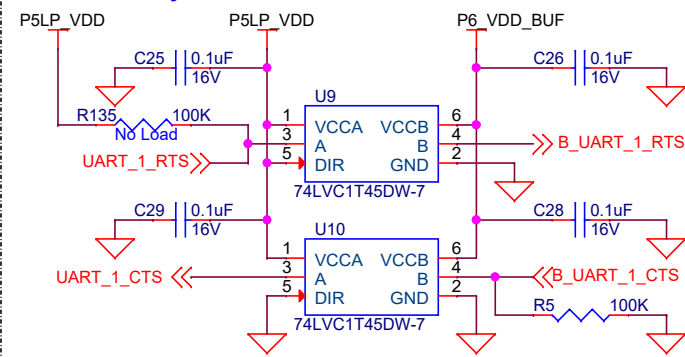
KitProg3 H/W Revision



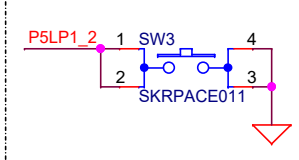
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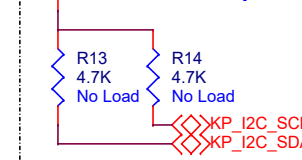
Primary UART H/W Flow Control Level Translator



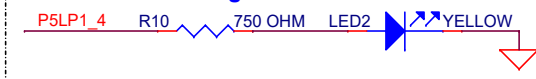
Mode Switch



I2C Pull-ups



KitProg3 Status LED



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Page Title : KitProg3 Controller

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Note: If R130 is loaded and external power is used, make sure to remove jumper shunt from J14 to prevent reverse voltage to on-board regulator

VTARG_REF

C27
1uF
10V

TVS2
ESD3V3D5-TP
30kV
No Load

J11

1 2
3 4
5 6
7 8
9 10

50MIL KEYED SMD

TMS_SWDIO
TCLK_SWCLK
TDO_SWCL
TDI
XRES_L_MCU

VDDIO_WL

C62
1uF
10V

TVS3
ESD3V3D5-TP
30kV
No Load

J13

1 2
3 4
5 6
7 8
9 10

WL_JTAG_TMS
WL_JTAG_TCLK
WL_JTAG_TDO
WL_JTAG_TDI
WL_JTAG_TRST_L

50MIL KEYED SMD
No Load

VTARG REF

J12

1 2 TMS_SWDIO

3 4 TCLK_SWCLK

5 6 TDO_SWO

7 8 TDI

9 10 XRES_L MCU

11 12 TRACE_CLK

13 14 TRACEDATA_0

15 16 TRACEDATA_1

17 18 TRACEDATA_2

19 20 TRACEDATA_3

HDR_S 10x2

No Load

R158 10K No Load
R157 10K No Load
R112 10K No Load

WL JTAG Pull-ups

VDDIO_WL

R111 10K No Load WL_JTAG TMS

R79 10K No Load WL_JTAG TCLK

R67 10K No Load WL_JTAG TDO

KP_SWDIO R37 0 OHM TMS_SWDIO
 KP_SWCLK R36 0 OHM TCLK_SWCLK
 RESET R35 0 OHM XRES_L_MCU

UART1_RX << R61 0 OHM >> ARD_D1
R116 0 OHM
No Load IO1

UART1_TX >> R21 0 OHM >> ARD_D0
R115 0 OHM
No Load IO0

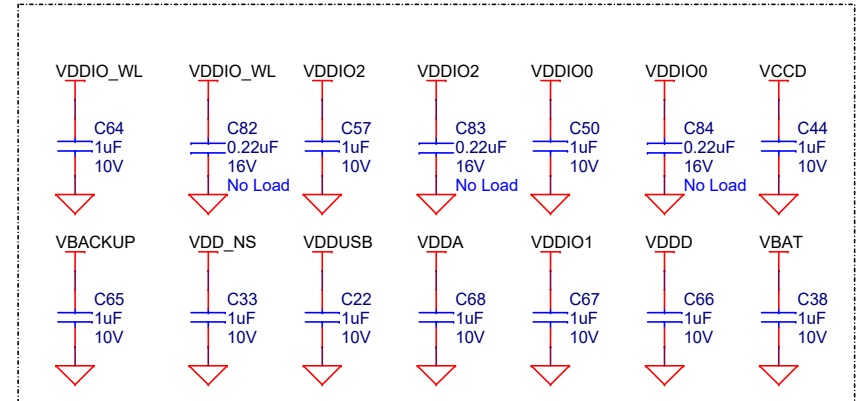
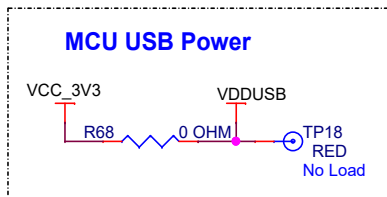
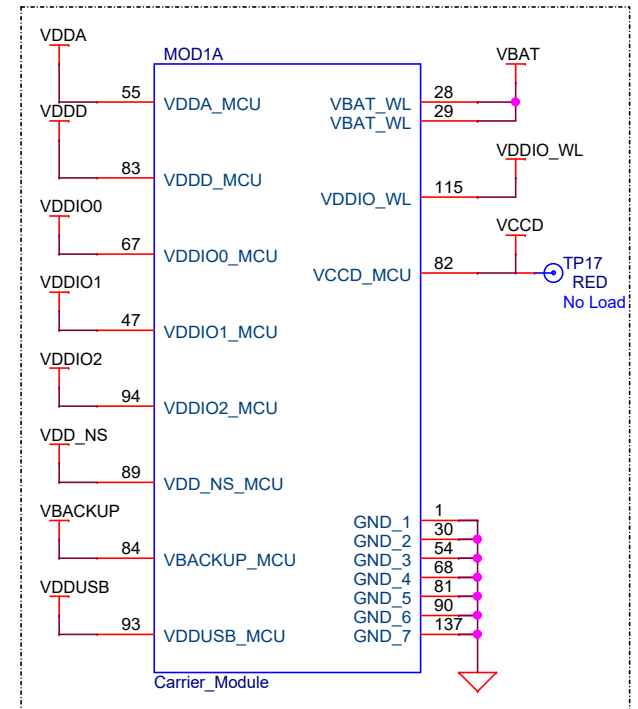
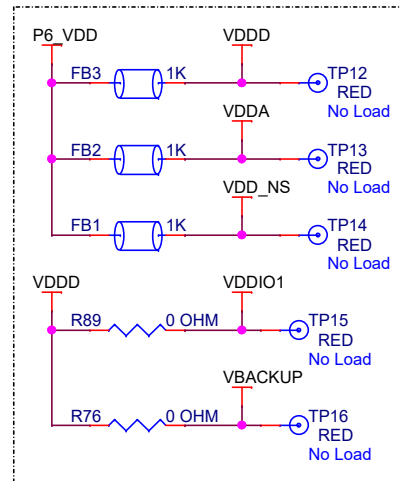
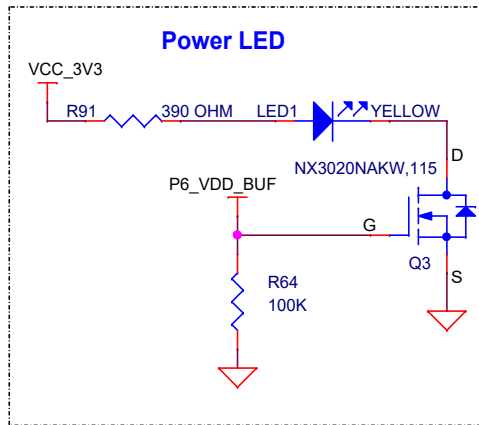
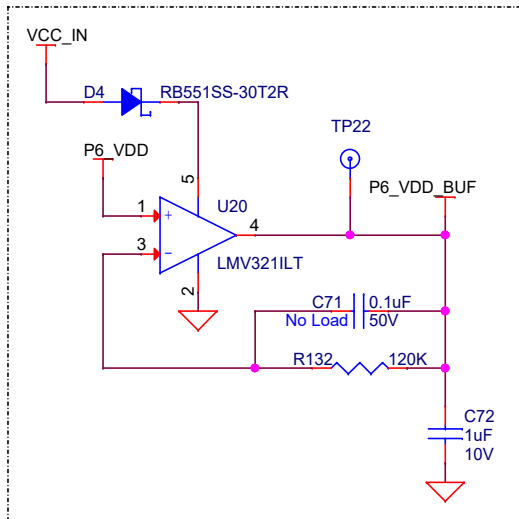
B_UART1_CTS << R19 0 OHM >> ARD_D2
B_UART1_RTS << R18 0 OHM >> ARD_D3

The schematic diagram illustrates the UART2 module connections. It shows four signal lines with their respective components and destinations:

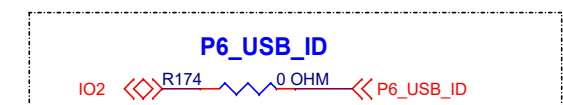
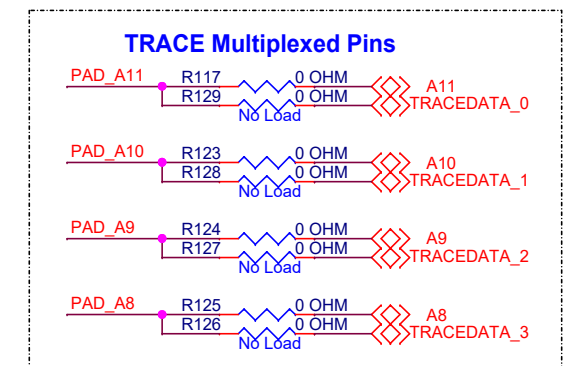
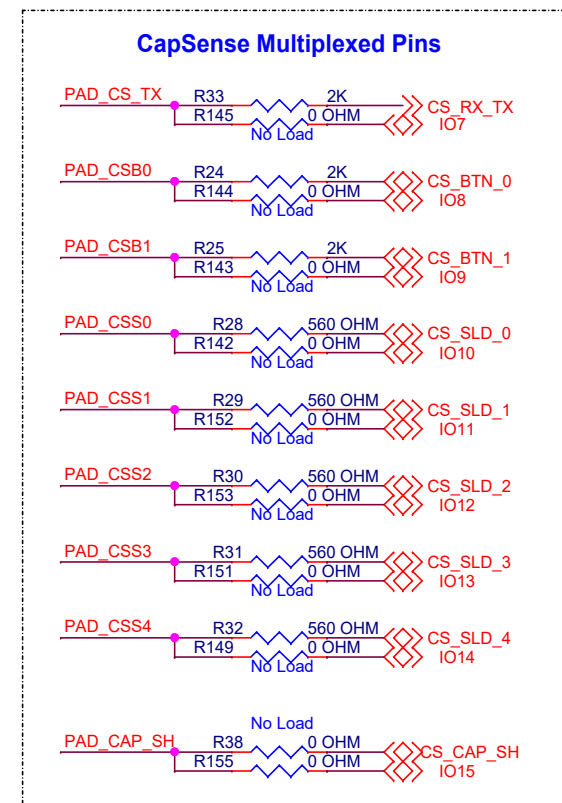
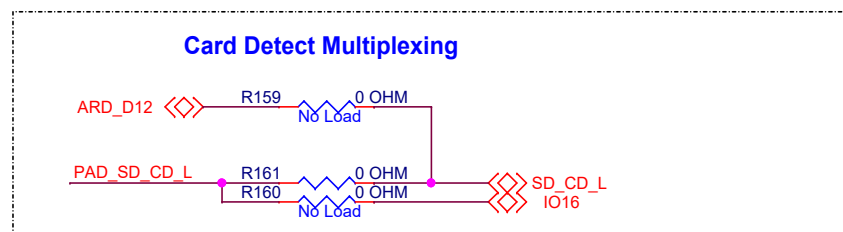
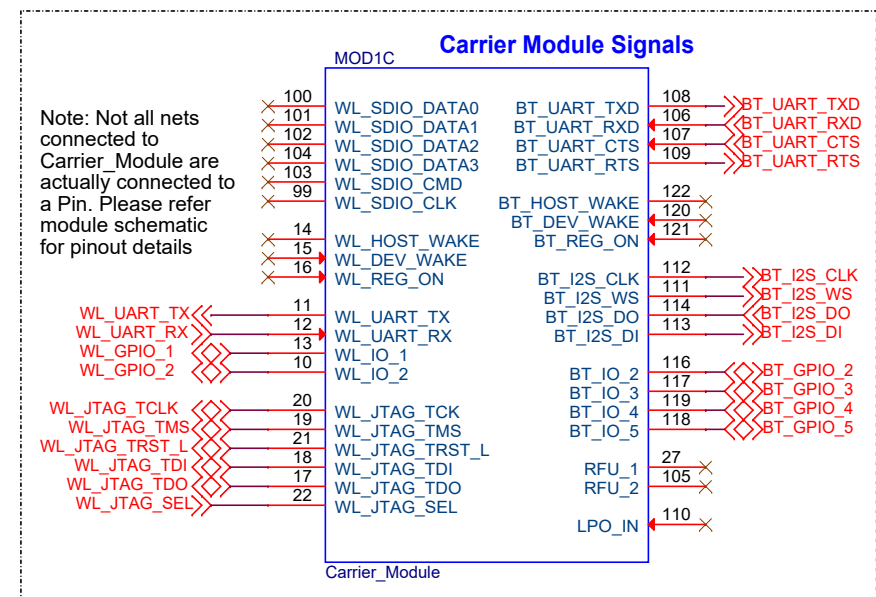
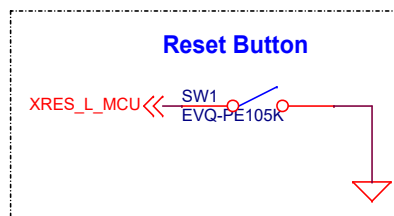
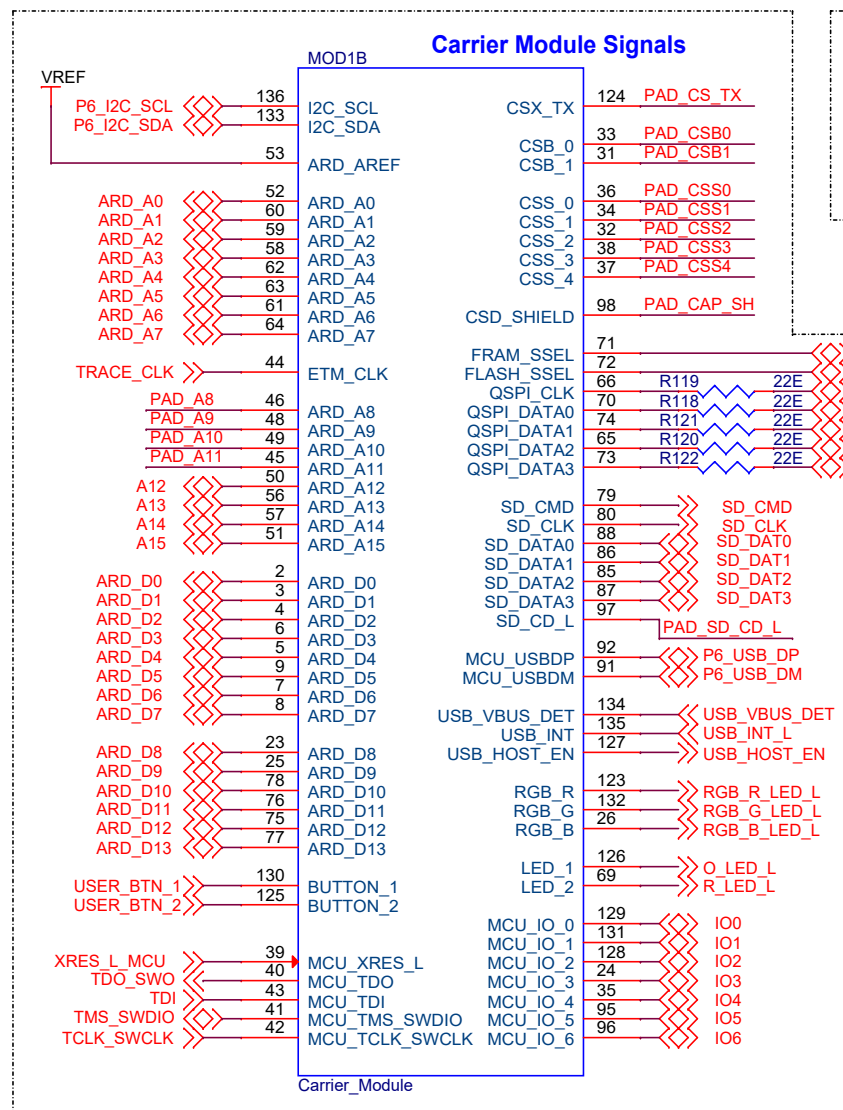
- B_UART_2_TX**: Connected to a network of **R52** and **R48** resistors. The output is split into **BT_UART_RXD** (0 OHM) and **WL_UART_RX** (0 OHM). A **No Load** label is present below the network.
- B_UART_2_RX**: Connected to a network of **R53** and **R49** resistors. The output is split into **BT_UART_TXD** (0 OHM) and **WL_UART_TX** (0 OHM). A **No Load** label is present below the network.
- B_UART_2_RTS**: Connected to resistor **R54** (0 OHM), which is then connected to **BT_UART_CTS**.
- B_UART_2_CTS**: Connected to a network of **R55** (0 OHM) and **R137** (100K) resistors. The output is connected to **BT_UART_RTS**. A **No Load** label is present below the network.



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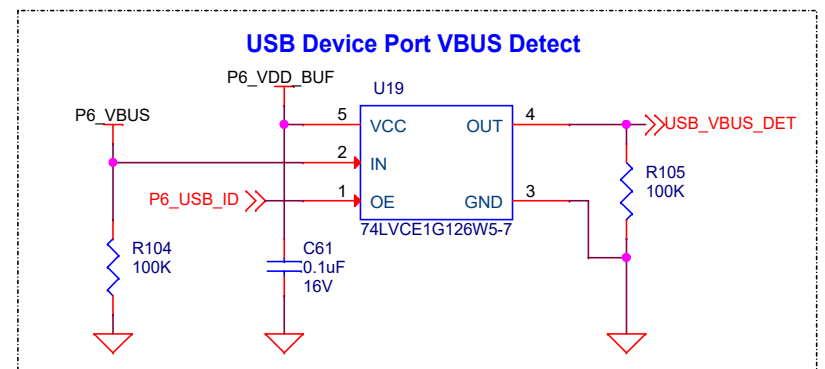
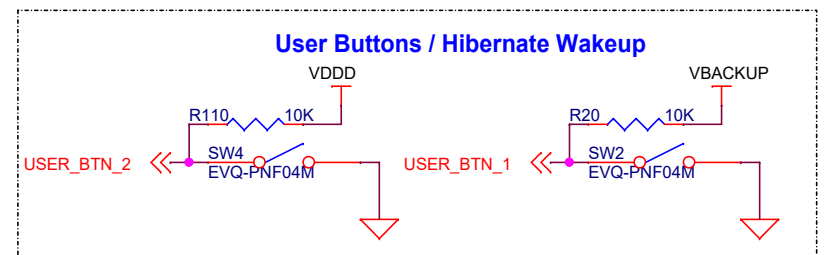
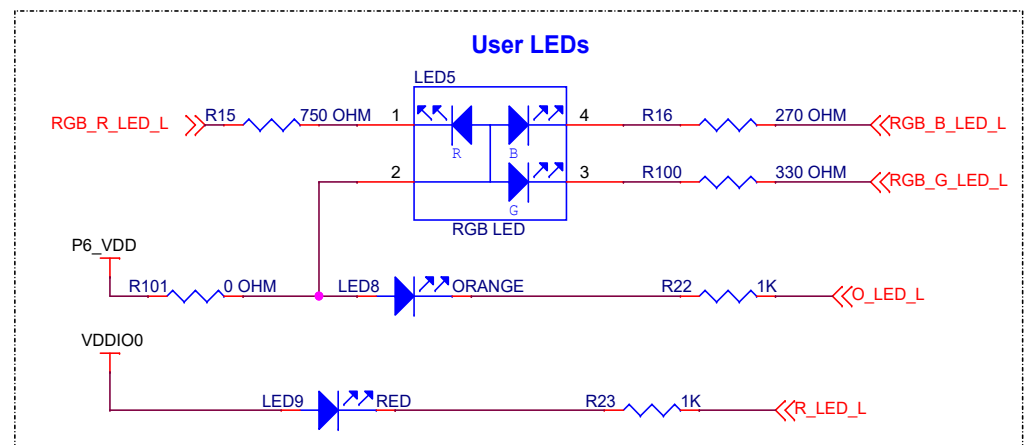
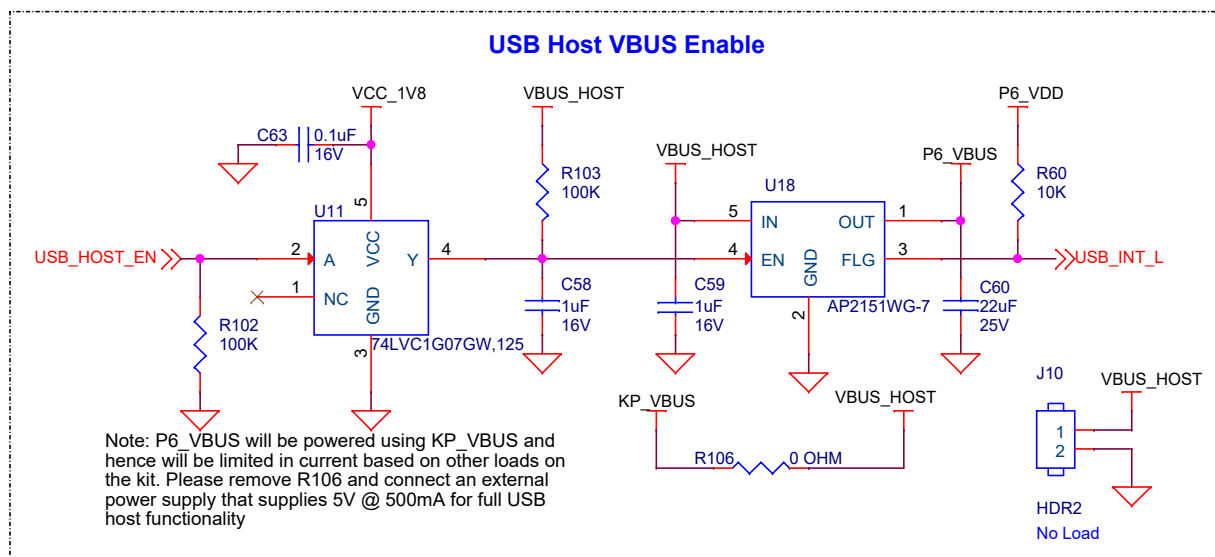
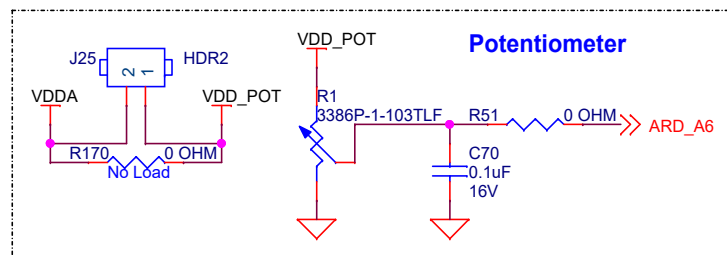
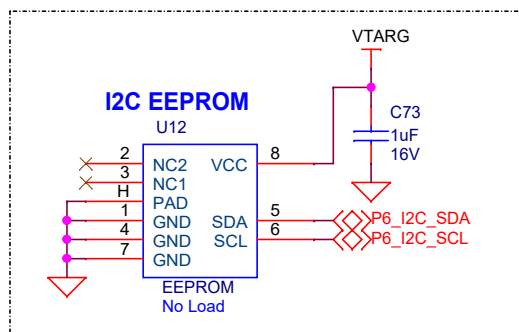
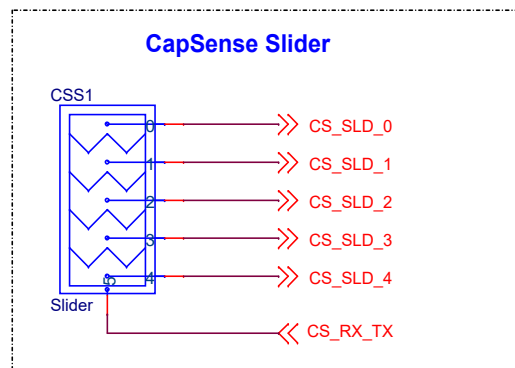
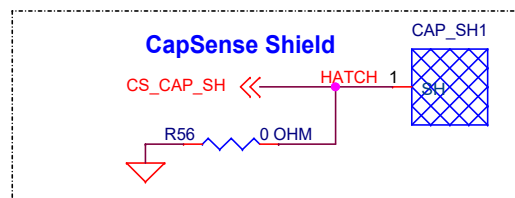
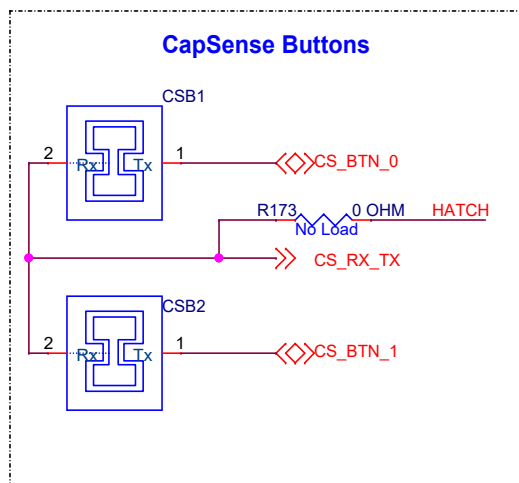
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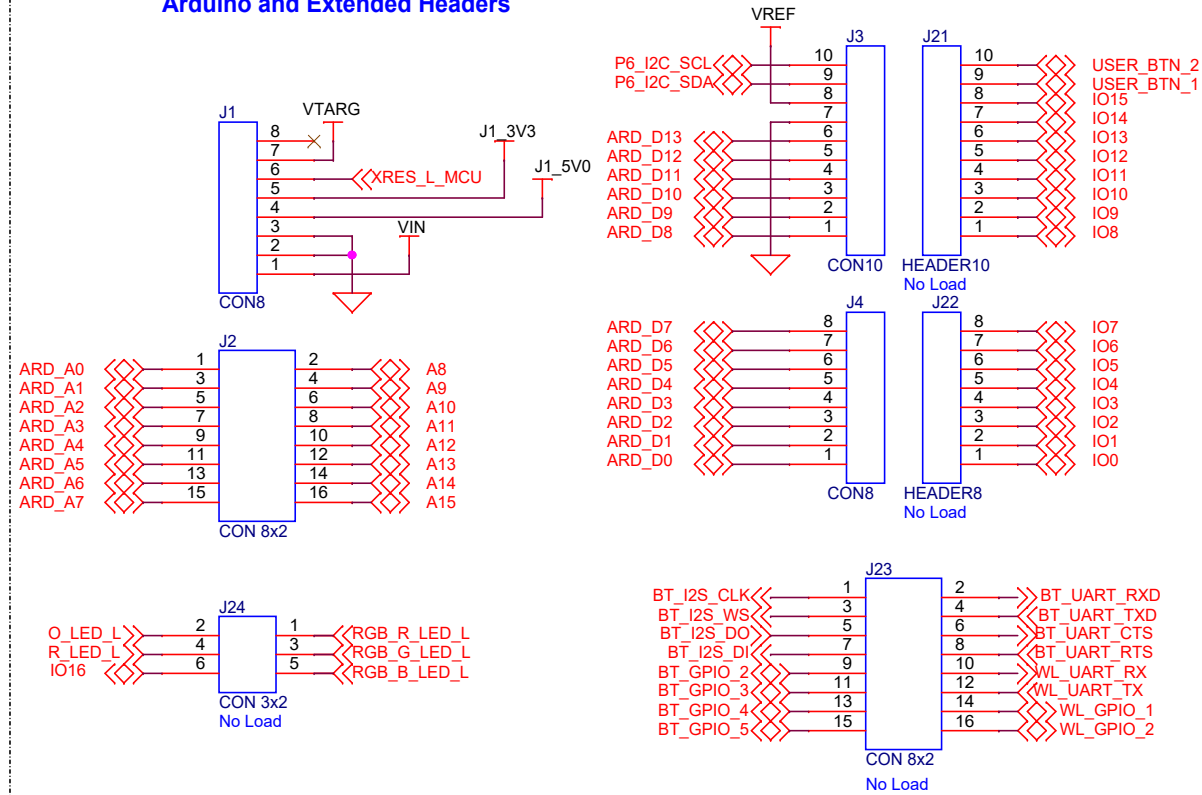
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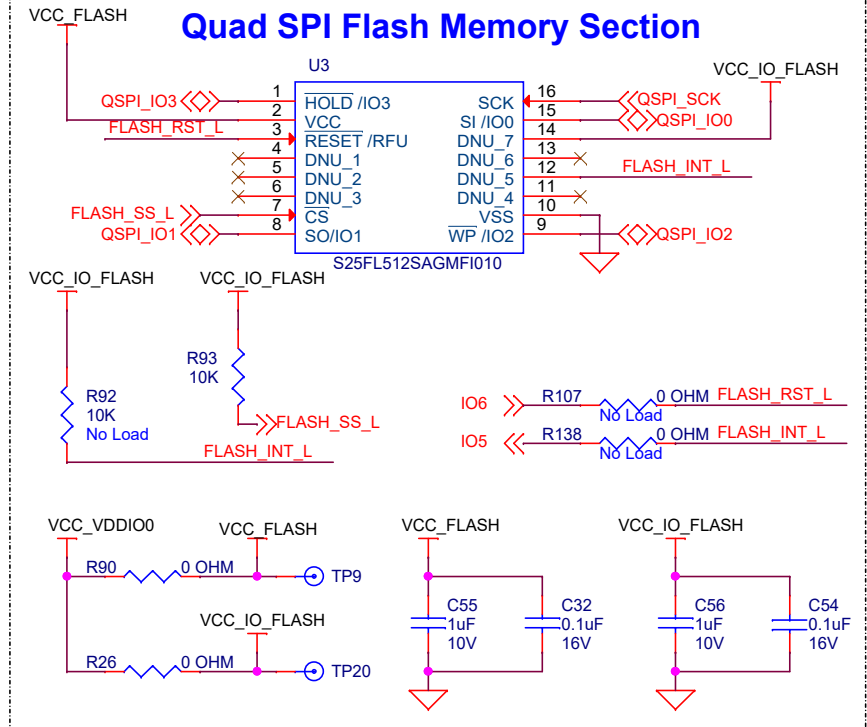
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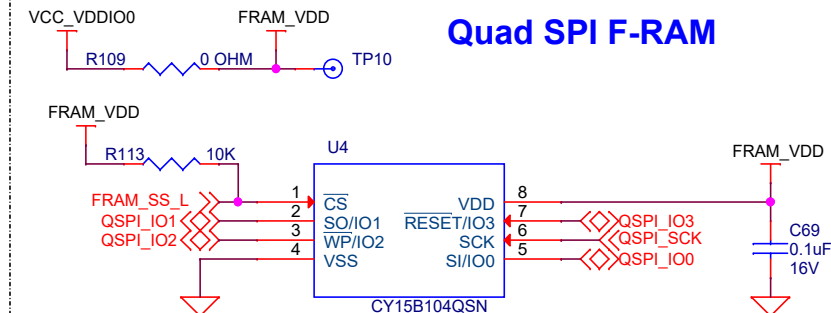
Arduino and Extended Headers



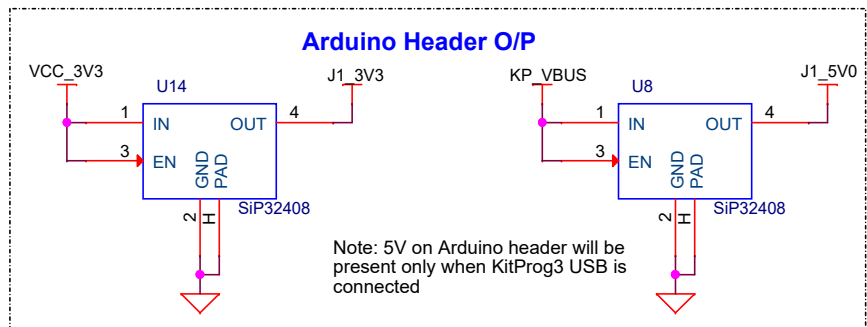
Quad SPI Flash Memory Section



Quad SPI F-RAM



Arduino Header O/P



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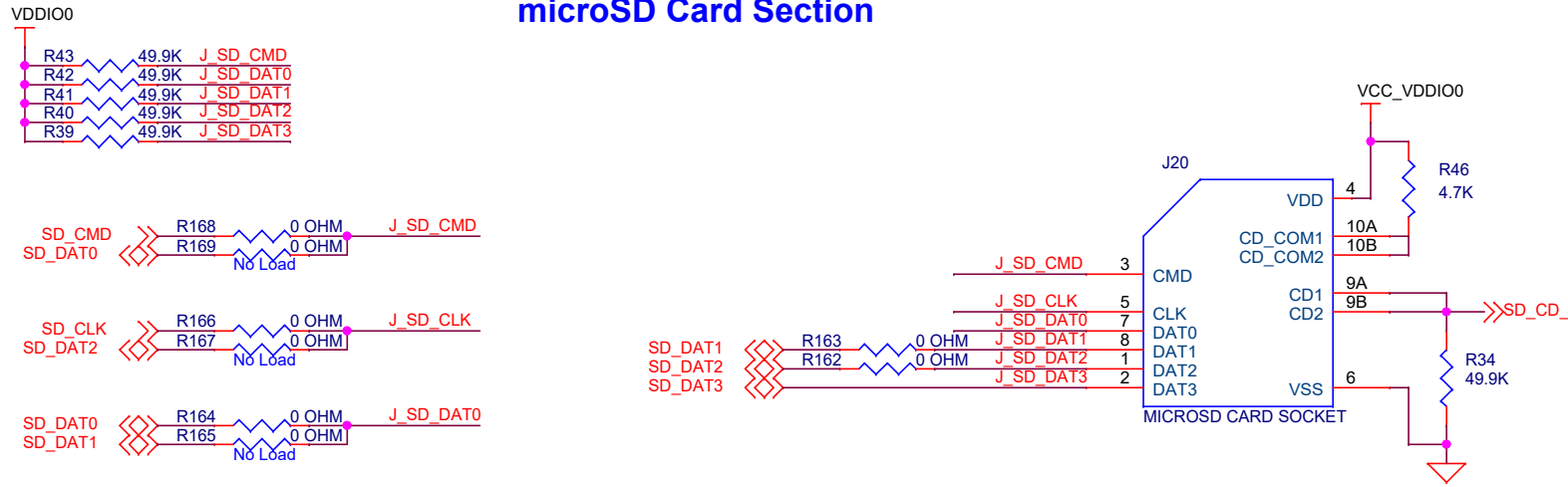
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Page Title : Expansion Headers & Memory

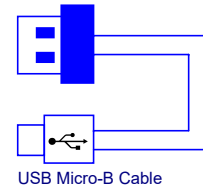
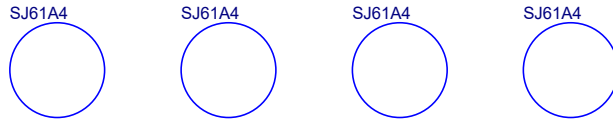
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microSD Card Section

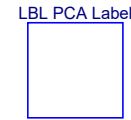


Accessories

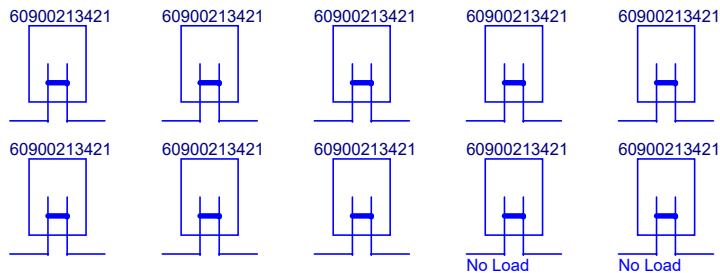
Cylindrical Bump-ons



PCBA label



Jumper Shunts



Acrylic Overlay

Overlay

Color: Clear, Transparent
Finish: Matt

Dimensions:
45.21mm - length
36.93mm - height
1mm - thickness



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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Internal Release	2019/05/13
02	Internal Release	2019/05/21
03	Internal Release	2019/07/23
04	Internal Release	2019/08/08
05	Initial Release	2019/09/18
06	Internal Release	2019/12/09
07	1. Added optional jumper header J26 at VCC_3V3 output voltage selection between 3.3V and 2.5V 2. VCC of USB Device VBUS Detect is changed from VTARG to P6_VDD_BUF	2020/01/28
08	Loaded R133, R134 instead of R13, R14	2020/02/13



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