



Application Note

AN000710

Communication Interface

Communication Mode (I²C)

v1-00 • 2020-Jul-21

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1 Introduction

This document describes how to step into **communication mode (I²C)** with the AS5715R.

The AS5715R will start up immediately in operational mode after powering up and is ready to be used in the final application.

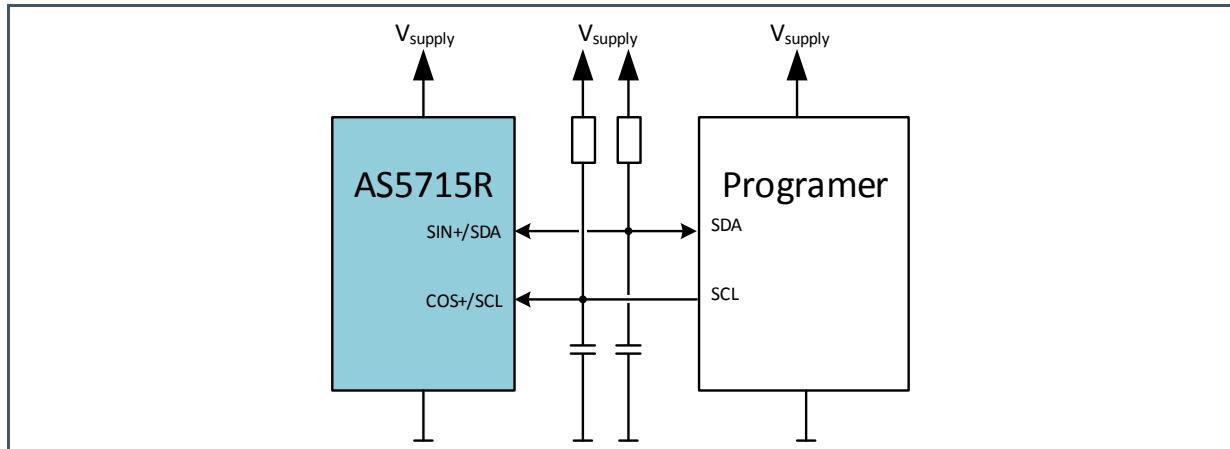
The customer can choose to personalize some settings in the customer OTP section. For this, the customer has to apply the customer **rma procedure** to activate the I²C interface and allow the writing and programming of the customer OTP section.

When the customer OTP section is already burned (finally and irreversible programmed), the AS5715R is fully locked! Thus, no execution of the customer rma procedure is possible anymore!

1.1 Setup

For Details, see chapter “Application Circuits” in the datasheet.

Figure 1 :
Communication/Programming Setup



The programmer should have **push pull-output** for **rma-procedure** and open-drain-output for communication mode (I²C).

2 I²C Communication

2.1 Activate Communication Interface

After powering up, the sensor is automatically in functional mode and the pin 11(SIN+/SDA) and pin 9 (COS+/SCL) are driven as analog output.

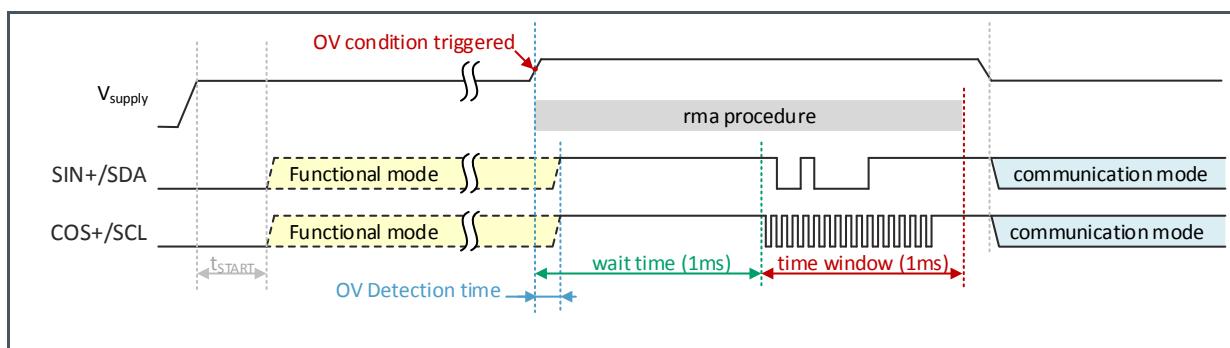
For changing into I²C Communication mode, the rma procedure has to be executed.



CAUTION

rma procedure can only be done, when the OTP section is not burned

Figure 2:
rma Procedure



The rma procedure consists of particular time frames, which starts when the sensor notices an overvoltage (OV Detection). Therefore, the supply voltage increases until the threshold voltage (VCCOVTH_{typ} or VDD3V3OVTH_{typ}). When the sensor detects an overvoltage, the output goes into high-Z after "OV Detection time".

After 1 ms "waiting time" there is a "time window", where the programmer can send the rma-pulses. After this procedure and at normal voltage supply, the sensor reaches communication mode.

At overvoltage, the sensor is in "safe state" (for safety reasons the output goes into high-Z). First, the supply voltage must decrease under the threshold voltage and its typical value, then the outputs/ I²C are reactivate.

For detailed information on "Overvoltage detection" see datasheet (AS5715R_DS000511_2-00), chapter "Power Supply".

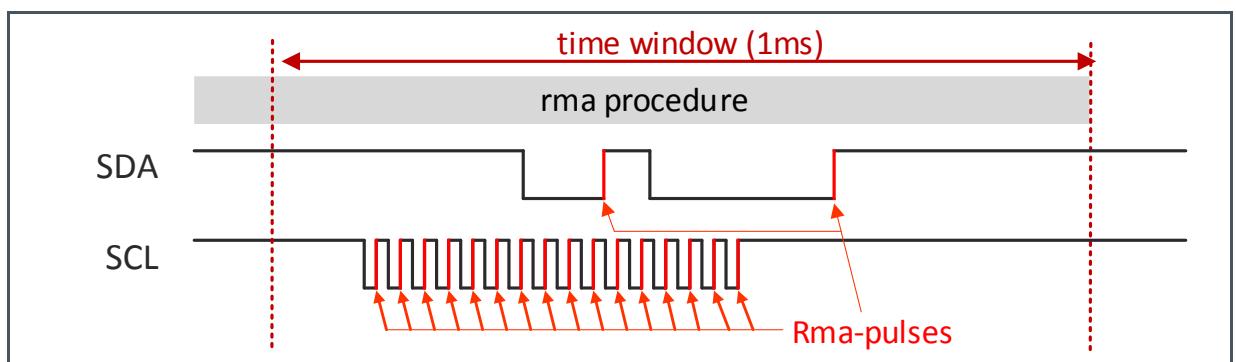
2.1.1 rma Pulses

Following pulses must be executed on SDA and SCL during the “time window” for changing the device into Communication mode.

16 pulses (16x rising edge) on **SCL**

2 pulses (2x rising edge) on **SDA**

Figure 3 :
Unlock Command



The pulses on SDA and SCL are independent of each other!

The pulses on SDA and SCL must be applied with a maximum frequency of 1MHz.

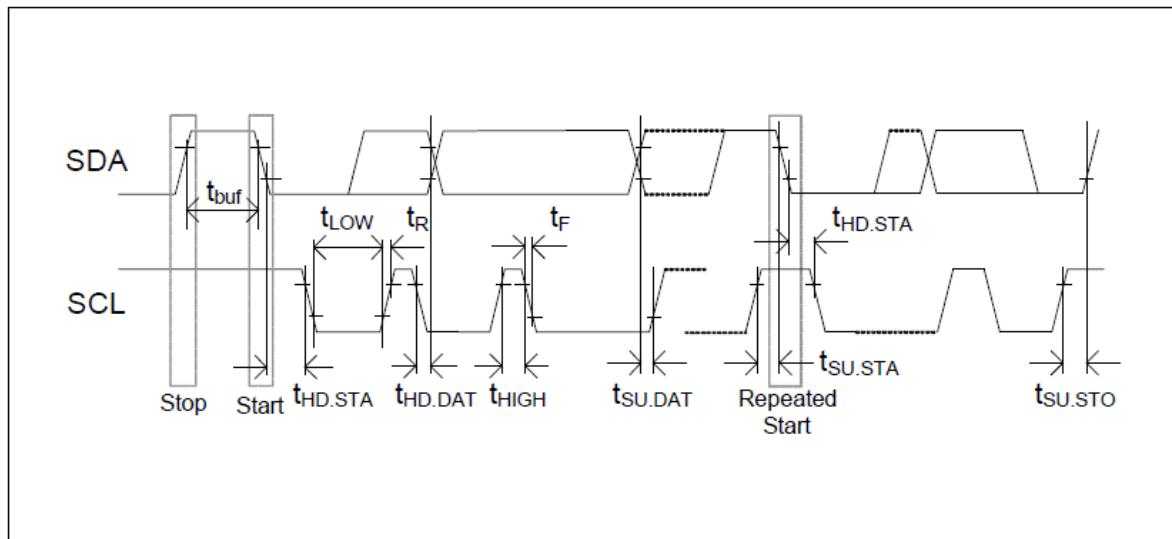
2.2 Deactivate Communication Interface

For changing into functional mode, the **pass2funct command** has to be executed.

The pass2funct command writes the value of 0x53 (01010011 bin) in the register PASS2FUNCT with address 0xf1.

Almost after the **acknowledge + 65 µs**, the sensor is already in functional mode.

2.2.1 Timing

Figure 4:
TimingFigure 5 :
I²C Timing

Symbol	Parameter	Min	Max	Unit
f _{SCLK}	SCL clock frequency		1.0	MHz
t _{BUF}	Bus free time (time between the STOP and START conditions)	0.5		μs
t _{HD,STA}	Hold time; (Repeated) START condition ⁽¹⁾	0.26		μs
t _{LOW}	Low phase of SCL clock	0.5		μs
t _{HIGH}	High phase of SCL clock	0.26		μs
t _{SU,STA}	Setup time for repeated START condition	0.26		μs
t _{HD,DAT}	Data hold time ⁽²⁾		0.45	μs
t _{SU,DAT}	Data setup time ⁽³⁾	50		ns
t _R	Rise time of SDA and SCL signals		120	ns
t _F	Fall time of SDA and SCL signals	10	120 ⁽⁴⁾	ns
t _{SU,STO}	Setup time for STOP condition	0.26		μs

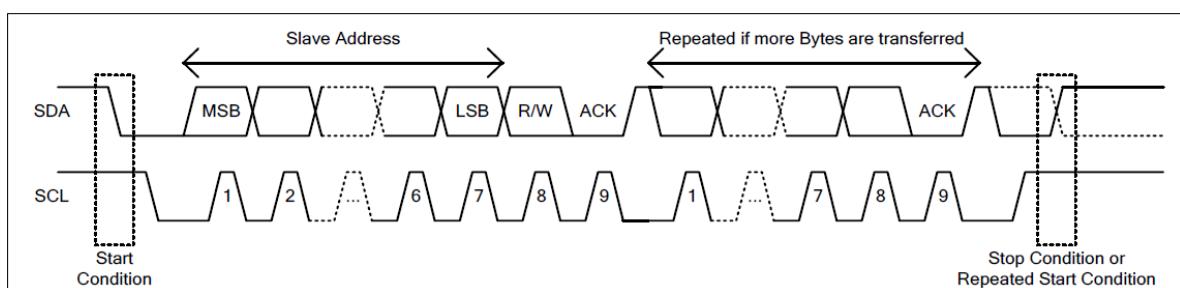
(1) After this time, the first clock is generated.

(2) A device must internally provide a minimum hold time of 120 ns (Fast-mode Plus) for the SDA signal (referred to the $V_{IH\min}$ of SCL).to bridge the undefined region of the falling edge of SCL.

- (3) A Fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}=250$ ns must be met. This is automatically done if the device does not stretch the low phase of SCL. If such a device does stretch the low phase of SCL, it must drive the next data bit on SDA ($t_{Rmax} + t_{SU:DAT}=1000+250=1250$ ns) before SCL is released.
- (4) In the Fast-mode plus, fall time is specified the same for both output stage and bus timings. If series resistors are used, this has to be considered for bus timing.

2.3 I²C Communication

Figure 6 :
I²C Communication



2.3.1 Data Transmission

The state of the data line represents valid data when, after START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

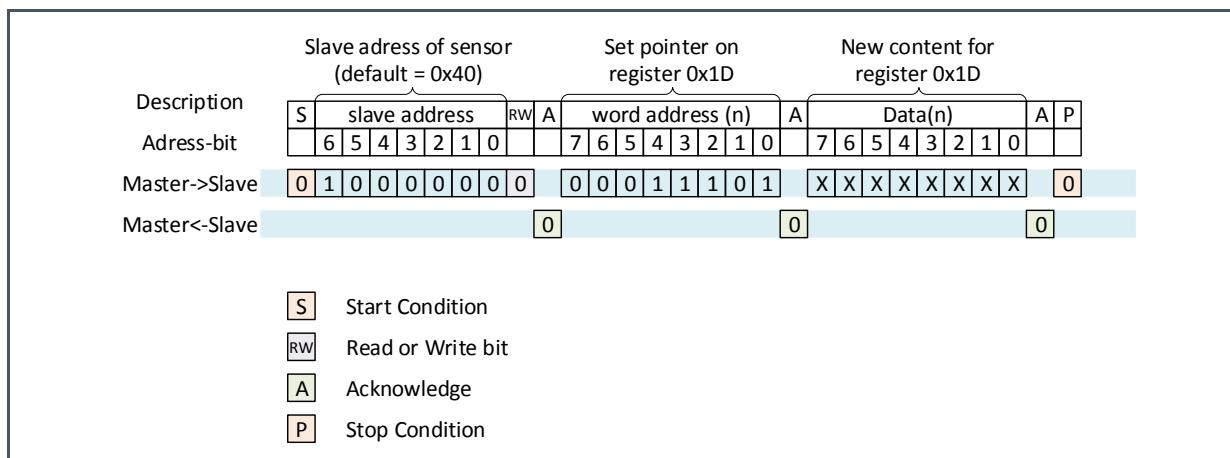
2.3.2 Acknowledge

The receiving device is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

2.3.3 Write

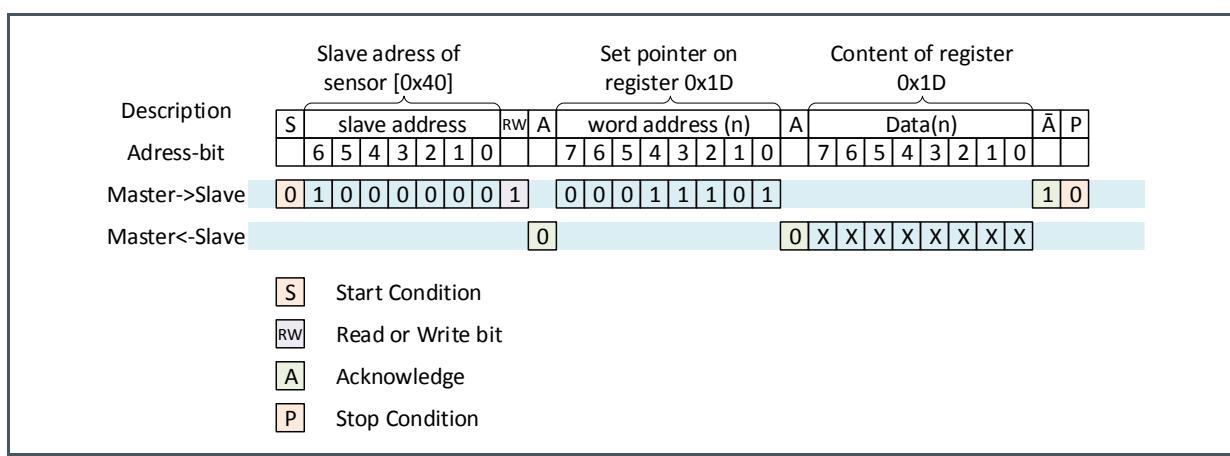
Figure 7 :
Write Data



In case of a write action (RW bit is 0) the master sends data packages (new content of sensor registers). The slave sends an Acknowledge after each data package. The communication ends when the master set the Stop Condition.

2.3.4 Read

Figure 8 :
Read Data



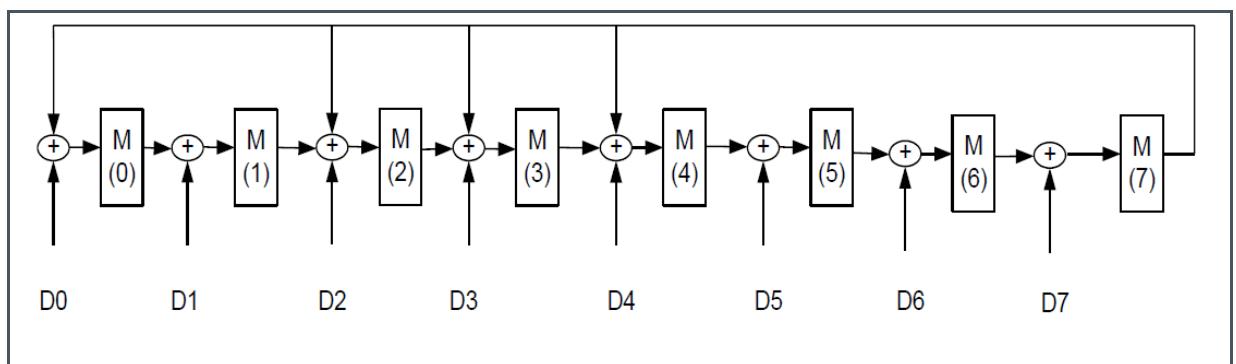
In case of a read action (RW bit is 1) the master receive data packages (actual content of sensor registers). The master sends an Acknowledge after each data package. The communication ends when the master sends an inverted acknowledge and set the Stop Condition.

2.4 Customer Signature Calculation

Before Burn procedure, the cust_signature has to be calculated and stored in the P2RAM_BYT_16 (0x1F) register.

The signature is used for a diagnostic check during power up by BIST module (Built-In-Self-Test). The stored signature will be compared IC internally to a calculated value during powering up. The signature calculation is characterized by following polynomial: $P(X)=1+X^2+X^3+X^4+X^8$ (29 dec)

Figure 9:
Signature CRC-8 Calculation



Customer registers: P2RAM_BYT_13 (0x1C), P2RAM_BYT_14 (0x1D) and P2RAM_BYT_15 (0x1E)

Code Example:

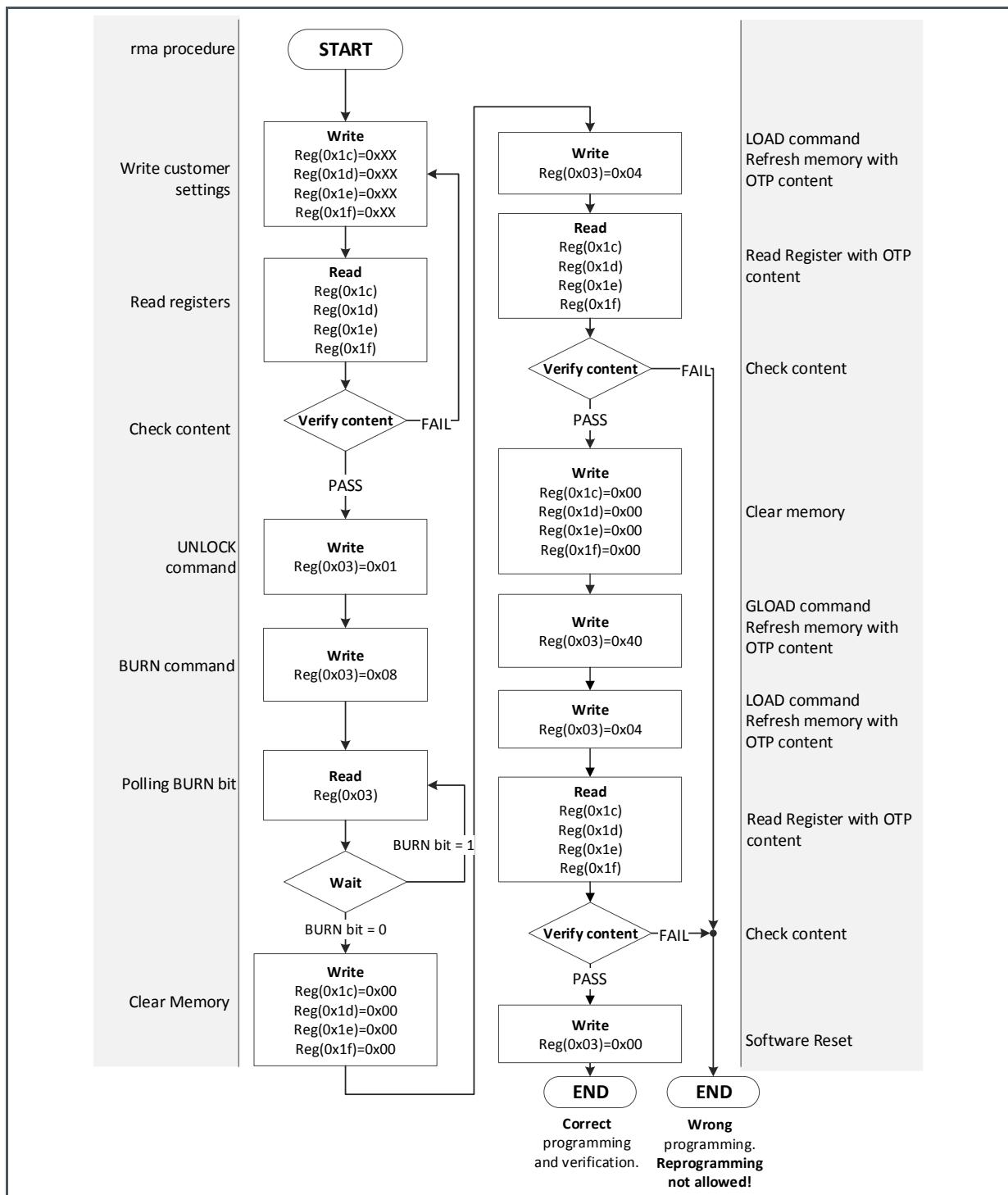
```
@content =($byte0, $byte1, $byte2, $byte3, $byte4, $byte5, $byte6, $byte7, $byte8, $byte9, $byte10, $byte11, $byte12, $byte13, $byte14, $byte15);

$misr = 0;
for($i=12; $i< 15; $i++) {
$misr_shift = ($misr<<1);
$misr_xor = ($misr_shift ^ $content[$i]) & 0xFF;
$misr_msb = $misr/(128);
if ($misr_msb eq 0) {
$misr = $misr_xor;
}
else
{
$misr = ($misr_xor ^ 29) & 0xFF;
}
```

2.5 Burn Procedure

After the customer OTP section is burned (finally and irreversible programmed), the AS5715R is fully locked! Thus, no execution of the customer rma procedure is possible anymore!

Figure 10 :
Programming Flow



3 Revision Information

Changes from previous version to current revision v1-00	Page
Initial version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

4 Legal Information

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