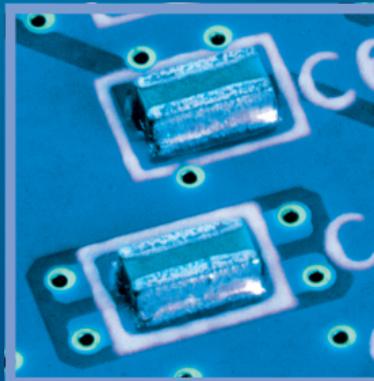
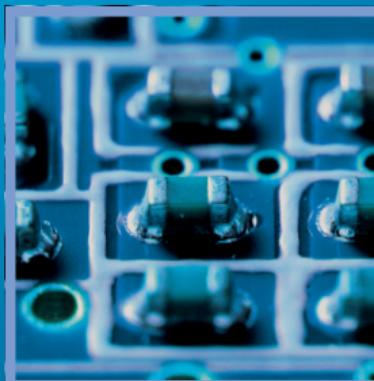
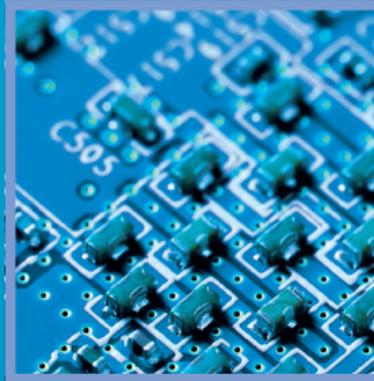
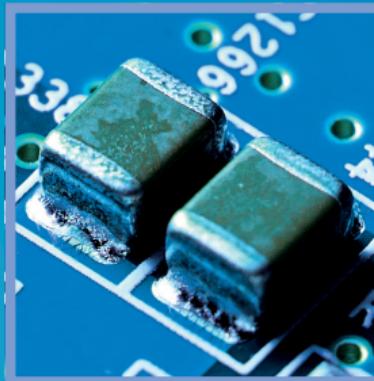


NE Handbook series 2013

# Capacitors Q&A



**N**  
**E**

Originally published by Nikkei Electronics

# Your First Web stop for capacitors

The screenshot shows the Murata website with several highlighted sections:

- Search Tools:** Multi-functional, powerful search tools for finding the most suitable product for design needs.
- Search Capacitors:** Options for search by features, lineups, specifications, or cross-reference.
- Examples of Problem Solving:** Examples of replacements, cost reductions, and noise countermeasures.
- Design Tools:** Software tools like SimSurfing (WEB) and S parameter.
- FAQ:** Quick reference to the most commonly asked questions on capacitors.
- Solutions Showcase:** Videos and articles presenting useful know-how to solving problems related to capacitors.
- Design tools:** Online software downloadable for smarter designs (Netlist, SPICE model, S parameter).

For more information

<http://www.murata.com/products/capacitor/>

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Originally published by Nikkei Electronics

## Full Support for the Entire Commercialization Process Maximizing Added Value of Capacitors

Murata Manufacturing Co., Ltd. is a leading supplier of monolithic ceramic capacitors. The firm's capacitor business is distinguished by its strong technical support, maximizing the added value of capacitors and thereby strengthening product competitiveness for the user.

Murata Manufacturing provides a wide spectrum of electronic components such as noise suppression elements, inductors, oscillators, filters, high-frequency components and modules, sensors, and power supply devices. Capacitors serve as a major pillar for the company's wide range of businesses, which include monolithic ceramic capacitors, polymer capacitors, and electrical double-layer capacitors. Murata's flagship product, the monolithic ceramic capacitor, is firmly recognized within the industry as a global leader in market and technology.

Murata stays ahead of the market with its technology ensuring continued miniaturization and larger capacity for the monolithic ceramic capacitor. Preferences for thinner, miniaturized, and multifunctional electronic devices in recent years have spurred interest in the advantageously small monolithic ceramic capacitor. At the same time, the product's high capacity makes it a suitable replacement for tantalum and aluminum electrolytic capacitors.

Murata's technical strengths continue to expand. In

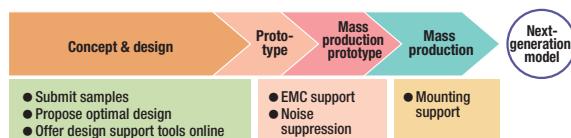


Figure 1. From concept and design to production, Murata delivers comprehensive support.

September 2012, the company announced development of the world's smallest monolithic ceramic capacitor. Its dimensions are only 0.25mm × 0.125mm. Its volume is approximately 25% of that of 01005 size (0.4mm × 0.2mm) typically used in the latest smartphones and other gadgets.

Murata's superior technology serves its robust range of monolithic ceramic capacitors, from general-purpose products covering many specifications to optimized application-specific products. The lineup includes automotive capacitors with enhanced reliability, integrating short-circuit protection and embedded mechanisms to alleviate component stress caused by board contraction and expansion. Murata also produces low equivalent series inductance (ESL) capacitors such as multi-terminal capacitors and LW-inverted (length and width) monolithic ceramic capacitors, and Hi-Q capacitors for high-frequency circuits.

### Expanding seamless support

Murata supplements this rich lineup of monolithic ceramic capacitors with equally committed technology and user support (Figure 1), providing full reinforcement throughout the entire product development process, from concept and design to prototype, production prototype, and production. Of course, technical support for users is not rare among electronic component manufacturers. Yet few become involved from the concept and design stage—normally the user's domain. Murata goes the distance, providing a variety of services to create seamless support all the way through production.

Murata recognized the vital need for full user support a few years ago. Prior to that, the company conscientiously provided technical backup according to users' development phases. However, with accelerated technical advances and emerging global markets, users increasingly face problems with effective use of capacitors as a fundamental electronic

device. Two facts further exacerbate this. First, circuitry handling high-speed digital signals operating at a few GHz—previously exclusive to personal computers—is now embedded into other electronic products. Secondly, devices embedding wireless communication systems using radio frequency (RF) circuits requiring experience and know-how are increasingly in demand. Murata realizes the importance of providing seamless support throughout the production process, enabling users to maximize Murata product merits in today's complex environment for efficient product development.

### **Murata delivers proactive know-how**

Murata continues expanding the full support upon which its services are premised. The company's website offers tools and information carrying the user through concept, design, and prototype stages: component characteristics, SPICE model and S parameters for simulations, and design support tools to enhance efficiency. In addition, Murata proposes alternate components and design improvements reducing cost, footprint, and number of parts. Finally, the company offers design services for printed circuit board areas demanding exceptional experience and technical expertise—specifically for the intricate layout in the capacitor areas integrating power supply lines for high-speed digital circuits and high-frequency analog signal circuits.

Murata's professional engineers offer developers solutions to inevitable electromagnetic compatibility (EMC) issues in the prototype and mass production stages. This is where Murata leverages its state-of-the-art equipment (**Figure 2**). The company boasts three electromagnetic anechoic chambers in Japan—in Yokohama, Kyoto, and Fukui—essential in evaluating and testing electromagnetic noise. Murata also established an electromagnetic anechoic chamber facility, called the Murata EMC-LAB, in Shanghai, China, and installed EMI noise measurement equipment in



Figure 2. The Murata EMC-LAB, an electromagnetic anechoic chamber facility, in Shanghai, China (left), and a magnetic near-field distribution measurement instrument installed at the Beijing Branch (right)

Shenzhen, Shanghai, and Beijing centers for EMC technical support. Murata stands ready to counter a variety of unexpected issues, such as noise with monolithic ceramic capacitors, which arise during production.

The company is currently reinforcing its support for mounting methods implemented in the prototype and mass production stages. In addition to problem solving for mounting issues, Murata offers ideas such as half-pitch taping packaging for lower environmental impact, new packaging for easy handling of ultra-small parts, and ideas for bulk mounting.

Electronic device design is becoming progressively more difficult as rising demand for mobile devices necessitates increasingly thin and miniaturized multi-function devices. At the same time, accelerated market changes emphasize the need for progressively efficient designs. As device manufacturers endeavor to produce highly competitive products in this challenging environment, Murata Manufacturing steps forward as a strong partner with full technical support solutions.



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<https://www.murata.co.jp/contact/product/contact.php>

## [Selecting Components]

## When Switching from a Tantalum Electrolytic Capacitor to a Monolithic Ceramic Capacitor

**Q** What cautions should one observe when switching from a tantalum electrolytic capacitor to a monolithic ceramic capacitor?

**A** Recently, there is an increasing trend to switch from tantalum electrolytic capacitors to monolithic ceramic capacitors. There are two driving factors behind this.

The first factor is the issue of reliability. Failure in the short circuit mode can cause the tantalum electrolytic capacitor to emit smoke or ignite. In fact, smoke or fire will cause fatal failure in the host electronic device.

The second factor is the procurement of tantalum. Tantalum is known as a rare metal and is produced in few areas of the world. When issues such as political instability arise in the countries producing tantalum, prices may spike and supply may waver. Use of rare metals inevitably subjects those choosing tantalum electrolytic capacitors to the above-mentioned risks.

Switching to a monolithic ceramic capacitor solves such problems. These capacitors are much less likely than their tantalum electrolytic counterparts to generate smoke or fire. Raw material prices and supply remain stable as rare metals are not required. And further incentives await.

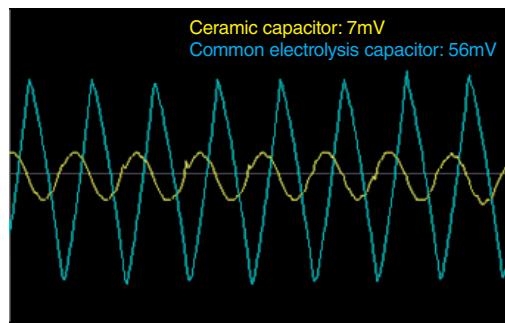
In general, there are two major benefits. One is the reduction of the mounting area as monolithic ceramic capacitors provide larger capacitance per volume. The second is the reduction in output ripple voltage when

a monolithic ceramic capacitor is used with an output smoothing circuit such as a DC-DC converter, owing to the low equivalent series resistance (ESR) of the monolithic ceramic capacitor. As shown in the example in **Figure 1**, the output ripple voltage of 56mV when using a tantalum electrolytic capacitor is reduced to 7mV with the monolithic ceramic capacitor.

### ■ Pointers for output smoothing applications

Note that replacement of the tantalum electrolytic capacitor with the monolithic ceramic capacitor is not a simple trade — the user must heed various cautions based on the type of application.

This typical example uses a DC-DC converter or similar output smoothing circuit. Although this highlights the benefit of suppressed output ripple voltage due to a low ESR, the low ESR characteristic can also be a double-edged



**Figure 1 Use of monolithic ceramic capacitor to suppress ripple**

The output voltage waveform when a DC-DC converter output capacitor is switched from a tantalum electrolytic capacitor to a monolithic ceramic capacitor. DC-DC converter switching frequency is 300MHz; tantalum electrolytic capacitor volume is 100 $\mu$ F. Three 22 $\mu$ F monolithic ceramic capacitors are used here. Ripple voltage is 56mV before the replacement, suppressed to 7mV after introduction of the monolithic ceramic capacitor.

sword in cases where it causes extreme rotation of the DC-DC converter's feedback loop response characteristic phase. In the worst-case scenario, the phase rotates 180 degrees, and the DC-DC converter output shows abnormal oscillation. In this case, the DC-DC converter cannot perform its role.

When the monolithic ceramic capacitor is used with the output smoothing circuit, abnormal oscillation can be suppressed by tuning the constant of the phase compensation portion. If the phase compensation circuits are integrated into the DC-DC converter IC, the user must measure the ESR of the tantalum capacitor to be replaced and introduce the equivalence in resistors in series to prevent abnormal oscillation.

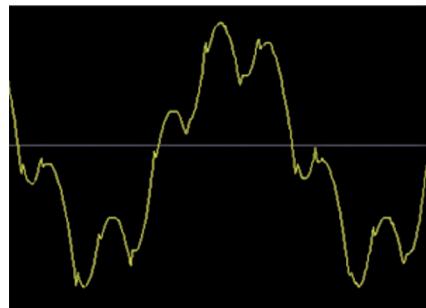
**Figure 2** provides an actual example. Figure 2(a) shows the output voltage waveform when a monolithic ceramic capacitor has replaced the tantalum electrolytic capacitor as the component in the output smoothing circuit for the DC-DC converter. Abnormal oscillation is occurring and the DC-DC converter output voltage fluctuates greatly.

Figure 2(b) shows results after tuning the constant of the phase compensation circuits for the feedback loop. Oscillation is normal and output voltage has been lowered to an acceptable level. This rectified waveform is quite suitable for actual use.

In general, a 45-degree or more phase margin is optimal for the feedback loop response characteristic of the DC-DC converter. The constant of the phase compensation circuits must be adjusted to meet this condition.

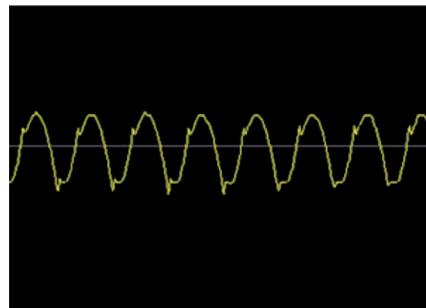
However, due to DC-DC converter IC innovations, we are now seeing an increase in products that do not generate abnormal oscillation even when using low-ESR monolithic ceramic capacitors. Carefully check the data sheet when selecting a DC-DC converter IC for a new development

(a) Before tuning



Tune the constant of phase compensation circuits.

(b) After tuning



**Figure 2 Output voltage waveform for abnormal and normal oscillation**

(a) shows output voltage waveform for abnormal oscillation and (b) shows that of normal oscillation. Abnormal oscillation is suppressed by tuning the constant of the phase compensation circuits for the feedback loop.

project; look for confirmation that the IC will operate smoothly even with use of monolithic ceramic capacitors. If there is no reference to monolithic ceramic capacitors on the data sheet, implement the previously mentioned measures.

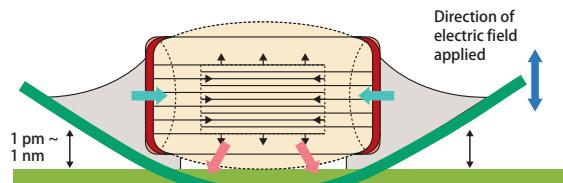
### [Selecting Components]

## Effective Suppression of Audible Noise with Low-permittivity Materials

**Q** What causes a monolithic ceramic capacitor to generate audible noise during power distribution and how can it be avoided?

**A** A slight beep is often heard when operating a notebook PC or smartphone. One cause may be noise generated from the capacitor, known as squealing.

This noise is due to electrostriction, a phenomenon generated by the ferroelectric ceramic used as a raw material in monolithic ceramic capacitors. A mechanical distortion occurs in the shape of the material when voltage is applied. Therefore, when ripple voltage (AC voltage) is applied to the capacitor, the capacitor itself stretches and contracts (Figure 1). This stretching and contracting is transmitted to the printed circuit board (PCB), causing it



**Figure 1 PCB vibration due to electrostriction**

A monolithic ceramic capacitor expands and contracts due to applied alternate current. When the capacitor is mounted on a PCB, this movement causes vibration of the PCB. Although the vibration amplitude is only 1pm to 1nm, if the oscillation frequency is within the audible frequency range (20Hz to 20kHz), it creates sound recognizable by the human ear.

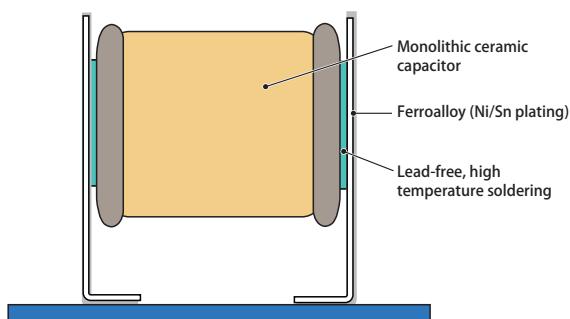
to vibrate. Although the amplitude of the PCB is only 1pm to 1nm, if the oscillation frequency is within the human audio-frequency range (20Hz to 20kHz), it creates an audible sound. The PCB literally functions as a speaker.

The problem of capacitor-induced squealing frequently occurs in notebook PCs and is increasingly common in smartphones as well. This is caused by the 200Hz frequency characterizing the switching function from LTE mode to 3G mode, a frequency audible to the human ear.

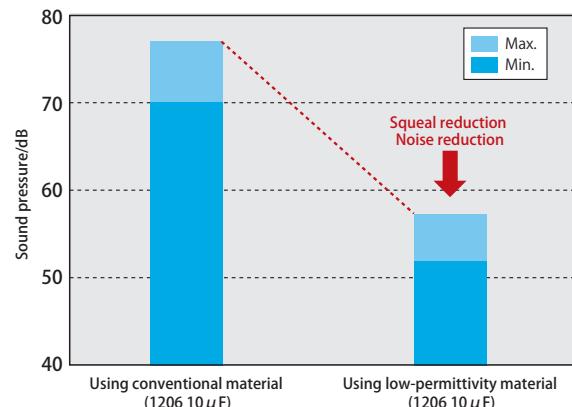
### ■ Changing capacitor types

Capacitor-generated squealing is an unpleasant phenomenon for the user, and cannot be left unchecked. There are various solutions available.

Re-designing of the PCB is one possible solution. However, this problem usually surfaces in the manufacturing phase. Implementing design changes at this point would increase costs and lead time, rendering this option impractical. At the same time, it is difficult to predict the revelation of this problem at the initial design stage. This is because many parameters can lead to this problem —



**Figure 2 Monolithic ceramic capacitor with metal terminals**  
Significantly suppresses vibration transmission to the circuit board when using metal terminals.



**Figure 3 Effect of low-permittivity Materials**

Comparison between measured squealing levels of a monolithic ceramic capacitor using conventional material and one using Low-permittivity material. Sound pressure can be reduced by some 20dB.

placement of the capacitor, board dimensions, thickness and number of layers, to name a few.

The best solution is changing the type of capacitor. There are two choices available. The first is a capacitor with metal terminals (Figure 2). The elasticity of these metal terminals absorbs the movement of the capacitor, effectively preventing the vibration from reaching the board and significantly suppressing capacitor squealing.

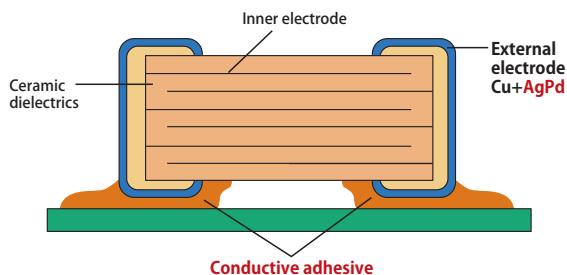
The other option is to switch to capacitors that use low-permittivity materials. Low permittivity lessens electrostrictive effects on the PCB, keeping the sound pressure to around 20dB (Figure 3). At this level, the squealing will be nearly inaudible to the human ear. Capacitors featuring metal terminals are not suitable for applications requiring miniaturized components. The recommended solution for suppressing squealing in smartphones is the switch to capacitors that employ low-permittivity materials.

### [Selecting Components]

## Conductive Adhesive Mounting for Capacitors with AgPd Electrodes in High-temperature Environments

**Q** When using conductive adhesive to mount monolithic ceramic capacitors at high temperatures, the adhesive corrodes and flakes off. What is the cause of this and is there a solution?

**A** Conductive adhesive is often used to mount monolithic ceramic capacitors on circuits used in extremely high-temperature environments, such as in engine control units (ECU) for vehicle engines and in various circuits used in sensors. These applications are often required to perform in environments with temperatures reaching over 150°C. Conventional soldering materials do not provide enough adhesive strength for mountings to withstand such severe conditions.



**Figure 1** Terminals featuring external electrodes made of AgPd

Terminal structure featuring external electrodes made of AgPd. Excellent component adhesion is achieved in high-temperature environments even when mounted with conductive adhesive.

Conductive adhesive is extremely heat-resistant and should provide highly reliable adhesion even in high-temperature environments. One must be careful, however, when mounting conventional monolithic ceramic capacitors with conductive adhesive. As the question indicates, using conductive adhesive to mount monolithic ceramic capacitors at high temperatures can cause the adhesive to corrode and flake off.

The fault lies in the capacitor's electrode structure. The conductive adhesive contains Ag filler in the epoxy resin, whereas the average electrode is plated with copper (Cu), nickel (Ni), and tin (Sn), respectively.

In the mounting process, the PCB is coated with conductive adhesive, the capacitor is placed on the board, and the adhesive is thermally cured, anchoring the capacitor. At this time, a difference in electrical potential is generated at the point of contact between Sn and Ag. As time elapses, the electric potential corrodes, causing the adhesive to oxidize and weaken. Durability tests in an environment reaching over 150°C demonstrate that the adhesive corrodes and does, indeed, flake off.

The problem can be solved by switching to a monolithic ceramic capacitor with an electrode structure featuring a coating of silver and palladium (AgPd) over the copper layer.

The AgPd layer resolves the issue by creating contact between the layer of Ag on the electrode and the Ag in the adhesive, preventing corrosion of the electrical potential. The added Pd prevents the Ag surface from oxidizing. The overall result is minimal weakening of the capacitor attachment created with the conductive adhesive. This solution enables the capacitor to be incorporated in applications used in high-temperature environments with no concerns about corrosion and loss of adhesiveness.

### [Selecting Components]

## Select Size 1206 or Smaller for Optimal, High-temperature Metallic Substrate Mountings

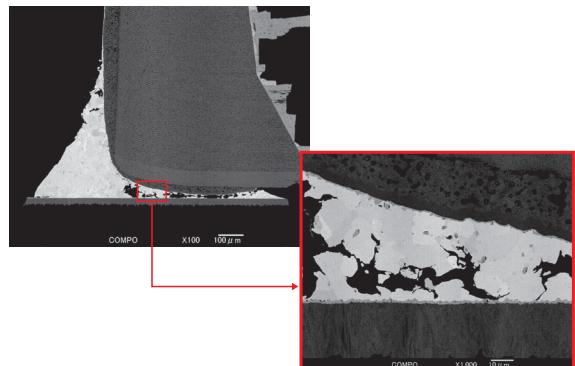
**Q** Why do cracks form in the solder used to mount monolithic ceramic capacitors on the metallic substrate of power supply modules?

**A** Metal substrates boast superior heat dissipation and vibration resistance characteristics, making them the perfect alternative to resin-based printed boards for use in automotive electronic control units (ECU), an environment characterized by extreme heat and vibration, as well as in applications requiring substantial electric power, such as air conditioner inverters and power supply modules.

Although the metal substrate offers users many merits, it also presents a significant demerit for the monolithic ceramic capacitor. When a metal substrate is mounted on a monolithic ceramic capacitor, the linear coefficient of expansion between the two differs significantly. As the capacitor is exposed to hot and cold heat cycles, the substrate expands and contracts, generating stress between itself and the capacitor, with functional stress accumulating at the point of contact. In the worst-case scenario, cracks form on the solder between both components (Figure 1).

### Avoid using a large capacitor

There are basically two ways to solve this problem. The first method is switching to a capacitor with metal terminals. The metal terminal absorbs the functional



**Figure 1 Example of cracked solder**

Propagation of cracks visible along the grain boundary of Sn (Tin) in solder. Shrinkage due to temperature fluctuation causes functional stress and cracking in the soldered area between the metal substrate and the monolithic ceramic capacitor having different coefficients of thermal expansion (CTE).

stress generated by the difference in the linear coefficient of expansion between the monolithic ceramic capacitor and the metal substrate, preventing cracks from forming in the solder.

The second method is to use a monolithic ceramic capacitor with smaller external dimensions, preferably a 1206 size (3.2mm × 1.6mm × 1.6mm) or even smaller.

A smaller capacitor provides a work-around as it presents less displacement when the substrate expands and contracts. In general, the amount of displacement generated due to expansion or contraction is calculated as follows: linear coefficient of (expansion) × (temperature) (difference) × (component length). Accordingly, the larger the component, the greater the displacement due to expansion or contraction related to temperature changes, and the higher the likelihood of solder cracks. In other words, the smaller the component, the smaller the displacement and the lower the tendency to crack.

## [Characteristics]

# Decreasing Terminal Voltage Demands Dielectric Absorption Countermeasures

**Q** The terminal voltage drops over time when using monolithic ceramic capacitors as DC-cut capacitors in microphone input circuits, eventually interfering with circuit function. Is this caused by capacitor insulation failure?

**A** Handheld devices, such as smartphones and tablets, digital still cameras, and e-book readers, face strong demand for both smaller size and higher performance. As a result, printed circuit boards (PCBs) are growing progressively smaller and thinner, continuously pushing the envelope in high-density packaging.

Applications using relatively large aluminum electrolytic and film capacitors are steadily shifting to thinner, more compact monolithic ceramic capacitors. Terminal voltage drop is a problem often encountered during this transition.

## ■ The capacitor is not the problem

The problem of dropping terminal voltage occurs when a charged monolithic ceramic capacitor is connected to a high-impedance circuit, or when the circuit is left open. The culprit is not poor capacitor insulation, but rather dielectric absorption.

This phenomenon is particularly noticeable in ferroelectric material. In general, when voltage is applied to the capacitor, polarization occurs in the dielectric material and the charge is stored. However, there is more

than one type of polarization at work here. Atomic and electronic polarization stabilize very quickly, but orientation and space-charge polarization require more time.

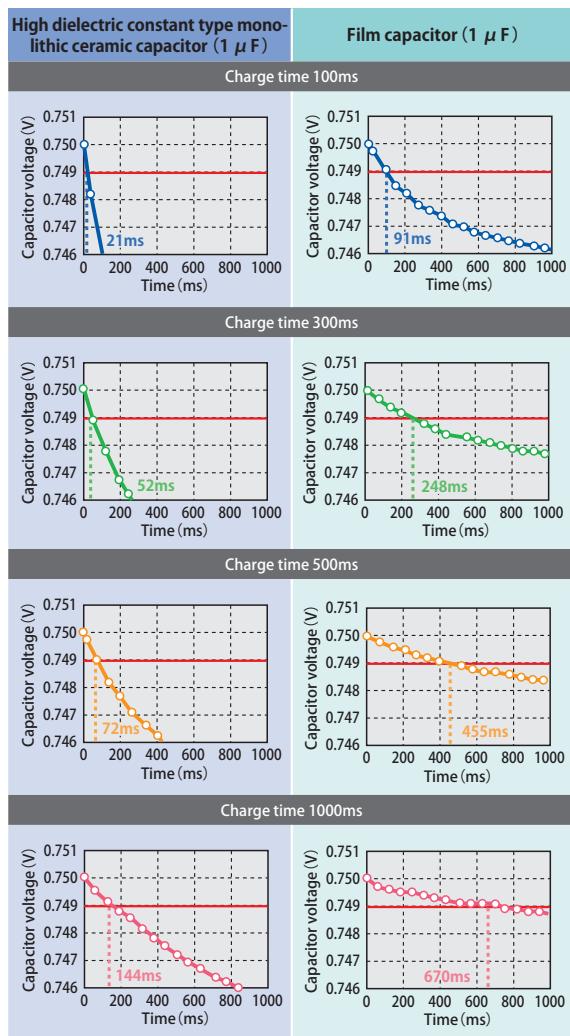
Barium titanate, a ferroelectric material, is a key material in monolithic ceramic capacitors with high dielectric constants (B/F characteristics). The charge is accumulated in the capacitor after all of the above-mentioned polarizations have occurred. When voltage is applied, the atomic and electronic polarizations complete first, and if the voltage is continued the more time-consuming polarizations occur, storing more charge.

The problem occurs after this capacitor is charged briefly and then connected to a high-impedance circuit, or when the circuit is left open. Time-consuming polarization is still under way in the capacitor in this situation, and the electrical charge moves from the faster polarization site to the slower one, causing voltage drop in terminal voltage. This phenomenon is known as dielectric absorption.

## ■ Integrating dielectric absorption into circuit design

The problem is not limited to only monolithic ceramic capacitors with high dielectric constants; film capacitors, which use paraelectric material, are also affected by the dielectric absorption phenomenon, but to a different degree. The voltage drop in monolithic ceramic capacitors is relatively large, but quite small in film capacitors. In addition, there is almost no voltage drop in temperature-compensating monolithic ceramic capacitors (e.g., CH characteristic) that use paraelectrics such as titanium oxide or calcium zirconate.

So just how large is this difference? **Figure 1** shows the actual experimental voltage drop. In the experiment, the capacitor was charged to a terminal voltage of 0.750V,



**Figure 1 Comparison of voltage drop over time**

A comparison of voltage drop times for a monolithic ceramic capacitor ( $1\mu\text{F}$ ) and a film capacitor ( $1\mu\text{F}$ ). The capacitors are charged until the terminal voltage reaches  $0.750\text{V}$ , then connected to a high-impedance circuit, and voltage drop measured over time (drop from  $0.750\text{V}$  to  $0.749\text{V}$ ).

then connected to a high-impedance circuit. Voltage drop time was defined as the time required for the voltage to drop to  $0.749\text{V}$ . The voltage drop time for a film capacitor charged for  $100\text{ms}$  is  $91\text{ms}$ , but only  $21\text{ms}$  for a high-dielectric constant monolithic ceramic capacitor. When the charge time was increased to  $1000\text{ms}$ , drop time increased to  $670\text{ms}$  for the former and  $144\text{ms}$  for the latter.

This experiment illustrates that the voltage drop time for high-dielectric constant monolithic ceramic capacitors is extremely short. Although the dielectric absorption effect cannot be eliminated, increasing the charge time will minimize the effect of voltage drop time.

The only way to avoid problems due to voltage drop is to take the phenomenon into account in circuit design. The usual approach is to slightly increase the capacitor charge voltage, which is usually accomplished by referencing threshold voltage to terminal voltage after sufficient time has elapsed, and not in the initial state. Another method is to increase the charging time.

In any case, when using a high-dielectric constant monolithic ceramic capacitor, be sure to take voltage drop due to dielectric absorption into consideration in circuit design.

## [Mounting]

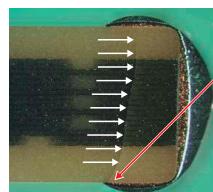
## Effective Underfill Prevents Damage to Capacitor Due to Drop Impact

**Q** In cellular phone drop tests, cracks form in the PCB-mounted monolithic ceramic capacitors. Time constraints prevent the pursuit of fundamental changes to PCB layout or to parts themselves. Is there a simple solution to this problem?

**A** Users inadvertently drop their cell phone or smartphone. This is an inevitable occurrence. A user-friendly design would protect the device from severe damage due to shock impact. A certain extent of impact-resistance is essential, and this is what any developer strives to achieve.

Most cellular phone manufacturers perform drop tests to measure handset durability before going to market. This test involves dropping the phones from a set height to check for dislodged parts and abnormal circuit behavior. In the question posed above, the monolithic ceramic capacitor incurred cracks in the drop test.

The impact of the cell phone hitting the floor may externally damage the handset body as well as cause vibration



Crack erupts from end of electrode terminal at the mounting point

**Figure 1** Cracks generated in a monolithic ceramic capacitor during a drop test (cross-section photo)

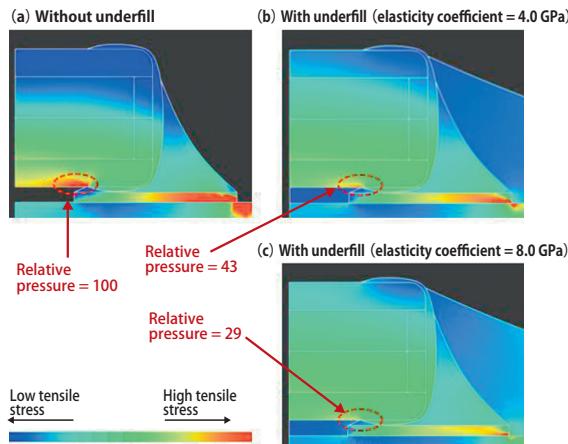
and distortion of the PCB. This vibration and distortion generates significant mechanical stress for the monolithic ceramic capacitor soldered to the PCB. If the capacitor cannot withstand the stress, it may become dislodged from the solder, creating cracks (Figure 1). As a result, circuit failure occurs.

### ■ Quick, low-cost solution

In recent years, the product cycle of cellular phone handsets has shortened significantly, reducing the development period for new models. Little time is left for resolving problems detected in the post-design drop test. Revising layout or parts would require redesigning the product, an impractical solution at this stage.

This is where the effective underfill comes into play. Underfill is a resin material added to semiconductor chips (IC) sealed in packages like the chip scale package (CSP) or ball grid array (BGA). The underfill mitigates mechanical stress caused by heat cycles, drop impact, bending, and other problems. Plugging the gap between the IC and the PCB with underfill can greatly reduce mechanical stress on the IC due to these various issues. Epoxy resin is commonly used for this purpose. First, the resin is applied to the board surface where the component will be mounted; the component is placed on top of the resin, plugging the gap between the PCB and the component.

This underfill can also be used to mount the monolithic



**Figure 2 Effects of underfill**

This figure shows the results of finite element method (FEM) analysis of underfill effectiveness. Photo (a) shows a capacitor with no underfill. Significant stress is applied to the electrode terminal tip on the mounting surface. Photo (b) shows stress of 100 applied to a board coated with an underfill of 4.0GPa (elasticity coefficient); the relative pressure is reduced to 43. In photo (c), a board coated with an underfill of 8.0GPa shows the relative pressure reduced to 29.

ceramic capacitor. **Figure 2** shows analysis of an impact test confirming the effect of underfill applied to monolithic ceramic capacitors mounted on a PCB.

The effect of underfill is tremendous. Electrode terminal tips must withstand a maximum stress of 100 (relative value) when underfill is not applied to the PCB surface. Applying an underfill of 4.0GPa (elasticity coefficient) reduces this by roughly half, to 43 (relative value). With an underfill of 8.0GPa (elastic coefficient), the result falls to 29 (relative value), less than one-third the maximum stress.

Underfill is relatively inexpensive, and can be applied to PCB mounting positions for monolithic ceramic capacitors and CSP/BGA ICs at the same time. It represents a low-cost, quick solution providing superior results.

## [Mounting]

# Heat Damage Caused during Hand Soldering

**Q** Cracks often occur in monolithic ceramic capacitors after hand-soldered repairs. Is this caused by the hand-soldering? What is the solution?

**A** Electric device components are often removed and reattached at the manufacturing plants in what is called “repair” work — measures to fix initial failures or make final adjustments during manufacturing. In these cases, automatic reflow soldering cannot be used; hand-soldering is the only way to reattach the parts.

As the question hints, the cracks forming on the monolithic ceramic capacitor are most likely caused during hand-soldering. The fact is, this type of problem dramatically increased after the transition from conventional leaded eutectic solder to lead-free solder (Sn-3.0Ag-0.5Cu, etc.).

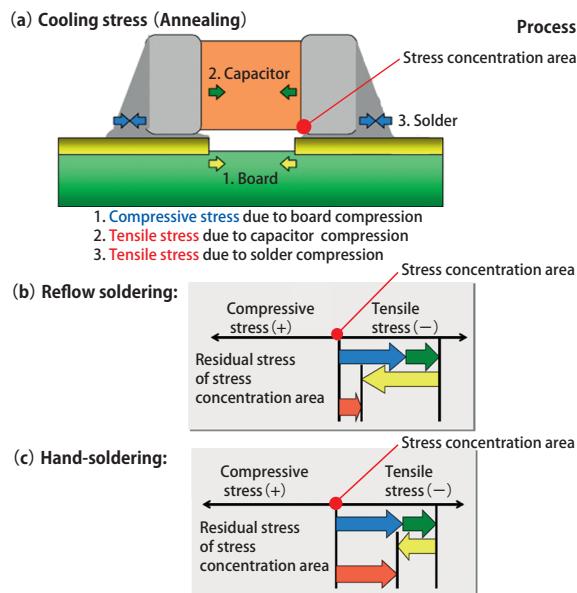
## ■ Problems accompanying transition to lead-free materials

What is causing such an increase in cracking issues? Two reasons stand out. One is the melting point of lead-free solder, which is 40°C higher than that of leaded eutectic solder. Such a high melting point requires the solder iron to be even hotter than for conventional materials, in order to melt the solder. If the tip of the iron happens to touch the monolithic ceramic capacitor during the soldering process, the capacitor will incur extensive thermal shock, greatly increasing the risk of damage.

The other reason is that lead-free solder is harder than leaded eutectic solder. A significant amount of mechanical

stress is applied to the PCB due to compression caused when the lead-free solder cools and hardens. This causes board distortion later in the manufacturing process, increasing the risk of cracks forming in the monolithic ceramic capacitor. In other words, lead-free solder reduces substrate bending resistance.

Let's take a closer look at these reasons. The concentration of stress on the monolithic ceramic capacitor mounted on the board culminates at the end of the electrode terminal on the board surface (Figure 1).



**Figure 1 Mechanism governing deterioration of substrate bending resistance**

(a) indicates the point where stress is generated during cooling. (b) shows the stress generated when mounting with reflow solder. As substrate contraction leading to compressive stress is great, residual stress lessens. (c) shows an example of hand-soldering. Compressive stress due to board compression is low, and residual stress is high.

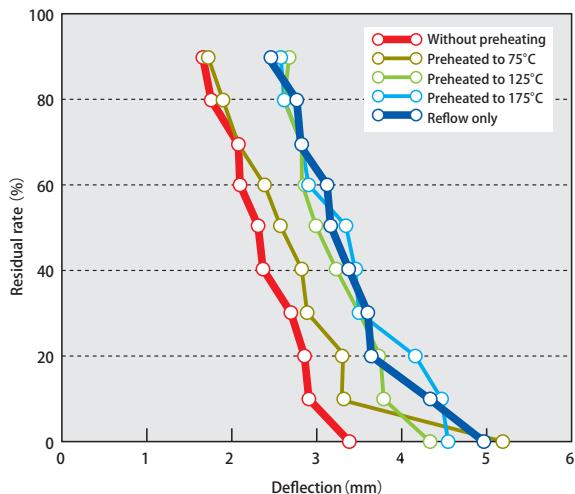
This point is the concentration of residual stress resulting from the compressive stress caused by the board contraction less the tensile stress caused by the capacitor and solder contractions. The residual stress can be sufficiently reduced by using automated reflow soldering equipment or the like and adequately preheating the solder material, which generates larger compressive stress due to board contraction. However, hand soldering when the board is not sufficiently preheated results in lower compressive stress due to board contraction, thus creating higher residual stress. As a result, when the board is distorted during the manufacturing process, the monolithic ceramic capacitor is more likely to crack with minor distortion.

#### ■ Preheating pointers

Observe the following two points to avoid problems when hand soldering. Firstly, perform soldering with extreme care to avoid contact between the capacitor and the solder iron tip. Secondly, sufficiently preheat the printed board before soldering.

The first point is rather easy to implement; it is the second point that poses a challenge. It is difficult to know how much preheating is necessary to avoid generating cracks. Figure 2 plots the relationship between preheating for hand soldering and the amount of board deflection that triggers cracks in the monolithic ceramic capacitor. When preheating to 175°C, the same level of substrate bending resistance can be achieved as when reflow soldering occurred. However, substrate bending resistance decreases significantly when preheating dips below 75°C, and drastically with no preheating (25°C).

Refer to the following for concrete preheating temperatures: Safety Application Guide for fixed ceramic capacitors for use in electronic equipment, published by



**Figure 2 Relationship between PCB preheating and substrate bending resistance**

The figure shows the relationship between the preheating temperature for hand soldering and the deflection amount of the board on which the cracked monolithic ceramic capacitor is mounted.

Japan Electronics and Information Technology Industries Association (JEITA). For example, when using 1206 size ( $3.2\text{mm} \times 1.6\text{mm}$ ) or smaller, the solder iron tip should be  $350^\circ\text{C}$  or lower, preheating temperature  $150^\circ\text{C}$  or higher, and thermal difference  $150^\circ\text{C}$  or lower. When using 1210 size ( $3.2\text{mm} \times 2.5\text{mm}$ ) or larger, the solder iron tip should be  $280^\circ\text{C}$  or lower, preheating temperature  $150^\circ\text{C}$  or higher, and thermal difference  $130^\circ\text{C}$  or lower.

A BC/300Ø soldering iron tip, providing higher heat capacity, is recommended over the smaller B/R0.5 type. Single-side boards should be preheated with a hot plate, double-sided boards with a spot heater. This ensures sufficient preheating of the board and helps suppress residual stress, avoiding the problem of cracks erupting in the monolithic ceramic capacitor.

### [Mounting]

## Taping Suggestions for 01005 High-Density Mounting

**Q** 01005-size ( $0.4\text{mm} \times 0.2\text{mm} \times 0.2\text{mm}$ ) monolithic ceramic capacitors offer smaller mounting footprints, but the parts are so small that mounting quality can deteriorate during production. What are the key points to consider?

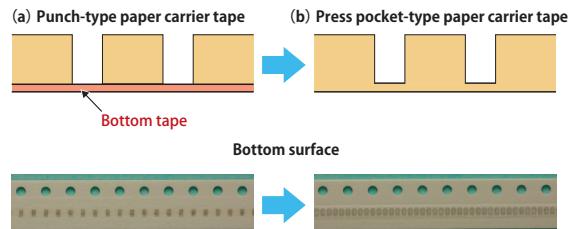
**A** Monolithic ceramic capacitors are growing steadily smaller, with 01005 packages already in use and even smaller designs ( $0.25\text{mm} \times 0.125\text{mm} \times 0.125\text{mm}$ ) on the verge of commercial adoption.

As parts shrink, mounting density and mounting process complexity increase. One major problem is detaching parts from the carrier tape (taping packaging) with surface mount equipment. Normally a suction nozzle is used to pick up the component, with the nozzle contacting the approximate center of the component's suction area. However, factors such as changes in pocket dimensions, or burrs or fluff on the tape, can cause nozzle misalignment. This makes it impossible to place the component accurately on the board. The component's position may also shift due to a static charge generated when the cover tape is removed, making it difficult to detach the component from the tape.

Consideration must be given to packaging specifications when using miniature parts such as 01005 capacitors. The downsizing of monolithic ceramic capacitors has progressed in parallel with packaging innovations. For example, punch-type paper carrier tape, with through-holes for components, is used with 0402 size ( $1.0\text{mm} \times 0.5\text{mm}$ ) products. Although the punched carrier tape

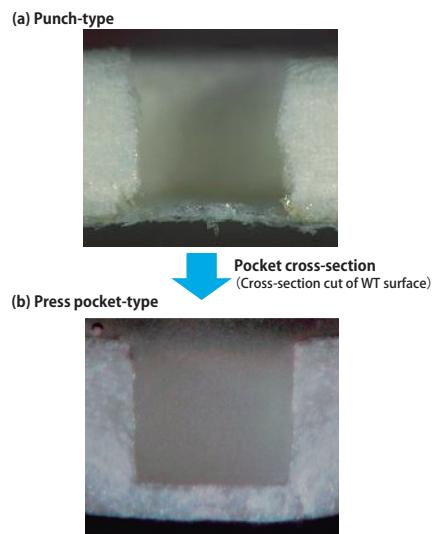
uses the bottom tape to secure components, the smaller the parts are, the harder it is to detach them from the adhesive tape. Bottom tape can also cause burrs and fluff.

Currently, most manufacturers recommend the use of press pocket-type paper carrier tape (Figure 1). This tape



**Figure 1** Structure of paper carrier tape

Type (b) offers better parts pick-up and reduced burrs and fluff.



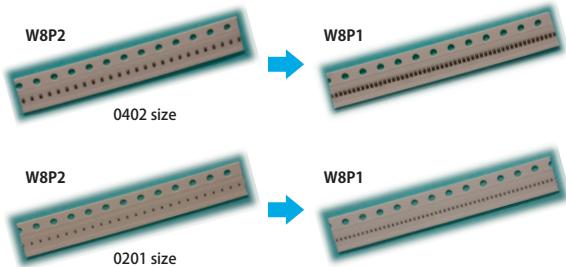
**Figure 2** Pocket cross-section

Press pocket-type paper carrier tape has a smooth surface that minimizes burrs and fluff.

is pressed with pockets to hold components, eliminating the need for a bottom tape. There are fewer burrs and less fluff because there is no bottom tape, stabilizing suction accuracy (Figure 2). Press pocket-type paper carrier tape is already the mainstream packaging for 0201 size (0.6mm × 0.3mm) capacitors.

Even smaller 01005 packages present a greater challenge when it comes to component pickup, leading many manufacturers to recommend embossed carrier tape, with pockets embossed into 4mm-wide plastic tape.

Miniature parts also reduce environmental impact. The tape most commonly used today is W8P2 (8mm width, 2mm pitch), which mounts components every 2mm. Newer tapes — W8P1 (8mm width, 1mm pitch) and W4P1 (4mm width, 1mm pitch) — reduce the pitch to only 1mm. Compared to W8P2, these new tapes carry more components per unit area, reducing total packaging and waste material. This reduces shipping and inventory costs, and means fewer reel changes (Figure 3).



**Figure 3** Paper carrier tape sizes

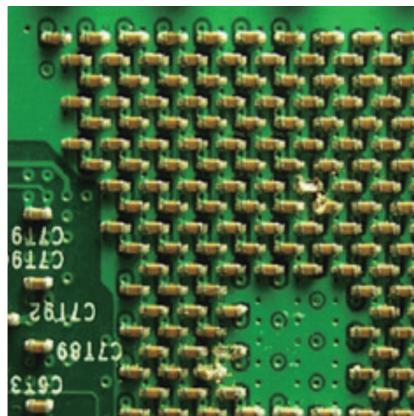
In a comparison with W8P2 (8mm width, 2mm pitch), the unit area of W8P1 (8mm width, 1mm pitch) allows more space for electronic parts, reducing reel exchange frequency and shipping and inventory costs. W8P1 is also more environment-friendly because it generates less waste after mounting.

## [Design]

## Low-ESL Products Slash Component Count: LW-reversed and Three-Terminal Capacitors

**Q** PCBs are mounting enormous quantities of monolithic ceramic capacitors these days. Is there any way to reduce this?

**A** Digital ICs are the cores of handheld devices, including smartphones, tablets, notebooks, and digital appliances, and are usually surrounded by rows upon rows of monolithic ceramic capacitors (Figure 1). Some boards mount more than 1000 capacitors, all necessary to ensure normal digital IC function. These capacitors fulfill two key roles, one of which is in power supply. In general, current demand varies greatly



**Figure 1** Board populated with monolithic ceramic capacitors

depending on the operational mode of a digital IC. For example, when a digital IC returns to full operating status from sleep, current demand surges. However, if the DC-DC converter is located too far away, the current supply cannot respond to the rapid load change. On the other hand, power can be stored in a monolithic ceramic capacitor mounted near the chip, ready to supply current as needed.

The capacitor's other key role is suppressing noise. The power supply waveform is weighted with high-frequency components, which generate EMI when propagated over long paths, or when released to ground. In addition, large fluctuations in supply voltage due to noise can cause digital IC malfunction. These problems can be prevented by inserting a monolithic ceramic capacitor between the power supply and the ground pattern. The harmonic impedance of the monolithic ceramic capacitor is low, so only the high-frequency noise component is routed to the ground pattern.

### ■ Suppressing loop impedance

Monolithic ceramic capacitors play a crucial role in IC function, so simply reducing the quantity used raises the risk of malfunction. Capacitor function must be maintained while the quantity of capacitors is reduced.

The first role, responding to rapid load change, requires a certain minimum capacitance, therefore reducing the quantity of capacitors used while sacrificing capacitance is not practical.

The point, then, is to focus on EMI-suppression capacitors, the second key role. This can be accomplished if the high-frequency impedance of the power supply is sufficiently low. Specifically, this is the low-impedance path from the IC power supply pin (HOT), through the monolithic ceramic capacitor, and back to the IC ground

pin. This is generally called loop impedance (Figure 2).

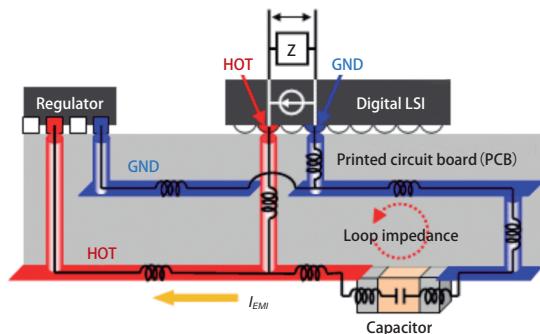
There are two methods of maintaining low loop impedance. One is to lower impedance by connecting capacitors in parallel, and although it is commonly used in electronic devices, it requires a large quantity of capacitors.

The second method is to use low-ESL (Equivalent Series L) monolithic ceramic capacitors, making it possible to maintain low loop impedance with fewer capacitors.

### Utilizing two low-ESL capacitors

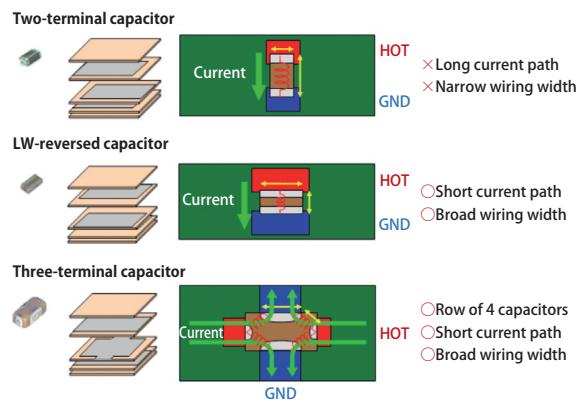
Two types of low-ESL monolithic ceramic capacitors are currently available (Figure 3), the first of which is the LW-reversed capacitor. In most monolithic ceramic capacitors, the electrodes are positioned longitudinally, but they are positioned laterally in LW-reversed components. This both shortens the current path and widens the trace, dropping ESL.

The other low-ESL type is the three-terminal capacitor, which integrates the two power-through pins common to all capacitors with a third one added as ground. Internally,



### Figure 2 Loop impedance

Loop impedance: the impedance of the path from the digital IC hot pin through the monolithic ceramic capacitor and back to the IC via the GND pin. The lower impedance helps suppress noise.



**Figure 3 Low-ESL capacitors**

Structures and current pathways of general-purpose two-terminal, LW-reversed, and three-terminal capacitors.

these capacitors alternate layers of power-through electrodes and ground electrodes. This significantly shortens and widens the current path from the supply pattern to ground, also known as the bypass direction. The effect of four current paths in parallel combines with the mutual inductance generated by the symmetric flow of current to ground, greatly reducing ESL.

Figure 4 shows ESL reduction with an LW-reversed capacitor and a three-terminal capacitor. The LW-reversed capacitor cuts ESL to one-third that of a typical monolithic ceramic capacitor, and to one-tenth with the three-terminal capacitor. Experiments used  $1 \mu\text{F}$  devices. Note that results are for lone capacitors. In actual use, capacitors would be mounted on PCBs, necessitating consideration of board and via inductance.

### Switching to three-terminal capacitors cuts total quantity to 25%

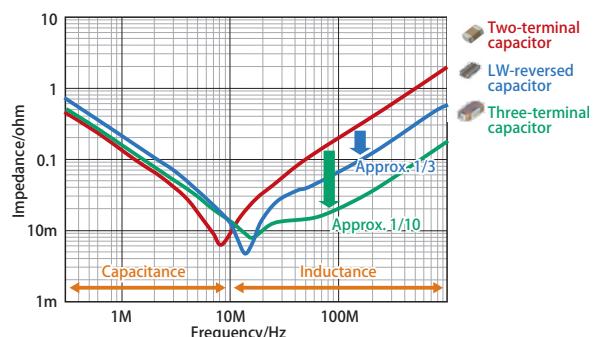
The use of LW-reversed and three-terminal capacitors

can significantly reduce the total quantity of capacitors required.

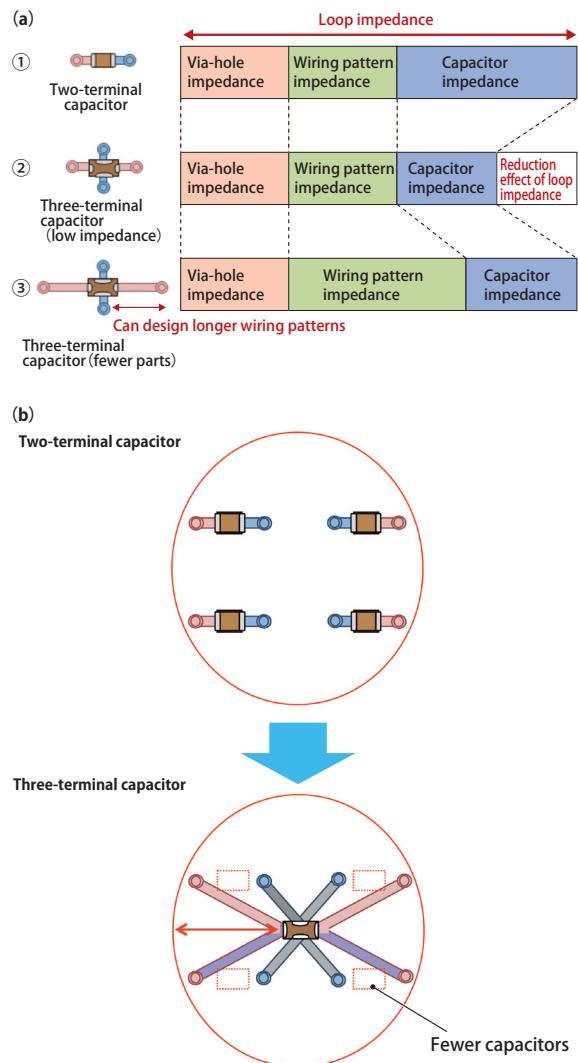
The LW-reversed capacitor (0402 size,  $4.3 \mu\text{F}$ ) attains a high-frequency impedance equivalent to that of two typical monolithic ceramic capacitors (0201 size,  $1 \mu\text{F}$ ), and the three-terminal type (0402 size,  $4.3 \mu\text{F}$ ) is lower than that of four (0201 size,  $1 \mu\text{F}$ ) connected in parallel. In other words, an LW-reversed capacitor can cut the total number of capacitors to half, and the three-terminal type to a quarter, compared to typical monolithic ceramic capacitors.

**Figure 5 (a)** illustrates the effect of three-terminal capacitors. Although the switch to three-terminal capacitors does not change the inductances of the vias or the wiring pattern (loop impedance), it does minimize capacitor ESL.

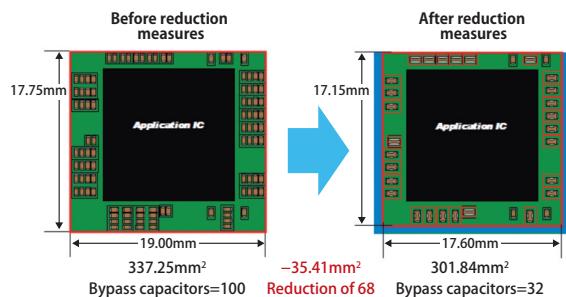
The ultimate goal, however, is to reduce the number of parts, not suppress ESL, so any resulting ESL reduction is distributed to the wiring pattern, by lengthening the wiring pattern accordingly. This enables one three-terminal



**Figure 4 Impedance frequency characteristics of capacitor**  
LW-reversed capacitor high-frequency impedance (inductance domain) is one-third that of two-terminal capacitors. Three-terminal capacitor high-frequency impedance is one-tenth.



**Figure 5 Fewer parts with three-terminal capacitors**  
The three-terminal capacitor has lower ESL than its two-terminal counterpart (a). This allows a longer wiring pattern, reducing the required quantity of capacitors (b).



**Figure 6 Fewer capacitors**

Cutting the quantity of capacitors around a smartphone processor from 100 to only 32 by switching to low-ESL parts.

capacitor to cover multiple power supply electrodes (Figure 5(b)), so that a single three-terminal capacitor can replace four monolithic ceramic capacitors.

#### ■ Cutting capacitor count from over 100 to only 32

Figure 6 is an actual application processor used in a smartphone, surrounded by more than one hundred 0201 monolithic ceramic capacitors. These can be replaced with low-ESL products to cut the quantity to only 32 and consumed board real estate from 337.25mm<sup>2</sup> to 301.84mm<sup>2</sup>, while maintaining loop impedance.

Low-ESL parts are extremely effective in reducing capacitor quantity, but there is also the issue of cost. In a simple comparison of unit cost, low-ESL capacitors are more expensive, but as Figure 6 illustrates, the lower quantity results in total savings in both parts and mounting costs. According to Murata Manufacturing, "When you look at overall cost, low-ESL capacitors are the most effective option." For the developer, switching to low-ESL parts is the optimal way to reduce capacitor quantity.

## ■ Design

# Adopting Low-ESL Design Upstream to Reduce Board Noise and Voltage Fluctuation

**Q** What is the best way to reduce loop impedance when the goal is to suppress noise and voltage fluctuation in electronic devices?

**A** The only way to suppress noise and voltage fluctuation in electronic devices is to maintain low loop impedance relative to the digital IC, whether application specific IC (ASIC), field programmable gate array (FPGA), or microprocessor. A guide to allowable loop impedance is the target impedance set for each digital IC, with an upper limit value defined for each frequency. Noise and voltage fluctuation problems can be minimized by maintaining loop impedance within this range.

However, achieving the assigned target impedance is not an easy task; the designer must take various factors into account, such as the position of the capacitors mounted around the digital IC, and board structure. There are a number of methods of reducing loop impedance.

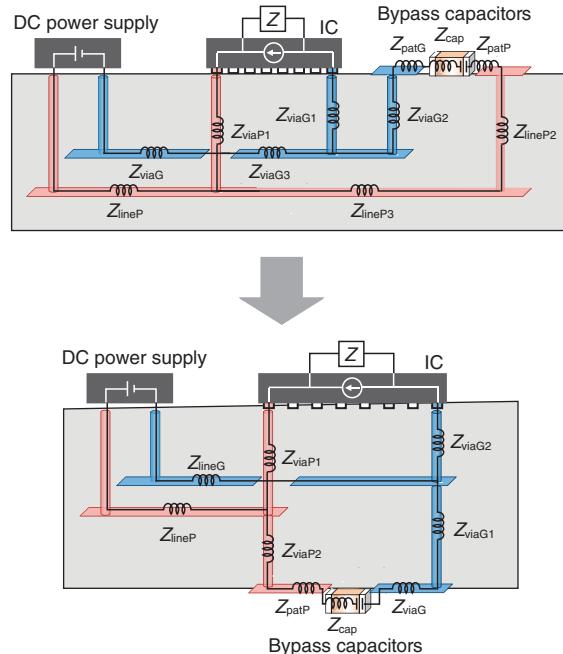
#### ■ Thick, short, and close

For digital ICs there are three main components in loop impedance: the impedance of the wiring pattern, vias, and bypass capacitors. Bypass capacitor impedance can be reduced with low-ESL capacitors, such as LW-reversed or three-terminal capacitors (page 32). Other methods are used to reduce wiring pattern and via impedance.

There are four concrete methods for reducing wiring

pattern impedance. One is to thicken and shorten the wiring pattern. The thicker and shorter the wiring, the lower the wiring pattern impedance.

The second method is to mount the bypass capacitors on the layer on the opposite side of the digital IC, rather than on the same layer (**Figure 1**). Same-layer mounting would require connections in the internal metallization of the PCB, extending the wiring pattern. Opposite-side mounting allows for a shorter wiring pattern, as some of the bypass capacitors can be mounted directly underneath



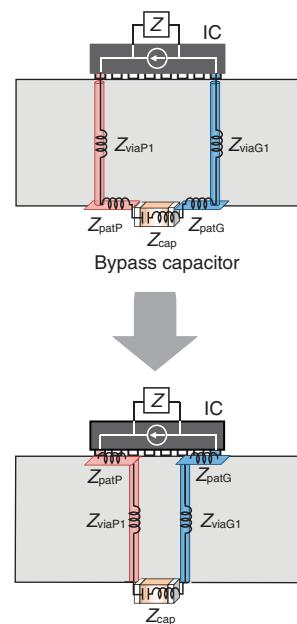
**Figure 1 Position the capacitors directly under the digital IC**

Lower the impedance by mounting the bypass capacitors on the opposite side of the layer mounting the digital IC, shortening the wiring pattern.

the digital IC.

The third option is mounting the bypass capacitors as close as possible to the digital IC in the event they must be mounted on the same layer. When using multiple types of capacitors, such as monolithic ceramic and tantalum electrolytic, the most effective technique is to mount them in order of ascending ESL values, with the lowest ESL device positioned closest to the digital IC.

The last option is to reduce the layer thickness between the PCB supply pattern and the ground pattern. For example, if the power supply pattern is on layer 5 and the ground pattern is on layer 2, move the supply pattern to



**Figure 2 Position vias to take advantage of mutual inductance**

Move reverse current vias closer to reduce via impedance.

layer 3, lowering the impedance of the supply pattern. The closer the supply pattern is to reference ground, the better.

### ■ Reducing ESL in upstream processes

There are three concrete methods for reducing via impedance.

The first is to thicken and shorten the via. As with the

wiring pattern, the thicker and shorter the via, the lower the impedance. This can be implemented by thinning the board and decreasing the distance between the ground and power supply patterns.

The second option is to use two or three vias, rather than just one, reducing impedance by increasing the number of parallel current paths.

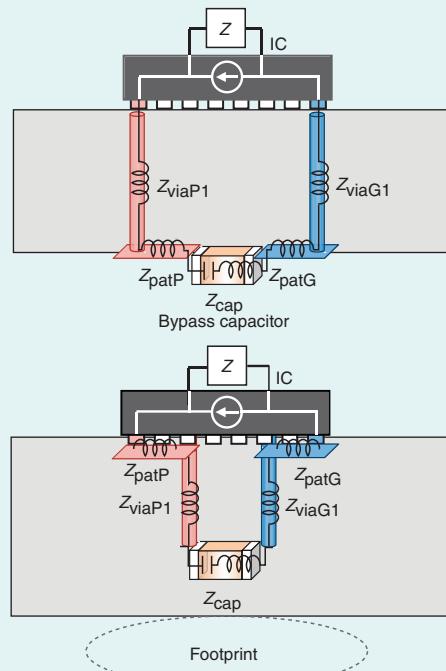
The third choice is to position the via for the reverse

## Major impedance reduction with embedded capacitors

The only way to reduce noise and voltage fluctuation is to minimize loop impedance by reconfiguring wiring patterns and vias. Impedance can be reduced by optimizing the shapes and positions of wiring patterns and vias. The method described here is complex, but if successfully implemented provides a significant reduction in impedance.

By embedding monolithic ceramic capacitors in PCB (Figure A), although the capacitor ESL remains unchanged, the wiring pattern and via are shortened, yielding very low impedance. The lower impedance, in turn, provides greatly reduced noise and voltage fluctuation. In addition, as capacitors no longer have surface footprints, designers can utilize front and back PCB surfaces more efficiently.

Many electronic parts manufacturers already offer embedded capacitors, such as the embedded monolithic ceramic capacitor from Murata Manufacturing, with a thickness of just 150  $\mu\text{m}$ . This commercially available product has a 1.0mm  $\times$  0.5mm footprint and a capacitance of 0.1  $\mu\text{F}$ , and cuts PCB impedance to a tenth compared to its SMT



**Figure A Effectiveness of embedded capacitors**

Embedding capacitors in the PCB allows for lower impedance, with shorter wiring and vias.

current closer to the forward via (Figure 2). Mutual inductance increases as the distance between the two decreases, keeping impedance low.

These methods must be considered in the upstream processes as they can require substantial board redesign. Although such modifications to conventional designs are labor-intensive, they make a clear contribution to lower noise and voltage fluctuation.

equivalent.

A few issues still remain, despite the excellent benefits presented by embedded capacitors. One is that it is impossible to externally confirm the connection between via and terminal electrode, or the mounting state, once embedded. Another is cost. Surface mount technology is already commonly used in volume production, and is therefore inexpensive.

Embedded technology is only just entering commercial use, and manufacturing costs are still so high that many companies are deferring implementation despite the outstanding impedance reduction gained.

Nevertheless, as digital ICs, including ASICs, FPGAs, and application processors, evolve to offer more features on lower voltage, resolving issues like noise and voltage fluctuation is becoming urgent. Semiconductor manufacturers will embed capacitors in digital IC packages and interposers soon, vitalizing the market with low-noise/low-voltage-fluctuation products.

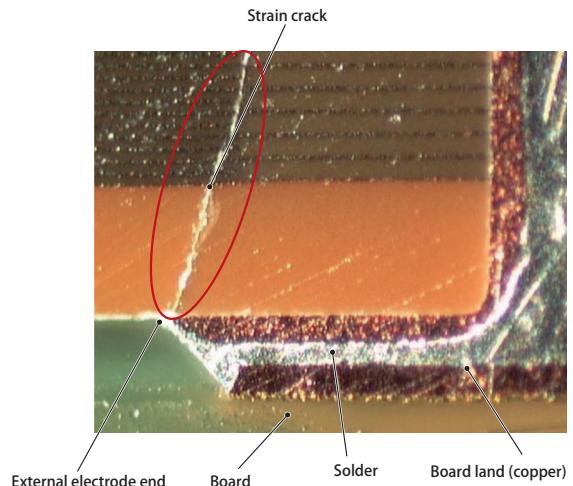
## [Design]

# Cracking Due to Board Strain: Minimizing Force Acting on Capacitors

**Q** How can monolithic ceramic capacitor cracking in PCB manufacturing and shipping inspection be minimized?

**A** Monolithic ceramic capacitors, just like porcelain, break when dropped or put under undue strain (Figure 1). In the above situation, capacitor cracks indicate a board has been exposed to excessive force during manufacturing or shipping inspection.

It is important to identify which process was responsi-



**Figure 1** Typical crack example

PCB strain causes severe stress on the monolithic ceramic capacitor, leading to cracking.

ble. Verification is difficult, as there are many possibilities, such as mounting the board on a jig, gripping board edges during transfer, or cutting a board out of the production panel. Pinpointing the cause requires a strain gauge mounted on a board to monitor force for each process.

It is possible to troubleshoot exactly how excessive force is applied to capacitors during the board cut process. In general, smartphone motherboards are produced by cutting a large production panel into individual motherboards. Manual handling can subject the board to heavy strain, applying considerable stress on the capacitors. In the worst case, this causes cracking.

If manual board separation is unavoidable, we recommend using a manual cropping jig to stabilize work performance. Grip the board as close as possible to the cut line to reduce the risk of cracking. It is also advisable to provide V-cuts along the separation lines on both sides of the board. These measures allow the board to be split with less force, minimizing stress on the capacitors. If the V-cuts that are too shallow or misaligned, however, more stress will result. If capital investment is available, a router-type board separator can provide dramatic stress reduction on boards.

Early prevention in the board-design phase is another solution. Specifically, capacitor mount positions should be as far away from the board separation point as possible, minimizing stress caused during board cutting.

## ■ [Design]

# Temperature-Compensating Capacitor Resolves Ultrasonic Sensor Failure

**Q** The in-vehicle parking assist system using ultrasonic sensors malfunctions in high-temperature environments. The phenomenon is obviously heat-related, but the exact cause is difficult to determine.

**A** Automotive electronics technology is growing increasingly sophisticated. One example is the parking assist system, employing ultrasonic sensors.

The ultrasonic sensor used in parking assist systems has both transmit and receive functions. When the ultrasonic wave from the emitter is reflected back from an object made of metal, concrete, glass, or plastic, the reflection is detected by the sensor.

The distance between the sensor and the object is determined by the round-trip signal time. If the object is extremely close, an alarm warns the driver, preventing minor collisions.

## ■ Using capacitors with negative temperature coefficients

The ultrasonic sensor is a very handy electronic device, but device characteristics must be fully understood to avoid the above problem. The most important issue here is temperature.

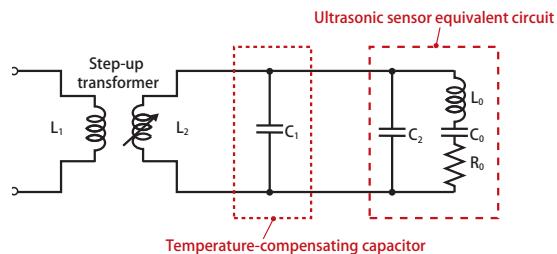
Most ultrasonic sensors use piezoelectric devices. When voltage is applied to a piezoelectric device, an ultrasonic wave is emitted based on the voltage and

frequency. When the ultrasonic wave reflects off an object and returns to the sensor, the piezoelectric device again generates electricity, and distance to the object can be calculated from the time elapsed between signal emission and detection.

The problem here is the temperature characteristic of the piezoelectric device. The device's equivalent circuit consists of an inductor, a resistor, and a capacitor. When used in a high-temperature environment, capacitance increases significantly, and can cause the parking assist ultrasonic sensor to malfunction.

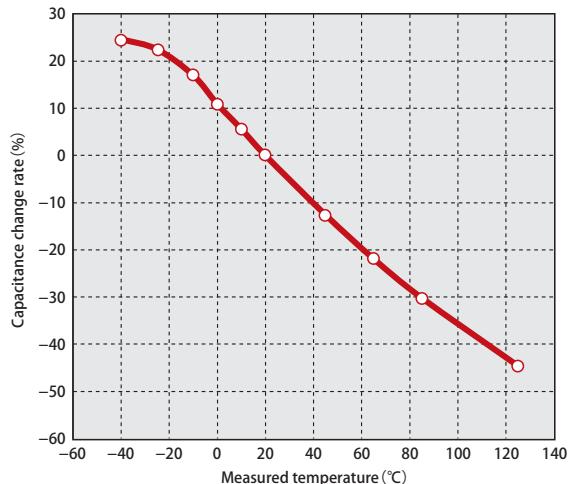
**Figure 1** shows the equivalent circuit for the parking assist system's receiver. Normally, when measuring short distances, ultrasonic wave emission is stopped when the drive signal to the ultrasonic sensor is terminated. Specifically, step-up transformer inductance ( $L$ ) and ultrasonic sensor capacitance ( $C$ ) form an LC serial resonance circuit. This resonance circuit absorbs excess oscillation energy, making it possible to halt ultrasonic wave emission instantly.

However, the ultrasonic sensor capacitance increases as operating temperature climbs. As a result, the ultrasonic



**Figure 1** Parking assist system receiver

The ultrasonic sensor equivalent circuit consists of an inductor, a resistor, and a capacitor. Combining this with a step-up transformer creates a resonance circuit.



**Figure 2** Using a monolithic ceramic capacitor with a negative temperature coefficient

Murata Manufacturing's ZLM series of temperature-compensating capacitors: capacitance decreases as operating temperature increases.

wave emission no longer stops instantly because the resonance frequency has become misaligned and excess oscillation energy can no longer be absorbed. In this situation, short distances cannot be measured as the reflection returns to the sensor before the emission pulse is terminated.

This problem can be resolved by eliminating changes in the sensor's capacitance due to high temperature. A temperature-compensating capacitor (with a negative temperature coefficient) can be used in parallel with the sensor as a resonance capacitor, reducing capacitance as the temperature rises (**Figure 2**). This will prevent any shift in the resonance frequency due to elevated temperature, enabling accurate measurement of even short distances.

## [Simulation]

## Utilizing Manufacturer Models for Accurate Consideration of DC Bias in Analysis

**Q** When designing a power supply circuit with a circuit simulator, calculation results can be inconsistent due to the DC-bias characteristic of monolithic ceramic capacitors. As a workaround, we obtained the DC-bias characteristic individually, and ran circuit simulations after manually correcting capacitance. Although the simulation produces consistent results, the process is quite laborious. Is there an easier way to accomplish this?

**A** Circuit simulators are now used in most electronic circuit design environments, allowing the developer to assess the behavior and characteristics of an electric circuit on the PCB without having to make a breadboard prototype. Faster design, in turn, enhances productivity within the increasingly short development period of electronic devices.

For that reason alone, the accuracy of the circuit simulator is crucial. If the actual and simulated measurements disagree significantly, there will be problems once a prototype is made. There is little point in saving time in the design phase with a simulator if it creates problems and forces later redesign.

There are many factors involved in enhancing the accuracy of circuit simulators, but the key point is the accuracy of the circuit model. If the model is inaccurate, simulated results will be inapplicable.

### ■ Circuit models taking DC-bias into consideration

The problem is directly related to the accuracy of the circuit model. SPICE circuit models and S parameters are available for monolithic ceramic capacitors as well, but most do not accommodate the DC-bias characteristic.

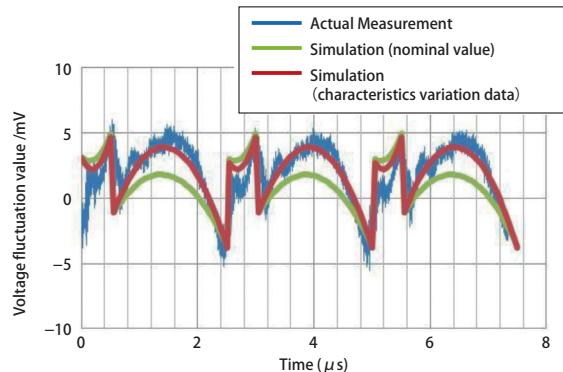
This characteristic describes the decrease in effective capacitance when DC voltage is input to a monolithic ceramic capacitor. DC voltage is input to all power supply circuits, including those for DC-DC converters. Therefore results of simulation using the model without consideration about DC voltage do not accord with actual results.

Figure 1 shows the analysis results for output voltage ripple and load response waveforms in a step-down DC-DC converter IC. In both cases, the model did not reflect the DC-bias characteristic (using nominal values), causing analytical results that differed considerably from actual results. When models that included the DC-bias characteristic were used, however, results were accurate and matched actual results closely.

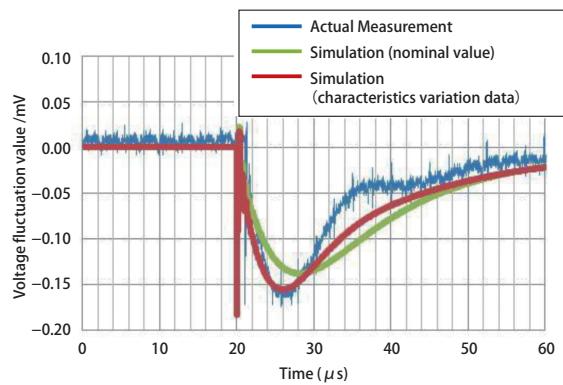
It is impractical for electronic device designers to obtain DC-bias characteristic data for monolithic ceramic capacitors and revise circuit models accordingly. Manufacturers, therefore, now provide circuit models that already reflect DC-bias characteristics.

A good example is the SimSurfing design support tool available on the Murata Manufacturing website, offering SPICE (with DC-bias characteristic) and S parameter data. Simply select the appropriate monolithic ceramic capacitor category and enter the circuit's input DC voltage. The corresponding equivalent circuit model with the DC-bias characteristic and S parameter will be displayed. The data can be downloaded and used in most circuit simulators. The SimSurfing tool vastly simplifies circuit

(a) Output voltage ripple waveform



(b) Load response waveform

**Figure 1 DC-bias data improves matching between simulated and actual results**

Actual and simulated results for output voltage ripple (a) and load response (b) in a step-down DC-DC converter. Results will be inaccurate unless the model incorporates DC-bias characteristic data. When such data is included, high accuracy results that match actual measurements are possible.

simulation with consideration for DC-bias characteristics, allowing shorter design times.

### [Simulation]

## Poor Matching between Simulated and Actual Results Due to Capacitance Change

**Q** In designing a time-constant circuit using monolithic ceramic capacitors, the charging characteristics in the prototype circuit do not match the simulated characteristics made using actual capacitance. Why is that so?

**A** Monolithic ceramic capacitors are becoming increasingly important as demand for high-density mounting rises. When used instead of aluminum electrolytic, tantalum electrolytic, or film capacitors, they can significantly reduce the board real estate needed for parts mounting.

However, the use of alternate capacitors requires attention to detail and careful calculation. The question above, using monolithic capacitors to create a time-constant circuit, is an excellent example. A time-constant circuit consists of a resistor and a capacitor, where the product of resistance and capacitance is time (s). For example, the combination of a  $1\text{k}\Omega$  resistor and a  $1\text{\mu F}$  capacitor produces a  $1\text{ms}$  time constant.

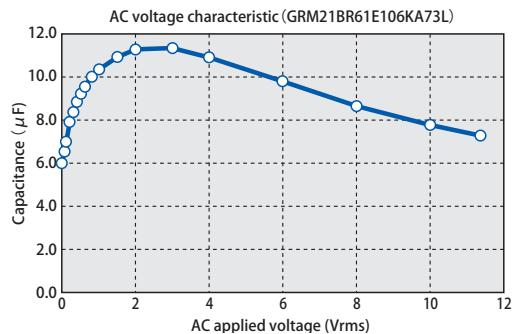
The capacitance value of the time-constant circuits using aluminum electrolytic, tantalum electrolytic, or film capacitors yields a highly accurate time constant that remains quite stable even through changes in circuit voltage or ambient temperature. However, with high-dielectric constant monolithic ceramic capacitors (B/F characteristics) using ferroelectric materials, changes in

voltage and ambient temperature can produce relatively large differences in capacitance. If this point is taken into consideration when choosing alternative capacitors, however, most problems can be avoided. Note that temperature-compensating monolithic ceramic capacitors using paraelectric materials (CH characteristic, etc.) rarely experience capacitance-related problems.

### ■ Using actual measured values in simulation

How much does a high-dielectric constant monolithic ceramic capacitor change? **Figure 1** shows capacitance measurements at various alternating currents. The monolithic ceramic capacitor used here was an 0805 (2.0mm × 1.25mm × 1.25mm), with a rated voltage of 25V and nominal capacitance of 10  $\mu$ F.

Capacitance changes are based on the measured input AC voltage (at 1kHz). Capacitance is 9.2  $\mu$ F when measured at 0.5Vrms, 11.2  $\mu$ F at 2Vrms, and 10.9  $\mu$ F at 4Vrms. To ensure accurate matching between actual and simulated

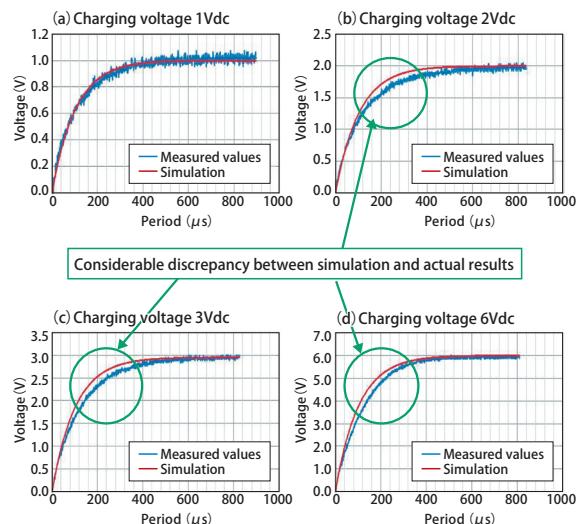


**Figure 1** AC voltage dependency of monolithic ceramic capacitor capacitance

The capacitance of monolithic ceramic capacitors varies according to the input alternating current (AC). The capacitor measured here was 0805 size, with rated voltage of 25Vdc and nominal capacitance of 10 $\mu$ F.

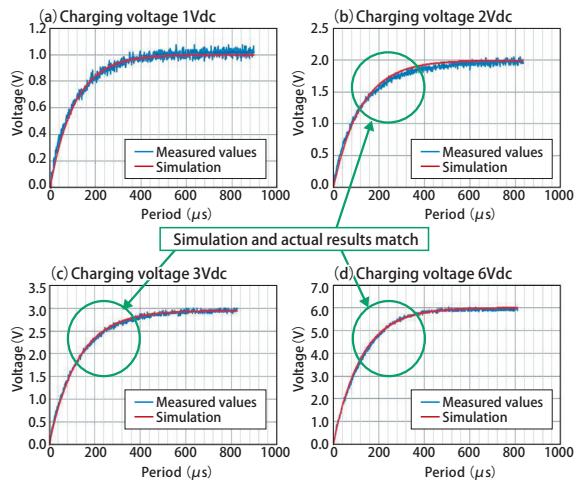
results, the capacitance of the actual input voltage must be measured in the time-constant circuit where the monolithic ceramic capacitor is located. This measured capacitance is then used to perform the simulation.

The concrete example shown in **Figure 2** is a comparison of simulated capacitor charging characteristics with actual results. In the simulation, capacitance was set at 9.2  $\mu$ F (value measured at 0.5Vrms AC), regardless of the actual input DC voltage. The charging characteristic with charging voltage 1Vdc exhibited relatively close matching between actual and simulated results. However, when measured at 2Vdc, 3Vdc, and 6Vdc, a large discrepancy developed, because capacitance was measured at 0.5Vrms



**Figure 2** Comparison of actual measurements with simulation results using actual measured capacitance at 0.5Vrms input

Simulation results closely match actual measurements at 1Vdc charging voltage, but not when charging voltage is 2, 3, or 6Vdc. This occurs because the actual capacitance measured at 0.5Vrms is also used at the other input voltages.



**Figure 3 Simulation results using the actual measured value with the AC applied voltage corresponding to the charging voltage**

Actual and simulation results are consistent with a high level of accuracy.

for all input voltages.

The capacitance values used in the simulation were then changed to the actual values measured at AC voltages corresponding to each charging voltage, and the simulation re-run. For example, for a charging voltage of 2Vdc, measurements were taken at 1.41Vms, making the peak voltage 2V. The results, shown in **Figure 3**, demonstrate that actual and simulated results exhibit excellent matching at all charging voltages.

In sum, the capacitance values of high-dielectric constant monolithic ceramic capacitors vary according to the AC input voltage. Capacitance varies based on the specifics of the circuit in use. Keeping these points in mind during circuit design and simulation will help prevent unforeseen problems.

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