CS2000_CS2100_CS2200_CS2300 to CS2600 Migration

Introduction

The Cirrus Logic CS2000/CS2100/CS2200/CS2300 and CS2600 are high-performance clocking devices. The CS2600 has an extended feature set, including several improvements and optimizations. The enhanced feature set is described in this document.

The CS2600 is available in commercial-grade 16-pin QFN package for operation from –40°C to +85°C. It is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

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1 Package

The CS2000, CS2100, CS2200, CS2300, and CS2600 are supplied in different packages as shown in Table 1. For further information, refer to the respective datasheets.

Table 1 Package Description

Device	Number of Pins	Package Type	Typical Package Dimensions
CS2000/CS2100/CS2200/CS2300	10	10L-MSOP	Refer to respective datasheet
CS2600	16	16-pin QFN	Refer to datasheet

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2 Features Overview

An overview of the CS2000, CS2100, CS2200, CS2300, and CS2600 features is provided in Table 2.

Table 2 Features Overview

Description	CS2000	CS2100	CS2200	CS2300	CS2600
Clock synthesizer incorporating delta-sigma fractional-N analog PLL. Generates low-jitter 6–75 MHz clock from 8–75 MHz timing reference.	8–56 MHz timing reference	—	8–56 MHz timing reference	—	✓
Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL. Generates low-jitter 6–75 MHz clock, synchronized to 50 Hz–30 MHz low-quality or intermittent frequency reference.	✓	✓	—	✓	✓
Flexible timing reference source – external clock, external crystal, or built-in oscillator.	external clock or crystal	external clock or crystal	external clock or crystal	built-in oscillator	external clock, crystal, or built-in oscillator
Clock-skipping mode – clock output maintained through short interruptions to timing reference.	✓	✓	—	✓	—
Holdover mode – glitchless clock output maintained indefinitely on interruption of timing reference.	—	—	—	—	✓
Automatic rate control – seamless transitions and stable clock output through changes in reference frequency.	—	—	—	—	✓
BCLK and FSYNC outputs – clock outputs for digital audio applications, derived from the main PLL output.	—	—	—	—	✓
Phase-alignment control – automatic phase alignment of BCLK/FSYNC outputs to the frequency reference.	—	—	—	—	✓
OTP memory – customer-programmable memory to configure the device on power-up.	—	—	—	—	✓
Hardware control mode – device configuration using external resistors, and no host controller required.	—	—	—	—	✓
Software reset	—	—	—	—	✓

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3 Device Performance

A summary of the CS2000, CS2100, CS2200, CS2300, and CS2600 performance is provided in Table 3.

Table 3 Device Performance

Description	CS2000	CS2100	CS2200	CS2300	CS2600
Crystal frequency range	8 – 50 MHz			N/A	8 – 50 MHz
Reference (REF_CLK) frequency range	8 – 56 MHz	8 – 75 MHz	8 – 56 MHz	N/A	8 – 75 MHz
Clock input (CLK_IN) frequency range	50 Hz – 30 MHz		N/A	50 Hz – 30 MHz	50 Hz – 30 MHz
Clock output (CLK_OUT) frequency range	6 – 75 MHz				
CLK_OUT period jitter, external timing reference	70 ps			N/A	40 ps[1]
CLK_OUT period jitter, internal oscillator reference	N/A			35 ps	35 ps[1]
CLK_OUT baseband TIE jitter, external timing reference (100 Hz – 40 kHz)	50 ps			N/A	50 ps[1]
CLK_OUT wideband TIE jitter, external timing reference (100 Hz corner)	175 ps			N/A	165 ps[1]
PLL lock time – Multiplier Mode	100 clock periods (CLK_IN), for f_{CLK_IN} < 200 kHz 1 ms for f_{CLK_IN} > 200 kHz		N/A	100 clock periods (CLK_IN), for f_{CLK_IN} < 200 kHz 1 ms for f_{CLK_IN} > 200 kHz	
PLL lock time – Synthesizer Mode	1 ms	N/A	1 ms	N/A	1 ms
Power supply current (unloaded)	40 mW (VDD=3.3V)			59 mW (VDD=3.3V)	13.2 mW (VDD=3.3V)[1] 7.2 mW (VDD=1.8V)[1]
I2C clock frequency	100 kHz (max)				400 kHz (max)
SPI clock frequency	6 MHz (max)				17.5 MHz (max)

Note 1 (CS2600) – these are target performance specifications.

4 I2C/SPI Control Port

The CS2600 control port enables I2C or SPI modes of operation. The CS2600 is configured similarly to the CS2000/CS2100/CS2200/CS2300, using either I2C mode or SPI mode. Note that the CS2600 uses 16-bit register operations.

5 Power Supply

The CS2600 supports the same power-supply configuration as CS2000/CS2100/CS2200/CS2300, as shown in Table 4. Additionally, the CS2600 can be powered from a 1.8 V supply. For further information, refer to the respective datasheet.

Table 4 Power Supply

Power Domain	CS2000/CS2100/CS2200/CS2300	CS2600
DC Power Supply	VDD (3.1 – 3.5V)	VDD (3.1 – 3.5V) VDD (1.71 -1.89V)

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6 Additional CS2600 Features

6.1 Holdover Mode

The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. If CLK_IN is missing or unstable, the CS2500 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK_OUT signal continues without any glitch or interruption.

For further information, refer to Section 4.4.2 in the CS2600 datasheet.

6.2 Automatic Rate Control (ARC)

The CS2600 supports an automatic rate control (ARC) function which detects the CLK_IN reference frequency and configures the PLL multiplier ratio for the required PLL output frequency. Auto-detection is supported across a range of sample-rate frequencies typically used in digital audio systems.

For further information, refer to Section 4.4.4 in the CS2600 datasheet.

6.3 ALTCLK Generator

The ALTCLK generator is an automatic divider that can be used to generate a fixed CLK_OUT frequency from a range of related PLL frequencies. The CLK_OUT signal can be derived either directly from the PLL or else from the ALTCLK generator. The clock source is selected using CLK_OUT_SEL.

For further information, refer to Section 4.5.1 in the CS2600 datasheet.

6.4 BCLK and FSYNC

The CS2600 supports BCLK and FSYNC outputs, intended for use in digital-audio applications. These clock outputs are derived from the main PLL output (MCLK) using configurable dividers.

For further information, refer to Section 4.5.2 in the CS2600 datasheet.

6.5 Phase Alignment

The phase-alignment function can be used to ensure the BCLK and FSYNC outputs are phase-aligned to the CLK_IN frequency reference. The function can be triggered manually using a control-register write, or automatically based on a configurable phase-offset threshold.

For further information, refer to Section 4.5.3 in the CS2600 datasheet.

6.6 Freezable Fields

The register map supports a number of freezable fields, as listed in Table 4-7 in the CS2600 datasheet. If FREEZE_EN is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until FREEZE_EN is cleared. This feature can be used to update multiple fields simultaneously.

For further information, refer to Section 4.7.3.1 in the CS2600 datasheet.

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6.7 OTP programming

The CS2600 incorporates a customer-programmable OTP memory which can be used to automatically configure the device after power-up. The OTP memory enables the device to be factory programmed for a specific target application, removing the need for a host system to configure the device.

For further information, refer to Section 4.8 in the CS2600 datasheet.

6.8 Hardware Control Mode

The CS2600 supports hardware and software control modes. In Hardware Control Mode, the device configuration is determined by external resistors connected to the hardware-control pins, CONFIG1–CONFIG6. The external resistors are connected to GND or VDD; different resistor values allow the CS2600 to detect eight configuration options per pin.

For further information, refer to Section 4.9 in the CS2600 datasheet.

6.9 Software Reset

A software reset is triggered by writing 0x5A to the SW_RST field. A software reset causes the CS2600 control registers to be reset to their default states.

7 Revision History

Revision History

Revision	Changes
R1 MAY 2024	• Initial version

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