

CS2100_CS2300 to CS2501 Migration

Introduction

The Cirrus Logic CS2100/CS2300 and CS2501 are high-performance clocking devices. The devices are identical in size, as well as pin layout & locations. The CS2501 can be placed onto the same PCB footprint as the CS2100/CS2300.

The CS2501 has a similar feature set to the CS2100/CS2300 and includes several improvements and optimizations, which are described in this document. The CS2501 can be used with existing control software as the register map is identical to the CS2100/CS2300.

The CS2501 is available in commercial-grade 10-pin TSSOP package for operation from -40°C to $+85^{\circ}\text{C}$. It is also available in the AEC-Q100-qualified grade-2 package for operation from -40°C to $+105^{\circ}\text{C}$.

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1 Package

The CS2100, CS2300, and CS2501 are supplied in similar packages as shown in Table 1. For further information, refer to the respective datasheets.

Table 1 Package Description

Device	Number of Pins	Package Type	Typical Package Dimensions
CS2100/CS2300	10	10L-MSOP	Refer to respective datasheet
CS2501	10	10L-TSSOP	Refer to datasheet

2 Features Overview

An overview of the CS2000, CS2200, and CS2500 features is provided in Table 2.

Table 2 Features Overview

Description	CS2100	CS2300	CS2501
Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL. Generates low-jitter 6–75 MHz clock, synchronized to 50 Hz–30 MHz low-quality or intermittent frequency reference.	✓	✓	✓
Flexible timing reference source – external clock, external crystal, or built-in oscillator.	external clock or external crystal	built-in oscillator	external clock, external crystal, or built-in oscillator
Clock-skipping mode – clock output maintained through short interruptions to timing reference.	✓	✓	✓
Holdover mode – glitchless clock output maintained indefinitely on interruption of timing reference.	—	—	✓
Software reset	—	—	✓

3 Device Performance

An overview of the CS2000, CS2200, and CS2500 features is provided in Table 3.

Table 3 Device Performance

Description	CS2100	CS2300	CS2501	
			External REF_CLK	Built-in oscillator
Crystal frequency range	8 – 50 MHz	N/A	8 – 50 MHz	
Reference (REF_CLK) frequency range	8 – 75 MHz	N/A	8 – 75 MHz	
Clock input (CLK_IN) frequency range	50 Hz – 30 MHz		50 Hz – 30 MHz	
Clock output (CLK_OUT) frequency range	6 – 75 MHz		6 – 75 MHz	
CLK_OUT period jitter	70 ps	35 ps	40 ps ¹	35 ps ¹
CLK_OUT baseband TIE jitter (100 Hz – 40 kHz)	50 ps		50 ps ¹	300 ps
CLK_OUT wideband TIE jitter (100 Hz corner)	175 ps	150 ps	165 ps ¹	300 ps
PLL lock time – Multiplier Mode	100 clock periods (CLK_IN), for $f_{CLK_IN} < 200$ kHz 1 ms for $f_{CLK_IN} > 200$ kHz		100 clock periods (CLK_IN), for $f_{CLK_IN} < 200$ kHz 1 ms for $f_{CLK_IN} > 200$ kHz	
Power supply current (unloaded)	40 mW (VDD=3.3V)	59 mW (VDD=3.3V)	13.2 mW (VDD=3.3V) ¹	7.2 mW (VDD=1.8V) ¹
I2C clock frequency	100 kHz (max)		400 kHz (max)	
SPI clock frequency	6 MHz (max)		17.5 MHz (max)	

Note 1 (CS2501) – these are target performance specifications.

4 Register Map

The CS2501 register map is compatible with the register map of the CS2100/CS2300. The register map is 8-bit wide.

Note there are some minor differences in the register maps regarding the Device Identification fields. Refer to AN0626R1 for further information.

5 I2C/SPI Control Port

The CS2501 control port enables I2C or SPI modes of operation, matching the behavior of the CS2100/CS2300. The CS2501 can be used with existing control software as the register map is identical to the CS2000/CS2200.

6 Power Supply

The CS2100/CS2300 and the CS2501 use same power-supply configurations, as shown in Table 4. Additionally, the CS2501 can be powered from a single 1.8 V supply. For further information, refer to the respective datasheet.

Table 4 Power Supply

Power Domain	CS2100/CS2300	CS2501
DC Power Supply	VDD (3.1 – 3.5V)	VDD (3.1 – 3.5V) VDD (1.71 -1.89V)

7 Additional CS2501 features

The CS2501 supports additional features to the CS2100/CS2300; these are described in the following sections.

7.1 Holdover Mode

The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. If CLK_IN is missing or unstable, the CS2501 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK_OUT signal continues without any glitch or interruption.

For further information, refer to Section 4.4.2 in the CS2501 datasheet.

7.2 Freezable Fields

The register map supports a number of freezable fields, as listed in Table 4-3 in the datasheet. If FREEZE_EN is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until FREEZE_EN is cleared. This feature can be used to update multiple fields simultaneously.

For further information, refer to Section 4.7.3.1 in the CS2501 datasheet.

7.3 Software Reset

A software reset is triggered by writing 0x5A to the SW_RST field. A software reset causes the CS2501 control registers to be reset to their default states.

8 Revision History

Revision History	
Revision	Changes
R1 MAY 2024	<ul style="list-style-type: none">Initial version.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

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