

## CS2000\_CS2200 to CS2500 Migration

### Introduction

The Cirrus Logic CS2000/CS2200 and CS2500 are high-performance clocking devices. The devices are identical in size, as well as pin layout & locations. The CS2500 can be placed onto the same PCB footprint as the CS2000/CS2200.

The CS2500 has a similar feature set to the CS2000/CS2200 and includes several improvements and optimizations, which are described in this document. The CS2500 can be used with existing control software as the register map is identical to the CS2000/CS2200.

The CS2500 is available in commercial-grade 10-pin TSSOP package for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . It is also available in the AEC-Q100-qualified grade-2 package for operation from  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

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### 1 Package

The CS2000, CS2200, and CS2500 are supplied in similar packages as shown in Table 1. For further information, refer to the respective datasheets.

**Table 1 Package Description**

Device	Number of Pins	Package Type	Typical Package Dimensions
CS2000/CS2200	10	10L-MSOP	Refer to respective datasheet
CS2500	10	10L-TSSOP	Refer to datasheet

## 2 Features Overview

An overview of the CS2000, CS2200, and CS2500 features is provided in Table 2.

**Table 2 Features Overview**

Description	CS2000	CS2200	CS2500
Clock synthesizer incorporating delta-sigma fractional-N analog PLL. Generates low-jitter 6–75 MHz clock from 8–75 MHz timing reference.	8–56 MHz timing reference	8–56 MHz timing reference	8–75 MHz timing reference
Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL. Generates low-jitter 6–75 MHz clock, synchronized to 50 Hz–30 MHz low-quality or intermittent frequency reference.	✓	—	✓
Flexible timing reference source – external clock or external crystal.	✓	✓	✓
Clock-skipping mode – clock output maintained through short interruptions to timing reference.	✓	—	✓
Holdover mode – glitchless clock output maintained indefinitely on interruption of timing reference.	—	—	✓
Software reset	—	—	✓

## 3 Device Performance

A summary of the CS2000, CS2200, and CS2500 performance is provided in Table 3.

**Table 3 Device Performance**

Description	CS2000	CS2200	CS2500
Crystal frequency range	8 – 50MHz		8 – 50MHz
Reference (REF_CLK) frequency range	8 – 56MHz		8 – 75MHz
Clock input (CLK_IN) frequency range	50 Hz – 30 MHz	N/A	50 Hz – 30MHz
Clock output (CLK_OUT) frequency range	6 – 75 MHz		6 – 75MHz
CLK_OUT period jitter	70 ps		40 ps <sup>1</sup>
CLK_OUT baseband TIE jitter (100 Hz – 40 kHz)	50 ps		50 ps <sup>1</sup>
CLK_OUT wideband TIE jitter (100 Hz corner)	175 ps		165 ps <sup>1</sup>
PLL lock time – Multiplier Mode	100 clock periods (CLK_IN), for $f_{CLK\_IN} < 200$ kHz 1 ms for $f_{CLK\_IN} > 200$ kHz	N/A	100 clock periods (CLK_IN), for $f_{CLK\_IN} < 200$ kHz 1 ms for $f_{CLK\_IN} > 200$ kHz
PLL lock time – Synthesizer Mode	1 ms		1 ms
Power supply current (unloaded)	40 mW (VDD=3.3V)		13.2 mW (VDD=3.3V) <sup>1</sup> 7.2 mW (VDD=1.8V) <sup>1</sup>
I2C clock frequency	100 kHz (max)		400 kHz (max)
SPI clock frequency	6 MHz (max)		17.5 MHz (max)

Note 1 (CS2500) – these are target performance specifications.

## 4 Register Map

The CS2500 register map is compatible with the register map of the CS2000/CS2200. The register map is 8-bit wide.

Note there are some minor differences in the register maps regarding Device Identification fields. Refer to AN0626R1 for further information.

## 5 I2C/SPI Control Port

The CS2500 control port enables I2C or SPI modes of operation, matching the behavior of the CS2000/CS2200. The CS2500 can be used with existing control software as the register map is identical to the CS2000/CS2200.

## 6 Power Supply

The CS2500 supports the same power-supply configuration as the CS2000/CS2200, as shown in Table 4. Additionally, the CS2500 can be powered from a 1.8 V supply. For further information, refer to the respective datasheet.

**Table 4 Power Supply**

Power Domain	CS2000/CS2200	CS2500
DC Power Supply	VDD (3.1 – 3.5V)	VDD (3.1 – 3.5V) VDD (1.71 -1.89V)

## 7 Additional CS2500 features

The CS2500 supports additional features to the CS2000/CS2200; these are described in the following sections.

### 7.1 Holdover Mode

The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. If CLK\_IN is missing or unstable, the CS2500 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK\_OUT signal continues without any glitch or interruption.

For further information, refer to Section 4.4.2 in the CS2500 datasheet.

### 7.2 Freezable Fields

The register map supports a number of freezable fields, as listed in Table 4-3 in the datasheet. If FREEZE\_EN is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until FREEZE\_EN is cleared. This feature can be used to update multiple fields simultaneously.

For further information, refer to Section 4.7.3.1 in the CS2500 datasheet.

### 7.3 Software Reset

A software reset is triggered by writing 0x5A to the SW\_RST field. A software reset causes the CS2500 control registers to be reset to their default states.

## 8 Revision History

**Revision History**

Revision	Changes
R1 MAY 2024	• Initial version.

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**Contacting Cirrus Logic Support**

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