Hardware User Guide

Sterling LWB5+ Development Kit

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	07 Dec 2020	Initial version	Jacky Kuo Dean Ramsier	Jonathan Kaye

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1 INTRODUCTION

The development kit is designed to support performance validation and software development for projects utilizing the Laird LWB5+ module. This document is intended to assist manufacturers and related parties with the integration of Laird Sterling LWB5+ into their host devices. Data in this document is drawn from several sources and includes information found in the Laird Sterling LWB5+ Architecture Document, Cypress CYW4373 datasheet, and FTDI FT232R datasheet.

IMPORTANT: The information in this document is subject to change. Please visit the Sterling LWB5+ product page for the latest information.

1.1 Purpose and Scope

The purpose of this document is to provide details regarding the setup and configuration of the Sterling LWB5+ mounted on the development board. This document covers a description and design examples of the Sterling LWB5+ DVK board and its features.

1.2 Related Documents

The following documents are available from the Sterling LWB5+ product page:

- Sterling LWB5+ Product Brief
- Sterling LWB5+ Datasheet

1.3 Kit Contents

The product kit contains the following:

Development Board x1	**The development board has the required Sterling LWB5+ module already soldered onto it and exposes all the various hardware interfaces available**
Power Option	AC/DC adapter 12V/1A USB Cable – Type A to Micro USB-AB. This cable is also used for the following: ▪ Bluetooth connectivity via the FTDI USB-RS232 converter on the DVK when the Sterling LWB5+ is configured for SDIO/UART interface ▪ Wi-Fi and Bluetooth connectivity when the Sterling LWB5+ is configured for USB/USB interface
RF Cable x1	SMA to MHF4 pigtail cable for conducted performance validation P/N: **CARSMF10RMHF4-001**
RF Antenna	▪ Laird DVK part # **453-00045-K1** has a chip antenna already soldered onto the LWB5+ module or (depending on kit purchased) ▪ Laird DVK part # **453-00046-K1** with MH4 RF connector to attach external antenna. This DVK ships with an external dipole antenna, Laird part # **001-0009**.
Jumper cap x3	Allows configuration using the various pin headers
Product insert card	Provides links to additional information including the Sterling LWB5+ user manual, firmware, application notes, schematics, quick start guides and firmware release notes

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2 STERLING LWB5+ DEVELOPMENT KIT SPECIFICATIONS

Table 1: Development board specifications

Characteristic	Specifications
Configuration Modes	SDIO / UART (Wi-Fi / Bluetooth) USB / USB (Wi-Fi / Bluetooth)
Host Interfaces	SDIO (Wi-Fi) UART (Bluetooth) USB (Wi-Fi and Bluetooth) PCM (Bluetooth audio)
Power supplies	VBAT configurable to 3v3, 3v6 or 4v8 and provided via one of ▪ 12V/1A power adapter, allowing 3v6 or 4v8 operation. ▪ USB1/USB2 or SDIO, allowing 3v3 operation. VDDIO configurable to 3v3 or 1v8 and provided via one of ▪ SDIO ▪ USB1/USB2
Antenna gain	2.0 dBi peak gain on 2.4 GHz and 5 GHz – reference antenna Laird part # 001-0009
Wake-up signals	Wi-Fi ▪ WL_HOST_WAKE ▪ WL_DEV_WAKE Bluetooth ▪ BT_HOST_WAKE ▪ BT_DEV_WAKE
GPIOs	5 GPIOs reserved for future use
Dimension	126.26 mm x 65 mm x 16 mm

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3 Sterling LWB5+ Development Kit – Main Development Board

The Sterling LWB5+ development board is a fully featured evaluation platform for the Sterling LWB5+ series module. It allows users to evaluate radio performance as well as the creation of prototypes and application-specific designs.

The board can be configured to support either the SDIO/UART or the USB/USB host interface. Power supplies are configurable, and headers provide access to key signals. An on-board level shifter circuit with headers allows external signals to be level shifted as needed.

3.1 Key Features

The Sterling LWB5+ development board has the following features:

- Sterling LWB5+ series module soldered onto the development board
  - Integrated chip antenna variant or
  - MH4 antenna connector variant
- Boot mode/interface strapping options (SW1, SW2 and SW3)
  - SDIO interface at either 1v8 or 3v3 (Wi-Fi)
  - UART interface exposed via FTDI UART/USB bridge (Bluetooth) (USB1)
  - USB bridge interface (Wi-Fi and Bluetooth) (USB2)
- Supports either High VBAT (3v6 or 4v8 from external power supply) or Normal VBAT (3v3 from SDIO/USB) options (SW4, J12)
- On-board 3v3 supplied from either USB or SDIO bus interfaces (SW5)
- Supports VDDIO at either 3v3 or 1v8 (SW6)
- Ability to hold either Wi-Fi or BT in reset via jumper (J8)
- LEDs for VBAT and 3V3 source indication
- Ability to measure LWB5+ module current (J11, J13, J17, J18)
- IO break-out 2.54 mm pitch pin header connectors (plated through-holes) bring out all Sterling LWB5+ module interfaces
  - PCM
  - GPIOs
  - Wakeup signals.
- Ability to disable external 32khz sleep clock (J4).
- Bi-directional 8-bit voltage level shifter (3v3 <-> 1v8) for application/prototyping use (J5, J6)

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4 Hardware Overview

4.1 Block Diagram

Figure 1 shows the block diagram of the development board.

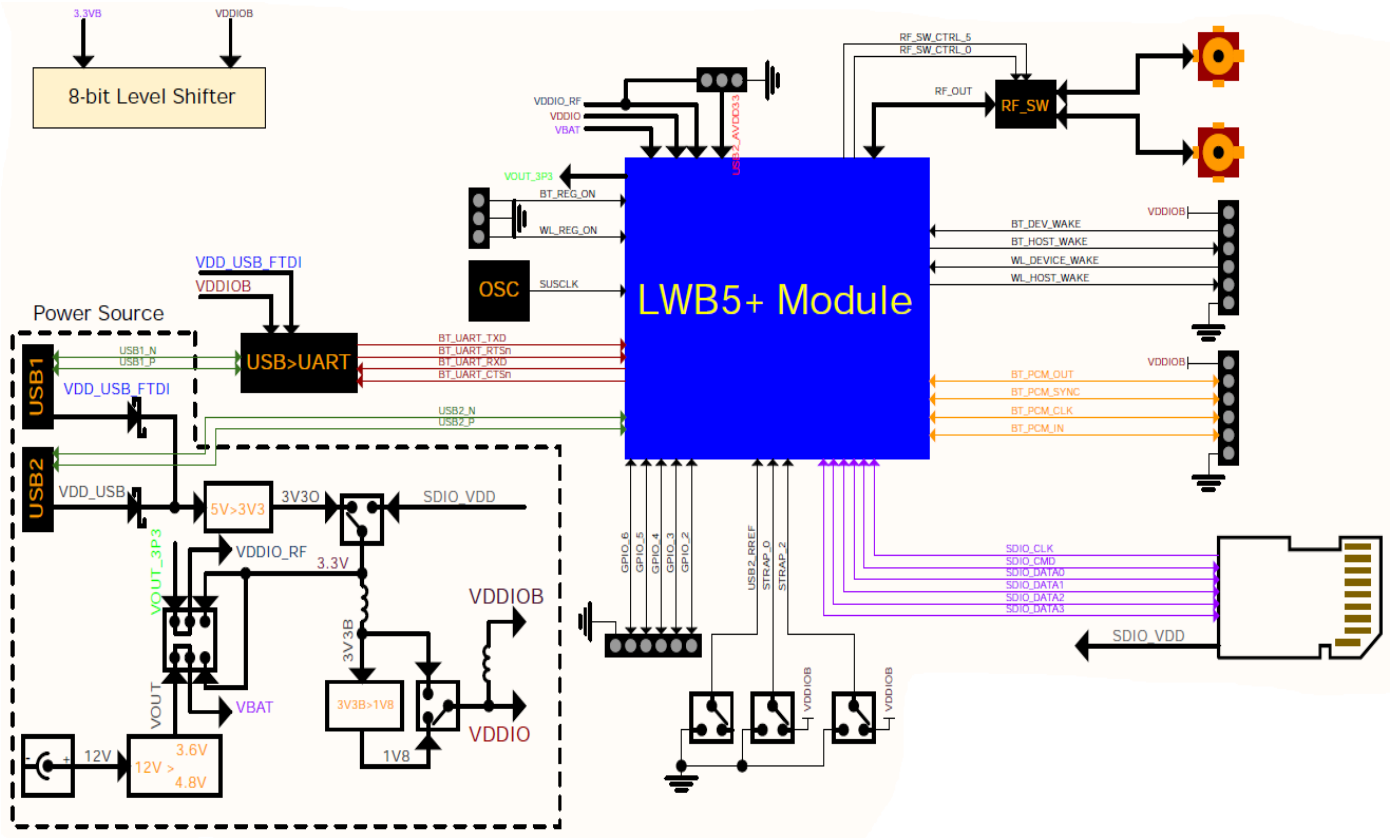

Figure 1: LWB5+ series module development board block diagram

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4.2 Understanding the Development Board

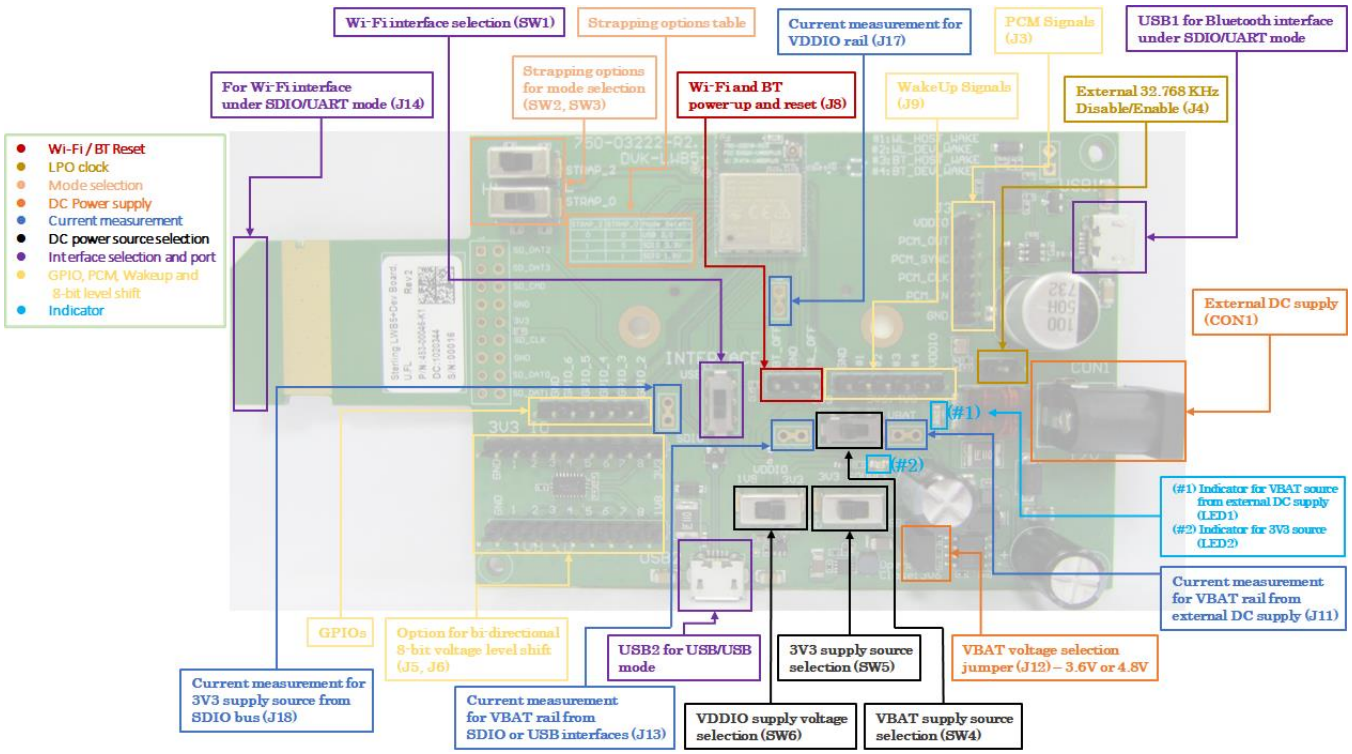

Figure 2: Switch and connector locations

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4.3 Switches and Connectors

Table 2: Configuration switches and jumpers

Connector	Descriptions
CON1	External DC power supply connector for optional DC12V/1A power source
J14	SDIO interface dedicated to Wi-Fi in SDIO/UART interface mode
USB1	UART interface (via Serial/USB bridge) dedicated to Bluetooth in SDIO/UART interface mode
USB2	USB interface supporting both Wi-Fi and Bluetooth USB/USB interface mode
SW1	USB reference voltage configuration dependent on interface mode selection (SDIO/UART or USB/USB)
SW2, SW3	Interface mode configuration ▪ SDIO (3v3)/UART – Supports SDIO Full Speed/High Speed modes only ▪ SDIO (1v8)/UART – Supports SDIO UHS modes up to SDR104 ▪ USB/USB
SW4	VBAT source selection ▪ 3v6/4v8 from external DC power supply adapter on CON1 ▪ 3v3 from SDIO or USB host interface
J12	VBAT voltage level configuration when supplied by external DC power adapter ▪ J12 with jumper – 3v6 ▪ J12 open – 4v8
J11	Current measurement header for VBAT supplied by external power supply adapter
SW5	3v3 power source selection ▪ SDIO host interface ▪ USB1/USB2 host interface
J13	Current measurement header for VBAT supplied by SDIO/USB host interface
J18	Current measurement header for SDIO host interface
SW6	VDDIO voltage level configuration (must match host IO signals) ▪ 3 v 3 ▪ 1 v 8
J17	Current measurement header for VDDIO
J8	Forcible disable Wi-Fi and/or Bluetooth
J4	Optionally disable external 32khz oscillator
J3	Header exposing Bluetooth PCM interface
J9	Header exposing Wi-Fi and Bluetooth DEV_WAKE/HOST_WAKE signals
J10	Header exposing GPIO signals (reserved)
J5, J6	Bi-directional 8-bit voltage translate between 3V3 and 1V8.

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4.4 Default Configuration

The out-of-box configuration supports operation in SDIO (3v3)/UART mode with all voltage rails supplied by the host SDIO interface at 3v3. See Figure 3 for the out-of-box settings.

Important! This configuration requires that the host provides sufficient power for radio operation via the SDIO interface. It also requires that the host SDIO interface operates only at 3v3 and does not attempt to switch to 1v8 to operate at SDR rates.

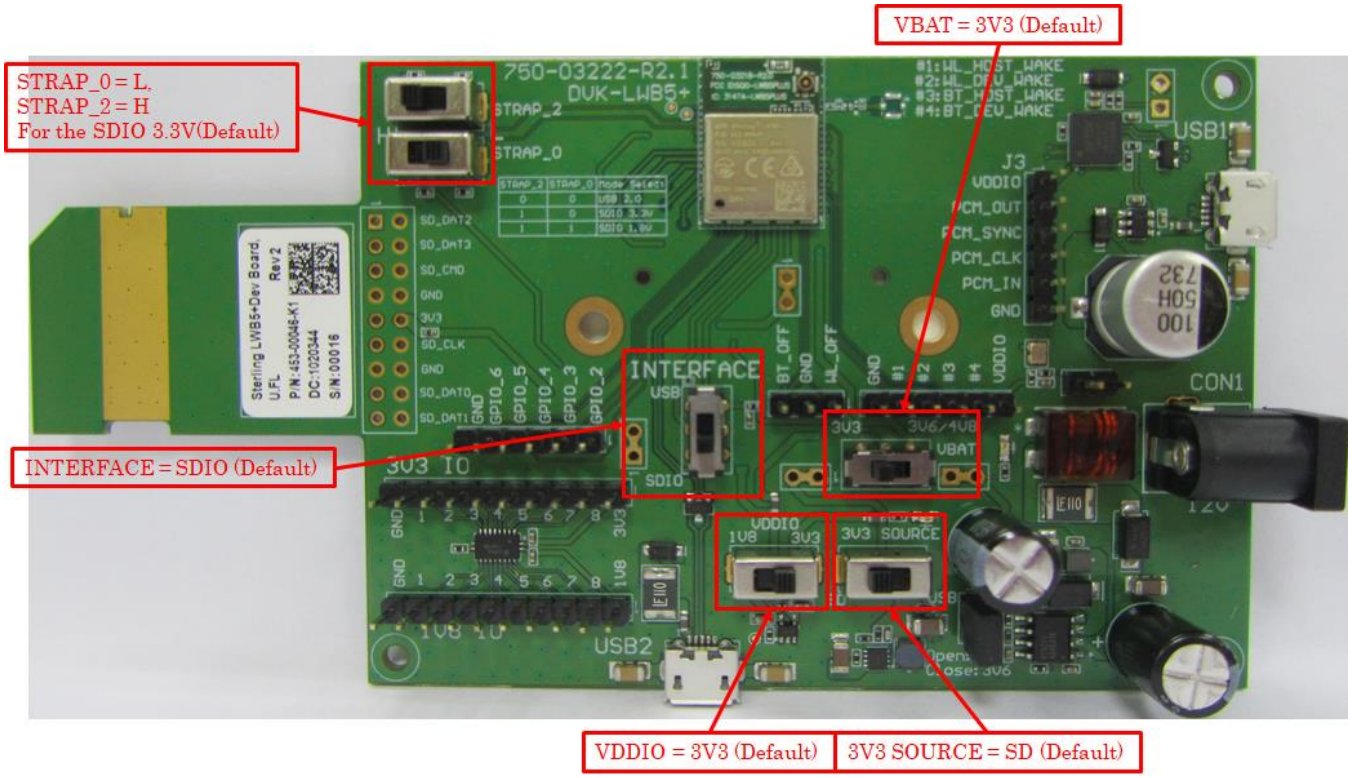

Figure 3: Out of box configuration

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5 FUNCTIONAL BLOCKS

5.1 Power Architecture

Figure 4 shows the Sterling LWB5+ development board power supply architecture.

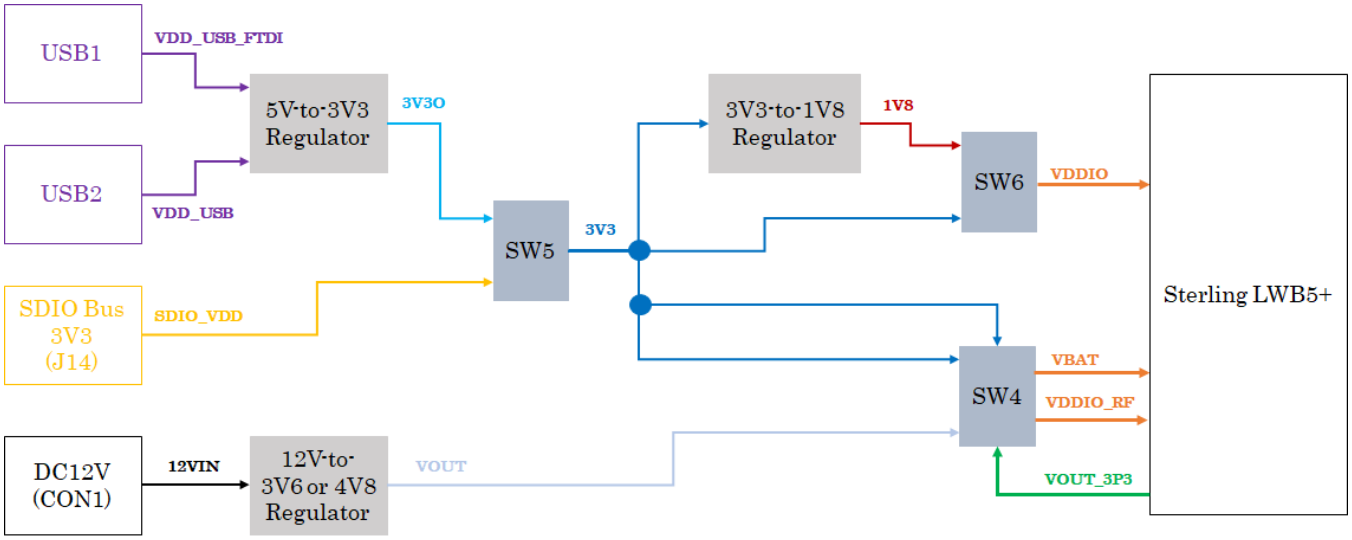

Figure 4: LWB5+ development board power architecture

The Sterling LWB5+ radio module requires two primary power sources that supply all other internal power rails – VBAT and VDDIO. The VDDIO source provides power for the radio IO portions, and the VBAT source provides power for all other radio needs. The VBAT source can operate on either a standard 3v3 rail or at higher voltage with slightly better RF characteristics.

The Sterling LWB5+ development board supports all power configurations. The VDDIO rail can be configured to come from either host interface (SDIO or USB). VDDIO is further configurable to operate at either 3v3 or 1v8 to match the host interface. The VBAT rail is either supplied by an on-board regulator from the selected host interface for 3.3V operation, or from an external 12V power supply for higher voltage operation. If the external supply is selected, a configurable on-board regulator supplies VBAT at either 3v6 or 4v8.

See Figure 5 and Figure 6 for an example of VBAT configured to operate from the external 12V power supply through the on-board regulator configured for 4v8.

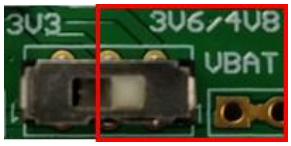

Figure 5: VBAT provided from external supply

Figure 6: VBAT external supply configuration (3v6 vs 4v8)

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5.2 Host Interface Mode

The Sterling LWB5+ radio module must be configured for one of three host interface modes that are selected by strapping options at the point the module powers up. The strapping options are implemented by SW2 and SW3 (labeled STRAP_0 and STRAP_2 respectively). In addition, SW1 (labeled Interface) must be configured to correspond with the selected strapping option to properly terminate internal USB reference voltage circuitry.

See Figure 7 for an example of the host interface configured for SDIO (1v8) / UART operation (SW1 is not shown).**Error! Reference source not found.**

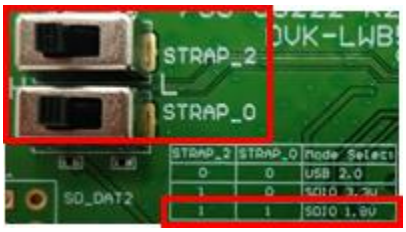

Figure 7: Strapping for SDIO (1v8) / UART

5.2.1 SDIO (3v3) / UART

The SDIO (3.3V) / UART configuration is used with SDIO 2.0 hosts with Wi-Fi on the SDIO interface and Bluetooth on the UART interface exposed by the uart-USB bridge at USB1. This configuration must not be used with SDIO3.0+ hosts that support and implement 1.8v UHS modes.

5.2.2 SDIO (1v8) / UART

The SDIO (1v8) / UART configuration is used with SDIO 3.0+ hosts with Wi-Fi on the SDIO interface and Bluetooth on the UART interface exposed by the uart-USB bridge at USB1. This configuration supports UHS-1 speed modes up to SDR104, in addition to the standard Full Speed/High Speed modes used by SDIO 2.0 hosts.

5.2.3 USB / USB

The USB / USB configuration supports both Wi-Fi and Bluetooth on the USB2 connector via a USB 2.0 hub internal to the LWB5+ module.

5.3 Miscellaneous

5.3.1 External Radio Control

The WL_REG_ON and BT_REG_ON signals on the LWB5+ module enable the Wi-Fi and Bluetooth radio circuitry respectively when pulled high. These pins are pulled high by default on the module but can be pulled low on the LWB5+ development board using the 1x3 pin header at J8. See Figure 8.

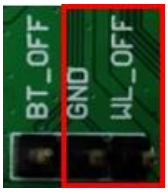

Figure 8: Wi-Fi / Bluetooth External Disable

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5.3.2 External 32.768 KHz Low-Power Oscillator

The Sterling LWB5+ module software is configured to use an external low power 32khz oscillator for optimized sleep mode timing. An external LPO is provided on the LWB5+ development board. This external oscillator allows lower power operation while in sleep mode than the corresponding internal LPO. The external LPO can be disabled with a jumper on J4 (see Figure 9**Error! Reference source not found.Error! Reference source not found.**) **but note that this mode is not supported by standard software. All designs must provide an external LPO for operation with the standard software release**.

Figure 9: External LPO configuration

5.3.3 GPIO Interface

There are five GPIOs available on the LWB5+ module and exposed on the development board (see Figure 10). These signals are not currently supported and are reserved for future use by radio firmware.

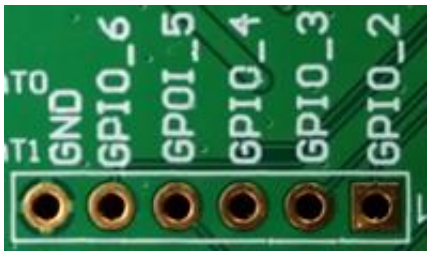

Figure 10: GPIO interface (reserved)

5.3.4 Wake Up Signals

The LWB5+ module supports host and device wake signals for both Wi-Fi and Bluetooth radios. These features require additional software support and configuration. Contact Laird for more details if these features are required.

Figure 11: Host/Device Wake

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5.3.5 PCM Interface

The LWB5+ Bluetooth radio can support a direct connection to an I2S/PCM interface on a host processor for offloading Bluetooth Audio from the host stack. This interface is exposed on the LWB5+ development board (see Figure 12). This feature requires additional software on the host platform and is not supported by default. Please contact Laird for more details if this feature is required.

Figure 12: PCM/I2S interface

5.3.6 Current Measurement

The Sterling LWB5+ development board provides several solder-bridge pads with headers to conduct current measurements. To measure current consumed by the LWB5+ module, cut the solder bridge pad then connect a current meter in series with the corresponding header. See Figure 13 for details.

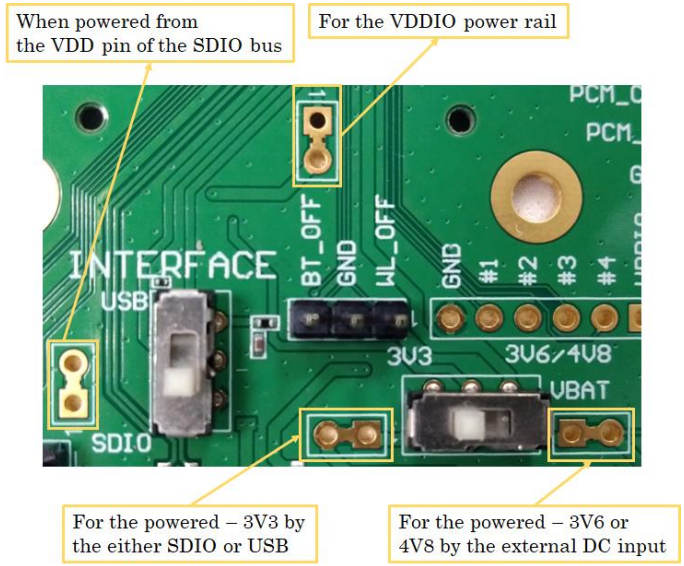

Figure 13: Current measurement points

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5.3.7 Bi-directional 8-Bit Voltage translator

The LWB5+ development board provides a bi-directional 8-bit voltage level shifter circuit that allows user connections to other circuits or applications. This circuit supports translation between 1.8V and 3.3V. See Figure 14 for details.

Note The /OE pin of this circuit is pulled low via a 10 K Ohm resister, so is configured for normal mode only. Tri-state mode is not supported.

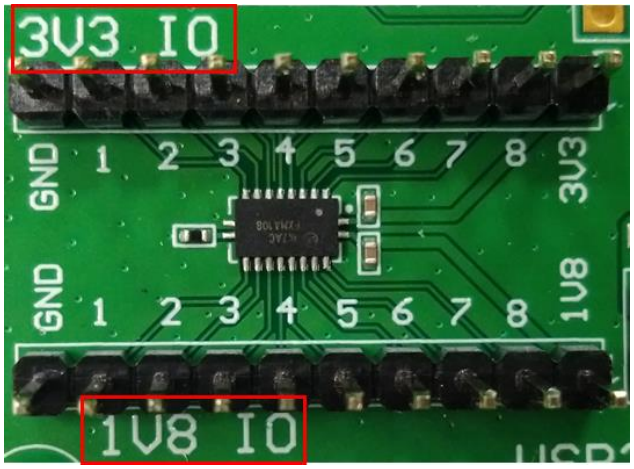

Figure 14: Level shifter circuit

6 Development Board Configuration

See Table 3 for the settings needed to properly setup each configuration supported by the Sterling LWB5+ development board.

Table 3 Development Board Configuration

Configuration	STRAP_2	STRAP_0	Interface	3v3 Source	VDDIO	VBAT	3V6/4V8
SDIO (1v8) / UART VBAT @ 3v3	H	H	SDIO	SD or USB	1V8	3V3	N/A
SDIO (1v8) / UART VBAT @ 3v6/4v8	H	H	SDIO	SD or USB	1V8	3V6/4V8	As needed
SDIO (3v3) / UART VBAT @ 3v3	H	L	SDIO	SD or USB	3V3	3V3	N/A
SDIO (3v3) / UART VBAT @ 3v6/4v8	H	L	SDIO	SD or USB	3V3	3V6/4V8	As needed
USB/USB VBAT @ 3v3	L	L	USB	USB	As needed	3V3	N/A
USB/USB VBAT @ 3v3	L	L	USB	USB	As needed	3V6/4V8	As needed

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7 Software

Software support for the LWB5+ family is available for Linux and Android. Please see the Laird GitHub site at https://github.com/LairdCP/Sterling-LWB-and-LWB5-Release-Packages/releases for the latest software release and associated documentation.

8 Additional Documentation

Laird offers a variety of documentation and ancillary information to support customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the product website at https://www.lairdconnect.com/wireless-modules/wifi-modules-bluetooth/sterling-lwb5-wifi-5-bluetooth-5-module#documentation. For additional questions, or to receive technical support for this Development Kit or for the Sterling LWB5+ module series, please contact Embedded Wireless Solutions Support at https://www.lairdconnect.com/resources/support

9 References

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