Hardware User Guide

Sterling LWB5+ M.2 Development Kit

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	08 Dec 2020	Initial version	Jacky Kuo Dean Ramsier	Jonathan Kaye

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1 INTRODUCTION

The LWB5+ M.2 Development Kit (DVK) is designed to support hardware integration, performance validation and software development for projects utilizing the Laird LWB5+ M.2 module. The DVK consists of an expansion board with an M.2 E-key connector, populated with an LWB5+ M.2 module. The LWB5+ M.2 module comes in two variants, one supporting Wi-Fi on SDIO and Bluetooth on UART, and the other supporting both Wi-Fi and Bluetooth on a shared USB 2.0 interface. The expansion board provides easy access to all interfaces on either module.

Data in this document is drawn from several sources and includes information found in the Laird Sterling LWB5+ Architecture Document, Cypress CYW4373 datasheet, and FTDI FT232R datasheet.

IMPORTANT: The information in this document is subject to change. Please visit the Sterling LWB5+ product page for the latest information

1.1 Related Documents

The following documents are available from the Sterling LWB5+ M.2 product page:

- Sterling LWB5+ M.2 Product Brief
- Sterling LWB5+ M.2 Datasheet

1.2 Kit Contents

Table 1: Product kit contents

Development board	This carrier board contains an M.2 E-key connector that supports either variant of LWB5+ M.2 module. SDIO and USB host interfaces are provided as well as headers that supply easy access to all M.2 interfaces.
LWB5+ M.2 module	The DVK includes either an SDIO/UART or a USB/USB LWB5+ M.2 variant populated in the development board M.2 connector
USB cable	Type A to Micro USB-AB. This cable is used for the following: ▪ Bluetooth connectivity via the FTDI USB-RS232 converter on the DVK when using the SDIO/UART LWB5+ M.2 variant ▪ Wi-Fi and Bluetooth connectivity when using the USB/USB LWB5+ M.2 variant
RF cable x2	SMA to MHF4 pigtail cable for conducted performance validation Laird P/N: CARSMF10RMHF4-001
RF antenna x2	External dipole antenna, Laird P/N: 001-0009
Jumper cap x3	Allows configuration using the various pin headers
Product insert card	Provides links to additional information including the Sterling LWB5+ M.2 user manual, firmware, application notes, schematics, quick start guides, and firmware release notes

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2 STERLING LWB5+ M.2 DEVELOPMENT KIT SPECIFICATIONS

Table 2: Development board specifications

Characteristic	Specifications
Configuration	Depends on LWB5+ M.2 module variant in use
Host Interfaces	▪ SDIO (Wi-Fi, when using LWB5+ M.2 SDIO/UART module variant) ▪ UART (Bluetooth, when using LWB5+ M.2 SDIO/UART module variant) This interface is exposed on a USB connector via an FTDI UART-USB bridge ▪ USB (Wi-Fi and Bluetooth, when using LWB5+ M.2 USB/USB module variant) ▪ PCM (Bluetooth audio)
Power supplies	DVK voltage is 3v3 provided by either ▪ SDIO host interface ▪ USB1/USB2 host interface **Note:** 3v3/1v8 VDDIO jumper must always be set to 1v8 in accordance with of the M.2 standard
Antenna gain	2.0 dBi peak gain on 2.4 GHz and 5 GHz
WakeUp signals	Wi-Fi ▪ WL_HOST_WAKE ▪ WL_DEV_WAKE Bluetooth ▪ BT_HOST_WAKE ▪ BT_DEV_WAKE
GPIOs	2 GPIOs reserved for future use
Dimension (mm)	97 x 69 x 12

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3 Sterling LWB5+ M.2 Development Kit – Main Development Board

The Sterling LWB5+ M.2 development kit is a fully featured evaluation platform for the Sterling LWB5+ series M.2 modules. It allows users to evaluate radio performance as well as create prototypes and application-specific designs.

The carrier board portion of the development kit supports both the SDIO/UART and the USB/USB LWB5+ M.2 module variants. These modules are powered by a 3v3 power rail provided by the selected host interface and contain on board antenna connectors. Headers on the carrier board provide easy access to key signals on the M.2 interface. An on-board level shifter circuit with headers allows external signals to be level shifted as needed.

3.1 Key Features

The Sterling LWB5-Plus-M.2 development board has the following features:

- Sterling LWB5-Plus-M.2 module populated in M.2 connector (either SDIO/UART or USB/USB variant)
- M.2 SDIO interface (with SDIO/UART M.2 card variant installed) exposed on standard full-size SDIO fingerboard connector
- M.2 UART interface (with SDIO/UART M.2 card variant installed) exposed on microUSB connector via FTDI USB/UART bridge (USB1)
- M.2 USB interface (with USB/USB M.2 card variant installed) exposed on micro USB connector (USB2)
- Powered by either SDIO or USB1/USB2 host interface
- Ability to hold either Wi-Fi or Bluetooth radio in reset via W_DISABLE1#/W_DISABLE2# M.2 interface signals (J10/J11/J1)
- LED for 3V3 source indication (LED3)
- Ability to measure LWB5+ M.2 module current (J5/SB1)
- IO break-out 2.54 mm pitch pin header connector (plated through-holes) that bring out all interfaces of the Sterling LWB5-Plus-M.2 card (J1, J2, J3)
  - PCM
  - GPIOs
  - Wakeup signals
  - W_DISABLEx#
- Bi-directional 8-bit voltage level shifter (3v3 <-> 1v8) for application/prototyping use (J7, J8)

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4 HARDWARE OVERVIEW

4.1 Block Diagram

Figure 1 shows the block diagram of the development kit.

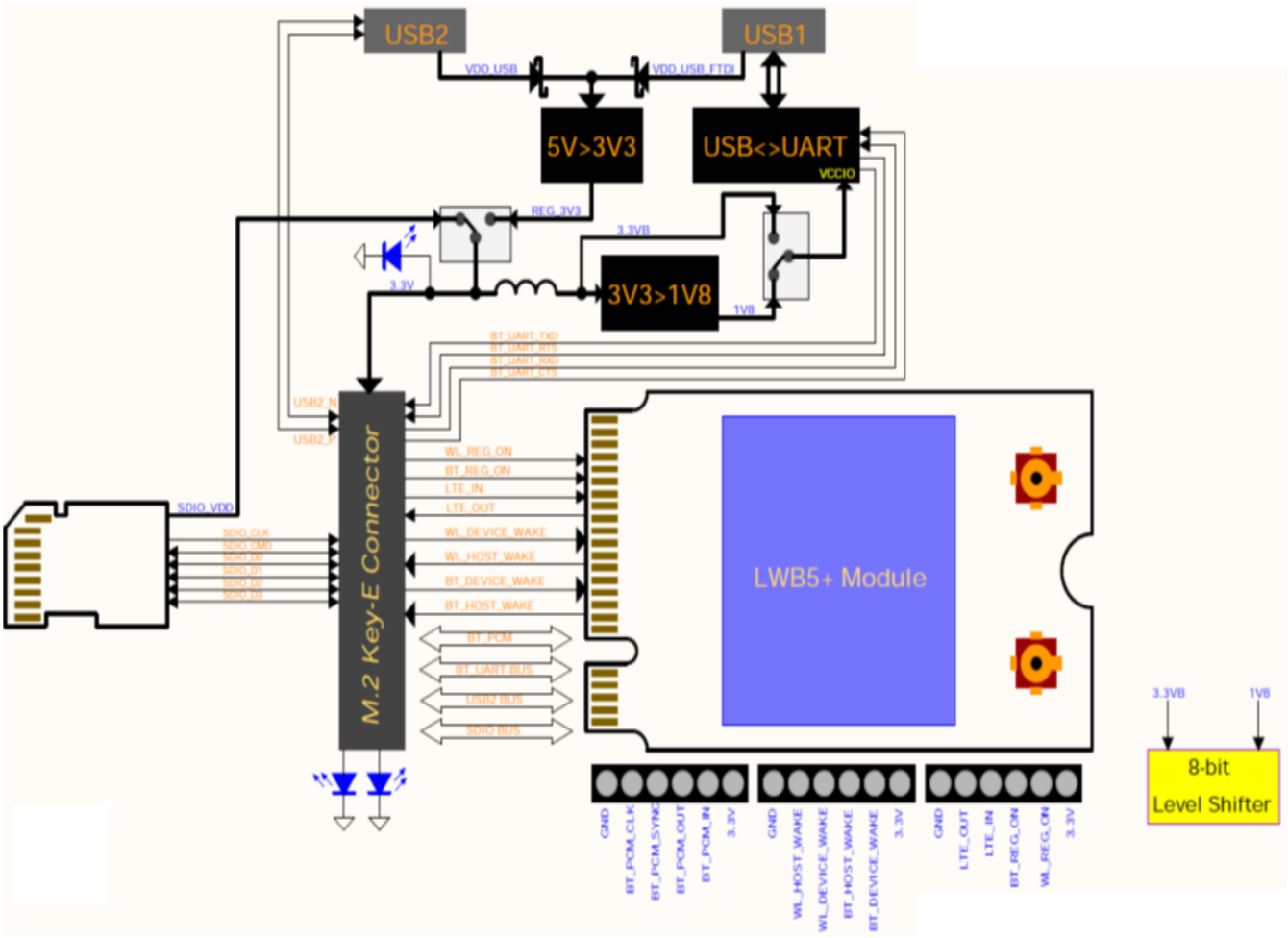

Figure 1: Sterling LWB5+ M.2 development kit block diagram

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4.2 Understanding the Development Board

The LWB5-Plus-M.2 development board supports both the SDIO/UART and USB/USB LWB5+ M.2 module variants. The M.2 module interface is configured by hardware strapping options on the LWB5+ M.2 module itself. It is important to know which M.2 module variant is installed on the development board, so the proper host interface is used.

4.2.1 LWB5+ M.2 SDIO/UART Module Variant

Figure 2 shows an LWB5+ M.2 SDIO/UART module variant with the hardware strapping resistors highlighted. If you don't know which variant M.2 module is installed in your LWB5+ M.2 DVK you can compare the highlighted resistor set with your board.

Important: The LWB5+ M.2 SDIO/UART variant is strapped for 1.8V IO operation because the M.2 interface requires 1.8V SDIO signalling. The required 1.8V VDDIO supply is generated locally on the M.2 module from the standard 3.3V power pins on the M.2 interface. The host platform must use 1.8v signals on the SDIO interface at all times.

Figure 2: Hardware strapping for the LWB5+ M.2 SDIO/UART variant

See Figure 3 for a detailed description of the development board components and configuration when used with the LWB5+ M.2 SDIO/UART module variant.

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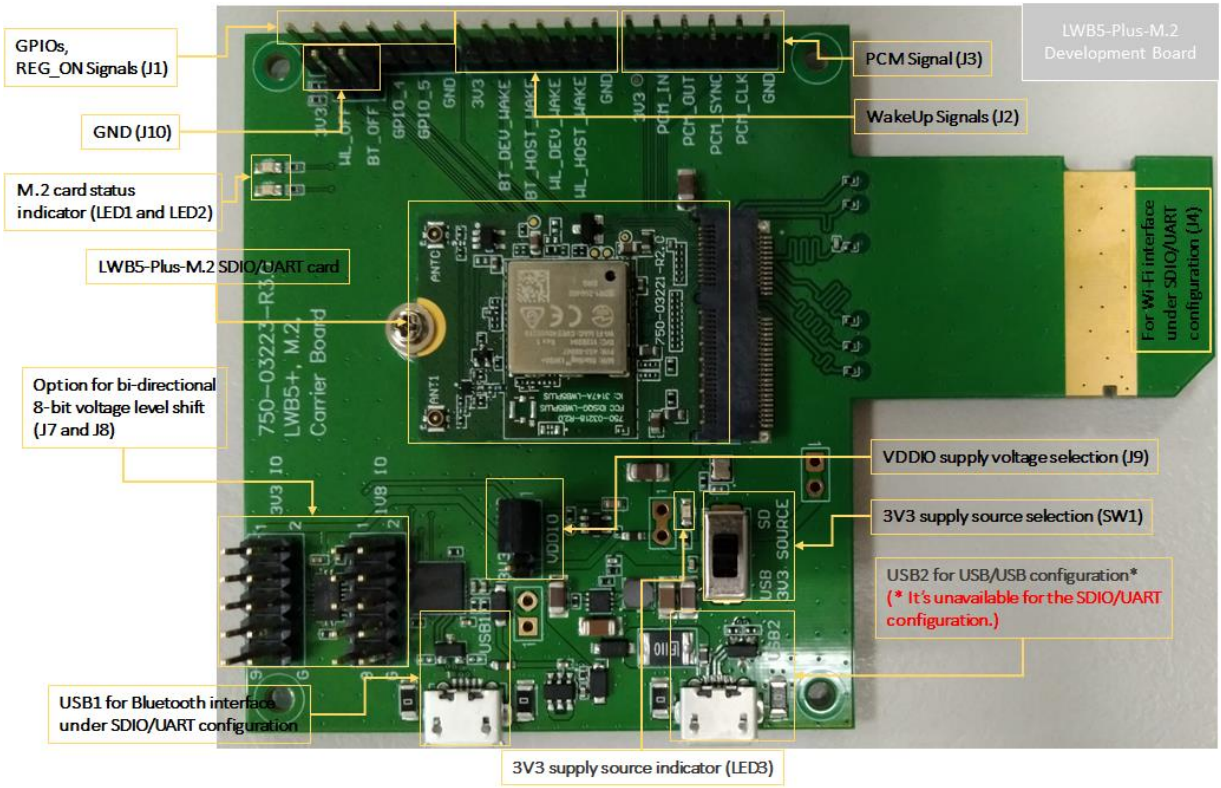

Figure 3: LWB5+ M.2 DVK with SDIO/UART module variant

4.2.2 LWB5+ M.2 USB/USB Module Variant

Figure 4 shows an LWB5+ M.2 USB/USB module variant with the hardware strapping resistors highlighted. If you don't know which variant M.2 module is installed in your LWB5+ M.2 DVK, you can compare the highlighted resistor set with your board.

Figure 4: Hardware strapping for the LWB5+ M.2 USB/USB variant

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See Figure 5 for a detailed description of the development board components and configuration when used with the LWB5+ M.2 USB/USB module variant.

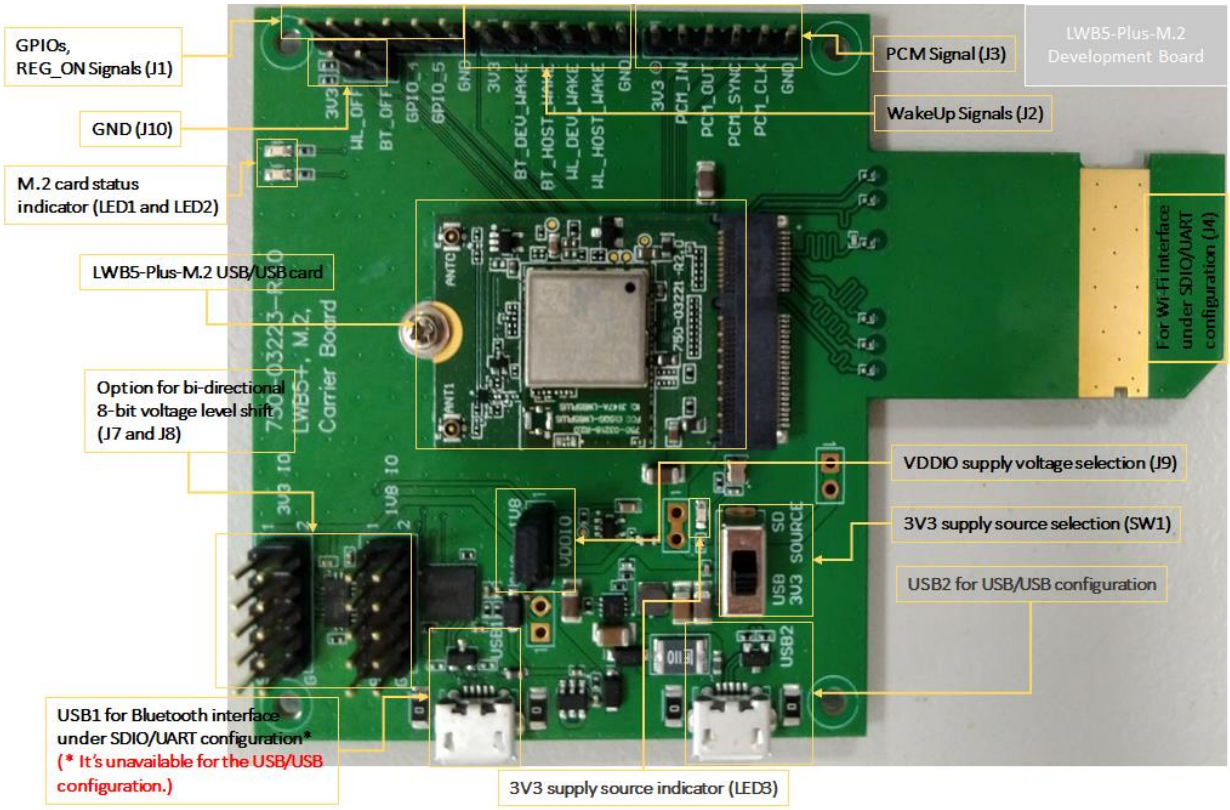

Figure 5: LWB5+ M.2 DVK with USB/USB module variant

4.3 Switches and Connectors

Table 3: Connectors, configuration switches, and jumpers

Component	Description
J4	SDIO interface dedicated to Wi-Fi when using the LWB5+ M.2 SDIO/UART variant
USB1	UART interface (via Serial/USB bridge) dedicated to Bluetooth when using the LWB5+ M.2 SDIO/UART variant
USB2	USB interface supporting both Wi-Fi and Bluetooth when using the LWB5+ M.2 USB/USB variant
SW1	3V3 supply source selection (SDIO or USB host interface as appropriate)
J9	Selects VDDIO used by FTDI bridge for BT UART signals. **This jumper must always be set for 1.8V**
J5	Current measurement header for main M.2 3v3 power rail
J1	Header exposing GPIO_4/5, and WiFi/BT REG_ON
J2	Header exposing Wi-Fi and Bluetooth wakeup signals
J3	Header exposing Bluetooth PCM interface
J10	W_DISABLE1# allows Wi-Fi radio to be held in reset via WL_REG_ON if jumper is installed
J11	W_DISABLE2# allows Bluetooth radio to be held in reset via BT_REG_ON if jumper is installed
LED1	3V3 power supply indicator
LED2, LED3	Not supported
J7, J8	Bi-directional 8-bit voltage translation between 3v3 and 1v8

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4.4 Default Configuration

Please see Figure 6 for the correct configuration supporting the LWB5+ M.2 SDIO/UART variant. See Figure 7 for the correct configuration supporting the LWB5+ M.2 USB/USB variant.

Important! These configurations require that the host provides sufficient power for radio operation via the selected host interface.

Important! The LWB5+ M.2 SDIO/UART variant requires that the SDIO interface operate only at 1.8V. The module will not operate properly if the host enumerates the module at 3.3V.

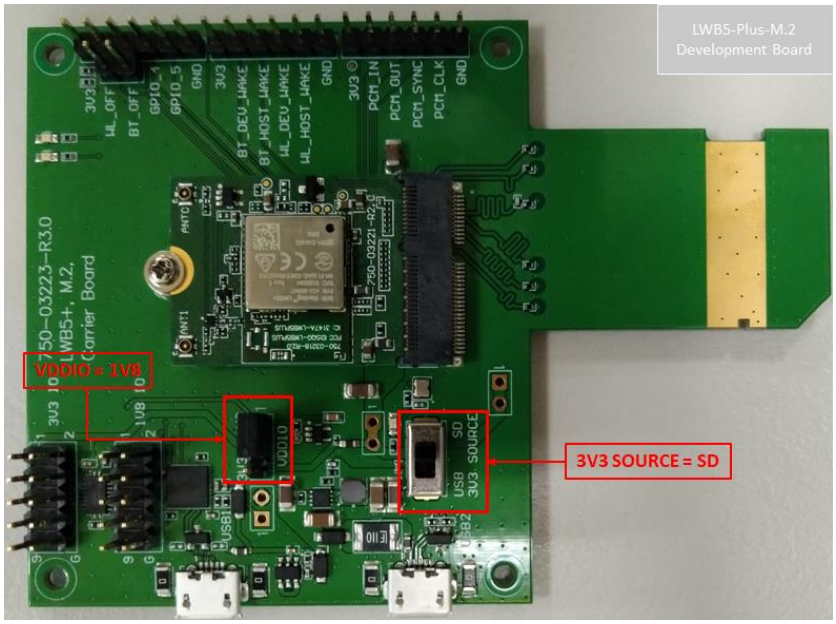

Figure 6: Configuration for LWB5+ M.2 SDIO/UART module variant

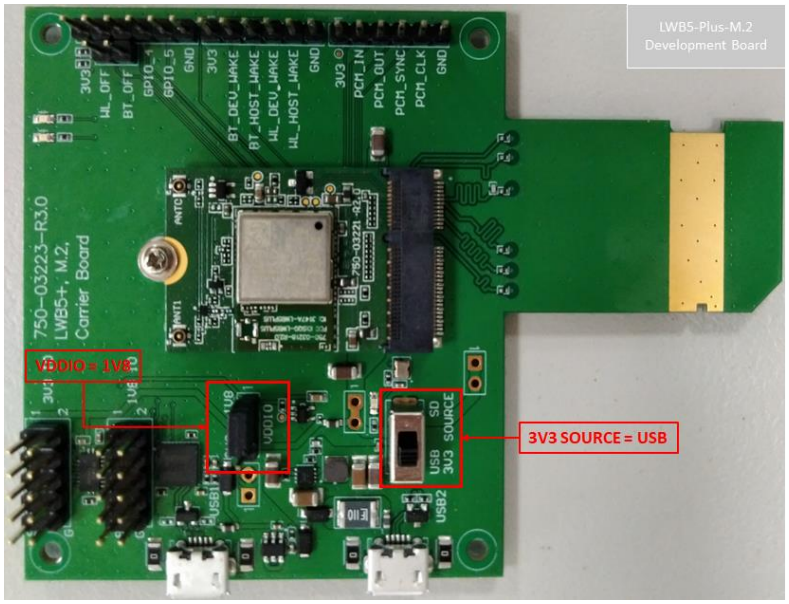

Figure 7: Configuration for LWB5+ M.2 USB/USB module variant

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5 FUNCTIONAL BLOCKS

5.1 Power Architecture

Figure 8 shows the LWB5+ M.2 development board power supply architecture.

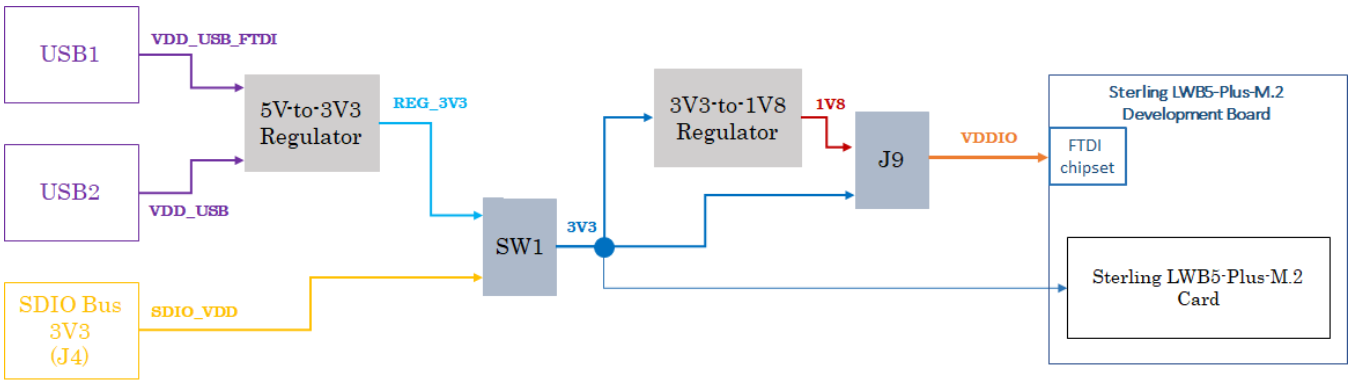
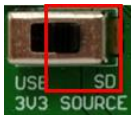


Figure 8: LWB5+ M.2 development board power architecture

The LWB5+ M.2 development board is powered from the host platform via one of the host interfaces (SDIO, USB1, or USB2). The selected interface is used to provide the required M.2 3v3 power rail. The VDDIO rail to the FTDI bridge is configurable for either 1v8 or 3v3, however this selection is for internal use only and must always be set for 1v8. The 3v3 setting is not compatible with an unmodified LWB5+ M.2 module.

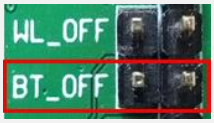
Table 4: Power configuration

Switch Designator	LWB5+ M.2 Module Variant	Position	Powering Port
SW1	SDIO/UART		SDIO
	USB/USB		USB1/USB2

5.2 External Radio Control

The W_DISABLE1# AND W_DISABLE2# signals on the M.2 interface hold the LWB5+ Wi-Fi and Bluetooth radios respectively in reset when asserted. These signals are pulled high by default but can be asserted by applying a jumper to the WL_OFF or BT_OFF headers (J10 and J11) on the LWB5+ M.2 development board. These headers should be left open for normal operation.

Table 5: External radio control

Signal	Pin Header	Description
WL_OFF		Jumper WL_OFF to hold Wi-Fi radio in low power reset
BT_OFF		Jumper BT_OFF to hold Bluetooth radio in low power reset

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5.3 External 32.768 KHz Low-Power Oscillator

The Sterling LWB5+ module firmware is configured to use an external low power 32KHz oscillator for optimized sleep mode timing. The LWB5+ M.2 module gets this required signal from the SUSCLK pin on the M.2 interface. This external oscillator allows lower power operation while in sleep mode than the corresponding internal LPO. **All designs must provide an external LPO for operation with the standard software release.**

5.4 GPIO Interface

The LWB5+ M.2 module exposes two GPIOs on the M.2 interface and are available on the LWB5+ M.2 development board (see Figure 9). These signals are not currently supported and are reserved for future use by radio firmware.

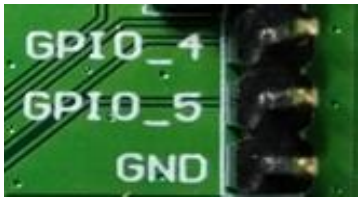

Figure 9: GPIO interface (reserved)

5.5 Wake Up Signals

The LWB5+ M.2 module supports host and device wake signals for both Wi-Fi and Bluetooth radios. These features require additional software support and configuration. Contact Laird Connectivity for more details if these features are required.

Figure 10: Host/device wake

5.6 PCM Interface

The LWB5+ M.2 Bluetooth radio can support a direct connection to an I2S/PCM interface on a host processor for offloading Bluetooth Audio from the host stack. This interface is exposed on the LWB5+ development board (see **Error! Reference source not found.**). This feature requires additional software on the host platform and is not supported by default. Please contact Laird for more details if this feature is required.

Figure 11: PCM/I2S interface

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5.7 Current Measurement

The LWB5+ M.2 development board provides solder-bridged through hole pads to conduct current/power measurements. To measure current consumed by the LWB5+ M.2 module, cut the solder bridge pad then connect a current meter in series with the pads. See Figure 12 for details.

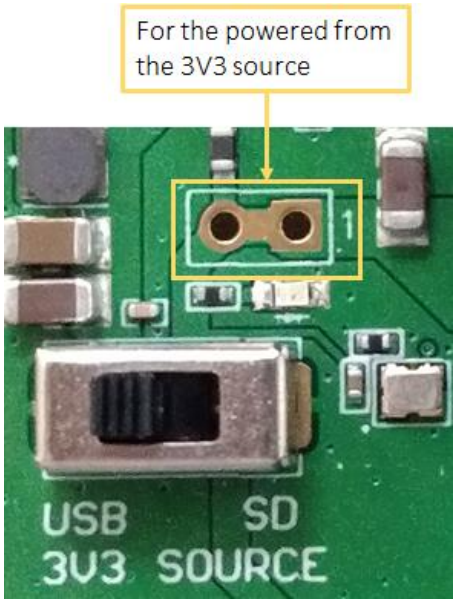

Figure 12: Current consumption measurement points

5.8 Bi-directional 8-Bit Voltage translator

The LWB5+ M.2 development board provides a bi-directional 8-bit voltage level shifter circuit that allows user connections to other circuits or applications. This circuit supports translation between 1.8V and 3.3V. See Figure 13 for details.

Note: The /OE pin of this circuit is pulled low via a 10 K Ohm resister, so is configured for normal mode only. Tri-state mode is not supported.

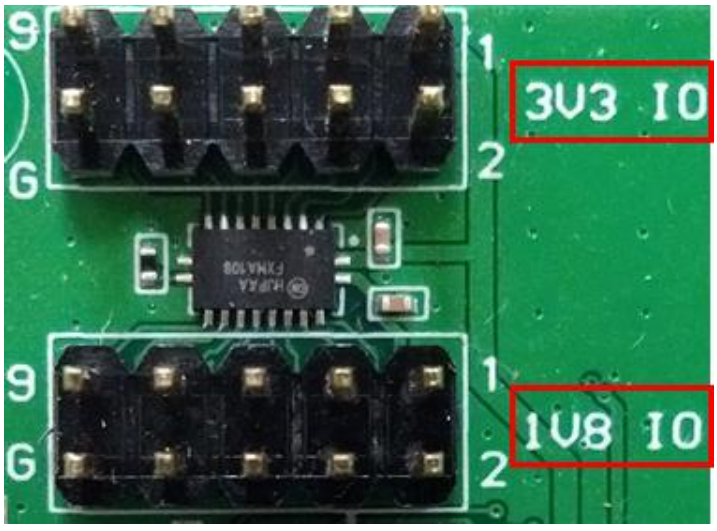

Figure 13: Level shifter circuit

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6 SOFTWARE

Software support for the LWB5+ family is available for Linux and Android. Please see the Laird GitHub site at https://github.com/LairdCP/Sterling-LWB-and-LWB5-Release-Packages/releases for the latest software release and associated documentation.

7 ADDITIONAL DOCUMENTATION

Laird offers a variety of documentation and ancillary information to support customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the product website at https://www.lairdconnect.com/wireless-modules/wifi-modules-bluetooth/sterling-lwb5-wifi-5-bluetooth-5-module#documentation. For additional questions, or to receive technical support for this Development Kit or for the Sterling LWB5+ module series, please contact Embedded Wireless Solutions Support at https://www.lairdconnect.com/resources/support

8 REFERENCES

1. CYW4373, Single-Chip Dual Band WiFi IEEE 802.11 a/b/g/n/ac MAC/Baseband/Radio with Integrated Bluetooth 5.0 datasheet, 002-18123 Rev. *F, Cypress Semiconductor Corporation.
2. FXLA108, Low-Voltage Dual-Supply 8-Bit Voltage Translator datasheet, Rev. 1.0.5, On Semiconductor Corporation.
3. TLV62065, 2-A 3-MHz Step-Down Converter datasheet, SLVSAC4B, TEXAS Instruments Incorporated.
4. TPS79718, 50-mA Low-Dropout Linear Regulators datasheet, SLVS332J, TEXAS Instruments Incorporated.
5. FT232R, USB UART IC datasheet, FT_000053, Future Technology Devices International Limited.

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