User Guide

BL654PA Development Kit

Part # 455-00022 and 455-00023

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	20 Aug 2019	Initial version	Raj Khatri	Jonathan Kaye

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1 Overview

The Laird BL654PA Development Kit provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Bluetooth Low Energy (BLE) plus Near Field Communication (NFC) applications.

The Laird BLE development kit is designed to support the rapid development of applications and software for the BL654PA series of BLE modules featuring Laird's innovative event driven programming language – *smart*BASIC. More information regarding this product series including a detailed module user's guide and *smart*BASIC user guides are available on Laird's BL654PA product page: https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl654-pa-series

This document is applicable to the version of development board which has PCB silk screen text DVK-BL654PA-R2.0.

2 Laird BL654PA Development Kit Part Numbers

Part Number	Product Description
455-00022	Development Kit for 453-00020 module – Integrated antenna
455-00023	Development Kit for the 453-00021 module – External antenna

Applicable to the following BL654PA module part numbers:

Part Number	Product Description
453-00020R or C	Bluetooth v5 PA module – Integrated antenna
453-00021R or C	Bluetooth v5 PA module – External antenna

3 Package Contents

All kits contain the following items:

Development Board	The development board has the required BL654PA module soldered onto it and exposes all available hardware interfaces.
Power Options	▪ USB cable – Type A to micro type B. The cable also provides serial communications via the FTDI USB – RS232 converter chip on the board. ▪ DC barrel plug for connection to external power supply (5.5 VDC max) ▪ 3x AAA battery holder fitted on underside of development board ▪ Coin-cell holder (powers module only) fitted on underside of development board
Two-pin jumpers for pin headers (5)	Five jumpers for 2.54 mm pitch headers used on BL654PA development board.
Fly leads (6)	Supplied (1 by 1 female to female jumper cable) to allow simple connection of any BL654PA module pins (available on plated though holes or headers on J44, J47, J48, J41, J29, J1, J12, J1, J5, J17, J21, J6 and J36).
External BLE antenna	Supplied with development kit part # 455-00023 only. External antenna, 2 dBi, FlexPIFA (Laird part #001-0022) with integral RF coaxial cable with 100 mm length and IPEX-4 compatible RF connector.
External NFC antenna	Laird NFC flexi-PCB antenna – Part # 0600-00061

4 BL654PA Development Kit – Main Development Board

This section describes the BL654PA development board hardware. The BL654PA development board is delivered with the BL654PA series module loaded with integrated *smart*BASIC runtime engine firmware but no onboard *smart*BASIC; because of this it starts up in AT command mode by default.

Applications in *smart*BASIC are simple and easy to develop for any BLE application. Sample *smart*BASIC applications scripts are available to download from the Laird GitHub repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications.

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The BL654PA development board is a universal development tool that highlights the capabilities of the BL654PA module. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers several header connectors that help isolate on-board sensors and UART from the BL654PA module to create different configurations. This allows you to test different operating scenarios.

The board allows the BL654PA series module to physically connect to a PC via the supplied USB cable for development purposes. The development board provides USB-to-Virtual COM port conversion through a FTDI chip – part number FT232R. Any Windows PC (XP or later) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from http://www.ftdichip.com/Drivers/VCP.htm

4.1 DVK-BL654 and DVK-BL654PA Differences

The DVK-BL654PA development board is identical to the DVK-BL654 development board but with one modification – the PCB footprint added for the BL654PA module.

Since the BL654PA module operating voltage range is 3.0V to 5.5V (whilst the BL654 is 1.8V to 5.5V), the following power selection switch positions **cannot be used** on the DVK-BL654PA.

- SW5 1.8V (silkscreen *1V8*) position cannot be used for DVK-BL654PA.

  SW5 default and ONLY valid position on DVK-BL654PA is marked with silkscreen **3V3**.

  Alternatively, you have the option to inject external supply voltage anywhere between 3.0V to 3.6V (for BL654PA) for the Normal Voltage mode via J8pin1 and GND of external supply on any DVK GND location pin for example TP14.

- SW8 2.5V (silkscreen **2V5**) position cannot be used for DVK-BL654PA.

  SW8 default and ONLY valid position on DVK-BL654PA is marked with silkscreen “AAA_5V5”.

  Alternatively, you have the option to inject external supply voltage anywhere between 3.0V to 5.5V (BL654PA) for the High Voltage mode via J28 pin1 and GND on J28pin2.

- J34 Coin cell holder and SW6 coin cell (silkscreen **coin-cell**) position cannot be used for DVK-BL664PA.

  Since the BL654PA module is high power module, coin cell (CR2032) operation is not possible (due to higher current draw) and therefore coin cell holder J34 cannot be used on DVK-BL654PA.

4.2 Key Features

The BL654PA development board has the following features:

- BL654PA series module soldered onto the development board
- The following power supply options for powering the development board:
  - USB (micro-USB, type B)
  - External DC supply (3.5-5.5V)
  - AAA batteries (three AAA battery holder fitted on underside of development board)
  - USB (micro-USB, type B) – For direct use of BL654PA USB interface as well
- Powering the BL654PA module in Normal Voltage mode (OPTION1) via selection switch (SW7). Regulated 3.3V or Regulated 1.8V via selection switch (SW5). **For DVK-BL654PA SW5 default and ONLY valid position is “3V3”(silkscreen).**

  Option to inject external supply voltage anywhere between 3.0V to 3.6V (for BL654PA) for the Normal Voltage mode (via J8pin1 and GND of external supply on any DVK GND location pin for example TP14).
- Powering the BL654PA module in High Voltage mode (OPTION2) via selection switch (SW7). Regulated 2.5V or 4.5V (from 3x AAA battery – 4.5V) via selection switch (SW8). **For DVK-BL654PA SW8 default and ONLY valid position is “AAA_5V5” (silkscreen).**

  Option to inject external voltage anywhere between 3.0V to 5.5V (for BL654PA) for the High Voltage mode (via J28).
- Coin-cell Power supply option for coin-cell (CR2032) operation of the BL654PA module **not possible** (J34 coin-cell holder cannot be used on DVK-BL654PA).
- USB to UART bridge (FTDI chip)
- BL654PA UART can be interfaced to:
  - USB1 (PC) using the USB-UART bridge (FTDI chip)
  - External UART source (using IO break-out connectors J1 – No-Pop, Plated Through Holes) when the development board is powered from a DC jack or AAA batteries) or from USB1 (when jumper fitted in J35).

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  - Atmel MCU by use of an analog switch to route the BL654PA UART (for those customers working with Nordic SDK). USB2 to Atmel to Atmel UART (via open solderbridges) to BL654PA UART.
- Current measuring options (BL654PA module only):
  - Pin header (Ammeter)
  - 10R Series resistor for differential measurement (oscilloscope)
- IO break-out 2.54 mm pitch pin header connectors (plated through-holes) that bring out all interfaces of the BL654PA module – UART, SPI, QSPI, I2C, SIO [DIO or AIN (ADCs)], PWM, FREQ, NFC – and allow for plugging in external modules/sensors.
- Pin headers jumpers that allow the on-board sensors (I2C sensor, LEDs) to be disconnected from BL654PA module (by removing jumpers).
- Four on-board sensors:
  - Analog output temperature sensor via header in series (no jumper by default)
  - I2C device (RTC chip U16) via headers in series (no jumper by default)
  - SPI device (EEPROM)
  - QSPI device (Flash IC) via open solderbridges (by default)
- Four buttons and four LEDs for user interaction
- One reset button (via an analog switch)
- NFC antenna connector on-board development board for use with supplied flexi-PCB NFC antenna
- *Optional* external 32.768 kHz crystal oscillator and associated load capacitors. Not required for operation of the BL654PA; is disconnected by open solder bridges by default.
- *Optional* external serial (QSPI) flash IC. Not required for operation of the BL654PA; is disconnected by open solder bridges by default.
- Access to BL654PA JTAG – also known as Serial Wire Debug (SWD)
- On-board SWD (JTAG) programmer circuitry (USB2 to BL654PA module SWD interface)
- *smart*BASIC runtime engine FW upgrade capability:
  - Via UART (using the FTDI USB1-UART)
  - Via SWD (USB2 to BL654PA SWD) using on-board JTAG programmer circuitry on the BL654PA Development Kit
- *smart*BASIC application upgrade capability:
  - Via UART (using the FTDI USB-UART)
  - Via OTA (Over-the-Air)

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5 Understanding the Development Board

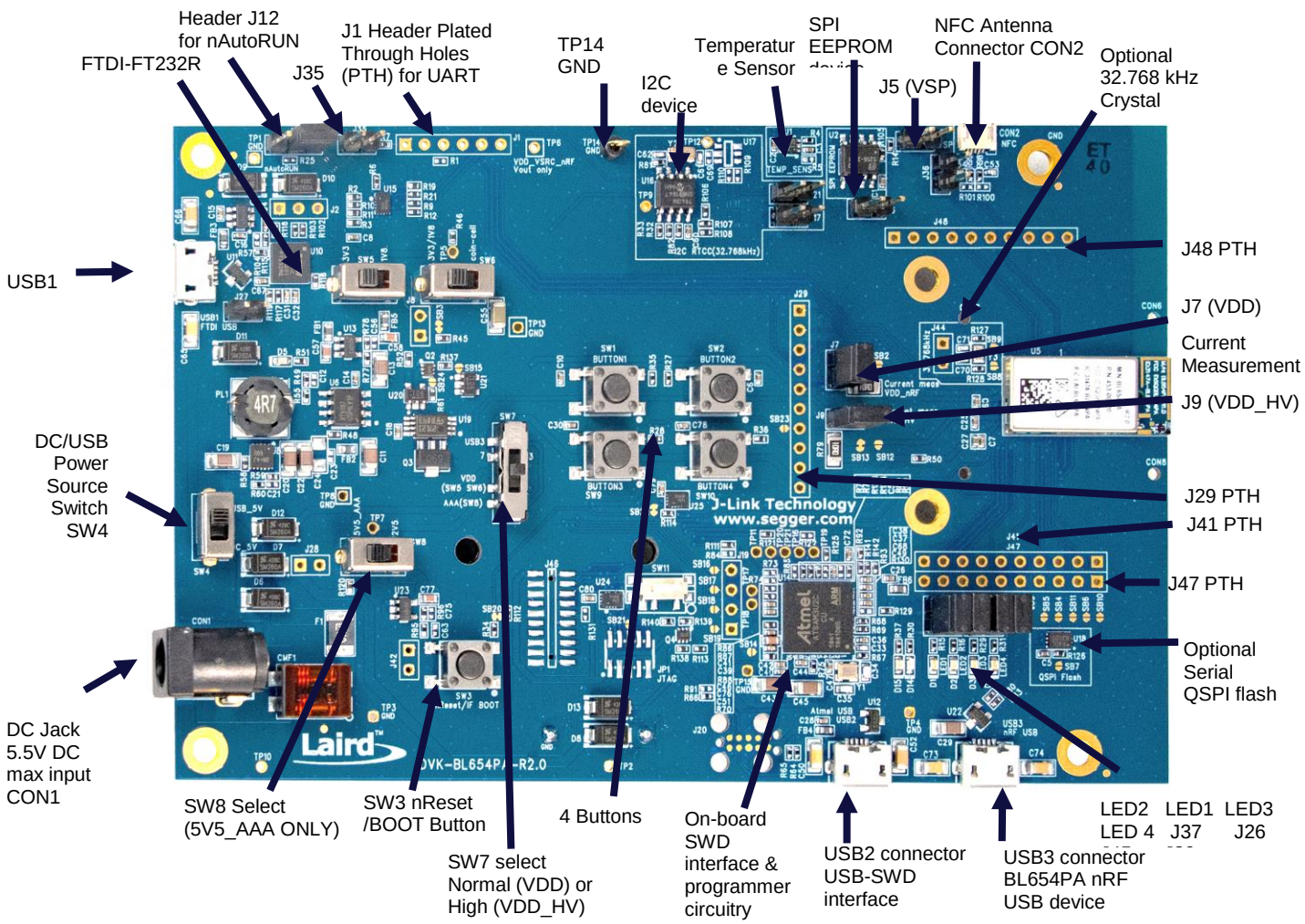

Figure 1: Dev board contents and locations

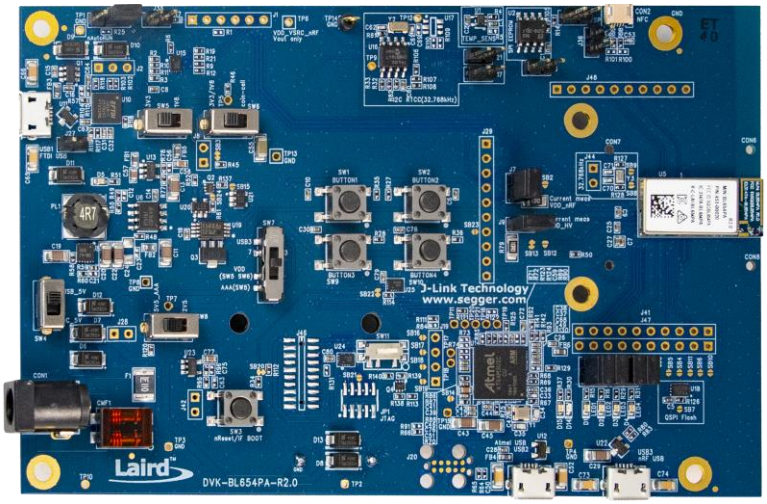

Figure 2: Development board 455-00022 (fitted with 453-00020 BLE module with integrated antenna)

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5.1 BL654PA Default Configuration and Jumper Settings

Important! To ensure correct out-of-the-box configuration, the **BL654PA** development board switches and jumpers must be configured as shown in

J12 Fit Jumper on Pins 2 & 1	SW5 default and ONLY position (3V3)	SW6 default and ONLY position (3V3/1v8)	TP14 Black Test Hook

Figure 3.

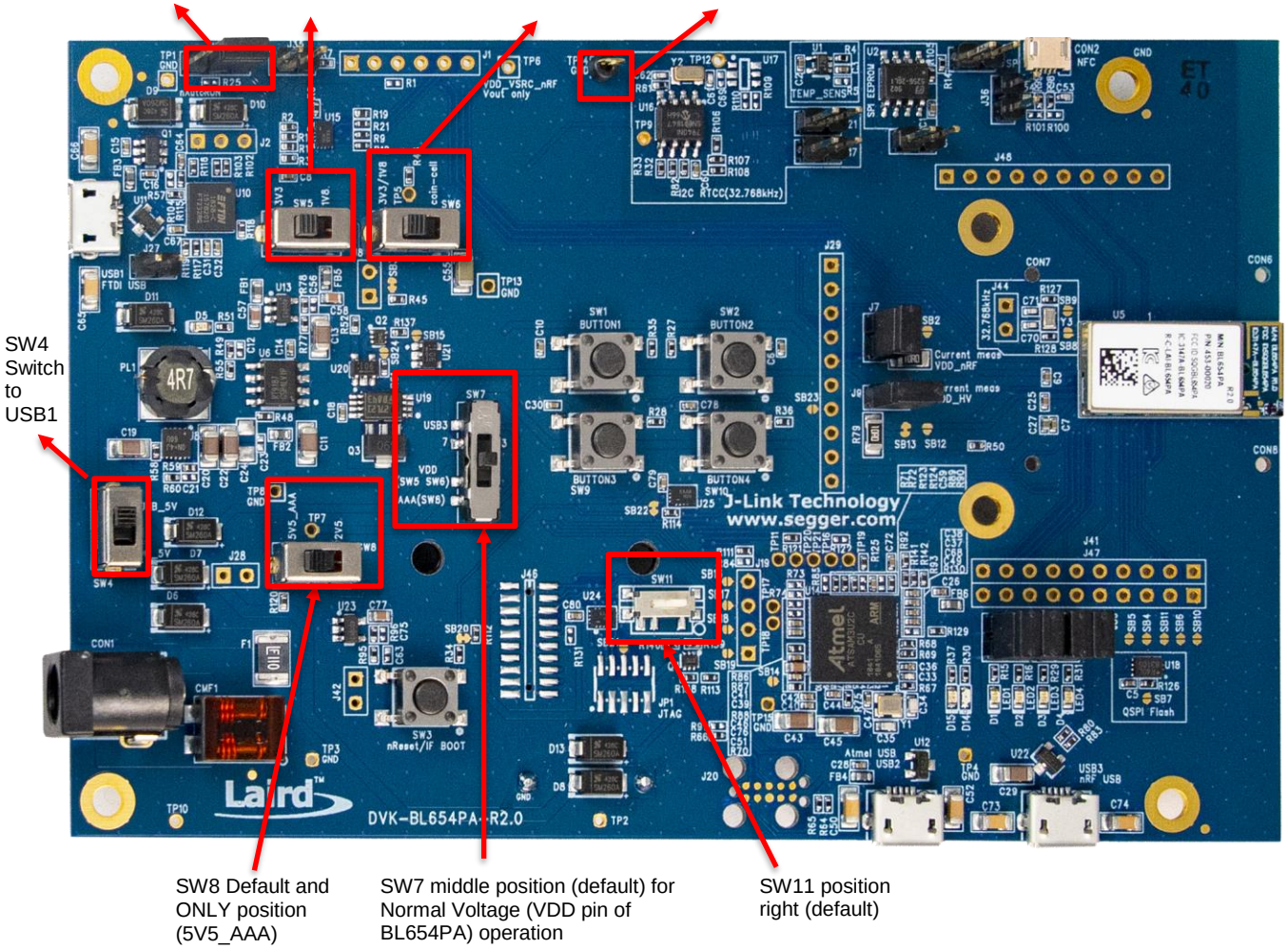

Figure 3: Correct BL654PA DVK board (455-00022 or 455-00023) jumper and switch settings - 455-00022 pictured

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6 Functional Blocks

6.1 Power Supply

Figure 4 shows the BL654PA development board Power Supply block.

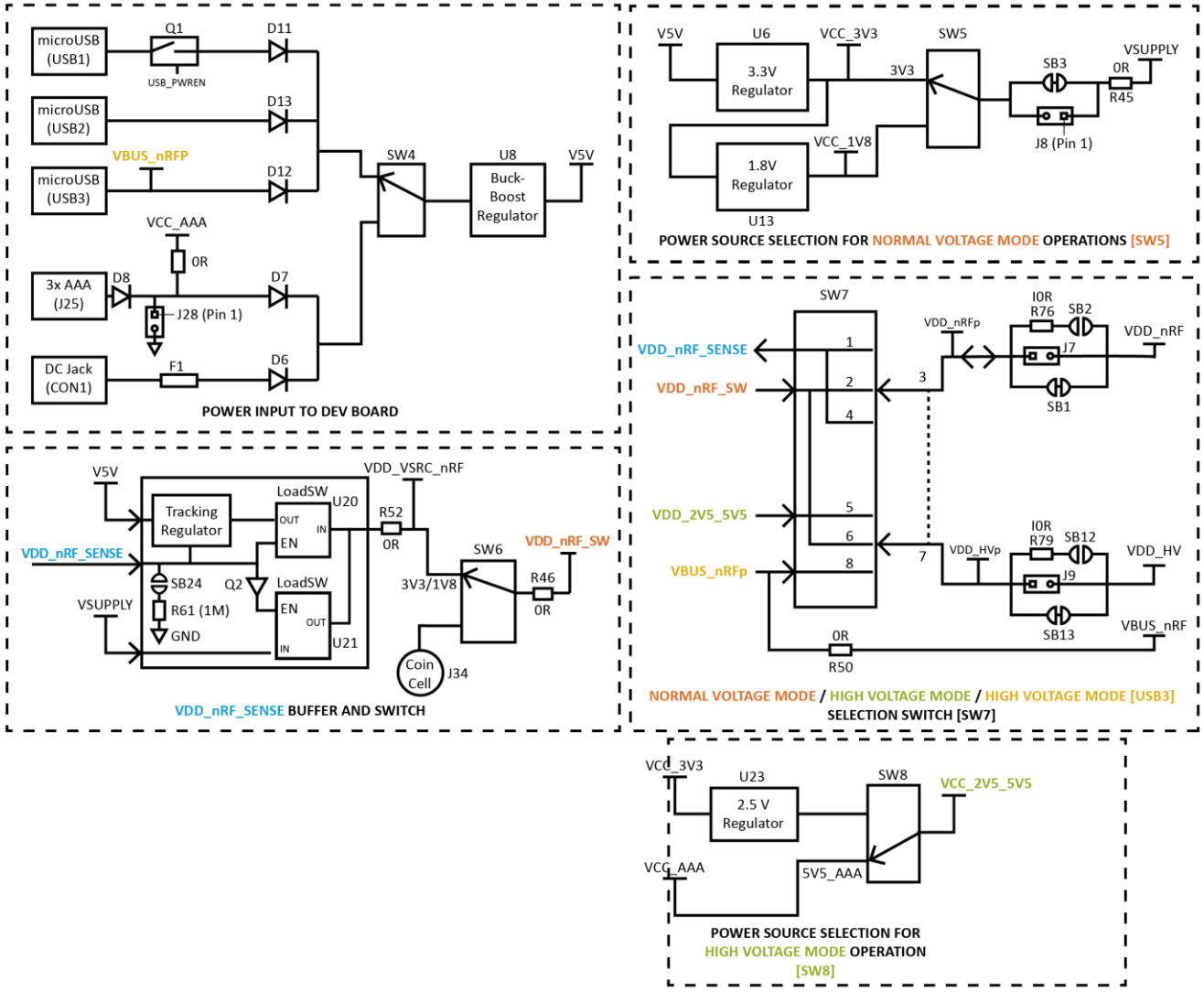

Figure 4: BL654PA development board power supply

Note: DVK-BL654PA SW8 default and only valid position is *5V5_AAA*. SW8 position *2V5* is invalid.
DVK-BL654PA SW5 default and only valid position is *3V3*. SW5 position *1V8* is invalid.
DVK-BL654PA SW6 default and only valid position is *3V3/1V8*. SW6 position *coin-cell* is invalid.

There are five options for powering the development board:

- USB1 USB type micro-B connector – If it requires the FTDI USB1-UART (BL654PA) path
- USB2 USB type micro-B connector – If it requires the Atmel USB2-SWD (BL654PA) path
- USB3 USB type micro-B connector – If it requires the USB3 to USB (BL654PA) path
- External DC supply (2.5V-5.5V), into DC jack connector (CON1),
- AAA batteries – Three AAA (4.5V) battery holder (J25) fitted on underside of development board

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The external power sources are fed into selection switch SW4 which allows a selection between either USB sources or the DC jack/AAA.

All the external power sources listed above are buck-boost regulated to a fixed 5V on the development board.

The BL654PA module has the following power supply pins:

- VDD pin (operating range of 3.0V to 3.6V) – Used for Normal Voltage mode
- VDD_HV pin (operating range of 3.0V to 5.5V) – Used for High Voltage mode
- VBUS pin (operating range of 4.35V to 5.5V) – Used for BL654PA USB mode

It can be powered in the following ways:

- **Option 1 – Normal voltage mode operation**

  Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within a 3.0V to 3.6V range to the BL654PA VDD and VDD_HV pins.

  For normal voltage mode operation, the BL654PA development board power supply section generates the following:
  - Regulated 3.3V
  - Regulated 1.8V (SW5 position *1V8* cannot be used for BL654PA)

  and then via selection switch SW5 (default is 3.3V position).

  Note: For the DVK-BL654PA, SW5 position *1V8* is not valid.

- **Option 2 – High voltage mode operation**

  High voltage mode power supply mode (using BL654PA VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within a 3.0V to 5.5V range to the BL654PA VDD_HV pin. Leave the BL654PA VDD pin unconnected.

  For high voltage mode operation, the BL654PA development board power supply section generates the following:
  - Regulated 2.5V (SW8 position *2V5* cannot be used for BL654PA)
  - 3 x AAA generated 4.5V (or inject external voltage into J28pin1 up to 5.5V)

  and then via selection switch SW8 (default and only valid position is *5V5_AAA*), you can select whether to use 2.5V or 4.5V.

  Note: For the DVK-BL654PA SW8 position *2V5* is not valid.

- **Option 3 – High voltage mode with voltage via USB3**

  For either high voltage option, if you use the BL654PA USB interface, the BL654PA VBUS pin must be connected to an external supply within the range of 4.35V to 5.5V.

The BL654PA development board power supply section is designed to cater to the options above. Follow these steps:

1. Set SW7 – Select one of the following three positions:
   - High voltage mode operation and BL654PA USB (connect USB cable to USB3 connector) – Top position. Source from USB3.
   - Normal voltage mode operation – Middle position (default). Source from SW5.
   - High voltage mode operation – Bottom position. Source from SW8.
2. Depending on chosen SW7 position, select one of the following three positions:
   - Plug in USB cable into USB3 – If SW7 is set to top position.
   - SW5 (either 3.3V or 1.8V) – Default and only position for SW5 on *3V3* position for BL654PA. If SW7 set to middle position.
   - SW8 – either 2.5V or 4.5V (3xAAA) – Default and only position on SW8 is *5V5_AAA* for BL654PA position. If SW7 set to bottom position.

Table 1 summarises the dev-board on-board power sources and switch positions.

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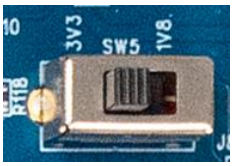
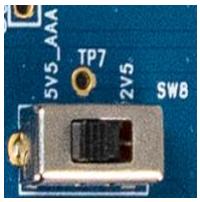
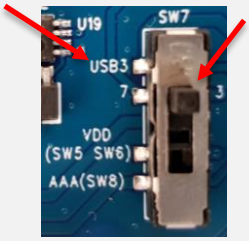
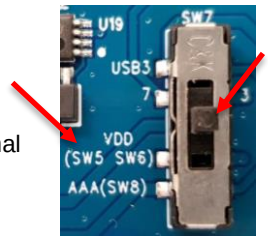
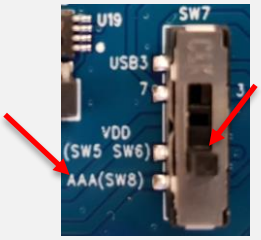
Table 1: Dev board power sources and switch positions

Selection Switch SW7 Position/Source/ Voltage Operating Mode		Dev Board Power Supply Switch Positions		
		SW5 default and only position *3V3* **Position *1V8* not valid for DVK-BL654PA**	**SW8 default and only *5V5_AAA*** **Position 2V5 not valid for DVK-BL654PA**	**Connect USB cable into USB3**
				
		Present selected voltage to the BL654PA pin		
		BL654PA VDD pin	**BL654PA VDD_HV pin**	**BL654PA VBUS pin**
SW7 top position **Source:** USB3 **Operating Mode:** High voltage using BL654PA USB (USB3)		Note 1:	USB3 voltage	USB3 voltage
SW7 middle position **Source:** SW5 - Note 2: **Operating Mode:** Normal voltage		Decided by SW5 (default and only SW5 position is *3V3*)	N/A	N/A
SW7 bottom position **Source:** SW8 **Operating Mode:** High voltage		Note 1	Decided by SW8 (default and only SW8 position *5V5_AAA* DVK-BL654PA)	N/A

Power Source and Switch Location Notes:

Note 1: No voltage is presented to VDD pin, as in High voltage mode, the VDD pin becomes an output voltage pin. It can be used to supply external circuitry from the VDD pin. Before any current can be taken from the BL654PA VDD pin, this feature must be enabled in the BL654PA. Additionally, the VDD output voltage is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V.

Note 2: SW6 default and valid position is *3V3/1V8*. SW6 position *coin cell* is not valid for BL654PA and therefore coin cell power supply option operation of the BL654PA module is not possible (J34 coin cell holder cannot be used

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on the DVK-BL654PA). Therefore, if SW6 is accidentally set to the *coin cell* position, then the voltage selected with SW5 (default position 3V3) is not presented to the BL654PA.

Note: The development board for BL654PA has on-board circuitry to allow access to BL654PA SWD interface (via USB connector USB2). Use USB2 only to power the development board when BL654PA SWD interface is needed. Refer to SWD Interface. When USB2 is used, USB1 does not need to be used for DC power.

The development board power supply circuitry's special feature is that it resolves whether the BL654PA VDD pin is an input supply pin (in Normal Voltage mode) or becomes an output supply voltage pin (in High Voltage mode).

On the development board, the power circuity net names are as follows:

- VCC_3V3 – Supplies regulated 3.3V power to the FTDI chip as well as temperature sensor (U1).
- VSUPPLY – Supplies regulated 3.3V (3V3) or 1.8V (1V8) via selection switch SW5 to net VSUPPLY which is connected to input of Load switch U21. For the DVK-BL654PA, the default and only valid SW5 position is 3V3.
- VCC_2V5_5V5 – Selection switch SW8 supplies either regulated 2.5V (*2V5*) or 3x AAA (*5V5_AAA*) battery voltage (4.5V) can be used for when BL654PA is powered in High Voltage mode (using the VDD_HV pin). For the DVK-BL654PA, the default and only valid SW8 position is *5V5_AAA*.
- V5V – The main development board power supply's buck-boosted output (that is 5V) supplies a discrete regulator made up of Q3 and U19. U19 OpAmp drives Q3 to generate regulated voltage (that then is connected to input of load switch U20) that tracks control signal VDD_nRF_SENSE.
- VDD_VSRC_nRF – Supplies the FTDI chip IO and all other sensors and circuitry. VDD_VSRC_nRF is generated from load switches U20 or U19.
- VDD_nRF_SENSE – Used as control signal to drive control pin of load switches U20 and U19. The source of VDD_nRF_SENSE is the BL654PA VDD pin. When BL654PA is powered in High Voltage mode (using the VDD_HV pin), the BL654PA VDD pin becomes an output.
- VDD_nRF_SW – Selection switch SW6 supplies either VDD_SRC_nRF or coin cell (J34). When the BL654PA operates in Normal Voltage mode (SW7 in middle position and voltage source is either 1.8V or 3.3V selected by SW5). Also supplies the I2C RTC chip (U16). The use case for powering this is that the RTC chip can be configured so that, after the pre-determined time, the RTC chip outputs (via RTC_ALARM pin) a transition level that can be used to wake up the BL654PA module from deep sleep.
- VDD_nRFp – Supplies the BL654PA series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J7 pin 1).
- VDD_nRF – Supplies the BL654PA series module only and is to the current that has come out of the current measuring block on the development board on header connector J7 pin 2.
- VDD_HVp – Supplies the BL654PA series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J9 pin1).
- VDD_HV – Supplies the BL654PA series module only and is to the current that has come out of the current measuring block on the development board on header connector J9pin2.
- VBUS_nRFp – This voltage from USB cable plugged into connector USB3, that is directly fed to BL654PA VBUS pin (via 0R resistor R50) on net VBUS_nRF.

TIP: Operating the development board at 75°C or above causes issue related to Q2 (it starts turning on) which results in VDD_VSRC_nRF supplying heading towards 0V or turning off. To overcome this temperature issue, bridge with solder the open-solderbridge SB24 which connects 1MOhms resistor to ground onto the gate of Q2.
The 1-MOhm resistor results in extra current consumption of (= VDD_nRF_SENSE/1Mohms) added to any current measurements made when operating the BL654PA module on devboard in High voltage mode (VDD_HV pin) ONLY which is when SW7 in Top position or Bottom position (and in that case by default VDD_nRF_SENSE is 1.8V). Figure 5 shows PCB location of SB24 and schematic showing SB24.

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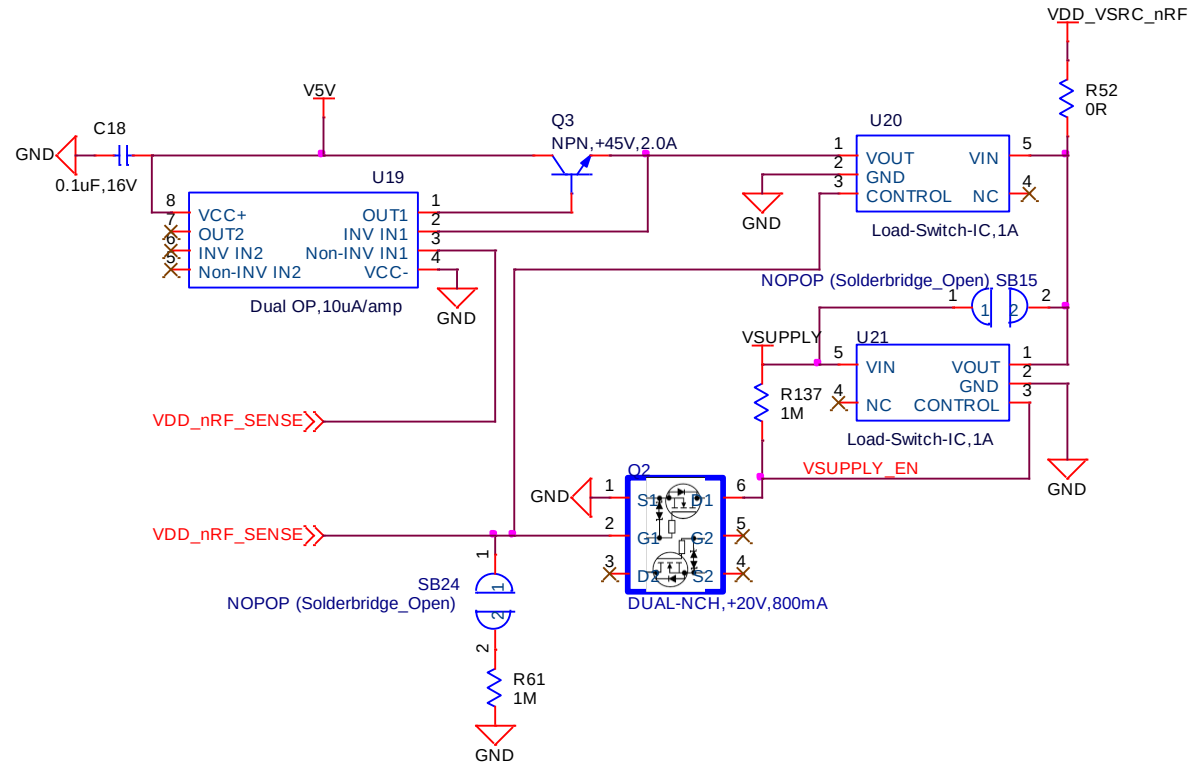

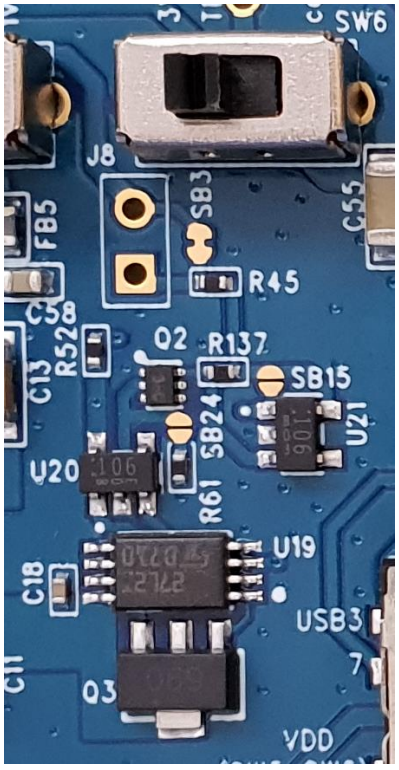

Figure 5: Schematic and PCB location of SB24

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6.1.1 Additional Power Option – Coin Cell

The coin cell operation of BL654PA module on the DVK-BL654PA devboard is **NOT possible**. A J34 coin cell holder cannot be used on the DVK-BL654PA SW6 default and only valid position is *3V3/1V8*. SW6 position *coin cell* is not valid for the BL654PA.

6.2 Reset Button

The development board has a reset button (SW3) with the net name BOOT_RESET_BLE. The BOOT_RESET_BLE (active low when SW3 pushed down) is routed to the BL654PA module nRESET_BLE pin via an analog switch U25. The placement of the Reset button is shown in Figure 6.

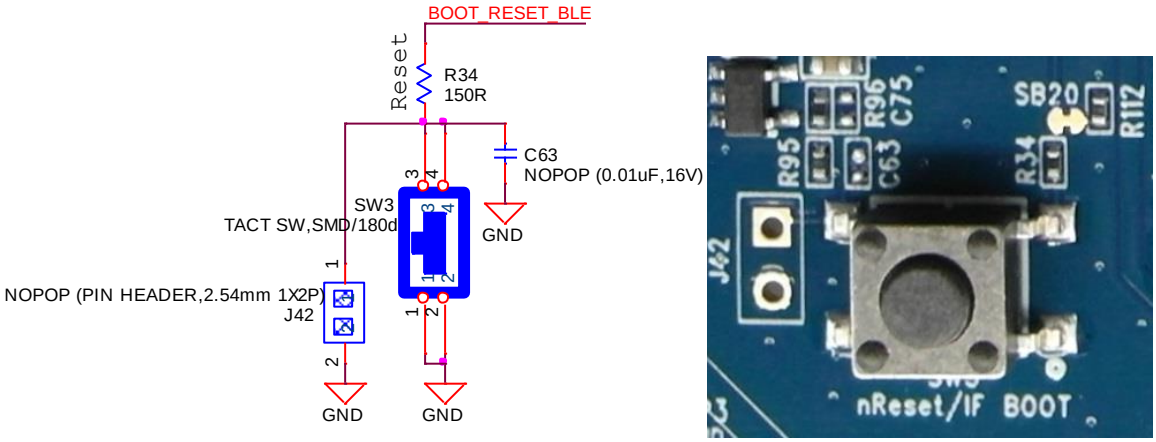

Figure 6: Reset button placement

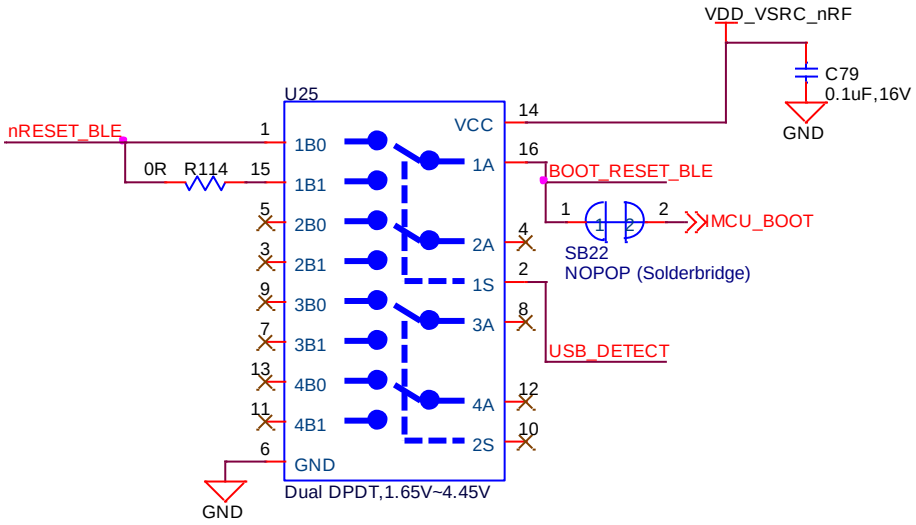

Figure 7: Reset button schematic and routing through analog switch and location diagram

By default, whether the analog switch (U25) control line (USB_DETECT) is low (USB2 cable not plugged in) or high (USB2 cable plugged in), the nReset button (SW3) is routed via the analog switch (U25) to BL654PA nReset pin (nRESET_BLE).

The development board has USB2 cable detection circuit that generates the USB_DETECT signal on its output, so if a USB cable is plugged into connector USB2, then USB2 cable detection circuit generates a HIGH on USB_DETECT or LOW if USB2 cable is not plugged in.

Table 2 displays the routing of SW3 reset button via analog switch U25 to the BL654PA reset pin (regardless of whether the USB cable is plugged into USB2 or not).

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Table 2: USB U4 USB-SWD to BL654PA SWD signal routing connections

SW3 Reset Button into Analog switch U25 (net name)	USB Cable Plugged into USB2 (USB_DETECT HIGH) Route SW3 Reset Button to BL654PA (U5) Reset Pin via Analog Switch U25 (net name)	No USB cable plugged into USB2 (USB_DETECT LOW) Route SW3 reset button to BL654PA (U5) reset pin via analog switch U25	Comments
BOOT_RESET_BLE	nRESET_BLE	nRESET_BLE	R114 0R resistor, if removed, allows SW3 to be disconnected from BL654PA reset pin when USB2 cable plugged in.

6.3 SWD (JTAG) Interface

The development board provides access to the BL654PA module two-wire SWD interface on JP1 via analog switch U24. This is ***required*** for customer use, since the BL654PA module supports *smart*BASIC runtime engine firmware over JTAG (as well as over UART).

Note: We recommend that you use JTAG (two-wire interface) to handle future BL654PA module firmware upgrades. You ***must*** wire out the JTAG (two-wire interface) on your host design (four lines should be wired out, namely SWDIO, SWDCLK, GND, and VCC). Firmware upgrades can still be performed over the BL654PA UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the BL654PA JTAG (two-wire interface).

Upgrading *smart*BASIC runtime engine firmware or loading *smart*BASIC applications also can be done using the UART interface.

For those customers (using Nordic SDK) that require access to BL654PA SWD (JTAG) interface, the BL654PA development board (see Figure 1) has on-board circuitry to allow access to BL654PA module SWD interface (via USB connector USB2).

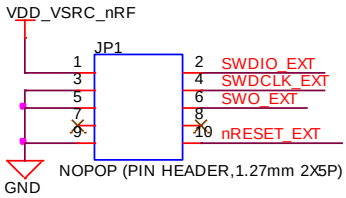

Figure 8: SWD on-board circuitry routing via analog switch U24

When the USB cable is plugged into connector USB2, the USB cable detection output generates a HIGH for USB_DETECT and USB_DETECTp when switch SW11 is in position 2-1 (default) and Atmel MCU SWD (JTAG) signals are routed to the BL654PA SWD interface. This is required to connect the two-wire SWD (JTAG) interface from U14 to the BL654PA SWD (JTAG) interface.

When the USB cable is plugged into connector USB2 and the SW11 is in position 2-3 (Low), there is a LOW on U24 control line USB_DETECTp and the Atmel MCU SWD (JTAG) signals are routed to connector JP1 (which is not populated).

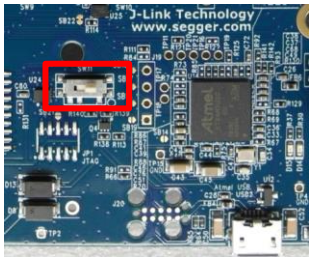

Figure 9: SW11 on development board (showing default position)

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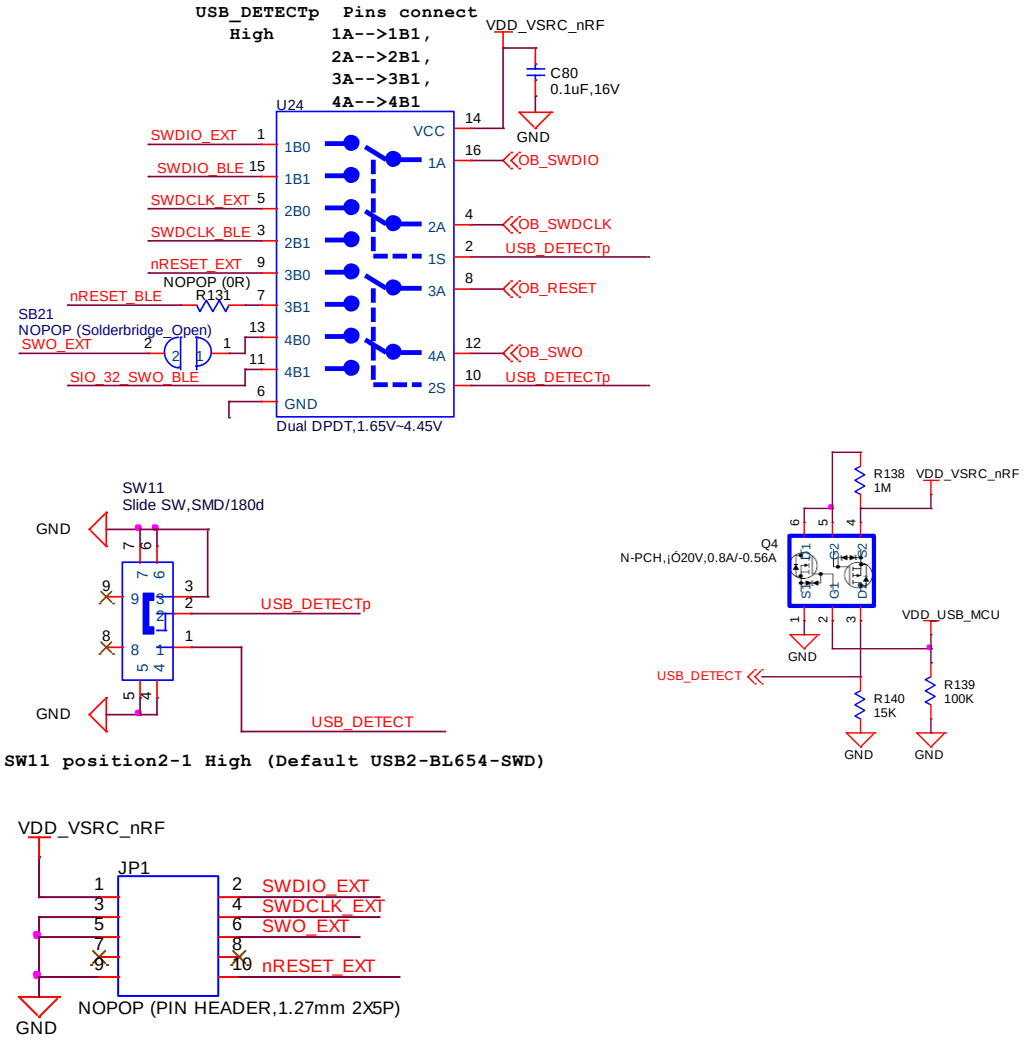

Figure 10: USB2 to SWD onboard circuitry routing via analog switch (U24)

Table 3 displays the four signals running from Atmel MCU U14 (SWD interface plus SIO_32 and nReset_BLE) to the BL654PA module (SWD interface plus SIO_32 and nReset_BLE).

Table 3: USB U4 USB-SWD to BL654PA SWD signal routing connections

U4 (Atmel MCU) Net SWD Interface into Analog switch U24	USB cable plugged into USB2 (USB_DETECTp HIGH)	No USB cable plugged into USB2 (USB_DETECTp LOW)	Comments
	Route SWD Interface from Atmel MCU (U4) to BL654PA Module Net Name	Route SWD Interface from Atmel MCU (U4) to JP1	
OB_SWDCLK	SWDCLK_BLE (pin 3)	SWDCLK_EXT (JP1 pin4)	
OB_SWDIO	SWDIO_BLE (pin 1)	SWDIO_EXT (JP1 pin2)	
OB_RESET	nRESET_BLE (pin 19) via R131 0R (Not populated)	nRESET_EXT (JP1 pin10)	
OB_SWO	SIO_32 (pin 7)	SWO_EXT (JP1 pin6) via SB21 open solderbridge	

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Notes: SIO_32 is a trace output (SWO or Serial Wire Output) and is not necessary for programming BL654PA over the SWD interface.

nReset_BLE is not necessary for programming BL654PA over the SWD interface.

6.4 Four-wire UART Serial Interface

The development board provides access to the BL654PA module four-wire UART interface (TX, RX, CTS, RTS) either through USB (via UT10 FTDI USB-UART convertor chip) or through a breakout header connector J1.

Note: The BL654PA module provides four-wire UART interface on the HW and the other four signals (DTR, DSR, DCD, RI), which are low bandwidth signals, can be implemented in a *smart*BASIC application using any spare digital SIO pins.

6.5 UART Mapping

The UART connection on the BL654PA series module and the FTDI IC are shown in Table 4. Figure 11 explains how the BL654PA series module UART is mapped to the breakout header connector J1. These connections are listed in Table 4.

Table 4: SIO/UART connections

BL654PA (U5) SIO	BL654PA Default Function	FTDI IC UART
SIO_06 (U5 pin35)	UART_TX (output)	USB_RX
SIO_08 (U5 pin29)	UART_RX (input)	USB_TX
SIO_05 (U5 pin39)	UART_RTS (output)	USB_CTS
SIO_07 (U5 pin37)	UART_CTS (input)	USB_RTS

Note: Additionally, SIO_35 (the nAutoRUN input pin on the module) can be driven by the USB_DTR output pin of the FTDI chip. This allows testing the $autorun$ application on boot without setting the autorun jumper on the development board. nAutorun can be controlled directly from Laird's UWTerminalX using the DTR tick box.

6.5.1 UART Interface Driven by USB

- **USB Connector:** The development kit provides a USB Type Micro-B connector (USB1) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB signals are connected to a USB-to-serial converter device (FT232R) when SW4 is set to the USB position.
- **USB – UART:** The development kit is fitted with a (U10) FTDI FT232R USB-to-UART converter which provides USB-to-Virtual COM port on any Windows PC (XP or later). Upon connection, Windows auto-installs the required drivers. For more details and driver downloads, visit the following website: http://www.ftdichip.com/Products/FT232R.htm.
- **UART Interface Driven by USB FTDI Chip:** In normal operation, the BL654PA UART interface is driven by the FTDI FT232R USB-to-UART converter.

6.5.2 UART Interface Driven by External Source

- **UART Interface Driven by External UART Source:** The BL654PA module UART interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1 in.) pitch header (J1). To allow the BL654PA UART interface to be driven from the breakout header connector (J1), the following must be configured:
  - The development board must be powered from a DC jack (CON1) or AAA batteries (J25) and with switch SW4 in DC position.
  - The FTDI device must be held in reset. This is achieved automatically by removal of the USB cable (from connector USB1), placing SW4 in the DC position or fitting a jumper on J27.
  - Fit a jumper on J35 (to switch the Analog switch U15 and route BL654PA UART to J1) when connecting an external UART source (for example FTDI USB-UART TTL (3.3V) converter cable) using J1. This isolates the BL654PA UART from the on-board USB-UART FTDI device. By default, the jumper on J35 is not fitted, so by default BL654PA UART is routed to U10 FTDI FT232R USB –UART converter.

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Note: The BL654PA UART signal levels always need to match the supply voltage net VDD_VSRC_nRF, of the BL654PA.

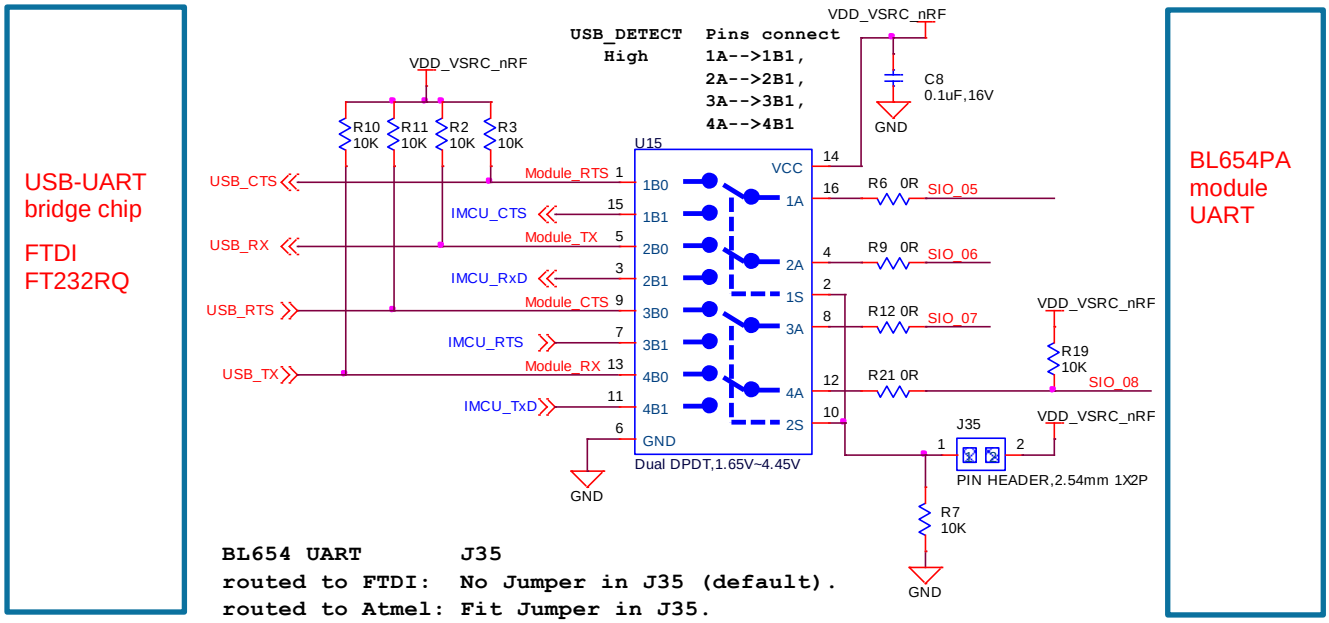

Figure 11: USB to UART (via FTDI chip on dev board) interface via analog switch U15

J1 pinout is designed to be used with FTDI USB-UART TTL (3.3V) converter cables (found at http://www.ftdichip.com/Products/Cables/USBTTLSerial.htm). One example is FTDI part TTL-232R-3V3.

If the BL654PA on the development board is powered from 1.8V supply, then you must use the 1.8V version of the FTDI USB-UART cable. UART signal levels always need to match the supply voltage net VDD_nRF_SW of the BL654PA development board.

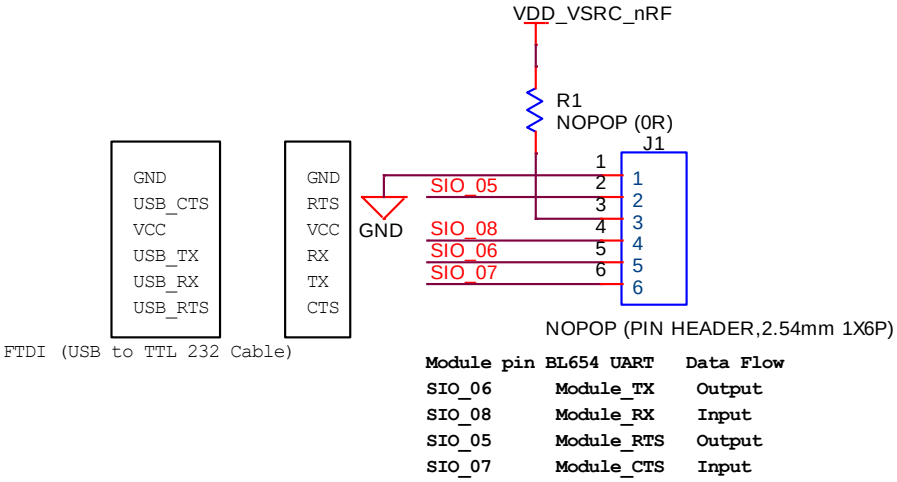

Figure 12: J1 wiring to match FTDI USB-UART cable (TTL-232R-3V3 cable)

Fit a jumper in J35 (to switch the Analog switch U15 and route BL654PA UART to J1) when connecting an external FTDI USB-UART TTL (3.3V) converter cable using J1.

Fitting a jumper in J35 also allows the BL654PA UART to be routed to Atmel MCU UART (signal also on J19 and net names beginning with IMCU_) via open solder bridges SB16 to SB19 shown in Figure 13. You must connect these bridges with solder. This may be useful for those customers wanting to work with the Nordic SDK.

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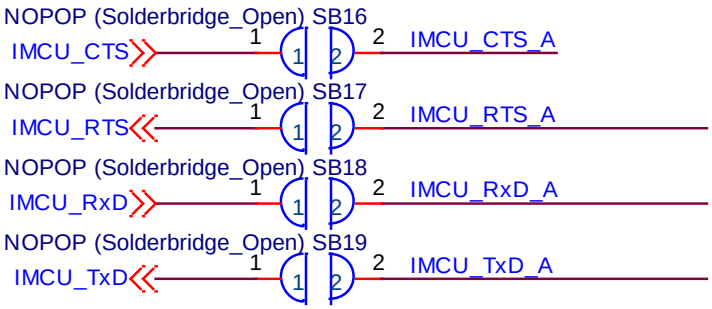


Figure 13: Open solder-bridges on the UART interface running from Atmel MCU (U4) to analog switch U15 (to BL654PA ultimately)

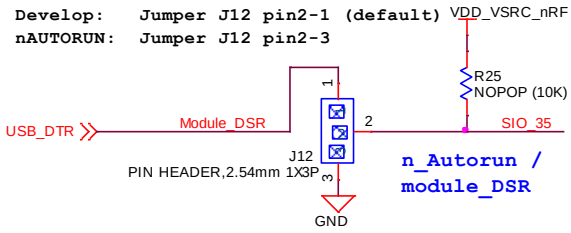
6.6 nAutoRUN Pin and Operating Modes

On the development board, the USB_DTR output (FTDI chip U10) from the PC is wired to BL654PA module pin SIO_35 (pin 5) which is the nAutoRUN pin.

Note: *smart*BASIC runtime engine FW checks for the status of nAutoRUN during power-up or reset. The nAutoRUN pin detects if the BL654PA module should power up into Interactive/Development Mode (3.3 V) or Self-contained Run mode (0V). The module enters Self-contained Run mode if the nAutoRUN pin is at 0V and an application called $autorun$ exists in the module's file system; then the *smart*BASIC runtime engine FW executes the *smart*BASIC application script automatically; hence the name Self-contained Run mode.

Tying nAutoRUN HIGH (to net name on devboard VDD_VSRC_nRF) inhibits the $autorun$ application from running. As an alternative to using USB_DTR, the J12 three-pin header allows a jumper to be fitted to select between the two operating modes.

Table 5: BL654PA nAutoRUN header

nAutoRUN Pin	BL654PA Operating Mode (pin28, nAutoRUN Mode/SIO_35)		
	Interactive/ Development Mode (SIO_35 set High Externally)	**Self-contained Run Mode (nAutoRUN mode) (SIO_35 Low Internally)**	**Circuit**
J12 Jumper Position	 **Develop** Jumper on J12 pins 2-1	 **nAutoRUN (default)** Jumper on J12 pins 2-3 BL654PA has internal pull-down enabled, jumper in J12 in 2-3 can also be left off	

The J12 header connector allows the USB_DTR signal from the FTDI chip to be disconnected from the BL654PA.

To connect the BL654PA nAutoRUN pin SIO_35 (pin 5) to PC FTDI USB_DTR line via the J12 header connector, do the following:

- Fit the jumper into the J12 (pin 2-1) header connector to allow the PC (using UwTerminal) to control nAutoRUN pin (SIO_35).

To disconnect the BL654PA nAutoRUN SIO_35 (pin 5) from the PC FTDI USB_DTR line, do the following:

- Remove the jumper on header connector J12 pin 2-1. Then nAutoRUN can be controlled by inserting the jumper onto J12 (pin 2-3) as shown in Table 5 (this is the default). The BL654PA by default has pull-down enabled on the SIO_35 (nAutoRUN) pin, so the jumper into J12 (pin 2-3) is optional.

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6.7 Virtual Serial Port Modes and Over-the-Air *smart*BASIC App Download

The Over-the-Air (OTA) feature makes it possible to download *smart*BASIC applications over the air to the BL654PA. To enable this feature, SIO_02 must be pulled high externally.

On the development board, header connector J5-pin1 brings out the BL654PA SIO_02; J5-pin 2 brings out VCC_nRF_SW. To pull BL654PA SIO_02 high (to net name VCC_nRF_SW on devboard), fit jumper into header J5.

Note: When SIO_02 is high, ensure that SIO_35 (nAutoRun) is NOT high at same time, otherwise you cannot load the *smart*BASIC application script.

This section discusses Virtual Serial Port (VSP) Command mode through pulling SIO_02 high and nAutoRUN (SIO_35) low. Refer to the documentation tab of the **BL654PA product page:**
https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl654-pa-series

Figure 14 shows the difference between VSP Bridge to UART mode and VSP Command mode and how SIO_02 and nAutoRUN (SIO_35) must be configured to select between these two modes.

- **VSP Bridge to UART mode** takes data sent from phone or tablet (over BLE) and sends to BL654PA to be sent out of the BL654PA UART (therefore data not stored on BL654PA).
- **VSP Command mode** takes data sent from phone or tablet and sends it to the BL654PA. This interprets as an AT command and the response is sent back. The OTA Android or iOS application can be used to download any *smart*BASIC application script over-the-air to the BL654PA, since a *smart*BASIC application is downloaded using AT commands.

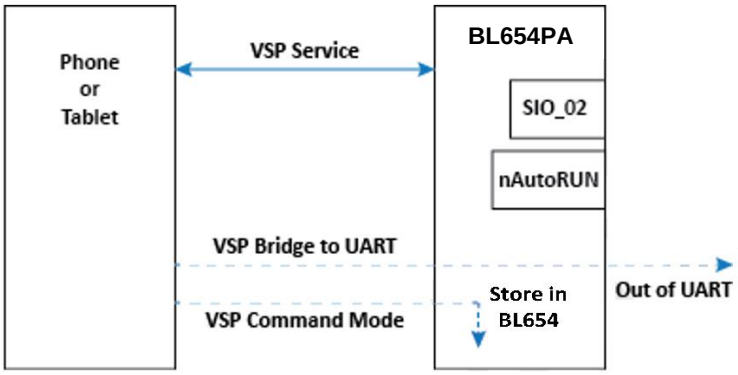

Figure 14: Differences between VSP bridge to UART mode and VSP Command mode

Table 6: vSP modes

Mode	SIO_02 and Jumper position J5	nAutoRUN (SIO_35) and Jumper position J12
VSP Bridge to UART mode	High by fitting jumper in J5	High by fitting jumper in J12 pin 2-1 and untick DTR box in UwTerminalX (the DTR box is ticked by default in UwTerminalX)
VSP Command mode	High by fitting jumper in J5	Low by fitting jumper in J12 pin 2-3

SIO_02 High (externally) selects the VSP service. When SIO_02 is High and nAutoRUN (SIO_35) is Low (externally), this selects VSP Command mode. When SIO_02 is High and nAutoRUN is High (externally), this selects VSP Bridge to UART mode.

When SIO_02 on module is set HIGH (externally), VSP is enabled and auto-bridged to UART when connected. However, for VSP Command mode, auto-bridge to UART is not required. With SIO_02 set to High and nAutoRUN (SIO_35) set to Low, the device enters VSP Command mode and you can then download the *smart*BASIC application onto the module over the air from the phone (or tablet).

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7 SOFTWARE

The development board connects the BL654PA module to a virtual COM port of a PC or other device. From a PC, you can communicate with the module using Laird's UwTerminalX (cross platform software available for Windows, Mac, and Linux). This utility allows connections to serial devices using any combination of the communications parameters listed in Table 7.

Table 7: UwTerminalX communication parameters for BL654PA

Port (Windows)	1 to 255
Port (Mac/Linux)	Any/dev/tty device
Baud Rate	1200 to 1000000 **Note:** Baud rate default is 115200 for BL654PA.
Parity	None
Data Bits	8
Stop Bits	1
Handshaking	None or CTS/RTS

Note: Baud rates higher than 115200 depend on the COM port capabilities of the host PC and may require an external USB – RS232 adapter or ExpressCard – RS232 card.

The benefits of using UwTerminalX include the following:

- Continually displayed status of DSR, CTS, DCD, and RI
- Direct control of DTR on the host PC via a check box
- Direct control of RTS, if CTS/RTS Handshaking is disabled when UWTerminalX is launched
- Sending UART BREAK signals. Following provides explanation UART Break. (https://en.wikipedia.org/wiki/Universal_asynchronous_receiver/transmitter#Break_condition)
- Additional built-in features (right click in Terminal tab screen) to accelerate development including Automation and various XCompile/Load/Run options for downloading *smart*BASIC applications into the BL654PA.

Note: Full details on *smart*BASIC are available in the *smart*BASIC User Guide available at the Laird product page for BL654PA, along with a document giving a basic introduction to UwTerminalX. A help file is included with UwTerminalX that gives an overview of the program. Visit the BL654PA product page at https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl654-pa-series

Tip: If the module returns a four-hex digit error code:
In UwTerminalX, select those four digits, right-click, and select **Lookup Selected Error-Code (Hex)**. A description of the error is then printed on screen.

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8 Breakout Connector Pinouts

8.1 SIO (Special Input/Output Sockets) Breakout Connectors

Access to all 46 BL654PA series module signal pins (SIO's = Signal Input /Output) is available on plated-through holes (for 2.54 mm pitch header connectors) on J44, J47, J48, J41, J29, J1, J12, J1, J5, J17, J21, J6, and J36.

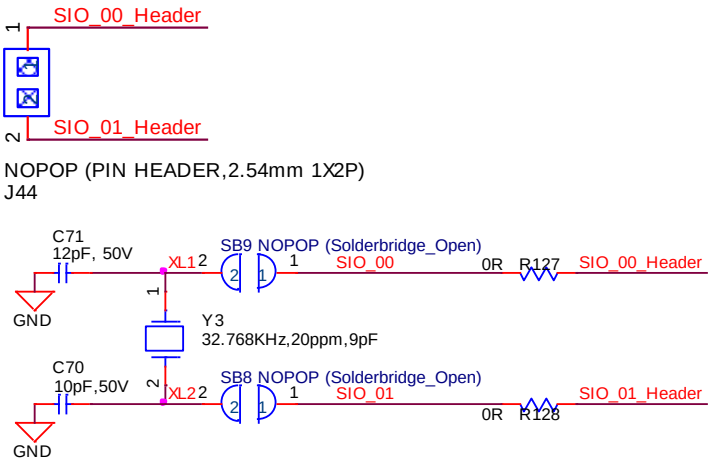
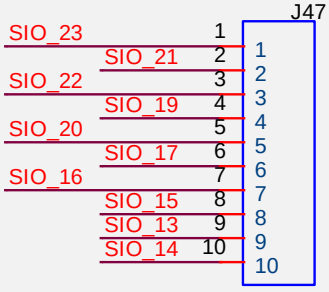
Note: The BL654PA module signal pins designation SIO (Signal Input /Output).

- DEFAULT type is DIO (Digital Input or Output) or UART (on fixed pins)
- ALTERNATE type is either AIN (Analog Input ADC), I2C, SPI, QSPI, DIO (on fixed pins), PWM, FREQ, and NFC
- DIO or AIN functionality is selected using the GpioSetFunc() function in *smart*BASIC
- I2C, UART, SPI, QSPI controlled by xxxOPEN() functions in *smart*BASIC
- SIO_05 to SIO_08 are DIO by default when $autorun$ app runs on power up
- SIO_09 and SIO_10 are NFC pins by default; they can be set to alternative function SIO using the GpioSetFunc() function in *smart*BASIC

These breakout connectors can interface to a wide array of sensors. The BL654PA is user configurable through the *smart*BASIC application script to change each SIO pin from the default function (DIO, UART) to alternate functions (AIN (ADC), I2C, SPI, QSPI, DIO), PWM, FREQ, and NFC. The BL654PA development kit incorporates additional fly-lead cables inside the box to enable simple, hassle-free testing of these multiple interfaces.

Table 8 shows the BL654PA module pins that are brought out to plated through Holes (suitable for 2.54 mm pitch headers).

Table 8: Module pins exposed by plated through holes

	Plated Through Holes or Header Connector	BL654PA Module Signals Exposed
J44		BL654PA pin plated holes for access: ▪ SI0_ 00 ▪ SI0_ 01 J44 connects to SIO_00 and SIO_01 via 0R resistors R127 and R128. By default, the optional external 32.768 kHz crystal circuit is not connected to BL654PA as SB8 and SB9 are open.
J47	NOPOP (PIN HEADER,2.54mm 1X10P) 	BL654PA pin plated holes for access: ▪ SI0_ 23 ▪ SI0_ 21 ▪ SI0_ 22 ▪ SI0_ 19 ▪ SI0_ 20 ▪ SI0_ 17 ▪ SI0_ 16 ▪ SI0_ 15 ▪ SI0_ 13 ▪ SI0_ 14

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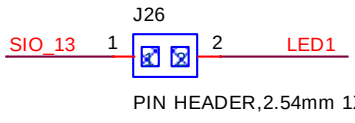
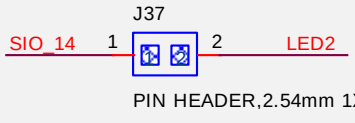
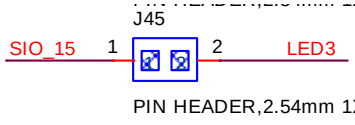
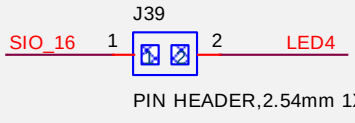
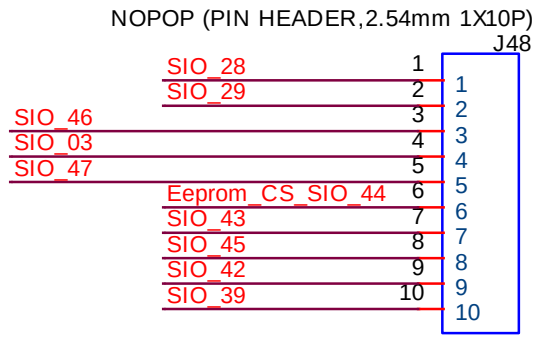
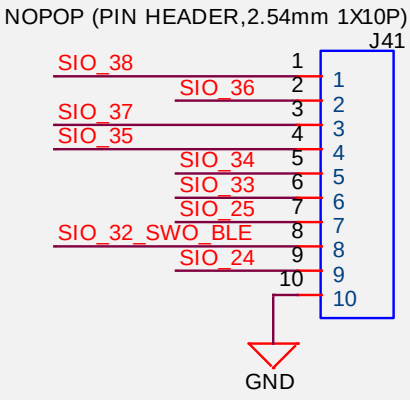
	Plated Through Holes or Header Connector	BL654PA Module Signals Exposed
J26		J26 Connects SIO_35 to LED1 J26 jumper fitted (default).
J37		J37 Connects SIO_14 to LED2 J37 jumper fitted (default).
J45		J45 Connects SIO_15 to LED3 J45 jumper fitted (default).
J39		J39 Connects SIO_16 to LED4 J39 jumper fitted (default).
J48		BL654PA pin plated holes for access: ▪ SI0_ 28 ▪ SI0_ 29 ▪ SI0_ 46 ▪ SI0_ 03 ▪ SI0_ 47 ▪ SI0_ 44 (connects to Eeprom_CS) ▪ SI0_ 43 ▪ SI0_ 45 ▪ SI0_ 42 ▪ SI0_ 39
J41		BL654PA pin plated holes for access: ▪ SI0_ 38 ▪ ~~SI0_ 36~~ DO NOT CONNECT pin ▪ SI0_ 37 ▪ SI0_ 35 ▪ ~~SI0_ 34~~ DO NOT CONNECT pin ▪ SI0_ 33 ▪ SI0_ 25 ▪ SI0_ 32 ▪ SI0_ 24 ▪ GND

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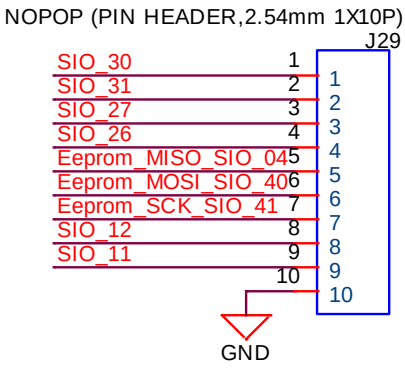
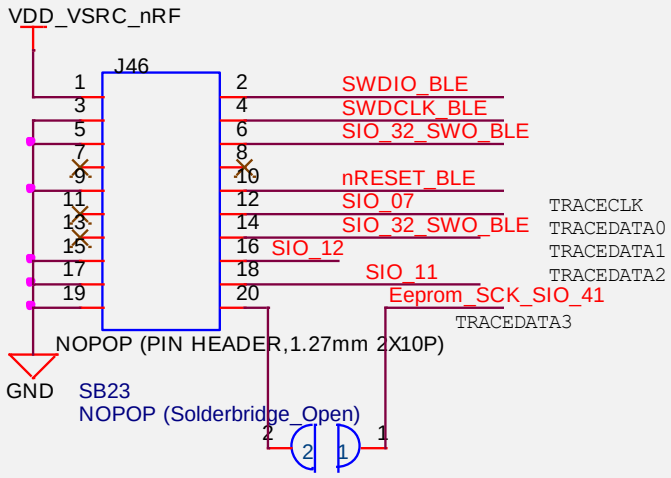
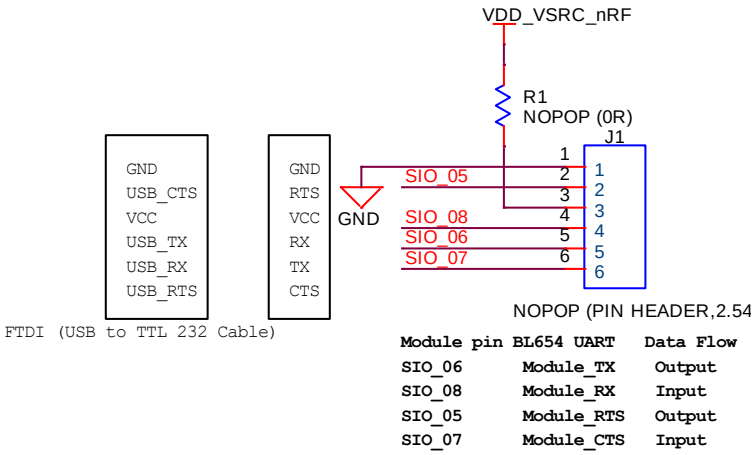
	Plated Through Holes or Header Connector	BL654PA Module Signals Exposed
J29		BL654PA pin plated holes for access: ▪ SI0_ 30 ▪ SI0_ 31 ▪ SI0_ 27 ▪ SI0_ 26 ▪ SI0_ 04 (connects to Eeprom_MISO) ▪ SI0_ 40 (connects to Eeprom_MOSI) ▪ SI0_ 41 (connects to Eeprom_SCK) ▪ SI0_ 12 ▪ SI0_ 11 ▪ GND
J46		J46 is NOPOP but is compatible to same connector on Nordic development board and brings out same signals. SIO_41 on BL654PA is SPI_CLK (as an alternative function) is disconnected from J46 on devboard by open solderbridge SB23. SIO_41 on BL654PA is directly connected to U2 (Eeprom) pin6 on devboard.
J1	 **Module pin BL654 UART Data Flow** **SIO_06 Module_TX Output** **SIO_08 Module_RX Input** **SIO_05 Module_RTS Output** **SIO_07 Module_CTS Input**	Serial Port plated holes for access:
J35	BL654PA UART J35 Routed to FTDI: No Jumper in J35 (default). Routed to Atmel: Fit Jumper in J35.	Jumper in J35 selects between BL654PA UART routed to FTDI Atmel MCU: **No Jumper on J35 (default)** Routes SIO_05 (RTS) to FTDI CTS Routes SIO_06 (TX) to FTDI RX Routes SIO_07 (CTS) to FTDI RTS Routes SIO_08 (RX) to FTDI TX

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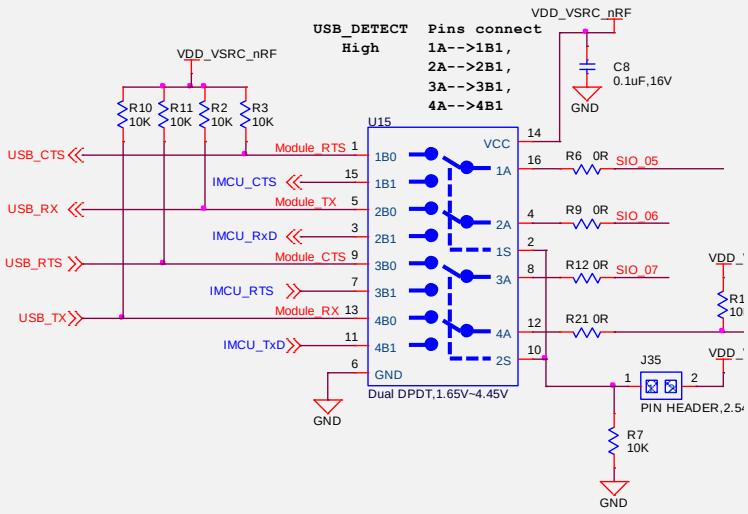
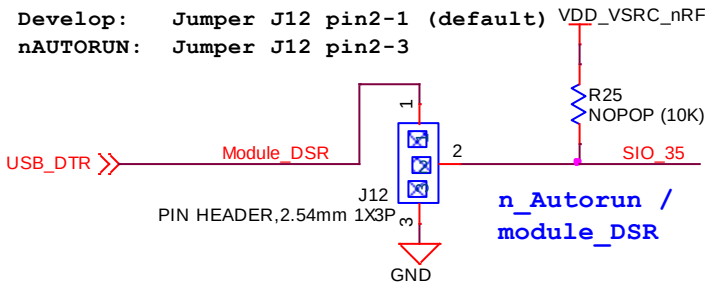
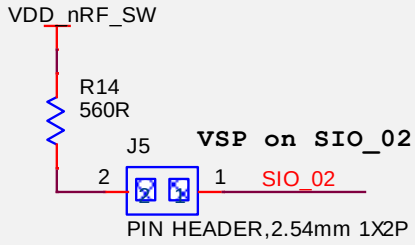
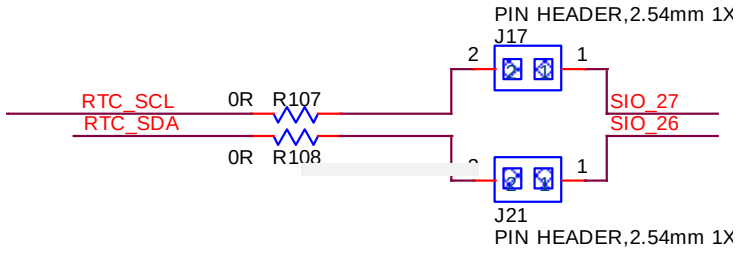
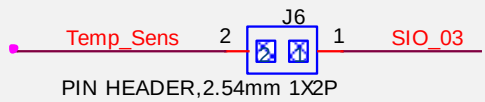
Plated Through Holes or Header Connector	BL654PA Module Signals Exposed
	**Jumper on J35 (Route to Atmel)** Routes SIO_05 (RTS) to IMCU_CTS Routes SIO_06 (TX) to IMCU_RxD Routes SIO_07 (CTS) to IMCU_RTS Routes SIO_08 (RX) to IMCU_TxD
J12 	Connects SIO_35 (nAutoRUN) to FTDI DTR Default jumper fitted in J12 pin 2-1.
J5 	SIO_ 02 (for VSP capability) Can be used to pull-up SIO_02 to VDD_nRF_SW Default: No Jumper fitted on J5 SIO_02
J17 **J21** 	J17 Routes SIO_27 (I2C SCL) to RTC_SCL device J17 pin 2-1 jumper NOT fitted (default). J21 Routes SIO_26 (I2C_SDA) to RTC_SDA device J21 pin 2-1 jumper NOT fitted (default).
J6 	J6 routes SIO_03 to Temp Sensor J6 pin 2-1 jumper NOT fitted (default)

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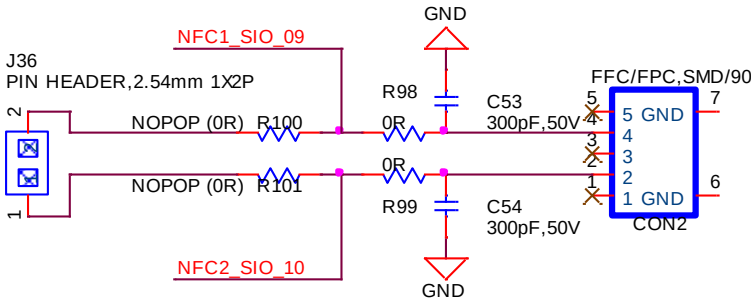
	Plated Through Holes or Header Connector	BL654PA Module Signals Exposed
J36		BL654PA pin plated holes for access: SI0_ 09 via R100 0R (default NOPOP) SI0_ 10 via R101 0R (default NOPOP) To use NFC1 pin as SIO_09 fit R100 0R and NOPOP R98. To use NFC1 pin as SIO_09 fit R101 0R and NOPOP R99.

8.2 Additional Peripherals/Sensors

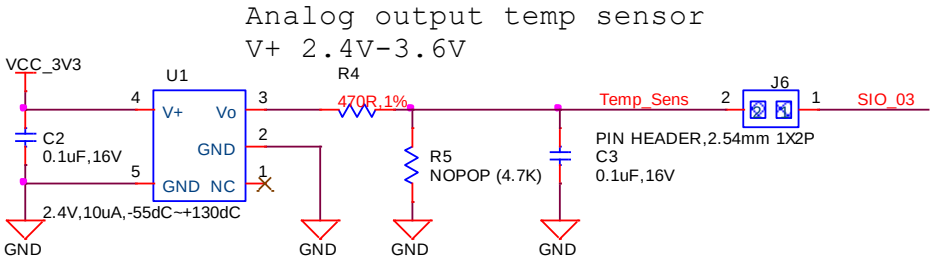
The BL654PA development board provides for simple and hassle-free connectivity to a wide range of sensors, but also includes several on-board sensors and options to enable a developer to test functionality straight out of the box.

In the *smart*BASIC application code written to use sensors on the development board, including the Temperature sensor (U1) – analog output, SPI EEPROM (U2), I2C RTC chip (U16), LED1(D1), LED2(D2), LED3(D3), LED4(D4) Button1(SW1), Button2(SW2), Button3(SW9) and Button4(SW10) the SIO pins direction and type must be set in the *smart*BASIC application to override the defaults in the BL654PA firmware.

For more information on these sample applications, see GitHub *smart*BASIC sample applications repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications.

8.2.1 Temperature Sensor

The temperature sensor (U1) by default is connected to the BL654PA module as jumper on J6 pin bridges TEMP_SENS and SIO_03.



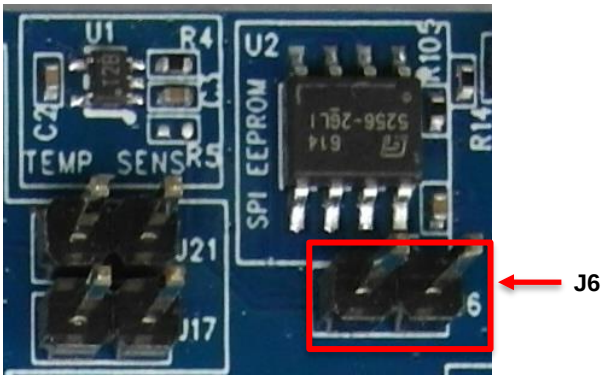


Figure 15: Temperature sensor schematic and PCB

The on-board temperature sensor (TI LM20BIM7 - www.ti.com/lit/ds/symlink/lm20.pdf) has an analogue output that can be connected to BL654PA module pin SIO_03; but since the LM20BIM7 has an analogue output, the BL654PA module SIO_03

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digital pin (DIO) must be configured as AIN analogue input (ADC). To configure the SIO_03 pin from DIO pin to Alternate function AIN, see the example file *ts.temperature.sensor.sb* in the GitHub *smart*BASIC sample applications repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications

Key specifications of the LM20BIM7 are as follows in Table 9.

Table 9: LM20BIM7 Specifications

Output type	Analogue output
Accuracy at 30ºC	±1.5ºC ±4ºC (max)
Accuracy at 40ºC to +85ºC	approx. ±2.5ºC ±5ºC (max)
Power supply voltage range	+2.4 V to 5.5 V
Current Drain	10 uA (max)
Output impedance	160 Ohms (max)

The LM20BIM7 datasheet states the relationship of Temperature (T) to Voltage output (Vo) can be approximated as a linear equation (for temperature range of -40ºC to +85ºC):

Vo(mV) = -11.67mV/ºC x T + 1858.3

gives the following calculated Vo versus temperature:

Table 10: LM20BIM7 Temperature to Voltage Output relationship

Temperature (T)	Typical Voltage
+80ºC	+924.7mV
+70ºC	+1041.4mV
+60ºC	+1158.1mV
+50ºC	+1274.8mV
+40ºC	+1391.5mV
+30ºC	+1508.2mV
+20ºC	+1624.9mV
+10ºC	+1741.6mV
+0ºC	+1858.2mV
-10ºC	+1975.0mV
-20ºC	+2091.7mV
-30ºC	+2208.4mV

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8.2.2 I2C Sensor (RTC Chip)

The I2C RTC chip (U16) allows the BL654PA I2C interface to be tested. The output of the RTC chip (U16) is on the I2C bus and is by default connected to the BL654PA module via jumpers on J17 and J21.

Table 11: I2C RTC chip BL654PA I2C signal mappings

I2C RTC EEPROM (U16)	BL654PA module (U5) SIO	Comments
(U16 pin6) RTC_SCL	(U5 pin38) SIO_27	Fit jumper on J17 to route
(U16 pin5) RTC_SDA	(U5 pin36) SIO_26	Fit jumper on J21 to route

Fitting a jumper on J17 routes the RTC_SCL signal to BL654PA SIO_27 and fitting a jumper on J21 routes the RTC_SDA to BL654PA SIO_26.

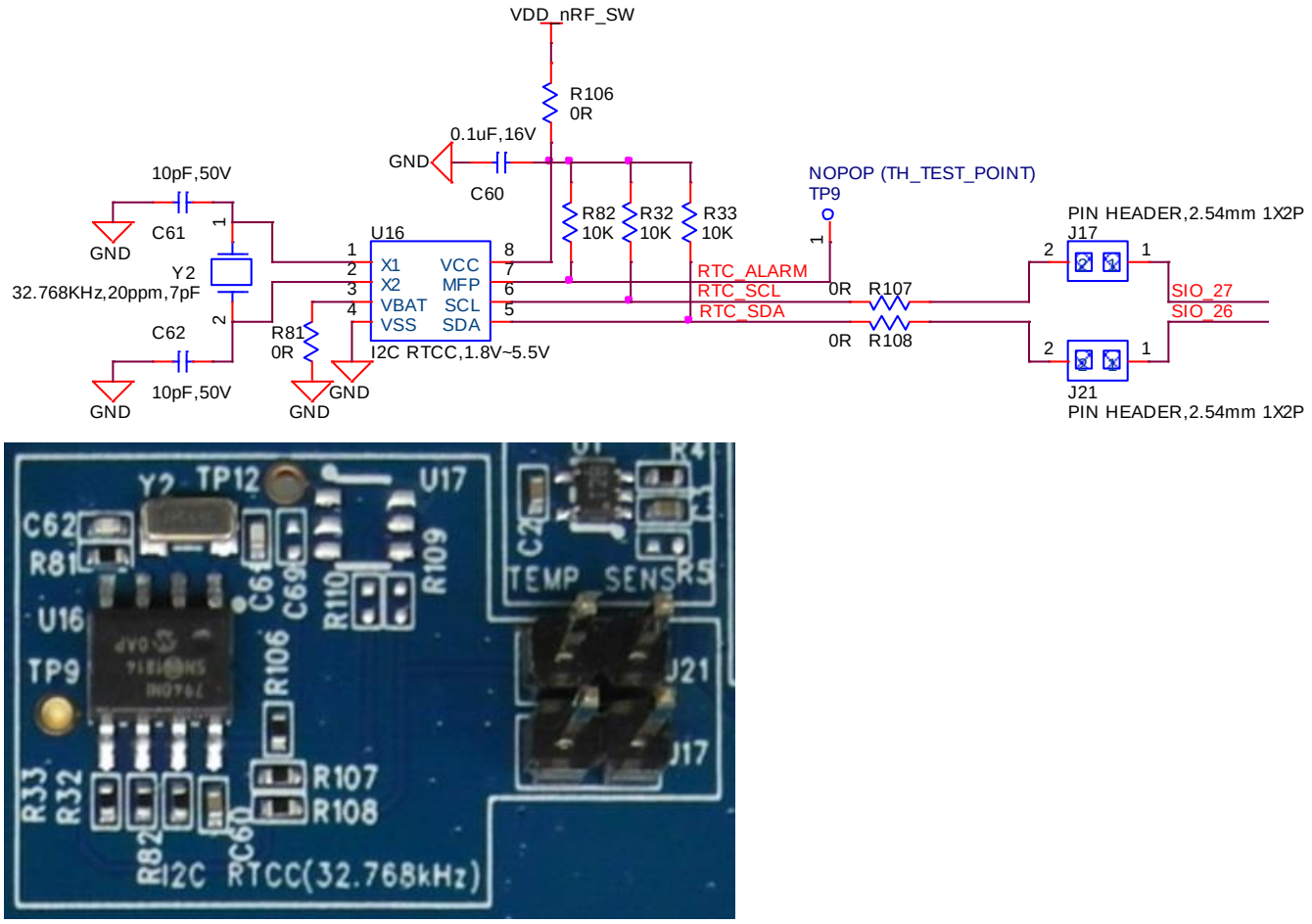

Figure 16: I2C device RTC chip schematic and PCB

To test the BL654PA I2C interface, use *smart*BASIC application *rtcs.erver.sb* in the GitHub *smart*BASIC sample application repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications. This application runs on the BL654PA and can be used with an Android phone (requires an app such as nRF connect, https://play.google.com/store/apps/details?id=no.nordicsemi.android.mcp&hl=en_GB) or another BT900/BL620/BL652/BL654PA loaded with "*rtcc.lient.sb*".

The *smart*BASIC application "*rtcs.erver.sb*" is a BLE RTC server, and it advertises the current time (which it gets from the I2C RTC chip (U4)).

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8.2.3 SPI Device EEPROM

The SPI EEPROM device (U2) is connected to the BL654PA SPI pins **directly**. By default, the BL654PA Module SIO_44 (used as the SPI_CS) is connected to EEPROM (U2) slave select line. Table 12 lists signal mappings of how the SPI EEPROM (U2) is wired to BL654PA SIO pins.

Table 12: SPI EEPROM to BL654PA SPI signal mappings

SPI EEPROM (U2)	BL654PA (U5) SIO	Comments
(U2pin6) Eeprom_SCK_SIO_41	(U5pin30) SIO_41	
(U2pin2) Eeprom_MISO_SIO_04	(U5pin34) SIO_04	
(U2pin5) Eeprom_MOSI_SIO_40	(U5pin32) SIO_40	
(U2pin1) Eeprom_CS_SIO_44	(U5pin54) SIO_44	Configure SIO_44 as an output and drive output low in *smart*BASIC application to select SPI slave (SPI EEPROM U2).

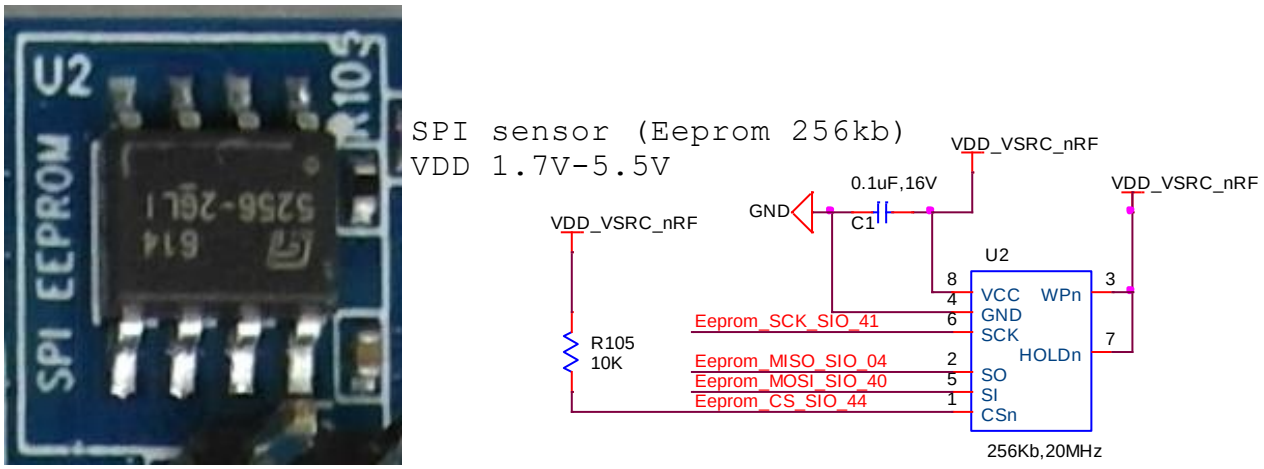

Figure 17: SPI EEPROM schematic and PCB

For a working example of the BL654PA SPI interface using the SPI EEPROM (U2), a *smart*BASIC application for this will be available in the future in the GitHub *smart*BASIC sample application repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications.

8.2.4 Push Button and LED Connected to BL654PA

The two push buttons and two LEDs on the BL654PA are connected to dedicated SIOs of the BL654PA module.

Table 13: LED's and Buttons to BL654PA SIO signal mappings

Part	BL654PA (U5) SIO	Comments
LED1 (D1)	Pin 20 SIO_13 (via header J26)	To connect LED1 to SIO_13, fit jumper in J26
LED2 (D2)	Pin 22 SIO_14 (via header J37)	To connect LED1 to SIO_14, fit jumper in J37
LED1 (D3)	Pin 18 SIO_15 (via header J26)	To connect LED1 to SIO_15, fit jumper in J45
LED2 (D4)	Pin 21 SIO_16 (via header J37)	To connect LED1 to SIO_16, fit jumper in J39
Button 1 (SW1)	Pin 27 SIO_11	
Button 2 (SW2)	Pin 28 SIO_12	
Button 3 (SW9)	Pin 10 SIO_24	
Button 4 (SW10)	Pin 8 SIO_25	

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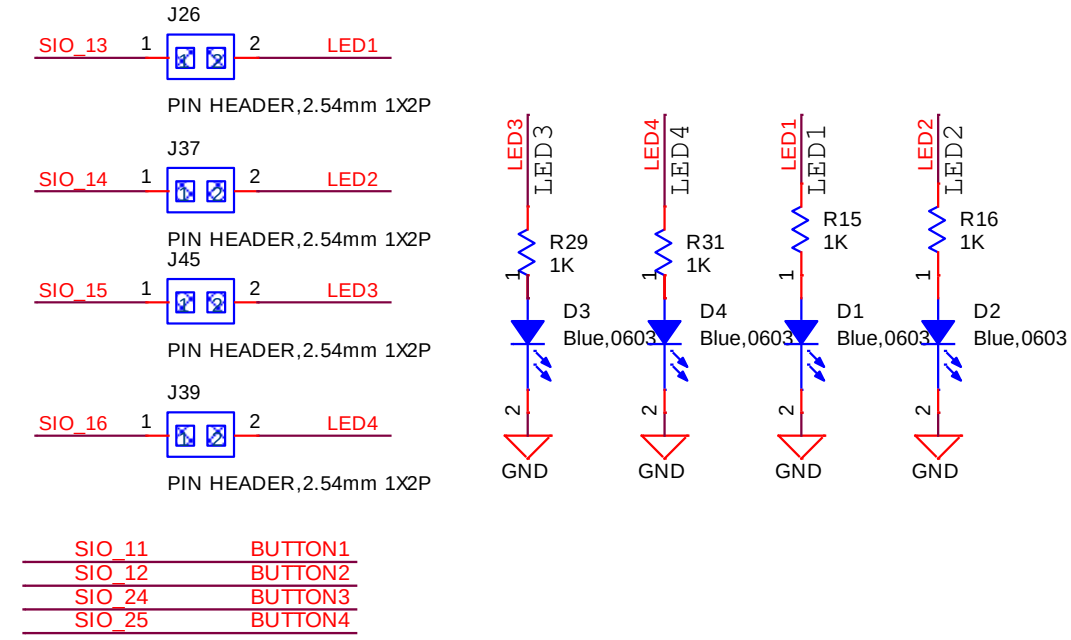

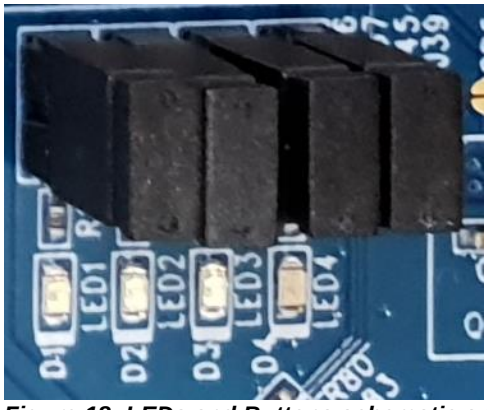

Figure 18: LEDs and Buttons schematic and PCB

The buttons (BUTTON1 and BUTTON2, for example) have no external pull-up resistor. To use the buttons, the SIO_11 and SIO_12 pins must be configured as inputs with internal pull-up resistors (which is the default). The following *smart*BASIC lines configure the pull-ups:

```
rc = GPIOSETFUNC(11,1,4)          '//sets SIO_11 (Button1) as a digital in,
                                    strong pull up
rc = GPIOSETFUNC(12,1,4)          '//sets SIO_12 (Button2) as a digital in,
                                    strong pull up
```

Refer to the *smart*BASIC application script example *btn.button.led.test.sb* in the GitHub *smart*BASIC sample application repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications

The LEDs are active high, meaning that writing a logical one (“1”) to the output pin illuminates the LED.

One example of when push buttons can be used is when a *smart*BASIC application is written to simulate a generic data profile. Push buttons can then be pressed to increment and decrement, such as a heart rate.

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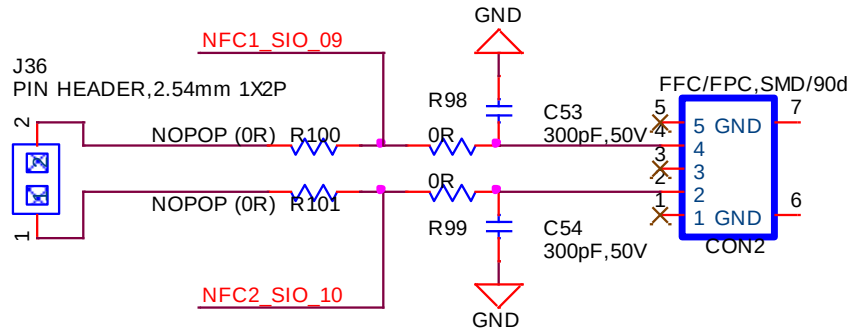
8.2.5 NFC External Antenna Connector and NFC Antenna RF Matching Circuit

The NFC antenna input connector (CON2) allows the Laird supplied flex-PCB NFC antenna to be plugged in. The BL654PA module NFC circuit uses two pins, pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) to connect the antenna. These pins are shared with GPIOs (**SIO.09** and **SIO.10).** BL654PA NFC pins are enabled by default. NFC can be disabled via *smart*BASIC application. Pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) are configured by default on the development board schematic to use NFC antenna, but if pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) are needed as normal GPIOs, R98 and R99 must be removed and R100 and R101 must be shorted by 0R.

C53 (300pF) and C54 (300pF) are RF tuning elements for the flexi-PCB NFC antenna.

Table 14: NFC input BL654PA SIO signal mappings

BL654PA (U5) SIO	Bring out SIO_9 and SIO_10 to NFC antenna connector (CON2)	Bring out SIO_9 and SIO_10 to Header connector (J36)
pin 59 (**NFC1/SIO_9**)	Fit R98 0R (default) Remove R100 0R (default)	Remove R98 0R Fit R100 0R
pin 57 (**NFC2/SIO_10**)	Fit R99 0R (default) Remove R101 0R (default)	Remove R99 0R Fit R101 with 0R



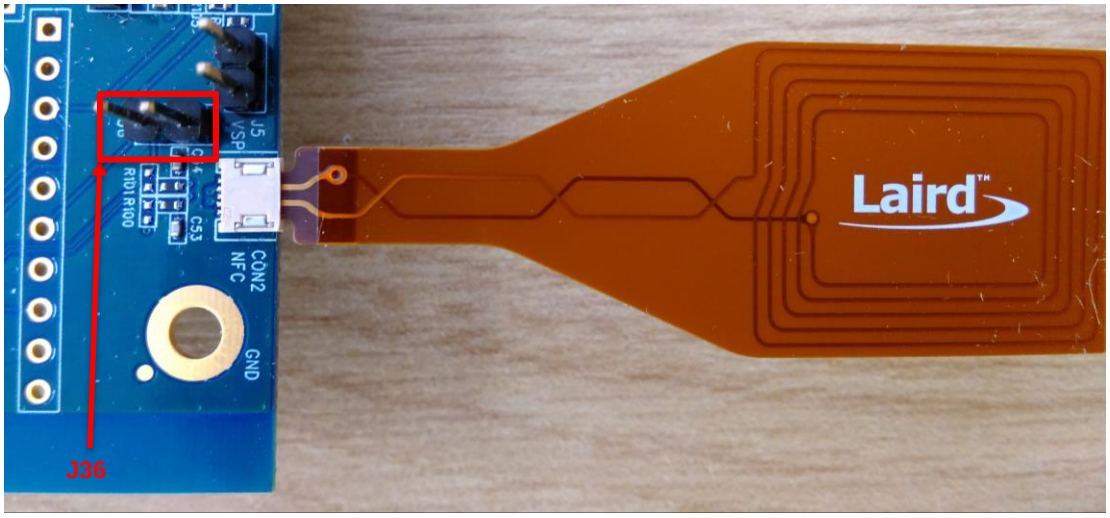


Figure 19: NFC antenna RF matching circuit, NFC antenna connector schematic and NFC plugged in to connector CON2

The *smart*BASIC application *nfc.all.launch.sb* in the GitHub *smart*BASIC sample application repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications exercises the following over the BL654PA NFC:

- On Android NFC enabled devices – Opens Laird Toolkit or shows it in the Google Play store if not installed
- On Windows NFC enabled devices – Opens the calculator
- On other NFC enabled devices – Shows the Laird website or text saying ***this is a BL654PA***

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8.2.6 Optional External Serial QSPI Flash IC

There is an optional external serial QSPI flash IC (U18) that may be used, for example, for data logging purposes. U18 can also capable of SPI mode.

Solder bridges SB4, SB5, SB6, SB7, SB10 and SB11 must individually be shorted to connect this optional external serial (QSPI) flash (U18 to the BL654PA module).

By default, these BL644 pins are GPIO pins.

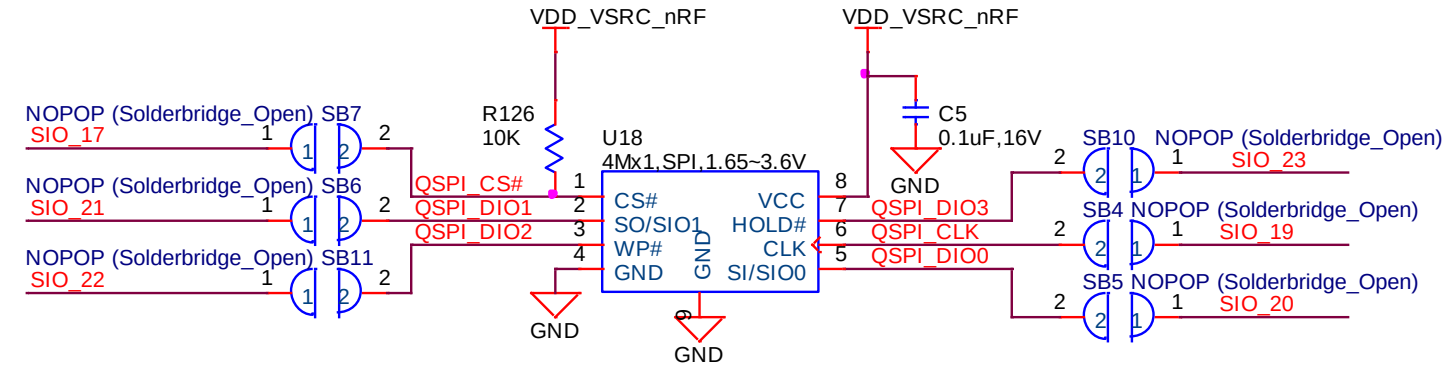

Figure 20: Optional external serial SPI flash IC (U18) schematic and PCB

Table 15 shows the U18 pin mapping to BL654PA SIO pin mapping (via open solder bridges).

Table 15: U18 SPI or QSPI flashc IC pin mapping to BL654PA GPIO mappings

BL654PA Pin (Pin Name)	U18 Pin (QSPI flash IC) and Pin Name	Via Open Solder bridge
Pin 16 (SIO_17/QSPI_CS)	Pin 1 CS#	SB7 BL654PA Dev board R126 10K pull-up on, therefore by default, device not selected. Drive from BL654PA line low to select.
Pin 14 (SIO_19/QSPI_CLK)	Pin 6 SCLK	SB4
Pin 13 (SIO_20/QSPI_DIO0)	Pin 5 SIO_0/SI	SB5
Pin 12 (SIO_21/QSPI_DIO1)	Pin 2 SIO_1/SO	SB6
Pin 11 (SIO_22/QSPI_DIO2)	Pin 3 SIO_2/WP#	SB11
Pin 9 (SIO_23/QSPI_DIO3)	Pin 7 SIO_3/HOLD#	SB10

The *smart*BASIC application for this external optional serial QSPI flash IC will be available in the future in the GitHub *smart*BASIC sample application repository: https://github.com/LairdCP/BL654PA-Applications

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8.2.7 Optional 32.76 kHz Crystal

The BL654PA on-chip 32.768kHz RC oscillator provides the standard accuracy of ±250 ppm, with calibration required every 8 seconds (default) to stay within ±250 ppm.

The BL654PA also allows, as an option, to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL654PA-SX-xx pins SIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42). This provides improved protocol timing and helps with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the Rx window must be open.

To connect the optional external 32.76kHz crystal oscillator circuit to the BL654PA module, remove R127 and R128 and short SB8 and short SB9.

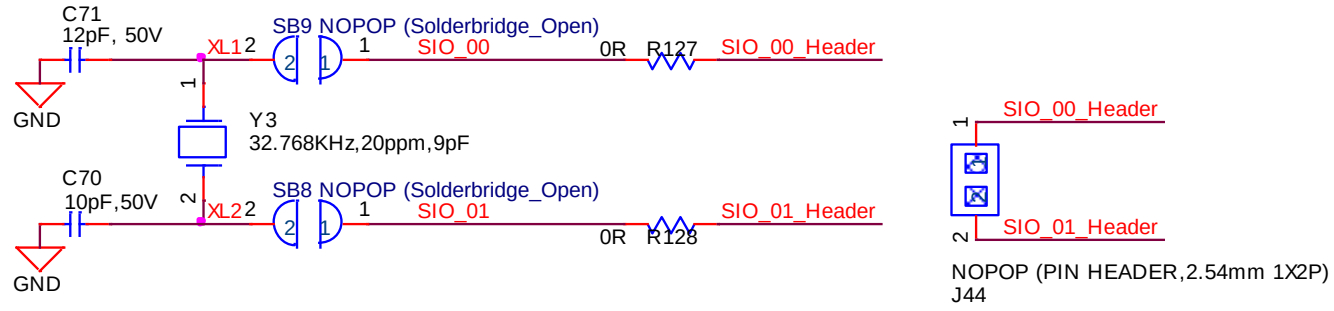

Figure 21: Optional external 32.768kHz crystal circuit schematic and PCB

A *smart*BASIC application will be available in the GitHub *smart*BASIC sample application repository at: https://github.com/LairdCP/BL654PA-Applications.

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9 OTHER FEATURES

9.1 Current Consumption Measurement

A removable jumper (on J7 and J9) is provided to break the power supply line directly to the module, allowing you to measure current consumption. For normal operation, the jumper on J7 (and J9) must be fitted (and is fitted by default).

IMPORTANT: To achieve the optimal power consumption of the BL654PA series module on the development board, see the "*lp.low.power.deep.sleep.sb*" file in the GitHub *smart*BASIC sample application repository on the BL654PA product page at https://github.com/LairdCP/BL654PA-Applications

Note: This measures the current consumption of the **BL654PA** series module ONLY.

The current drawn by the BL654PA series module can be monitored on the development board. Figure 22 shows the schematic and location of measuring points on the PCB related to current measurements.

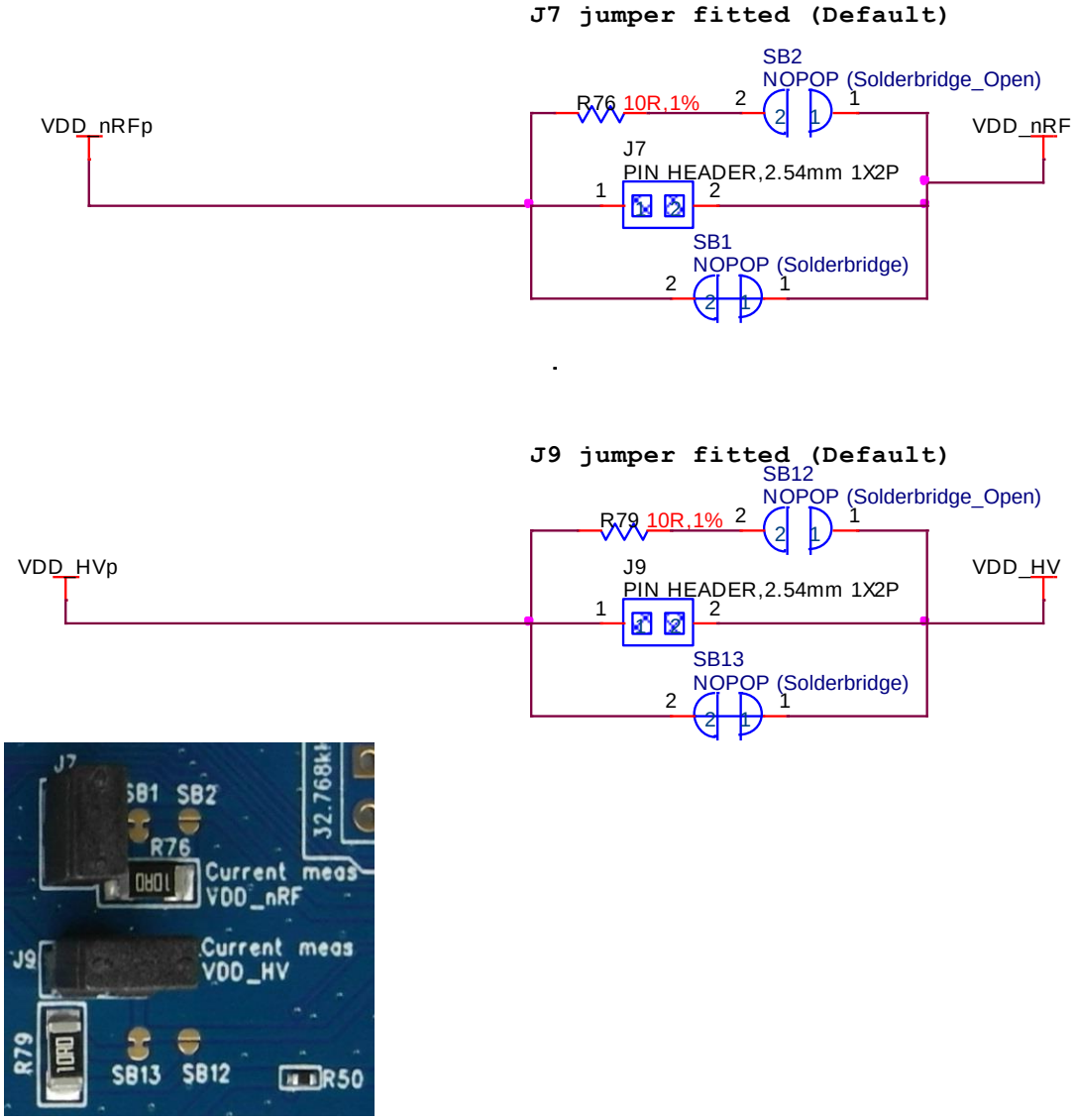

Figure 22: Current measurement schematic and PCB

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There are two primary ways to measure the current consumption:

- **Using Ammeter –** Cut solder bridge SB1 and connect an ampere meter between the two pins of J7 pins 1-2; and cut solder bridge SB13 and connect an ampere meter between the two pins of J9 pins 1-2. This monitors the current directly. This is when BL654PA is powered using the Normal voltage Mode (BL654PA operated VDD pin and VDD_HV). If the BL654PA is powered using the high voltage Mode (BL654PA operated VDD_HV pin), then only cut solder bridge SB13 and connect an ampere meter only between the two pins of J9 (pins 1-2).
- **Using Oscilloscope –** The open solder bridge SB2 first needs to be shorted with solder, then the on-board 10 Ohm resistor R76 which is mounted across J7 pins 1-2 can be used as current sense resistor. Connect an oscilloscope or similar with two probes on the pins on the J7 connector and measure the differential voltage drop. The voltage drop is proportional with current consumption. If the 10 Ohm resistor is chosen, 10 mV equals 1mA.

  This method allows the dynamic current consumption waveforms to be shown on an oscilloscope as the BL654PA radio operates. This can provide insight into power optimization.
- **Power Profiler Kit (PPK) from Nordic –** For more details, refer to http://www.nordicsemi.com/eng/Products/Power-Profiler-Kit/(language)/eng-GB

10 Additional Documentation

Laird offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the Laird BL654PA Product Page.

For any additional questions or queries, or to receive technical support for this Development Kit or for the BL654PA module series, please contact Embedded Wireless Solutions Support: https://www.lairdconnect.com/resources/support

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