

Dunglass System (CDB-PROAUDIO) User Guide

Introduction

The Dunglass system (CDB-PROAUDIO) is the hardware platform for evaluating Cirrus Logic high-performance ADC, DAC and codec devices. It provides audio inputs and outputs to Cirrus Logic devices and allows configuration and programming for a variety of possible use cases.

The Dunglass system enables streaming of 8-channel USB audio using the Jura module. It also supports SPDIF input/output (optical and electrical), as well as external audio serial port connections.

This document describes the features and usage of the Dunglass system in detail.

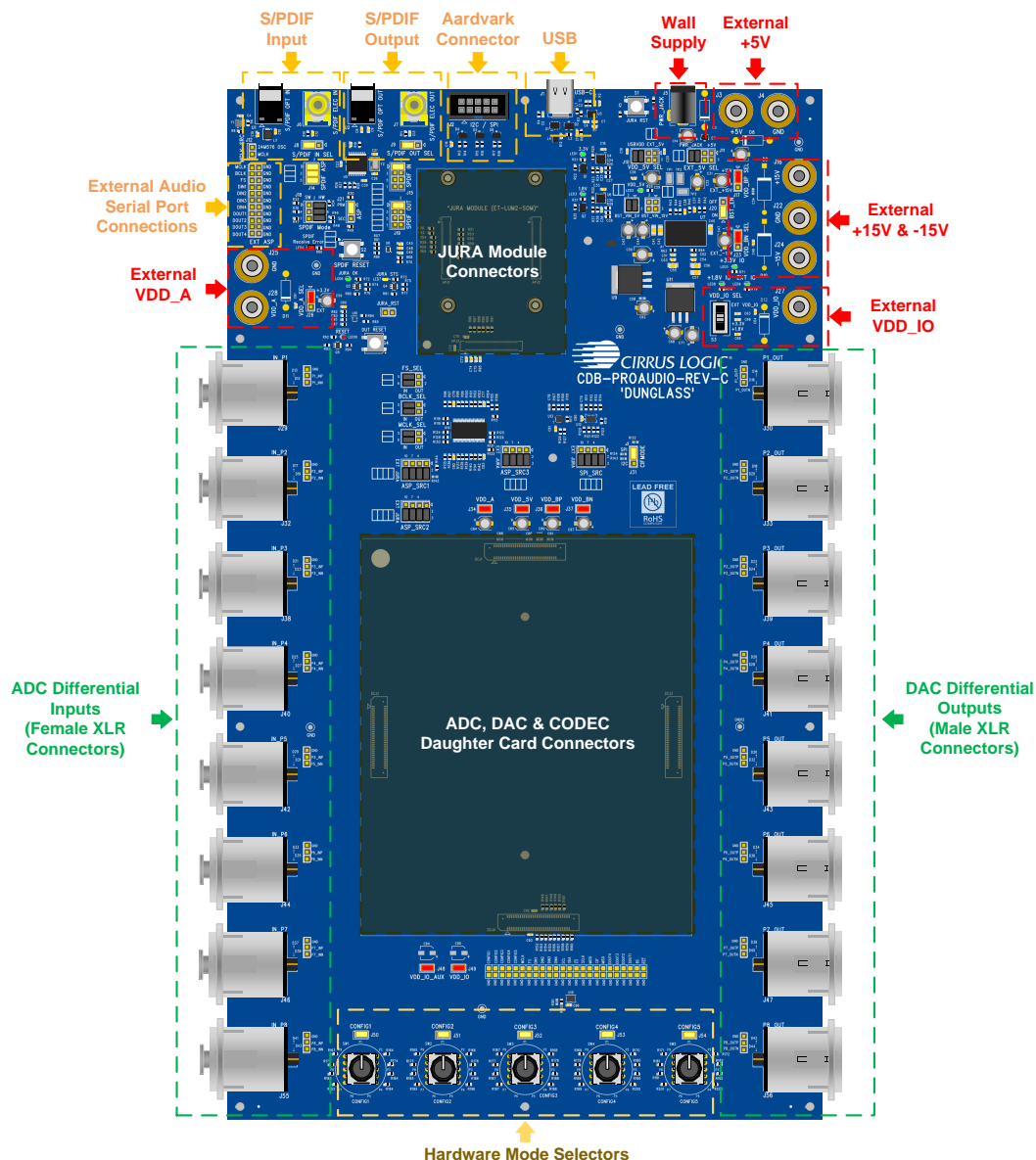


Figure 1: Dunglass (CDB-PROAUDIO) Board Overview

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1.1.1 JURA Module

The Jura module supports I2C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The Jura module is connected to the Dunglass board as shown below:

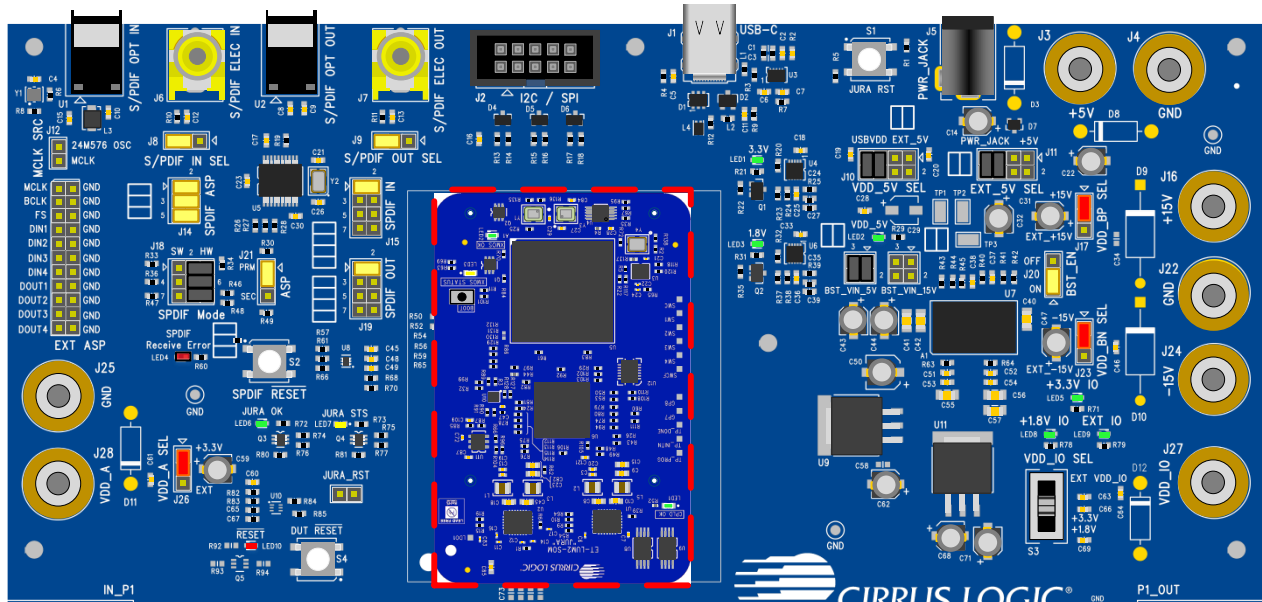


Figure 3: How to Connect JURA Module to Dunglass System

1.1.2 Dunglass Boot Procedure with Jura Module

The USB-C cable must be connected between the Dunglass system and the PC/Mac prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the Jura Module, but is typically in the range of 2 to 5 seconds after applying power to the board.

1.2 Power Options

The Dungalass system generates all the required supplies for Cirrus Logic ADC, DAC and codec daughter cards from the 5V supply rail. Alternatively, the +5V, VDD_A, VDD_IO, VDD_BP and VDD_BN power domains can be provided from individual external supplies via 4mm banana plugs.

Caution:

When connecting external power supplies, ensure that the supplies are disabled before connecting to the appropriate connector. Once all supplies are connected, enable VDD_A before all other supplies.

1.2.1 External VDD_A (+3.3V) Supply

To provide an external supply for **VDD_A**, connect a +3.3V power supply between J28 (VDD_A) and J25 (GND) and move **VDD_A SEL** (J26) Link to **EXT**.

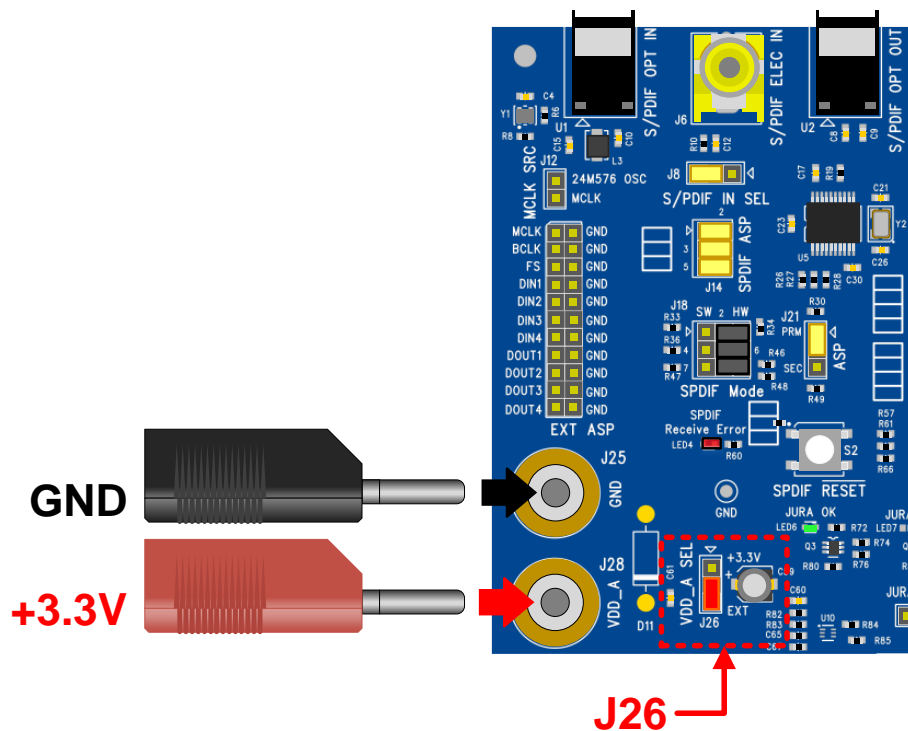


Figure 4: How to Connect External VDD_A Supply

1.2.2 External VDD_IO (+1.8V to 3.3V) supply

To provide an external supply for **VDD_IO** (+1.8V to +3.3V), connect a power supply in the range of +1.8V to +3.3V between J27 (VDD_IO) and J22 (GND) and move **VDD_IO SEL** (S3) Slider Switch to **EXT VDD_IO**.

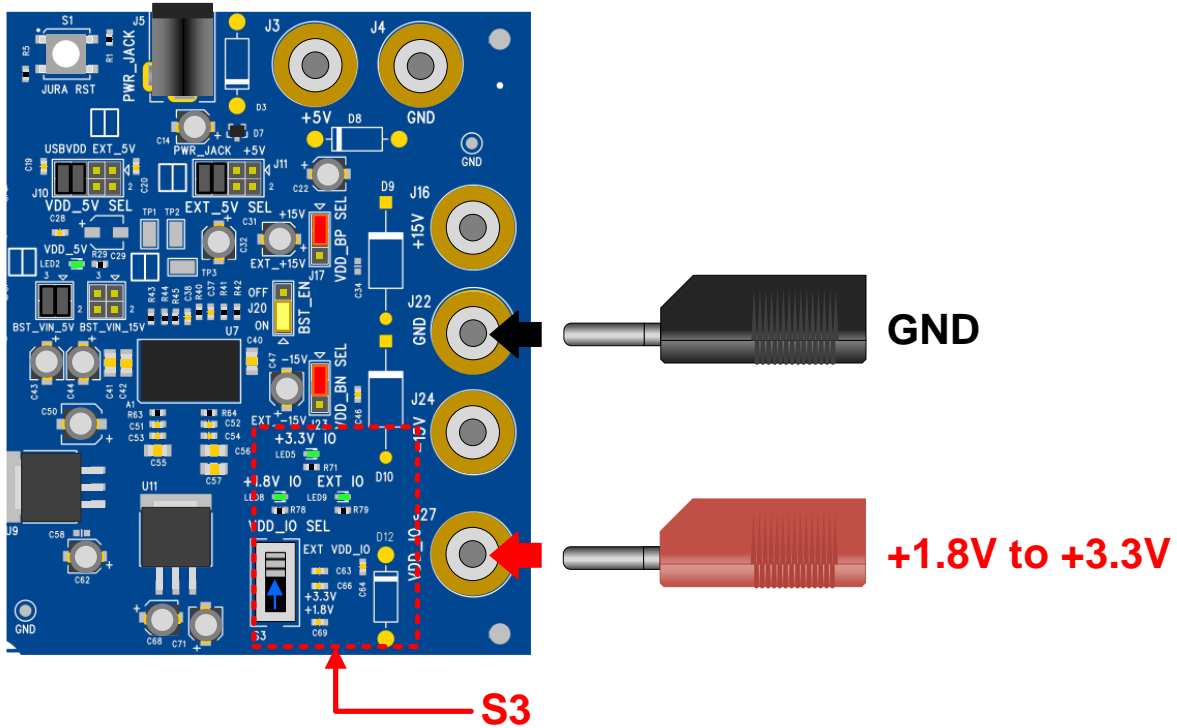


Figure 5: How to Connect External VDD_IO Supply

1.2.3 +5V Supply Source

The **+5V** supply can be provided through the PWR_JACK (J5) or else through 4mm banana plugs (J3 & J4). To select the 4mm plug source, connect a power supply between J3 (+5V) and J4 (GND) and move **EXT_5V SEL** (J11) Link to **+5V**.

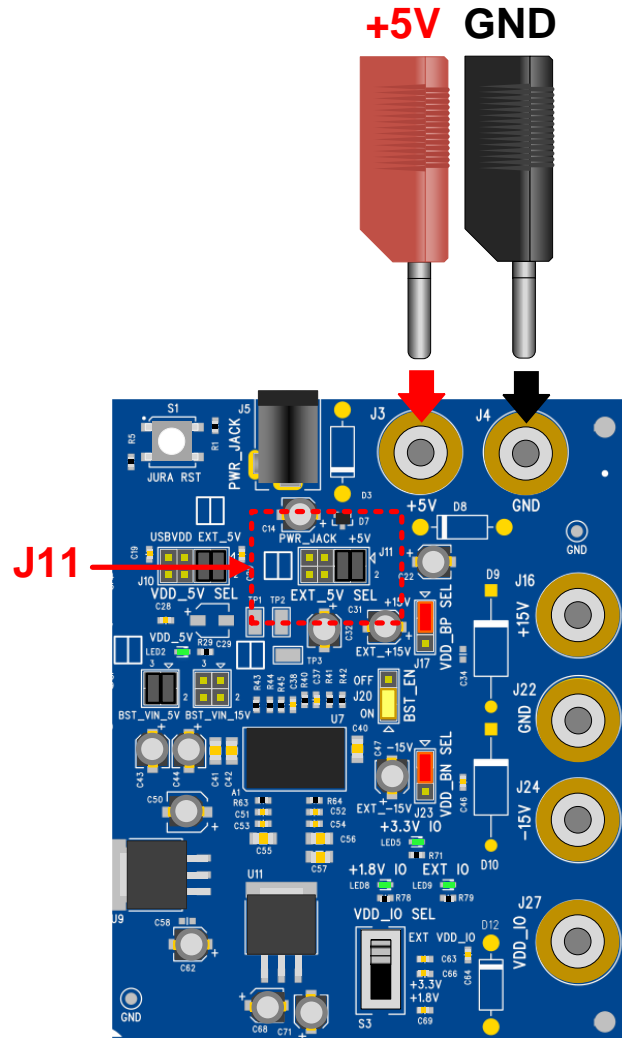


Figure 6: How to Connect External +5V Supply

1.2.4 External +15V & -15V Supply

The **+15V** and **-15V** supplies are used to power the input/output buffer filters circuits **BP** & **BN** for the ADC, DAC and codec daughter cards.

To provide an external supply for +15V & -15V, connect a +15V supply to J16 (+15V), connect a -15V supply to J24 (-15V) and connect the supply ground to J22 (GND). Move **VDD_BP SEL** (J17) link to EXT_+15V and move **VDD_BN SEL** (J23) link to EXT_-15V.

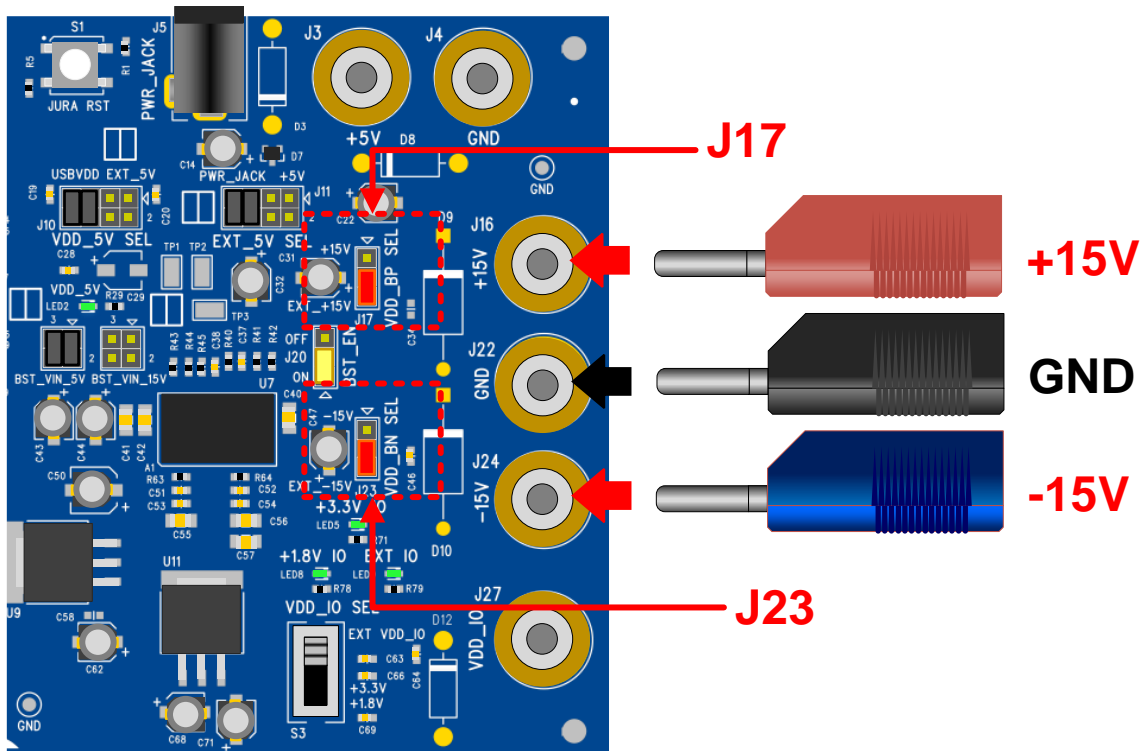


Figure 7: How to Connect External +15V & -15V Supplies

1.3 Daughter Cards

The Dunglass system works with interchangeable daughter cards to allow for a variety of ADC, DAC and codec devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

The daughter cards are connected to the Dunglass board as shown below:

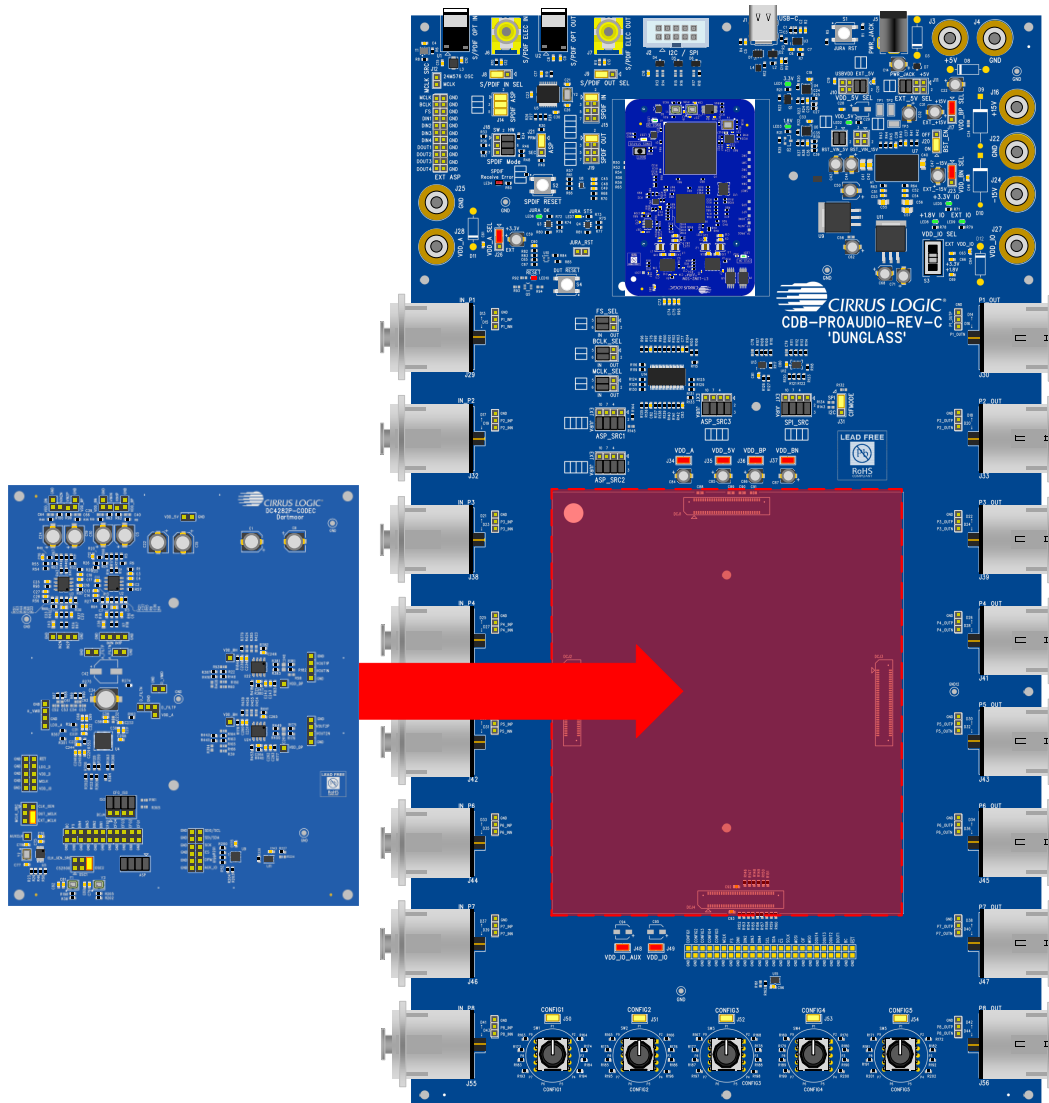


Figure 8: How to Connect Daughter Cards to Dunglass System

The DC5308P is a 4-header daughter card and should be plugged onto DCJ1, DCJ2, DCJ3 and DCJ4. The daughter card connectors are keyed and only plug in one way. There is also an alignment dot on each board to help with placement.

1.4 Buttons/Switches

Push buttons on the Dunglass system are related to power and reset functionality.

Table 1: Dunglass Buttons/Switches

Refdes	Name	Description
S1	JURA RST	Resets the Jura module to default state
S2	SPDIF RESET	Resets the SPDIF Transceiver to a default state
S3	DUT RESET	Resets all the devices on the daughter cards to a default state.

1.5 LED Indicators

Status LEDs on the Dunglass system indicate the current state of operation.

Table 2: Dunglass LED Indicators

Refdes	Color	Name	Normally Lit?	Description
LED1	Green	3.3V	Yes	Indicates the on-board 3.3V supply is enabled
LED2	Green	VDD_5V	Yes	Indicates there is +5V supply on the board
LED3	Green	1.8V	Yes	Indicates the on-board 1.8V supply is enabled
LED4	Red	S/PDIF RECEIVE ERROR	No	Set to red when there is an error receiving S/PDIF signals
LED5	Green	+3.3V IO	N/A	Indicates VDD_IO source has been set to the on-board 3.3V supply
LED6	Green	JURA OK	Yes	Indicates the Jura module has booted correctly
LED7	Yellow	JURA STS	No	Indicates the status of the Jura Module. This is illuminated during boot up
LED8	Green	+1.8V IO	N/A	Indicates VDD_IO source has been set to the on-board 1.8V supply
LED9	Green	EXT IO	N/A	Indicates VDD_IO source has been set to External VDD_IO connection
LED10	RED	RESET	No	Set to red when the daughter card is in reset

1.6 Header Connections

Headers on the Dunglass board allow for connections to other systems.

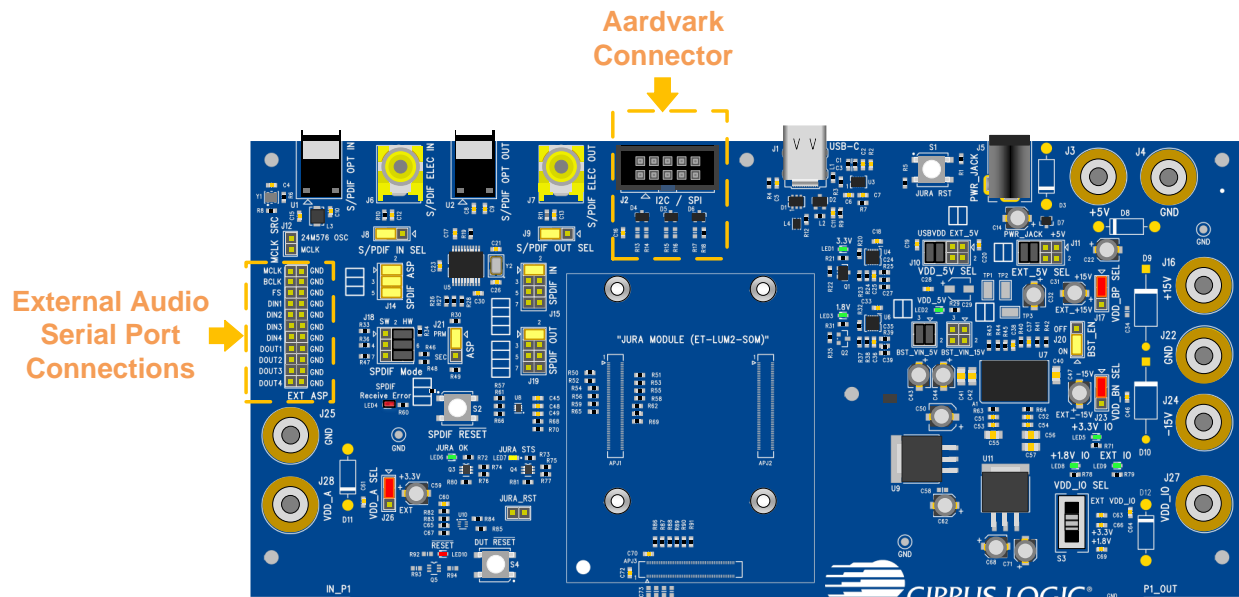


Figure 9: Aardvark & External Audio Serial Port Connections

1.6.1 I2C/SPI (Aardvark)

Header J2 (I2C/SPI) enables connection to Total Phase Aardvark™ systems for legacy compatibility and customer driver development. Note that the I2C/SPI communications for most use cases are now expected to go through the Jura module using a standard USB link that also provides USB audio streaming capability.

The Aardvark I2C/SPI signal levels must be 3.3V; on-board level shifters are provided to convert these signal levels to the VDD_IO voltage domain.

1.6.2 External ASP (Audio Serial Port)

The EXT ASP header supports connection to Audio Precision testing equipment through the PSIA (Programmable Serial Interface Adapter) hardware. This is an I2S-based digital audio interface with 3.3V signal levels.

MCLK	●	GND
BCLK	●	GND
FS	●	GND
DIN1	●	GND
DIN2	●	GND
DIN3	●	GND
DIN4	●	GND
DOUT1	●	GND
DOUT2	●	GND
DOUT3	●	GND
DOUT4	●	GND
EXT ASP		

Figure 10: External Audio Serial Port Connections

The silkscreen markings on the Dunglass system identify the pin functions. Note the DIN and DOUT directions are

referenced to the daughter card device, i.e., the pin marked "DOUT" is an output from the device on the daughter card.

1.7 Jumper Links

Jumper links are provided on the Dunglass board; these are related to signal routing and power supply rails.

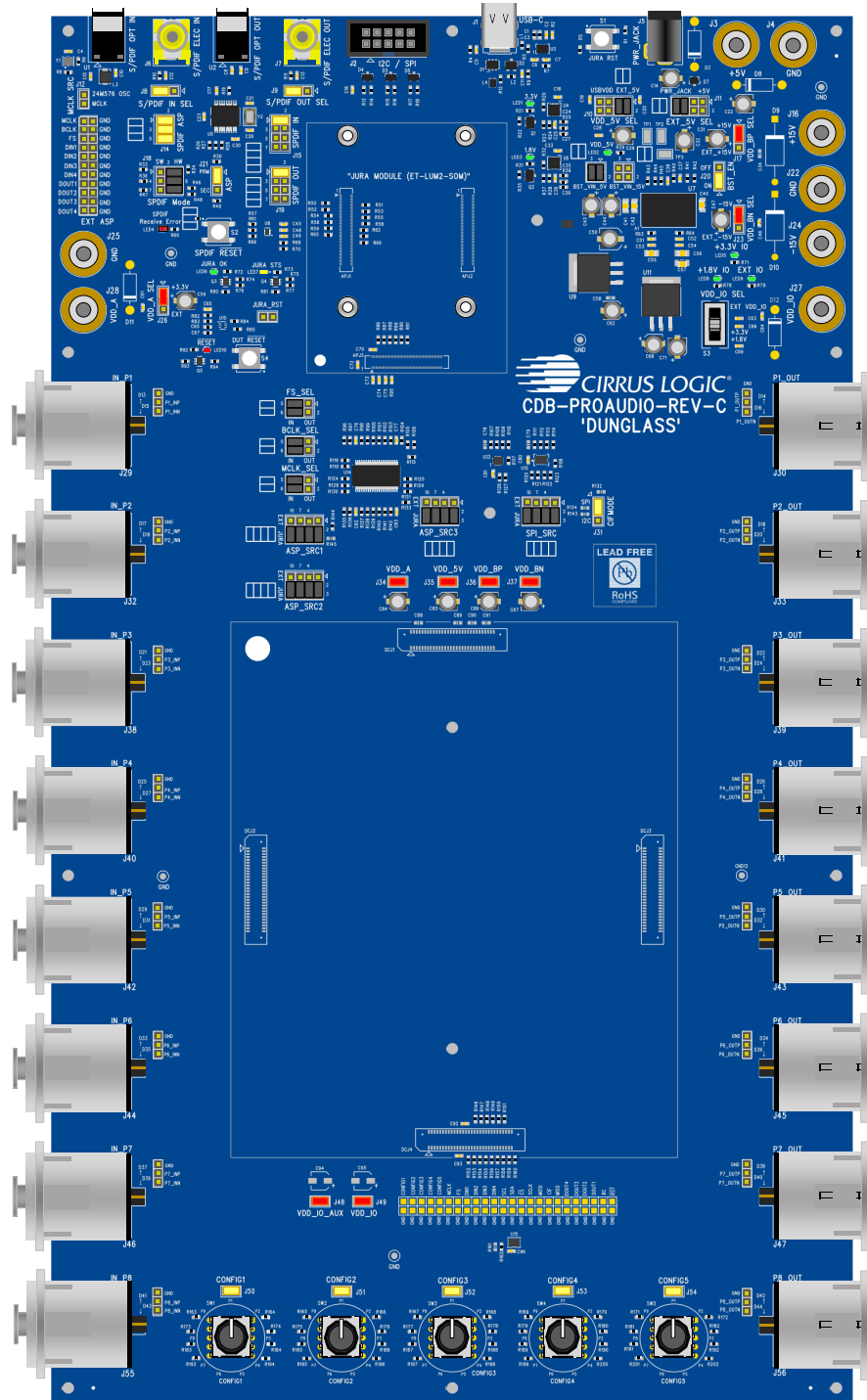


Figure 11: Dunglass Jumper Links

1.7.1 Power Supply Jumper Links

The power-supply jumper links allow isolation of supply rails from the daughter card, or selection of a power supply.

Table 3: Power Supply Jumper Links

Header Name	Description	Default Link Position	Notes
VDD_5V SEL (J10)	Main board +5V source	EXT_5V	
EXT_5V SEL (J11)	External +5V source	PWR_JACK	Selects the source for the external +5V supply.
BST_EN (J20)	Enable for onboard +15V & -15V boost/invertor convertor	ON	The boost should only be disabled if an external +15V and -15V is supplied Via J16 & J24.
VDD_BP SEL (J17)	Positive buffer/filter supply source	+15V	Selects the source for the positive buffer/filter supply
VDD_BN SEL (J23)	Negative buffer/filter supply source	-15V	Selects the source for the negative buffer/filter supply
VDD_A SEL (J26)	Analog (VDD_A) supply source	+3.3V	+3.3V is the on-board 3.3V supply
VDD_A (J34)	VDD_A supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_A supply to daughter card.
VDD_5V (J35)	VDD_5V supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_5V supply to daughter card.
VDD_BP (J36)	VDD_BP supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_BP supply to daughter card.
VDD_BN (J37)	VDD_BN supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_BN supply to daughter card.
VDD_IO_AUX (J48)	VDD_IO_AUX supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_IO_AUX supply to daughter card.
VDD_IO (J49)	VDD_IO supply isolation for daughter card	ON	Can be used to isolate or measure current of VDD_IO supply to daughter card.

1.7.2 Signal Routing Jumper Links

The signal-routing links configure where the audio serial port and control interfaces are connected to.

Table 4:Signal Routing Jumper Links

Header Name	Description	Default Link Position	Notes
MCLK_SRC (J12)	24.576MHz CMOS oscillator selector	OFF	The 24.576MHz oscillator is available to support SPDIF and EXT ASP connections.
S/PDIF IN SEL (J8)	S/PDIF input source (electrical or optical)	Electrical (1-2)	
S/PDIF OUT SEL (J9)	S/PDIF output source (electrical or optical)	Electrical (1-2)	
SPDIF ASP (J14)	SPDIF MCLK, BCLK & FSYNC isolation to EXT_ASP header	ON (1-2)	These headers must be populated when using the SPDIF transceiver
SPDIF IN (J15)	SPDIF IN isolation to EXT_ASP header	DIN1 (1-2): ON DIN2 (3-4): OFF DIN3 (5-6): OFF DIN4 (7-8): OFF	At least one of these headers must be populated when using the SPDIF receive
SPDIF OUT (J19)	SPDIF OUT isolation to EXT_ASP header	DOUT1 (1-2): ON DOUT2 (3-4): OFF DOUT3 (5-6): OFF DOUT4 (7-8): OFF	A maximum of one of these headers must be populated when using the SPDIF transmit
ASP (J21)	SPDIF transceiver ASP mode	SEC (2-3)	
SPDIF Mode (J18)	SPDIF transceiver control mode (software or hardware mode)	SW (1-2, 4-5, 7-8)	
JURA_RST	JURA connection to DUT RESET line	ON (1-2)	
SPI_SRC	Source for SPI Interface (JURA or EXT(J2))	JURA (2-3, 5-6, 8-9, 11-12)	EXT = SPI interface connected to I2C/SPI (Aardvark) Header (J2). JURA = SPI interface connected to Jura SPI interface
CIFMODE	Configures which control interface the devices on the daughter cards use. (SPI or I2C)	SPI (1-2)	SPI = Daughter card control interface is SPI I2C = Daughter card control interface is I2C
MCLK_SEL	Selects the direction of the external MCLK signal (IN or OUT)	IN (3-5, 4-6)	IN = EXT ASP Headers to daughter card OUT =Daughter card to EXT ASP Headers
BCLK_SEL	Selects the direction of the external BCLK signal (IN or OUT)	IN (3-5, 4-6)	IN = EXT ASP Headers to daughter card OUT =Daughter card to EXT ASP Headers
FS_SEL	Selects the direction of the external FSYNC signal (IN or OUT)	IN (3-5, 4-6)	IN = EXT ASP Headers to daughter card OUT =Daughter card to EXT ASP Headers
ASP_SRC1	Selects the ASP connection (EXT or JURA)	JURA (2-3, 5-6, 8-9, 11-12)	EXT = EXT ASP connected to daughter card ASP JURA = JURA connected to daughter card ASP
ASP_SRC2	Selects the ASP connection (EXT or JURA)	JURA (2-3, 5-6, 8-9, 11-12)	EXT = EXT ASP connected to daughter card ASP JURA = JURA connected to daughter card ASP
ASP_SRC3	Selects the ASP connection (EXT or JURA)	JURA (2-3, 5-6, 8-9, 11-12)	EXT = EXT ASP connected to daughter card ASP JURA = JURA connected to daughter card ASP
CONFIG1 (J50)	CONFIG1 signal isolation for daughter card	ON	
CONFIG2 (J51)	CONFIG2 signal isolation for daughter card	ON	
CONFIG3 (J52)	CONFIG3 signal isolation for daughter card	ON	
CONFIG4 (J53)	CONFIG4 signal isolation for daughter card	ON	
CONFIG5 (J54)	CONFIG5 signal isolation for daughter card	ON	

2 Hardware Mode Control

The Dunglass system supports the hardware control modes for Cirrus Logic high-performance ADC, DAC and codec devices. These are supported via the rotary switches on the Dunglass system.

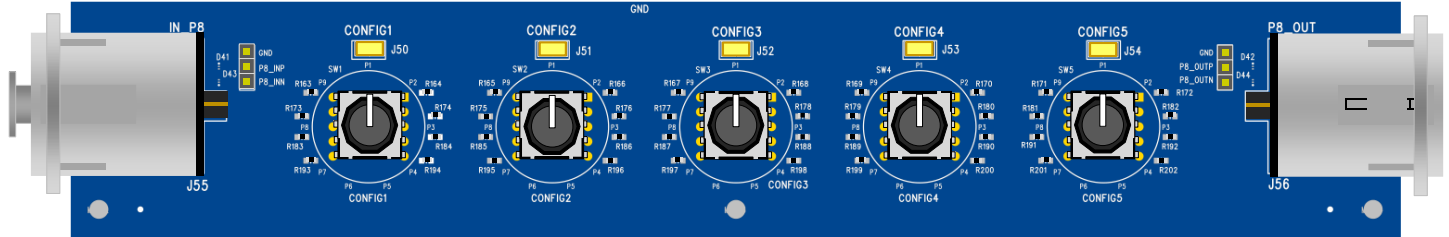


Figure 12: Dunglass Rotary Switches for Hardware Control Mode

The board silkscreen indicates the position of each switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground. See Table below:

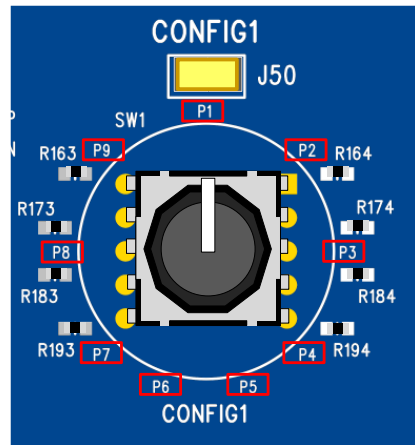


Figure 13: Rotary Switch

Table 5: Dunglass Rotary Switch Positions

Switch Position	Config Pin Configuration	
P1	Pull-up to VDD_A	0 Ω
P2		4.7 k Ω
P3		22 k Ω
P4		100 k Ω
P5	Pull-Down to GND	100 k Ω
P6		22 k Ω
P7		4.7 k Ω
P8		0 Ω
P9	No Connection	

3 I2C/SPI Software Control

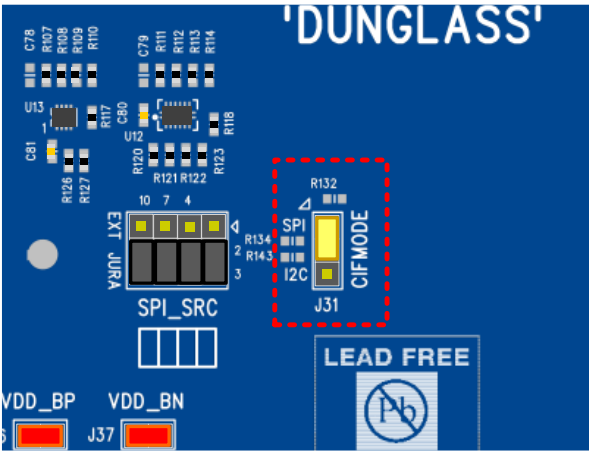
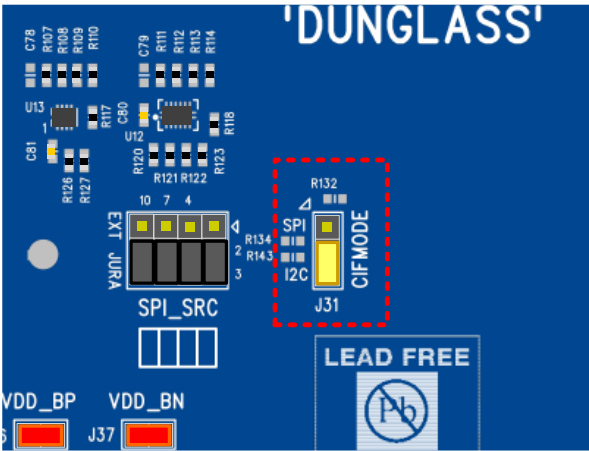
Software control of the Dunglass system and the connected daughter card is supported via the Jura module and the I2C/SPI (Aardvark) header (J2). The system supports I2C and SPI control modes.

3.1 Selecting Control Interface Mode

The control mode used for the daughter card is configured using the **CIFMODE (J31)** header.

- SPI = Daughter card control interface is SPI
- I2C = Daughter card control interface is I2C

Table 6: Control Interface Mode Selection

 <p>Select SPI Control Interface for Daughter Card</p>	 <p>Select I2C Control Interface for Daughter Card</p>
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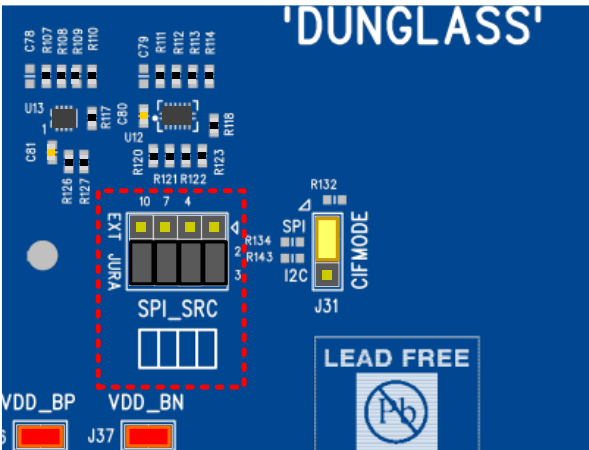
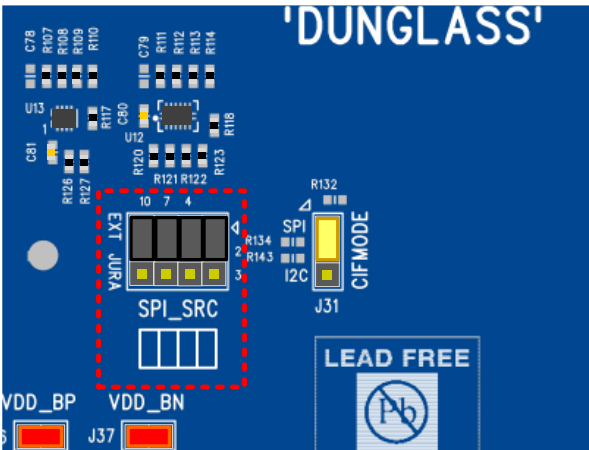
The I2C control interface is supported simultaneously on the Jura module and Aardvark header. If the SPI interface mode is selected, the controller must be selected as described in Section 3.2.

3.2 Configuring the SPI Interface Controller

The SPI control interface can be provided by the Jura module or by the I2C/SPI (Aardvark) header (J2). The source of the SPI interface is configured using the **SPI_SRC** header.

- JURA = SPI interface connected to Jura SPI interface
- EXT = SPI interface connected to I2C/SPI (Aardvark) header (J2)

Table 7: SPI Control Interface Source

 <p>Select Jura Module as SPI Interface Source</p>	 <p>Select I2C/SPI Header as SPI Interface Source</p>
---	---

4 Driver Installation and SoundClear Studio Support

4.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

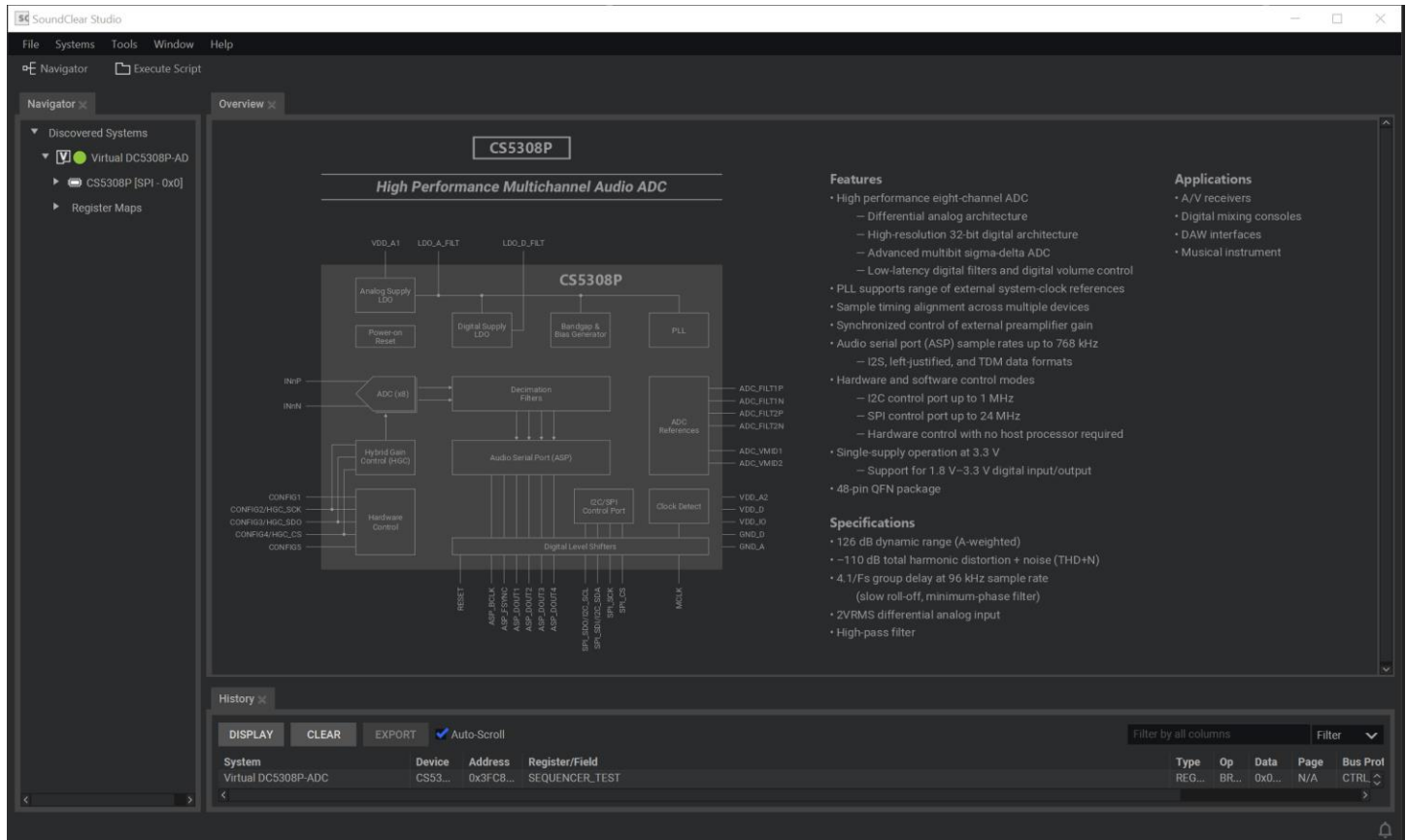


Figure 14: SoundClear Studio

4.1.1 Download SoundClear Studio Software

By downloading software from the Cirrus Logic website, you agree to the terms of our license agreement. Please read it before downloading.

- The latest release of SoundClear Studio is available on the Cirrus Logic website from the product pages of supported devices such as CS5308P: <https://cirrus.com/products/cs5308p/>

4.2 SoundClear Studio Quick Start Guide

4.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

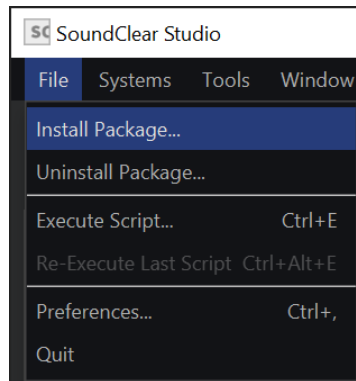


Figure 15: SoundClear Studio – Installing Board Packages

4.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

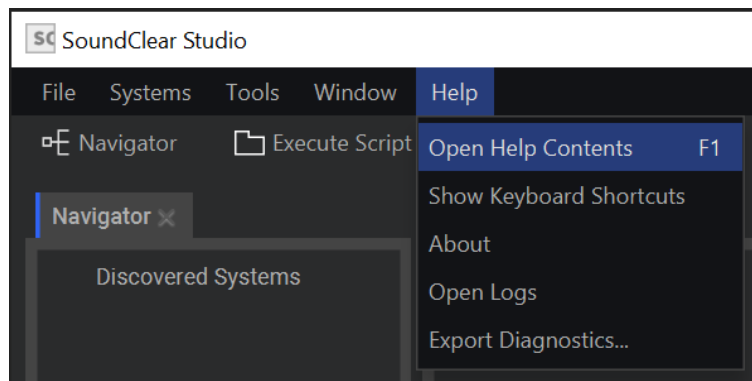


Figure 16: SoundClear Studio – User Guide

A virtual (non-hardware) version of the system can be created using “**Systems → Add Virtual System...**”



sc

Add Virtual System

×

ADD VIRTUAL SYSTEM

Name

Virtual DC5308P-ADC

☒ Add an installed system

DC5308P-ADC

×

☐ Add from a definition file

Choose definition file

☐ Create an empty system

System: DC5308P-ADC

Hardware ID: a5d3c080

File path: C:\ProgramData\Cirrus Logic\SCS_1.7\systems\cs5308p\cs5308p.xml

Device count: 1

Device type: CS5308P

Name: CS5308P

Revision: 0

Control interface: CTRL_I2C

...

CANCEL

ADD

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

4.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select “**Add Device...**”

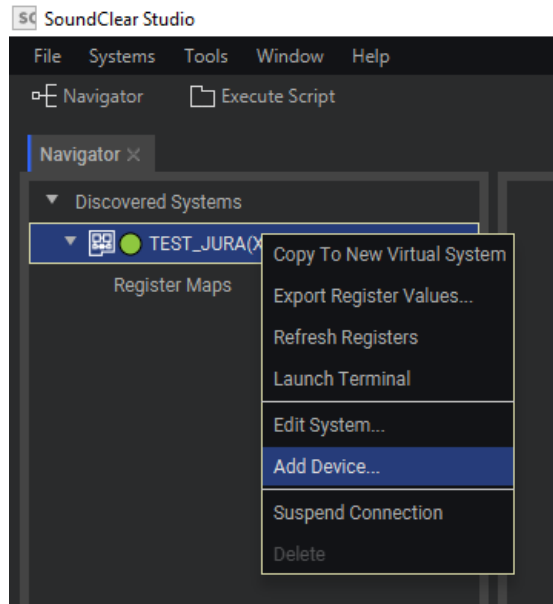


Figure 19: SoundClear Studio – Adding an Existing System

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected “**Edit Device...**”):

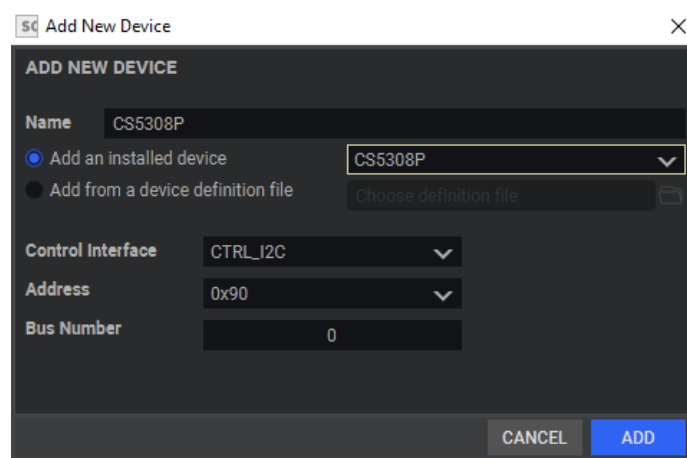


Figure 20: SoundClear Studio – Adding an Existing System

4.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the device into desired states, which can then be executed from SoundClear Studio using **“File→Execute Script...”**

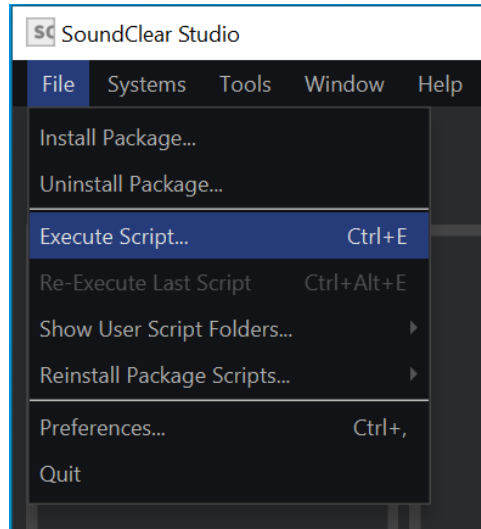


Figure 21: SoundClear Studio – Executing Script

The daughter card SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

This folder can be accessed via **“File→Show User Script Folder...→<Package Name>”**

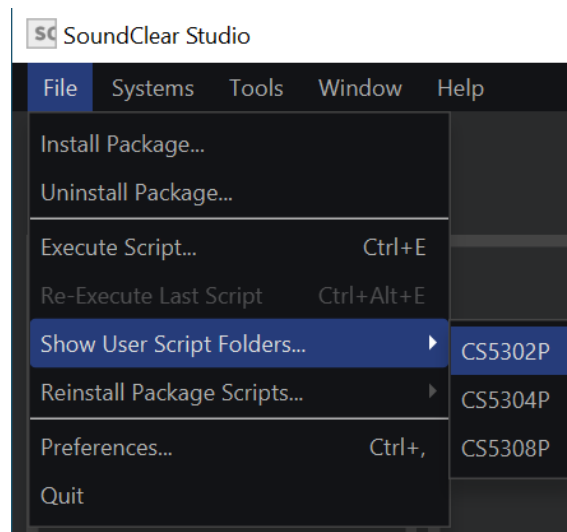


Figure 22: SoundClear Studio – Show User Script Folder

5 Digital Audio

This section describes the digital audio inputs and outputs on the Dunglass system, and how to configure the routing. The digital audio signals to/from the daughter card can be connected to the Jura module or to the EXT ASP header/SPDIF.

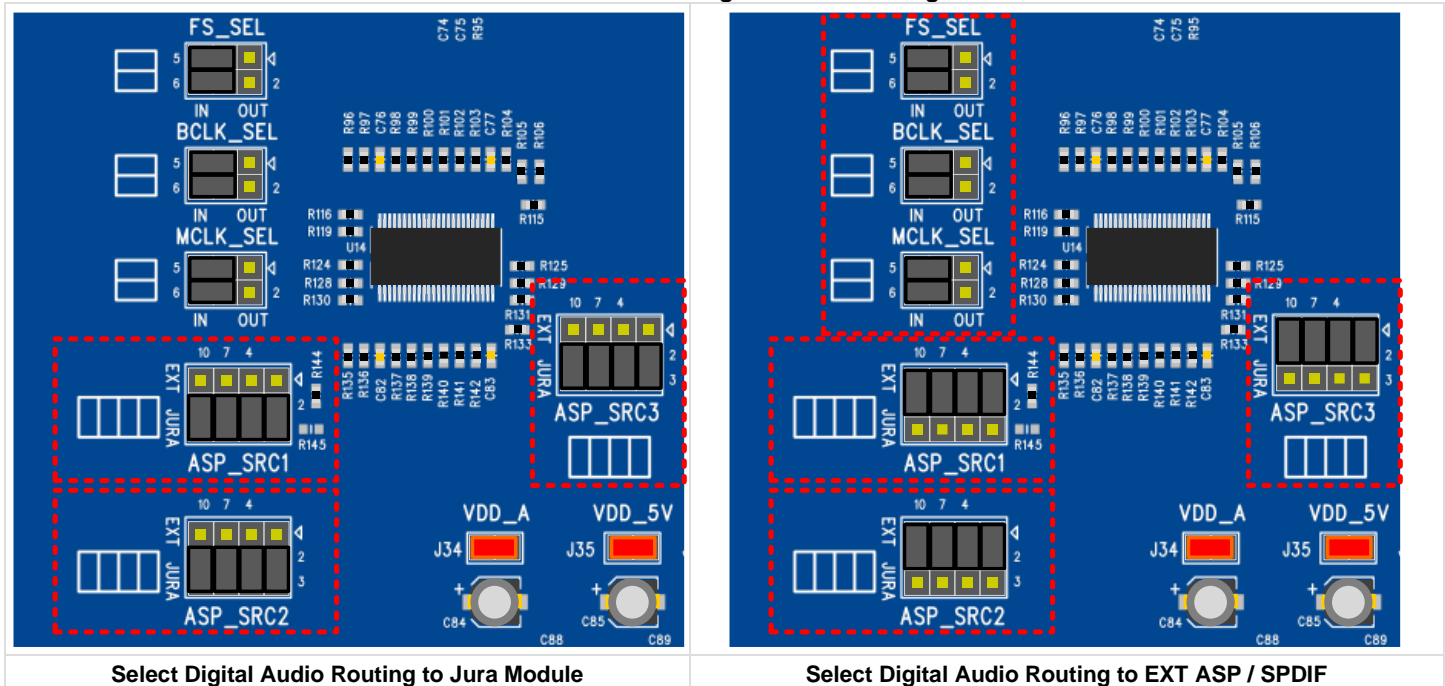
5.1 Routing the Digital Audio Signals

The digital audio paths to/from the daughter card can be routed to the Jura module, or else to the EXT ASP header and S/PDIF transceiver. The routing is configured using the **ASP_SRC1**, **ASP_SRC2** & **ASP_SRC3** headers.

- JURA = Digital audio signals routed to Jura module.
- EXT = Digital audio signals routed to EXT ASP header/SPDIF.

The **ASP_SRC1**, **ASP_SRC2** & **ASP_SRC3** headers are configured as shown in Table 8.

Table 8: Digital Audio Routing



The Jura module always operates in Primary Mode – the MCLK, BCLK and FSYN are generated by the Jura module, as inputs to the daughter card.

If the digital audio is routed to the EXT ASP header and S/PDIF transceiver, the direction of the MCLK, BCLK, and FSYN signals must be configured using the MCLK_SEL, BCLK_SEL & FS_SEL headers:

- The MCLK_SEL sets the direction of the MCLK signal to/from the daughter card; IN configures the EXT ASP header/SPDIF as the MCLK input to the daughter card; OUT configures the daughter card as the MCLK source.
- The BCLK_SEL and FS_SEL links select the direction of the BCLK and FSYN signals to/from the daughter card.

See Section 1.6.2 for details of the EXT ASP header. Note that the EXT ASP header and S/PDIF transceiver use 3.3V logic levels; a level shifter is incorporated to interface with the configured VDD_IO domain.

5.2 SPDIF

The Dunglass system supports S/PDIF input/output via optical and electrical connectors. The Dunglass system uses the WM8804 S/PDIF transceiver chip at sample rates up to 96kHz (optical) or up to 192kHz (electrical).

The board configuration for S/PDIF input/output differs depending on which daughter card is connected. Refer to the daughter card documentation to configure the Dunglass system for S/PDIF input/output.

6 Jura module - USB Audio Streaming

The Jura module board presents itself as a USB audio device (Class 2) to the host PC to transfer audio data.

Do not reset or power down when streaming USB Audio.

If the Jura module board is streaming USB Audio when it is reset, the Windows audio drivers will stall. This is a common issue with Windows audio drivers when using external USB sound cards. When the Jura module is reconnected to the system, it may then fail to connect to SoundClear Studio due to audio driver issues. In this case it is recommended to restart SoundClear Studio and the application streaming audio. If a failed attempt at connecting to SoundClear Studio has already occurred, the Dunglass+Jura system may need to be powered down and powered back up again along with restarting the software in order to re-establish communications with the system.

6.1 CLUSBAudio Control Panel

The CLUSBAudio Control Panel on Windows is for the Jura module USB audio streaming system. A link to the panel can be found in the Cirrus Logic folder in the Start Menu:

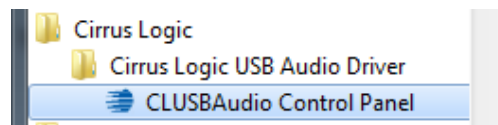


Figure 23: CLUSBAudio Control Panel

The main **Status** tab of the CLUSBAudio Control Panel indicates the current sample rate of the Jura module. This is determined by either the Windows drivers setting (for DirectSound) or the audio software (for ASIO or WASAPI).

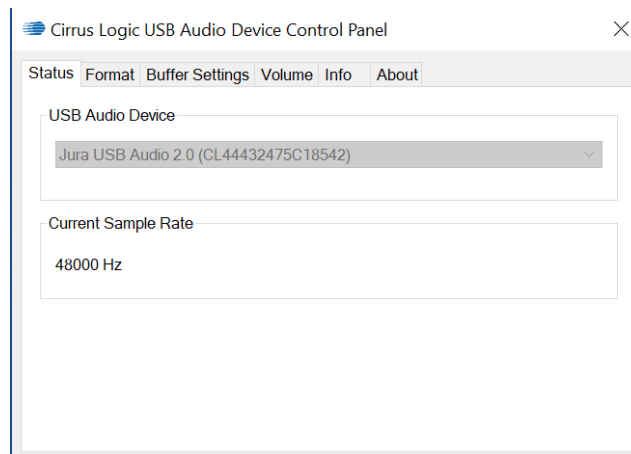


Figure 24: CLUSBAudio Control Panel – Status Tab

The **Format** tab can be used to specify the audio format.

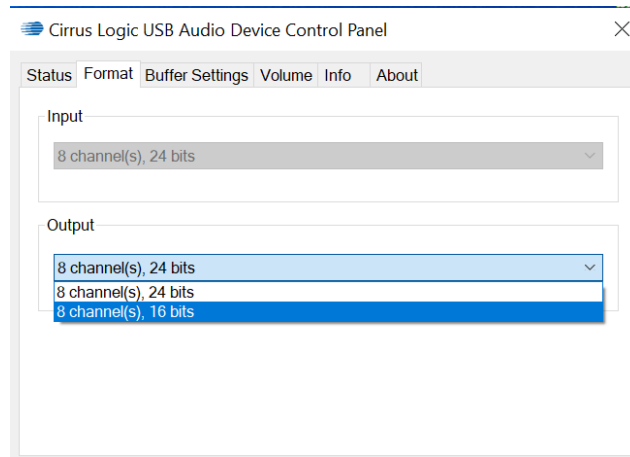


Figure 25: CLUSBAudio Control Panel – Format Tab

For all use cases, the recommended setting is “8 channels, 24 bits”.

The format of the input channels should match that of the output channels. Note that the input and output format selection made here applies to the audio streaming device regardless of the audio drivers used (ASIO, WASAPI, DirectSound) so it is important to make sure this selection is correct.

The **Buffer Settings** tab settings can be modified to provide a larger or smaller USB buffer, but be aware that some applications (e.g. Adobe Audition) may have problems with particular combinations of sample rate and buffer size. The "safe mode" setting provides extra tolerance for ASIO audio applications if they are not able to keep up with the audio demand at the expense of a slightly increased latency. It is recommended to keep this option enabled.

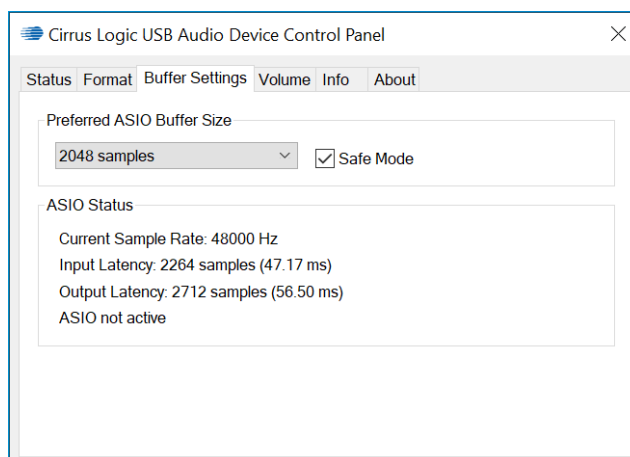


Figure 26: CLUSBAudio Control Panel – Buffer Settings Tab

6.2 Using Jura module with Windows WDM

Jura module can act and function as a normal stereo USB audio device on a Windows system using Windows WDM drivers. Although Windows Vista introduced native support for WASAPI, WDM is still the default audio driver for all Windows OS versions.

Stereo audio from standard Windows applications (Media Player, iTunes®, Spotify®, web browsers) can be routed through the Jura module by simply selecting it as the default audio device on the system within the control panel.

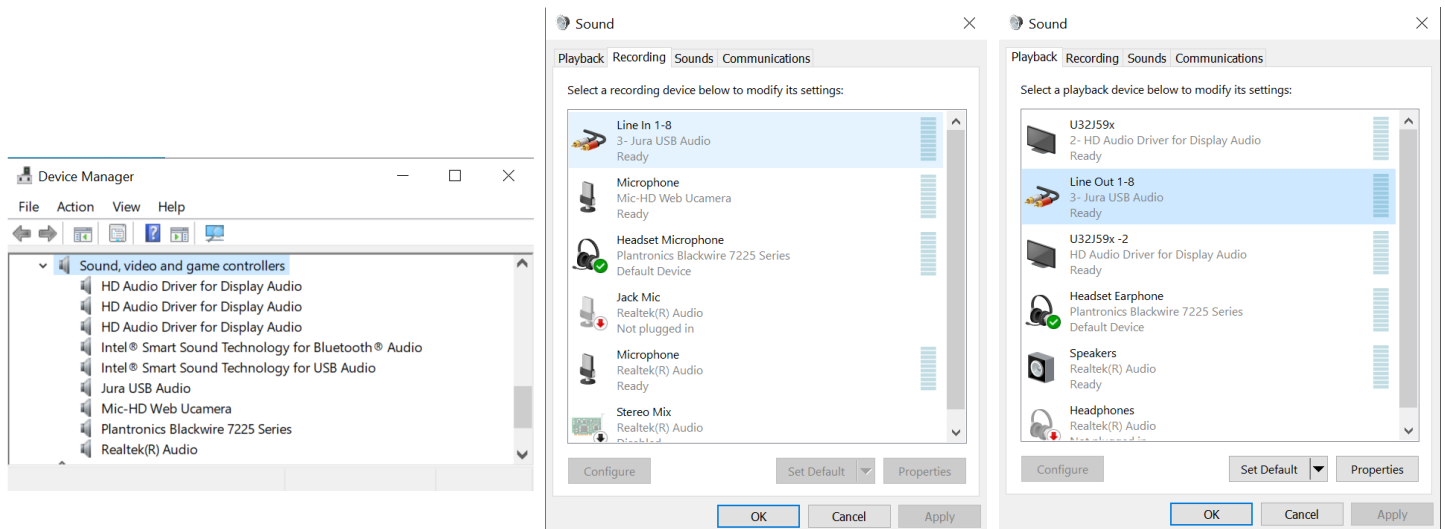


Figure 27: Windows WDM

The WDM driver has some limitations. The driver only supports two channels, and all audio is resampled by Windows to the sample rate set within the advanced panels of the "Recording Properties" display (accessed by right-clicking on "Line IN 1-8/ Jura USB Audio" in the window shown above). The input channels operate at the rate set within the advanced panel of the "Line Properties" display.

The playback and record sample rates must be set to the same value. It is also important to ensure that the format for the recording device matches the configuration of the CLUSBAudio panel in terms of number of channels and bit depth.

6.3 Using Jura module with ASIO

ASIO drivers for Windows are installed as part of the Jura module SoundClear Studio package.

Using ASIO allows up to eight channels (full duplex) to be transferred to/from the Jura module board and provides higher bandwidth, lower latency, less jitter and un-mixed/un-distorted audio that bypasses the Windows kernel mixer. However, this requires specialist audio software such as Adobe Audition to interface with the ASIO drivers.

6.4 I2S Format on Jura Module

Regardless of which audio driver type is used, the onboard USB audio streamer device converts the eight channels of audio data from the PC into four data streams, each in 2-channel I2S format.

The output format from the USB streaming peripheral uses a two-channel I2S format, regardless of the number of active channels transmitted or received from the PC. The USB streamer always drives the BCLK and LRCLK signals (Primary Mode), as the sample rate is dictated by the CLUSBAudio driver. When the USB streaming audio is routed to a Cirrus Logic smart codec ASP peripheral, the ASP port of the Cirrus Logic device should be configured in Secondary Mode and should expect data in this format.

6.5 Jura module USB Audio BCLK Rates

The USB audio streaming peripheral always generates the MCLK, BCLK and LRCLK signals on the I2S bus, and the sample rate is dictated by the PC side through the audio drivers. This means that the BCLK generated by the USB audio streamer is determined by the sample rate settings on the PC.

Table 9: Jura Module USB Audio BCLK Rates

Sample rate (kHz)	BCLK Frequency (MHz)
44.1	2.8224
48.0	3.072
88.2	5.6448
96.0	6.144
176.4	11.2896
192.0	12.288

7 Notices

Jura firmware development utilizes components under the following licenses:

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Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

8 Revision History

Revision History

Revision	Changes
R1 May 2023	• Initial version.
R2 OCT 2023	• Soundclear Studio Scripts section updated
R3 JUN 2024	• Diagrams updated

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.

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