Application Note

AEAT-9955

Magnetic Encoder IC: 10-Bit to 18-Bit Programmable Angular Magnetic Encoder with Safety

Description

The Broadcom® AEAT-9955-Q32 is a CMOS magnetic sensor structure that is suitable for contactless 360° encoding based on the Hall effect. It provides an angle output up to 18 bits of resolution and simultaneous incremental output up to 20,000 CPR. An integrated Hall structure at the core of the device uses a single 2-pole disc or ring magnet to convert the magnetic field vector in the chip plane into an AC signal whose amplitude and phase correspond to the magnitude and direction of the field.

An internal digital-signal-processing unit then processes and conditions the raw AC signal from the sensor. The output signals are available in three different forms:

- Pulse-width modulation (PWM)
- Absolute 18-bit position through the 3-wire and 2-wire Synchronous Serial Interface (SSI) and the 4-wire Serial Protocol Interface (SPI)
- Incremental output (ABI and UVW signals)

These features can be programmed by configuring the internal registers in program mode.

More information about the AEAT-9955-Q32 product specifications is available in the product data sheet.

Operation Mode

The AEAT-9955-Q32 features two types of operational modes: normal operation mode and configuration mode.

Normal Operation Mode

Normal mode is the normal operating mode of the chip. The absolute output (10-bit to 18-bit absolute position data) is available through serial protocol pins (M0, M1, M2, and M3). The following are the output signal conditions during AEAT-9955-Q32 initialization:

- PWM signals all 0s.
- ABI signals all 1s.
- UVW signals all 0s.

The incremental positions are indicated on ABI and UVW signals with a user-configurable CPR from 0 to 20,000 of ABI signals and pole pairs from 1 to 32 (2 to 64 poles) for UVW commutation signals.

Configuration Mode

The AEAT-9955-Q32 has a built-in memory for multiple-time programming (MTP).

Programming of the AEAT-9955-Q32 can be performed with the HEDS-9955 programming kit or any tester/programmer device using the guidelines provided.

Absolute and Incremental Programming

The absolute resolution can be set to 10, 11, 12, 13, 14, 15, 16, 17, or 18 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI protocol. Writing specific commands to specific addresses of the internal registers will program values of shadow registers to memory. The memory can be programmed multiple times.

Memory Map

The AEAT-9955-Q32 uses nonvolatile EEPROM as shown in the tables that follow. The memory is separated into 32 pages with 8 bits per address. EEPROM programming can be performed at 3.3V or 5V supply.

Nonvolatile Register (EEPROM)

MTP shadow registers are volatile registers that are loaded with corresponding MTP values after power-on.

All bits (except addresses 0x10 and 0x20–0x27) are in LOCK mode by default after power-on. To enter UNLOCK mode, write 0xAB to address 0x10.

In UNLOCK mode, you may write to any registers. Values written will remain until power-off.

The UNLOCK state is maintained until the power supply is turned off or any value (except 0xAB) is written to address 0x10.

MTP Shadow Registers

1. MTP shadow registers are volatile (upon power-up, the values are reloaded from EEPROM) and are not automatically written to EEPROM.
2. To write MTP shadow registers values to EEPROM (nonvolatile) memory, see EEPROM Programming.
3. The MTP shadow registers are from address 0x10 to address 0x27.

The tables that follow show the registers.

Customer Configuration Registers

The following registers are available for users to store information and configure the encoder as required.

Table 1: Customer Reserved Registers

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h0
0x01	[7:0]	Customer Reserve 1	User programmable	8'h0
0x02	[7:0]	Customer Reserve 2	User programmable	8'h0
0x03	[7:0]	Customer Reserve 3	User programmable	8'h0
0x04	[7:0]	Customer Reserve 4	User programmable	8'h0
0x05	[7:0]	Customer Reserve 5	User programmable	8'h0
0x06	[7:0]	Customer Reserve 6	User programmable	8'h0
0x07	[7:0]	Customer Reserve 7	User programmable	8'h0
0x08	[7:0]	Customer Reserve 8	User programmable	8'h0
0x09	[7:0]	Customer Reserve 9	User programmable	8'h0
0x0A	[7:0]	Customer Reserve 10	User programmable	8'h0
0x0B	[7:0]	Customer Reserve 11	User programmable	8'h0
0x0C	[7:0]	Customer Reserve 12	User programmable	8'h0
0x0D	[7:0]	Customer Reserve 13	User programmable	8'h0
0x0E	[7:0]	Customer Reserve 14	User programmable	8'h0
0x0F	[7:0]	Customer Reserve 15	User programmable	8'h0

Table 2: Customer Configuration 0 Registers

Address	Bit(s)	Name	Description	Default
0x00	[7]	Safety Bit	Enables the safety feature in the serial interface. 1: Enable safety 0: Disable safety	1
	[6]	CRC Select	Selects the CRC type when the “Safety bit” = 1. 1: 16b CRC (CCITT False) 0: 8b CRC (SAE J1850)	1
	[5:4]	CRC Initialize	CRC initialize value when the “Safety bit” = 1. 00: 16’h0000 / 8’h00 01: 16’h5555 / 8’h55 10: 16’hAAAA / 8’hAA 11: 16’hFFFF / 8’hFF	00
	[3:0]	SC Initialize	Sequence Counter initialize value when the “Safety bit” = 1. 0000: 1 : 1111: 16	0000
0x01	[7]	Alarm Latch	Alarm report condition. 1: Triggered alarm remains until user clears or power-cycles. 0: Triggered alarm resets once error recovered.	1
	[6]	SPI Output High-Z	Enable high impedance mode 1: Disable high-z 0: Enable high-z	
	[5:0]	Reserved	Reserved	0000000
0x02	[7:4]	Magnetic High	Magnetic field input high limit. 0000: 0 (lowest limit) 1111: 15 (highest limit)	1001
	[3:0]	Magnetic Low	Magnetic field input low limit. 0000: 0 (lowest limit) 1111: 15 (highest limit)	0101
0x05	[7:5]	Multi-Index	Number of indexes per revolution 000: 1 pulse 001: 2 pulses 010: 4 pulses 011: 8 pulses 100: 16 pulses 101: 32 pulses 110: 64 pulses 111: 128 pulses	000
	[4:0]	Reserved	Reserved	00000

Table 2: Customer Configuration 0 Registers (Continued)

Address	Bit(s)	Name	Description	Default
0x06	[7]	Auto-calibration Hardware	Enables auto-calibration on the M1 pin. 0: Disable calibration 1: Enable calibration	0
	[6:4]	Sensing Axis	Sensing axis configuration selection. 000: On-Axis 101: Off-Axis (radial) 110: Off-Axis (axial) 111: Off-Axis (side shaft)	000
	[3:0]	Vertical Hall Selection[a]	Vertical Hall selection (off-axis only). 1000: VH#1 0100: VH#2 0010: VH#3 0001: VH#4 Other 4-bit combination values are invalid.	0000
0x07	[7:6]	SPI4 Mode	SPI4 mode selection (per the MATS table). 00: SPI4A 16b parity 01: SPI4B 24b parallel CRC 10: SPI4C 24b serial CRC 11: SPI4D 8b safety	00
	[5:0]	UVW Resolution[a]	Commutation output pole-pair selection. 000000: 0 pole pairs / OFF 000001: 1 pole pair : 011111: 31 pole pairs 100000: 32 pole pairs 100001: 32 pole pairs * Out-of-range limit to 32 pole pairs.	000000

Table 2: Customer Configuration 0 Registers (Continued)

Address	Bit(s)	Name	Description	Default
0x08	[7:4]	PWM Resolution[b]	0000: PWM fixed period = 10bit 0001: PWM fixed period = 11bit 0010: PWM fixed period = 12bit 0011: PWM fixed period = 13bit 0100: PWM fixed period = 14bit *0101-0111: Out of range, PWM fixed period = 14bit 1000: PWM fixed clock = 10bit 1001: PWM fixed clock = 11bit 1010: PWM fixed clock = 12bit 1011: PWM fixed clock = 13bit 1100: PWM fixed clock = 14bit *1101-1111: Out of range, PWM fixed clock = 14bit	0000
	[3:2]	Index State	Index location within incremental period selection. 00: A low B low 01: A low B high 10: A high B high 11: A high B low	00
	[1:0]	Index Width	Index width selection. 00: 90e° 01: 180e° 10: 270e° 11: 360e°	00

a. See Off-Axis Sensing Orientation.

b. UVW: Flexible 6-bit UVW resolution up to 32 pole pairs.
PWM: Only the shown setting is available; other combinations are invalid.

Table 3: Customer Configuration 1 Registers

Address	Bit(s)	Name	Description	Default
0x09	[7]	PSEL[a]	Protocol mode selection with the MATS table. 0 : SSI3a / SSI2a / All SPI4 modes 1: SSI3b / SSI2b / PWM	0
	[6:0]	Incremental Resolution [13:8][b]	Incremental resolution selection. 000-0000-0000-0000 : 0 CPR (OFF) 000-0000-0000-0001 : 1 CPR 000-0000-0000-0010 : 2 CPR 000-0000-0000-0011 : 3 CPR : 000-0000-1000-0000 : 128 CPR : 000-0100-0000-0000 : 1024 CPR : 010-0000-0000-0000 : 8192 CPR : 100-1110-0010-0000 : 20,000 CPR	0000100 00000000
0x0A	[7:0]	Incremental Resolution [7:0][b]		

a. In conjunction with the MATS table for input/output configuration.

b. Flexible 15-bit Incremental resolution up to 20,000 CPR. Combinations above 20,000 are invalid.

Table 4: Customer Configuration 2 Registers

Address	Bit(s)	Name	Description	Default
0x0B	[7:5]	Hysteresis	Incremental output hysteresis selection. 000: Hysteresis OFF 001: 0.01m° 010: 0.02m° 011: 0.04m° 100: 0.08m° 101: 0.17m° 110: 0.35m° 111: 0.70m°	100
	[4]	Direction	Counting direction selection. 0: Count up in clockwise direction 1: Count up in counter-clockwise direction	0
	[3:0]	Single Turn Resolution	Absolute output resolution selection. 0000: 18bit 0001: 17bit : 1000: 10bit * Out-of-range limit to 8bit minimum.	0000

Table 5: Customer Single-Turn Reset

Address	Bit(s)	Name	Description	Default
0x0C	[7:0]	Zero Reset 2	MSB bit-17 to bit-10 of absolute single-turn	0000-0000
0x0D	[7:0]	Zero Reset 1	Bit-9 to bit-2 of absolute single-turn	0000-0000
0x0E	[7:6]	Zero Reset 0	LSB bit-1 to bit-0 of absolute single-turn	00

EEPROM Passcode (Level 2 Memory Access)

Perform the following steps to set a memory passcode:

1. Write value 8'hAB to address 0x10 to unlock Level 1 memory access.
2. Write the user-desired passcode 7x8bits to the memory address from 0x18 to 0x1E.
3. Write 8'hBA to address 0x1F to set the passcode.

NOTE: The factory/default passcode is h00-h00-h00-h00-h00-h00-h00.

EEPROM Unlock

Perform the following steps to unlock the MTP register:

1. Write value 8'hAB to address 0x10 to unlock Level 1 memory access.
2. Write the correct user passcode 7x8bits to the memory address from 0x18 to 0x1E to unlock Level 2 memory access.
3. Read and write MTP registers are now accessible.

EEPROM Page

Perform the following steps to load the EEPROM page to the MTP register:

1. Perform the steps in EEPROM Unlock to unlock the EEPROM.
2. Write one of the following values to address 0x16 to load the selected EEPROM page to the MTP register:
   – 8h'01 to load the Customer Reserve register.
   – 8h'00 to load the Customer Configuration register.

NOTE: Upon power-up, the MTP register is loaded with the Customer Configuration register.

EEPROM Programming

Perform the following steps to program the MTP shadow register to EEPROM:

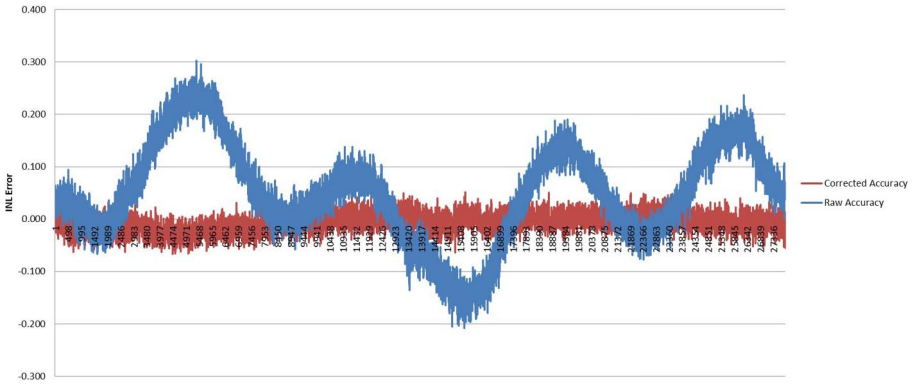
1. Write the desired values to the current MTP register (Customer Reserve / Configuration Shadow register).
2. Verify the written value by reading back all registers.
3. Write value 8'hA1 to address 0x14 to program the current MTP registers to EEPROM.
4. Read memory busy bit[7] address 0x2A:
   – 0 : EEPROM programming completed
   – 1 : EEPROM programming in progress

NOTE: EEPROM programming is required before changing the EEPROM page.

Encoder Calibration

Accuracy Angle Calibration

To achieve a high degree of angle accuracy, the AEAT-9955-Q32 comes with a built-in correction algorithm. This algorithm corrects errors upon installation of the encoder to the motor. The following figure shows the comparison between raw and corrected accuracy over one rotation.



NOTE: If the start of operation is at an extreme temperature, a minimum of 10 revolutions is needed to stabilize the accuracy to be optimum.

The following are the calibration procedures.

Via SPI Register

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at a constant speed ranging from 10 RPM to 2000 RPM.
3. Once the speed stabilizes, write value 8'h2 to address 0x12 to initiate the calibration sequence.
4. Read the calibration status on bit [1:0] address 0x22.
   – 10 : Calibration Pass
   – 11 : Calibration Fail
5. Write value 8'h0 to address 0x12 to exit the calibration sequence.
6. The calibration value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write value 8'h1 to address 0x12.
   – To return to operation mode, write value 8'h0 to address 0x12.

Via Hardware Pin M1

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at a constant speed ranging from 10 RPM to 2000 RPM.
3. Once the speed stabilizes, pull the signal high, M1 for more than 50 ms to initiate the calibration sequence.
4. Read the calibration status on output pin ABI.
   – If AB=1, I=0 : Calibration Pass
   – If AB=1, I=1 : Calibration Fail
5. The calibration value is automatically stored in memory; no further programming is required.

NOTE: Hardware pin calibration is automatically disabled upon completion. To re-enable this function, the user must write value 8'h64 to address 0x07.

Zero Reset Calibration

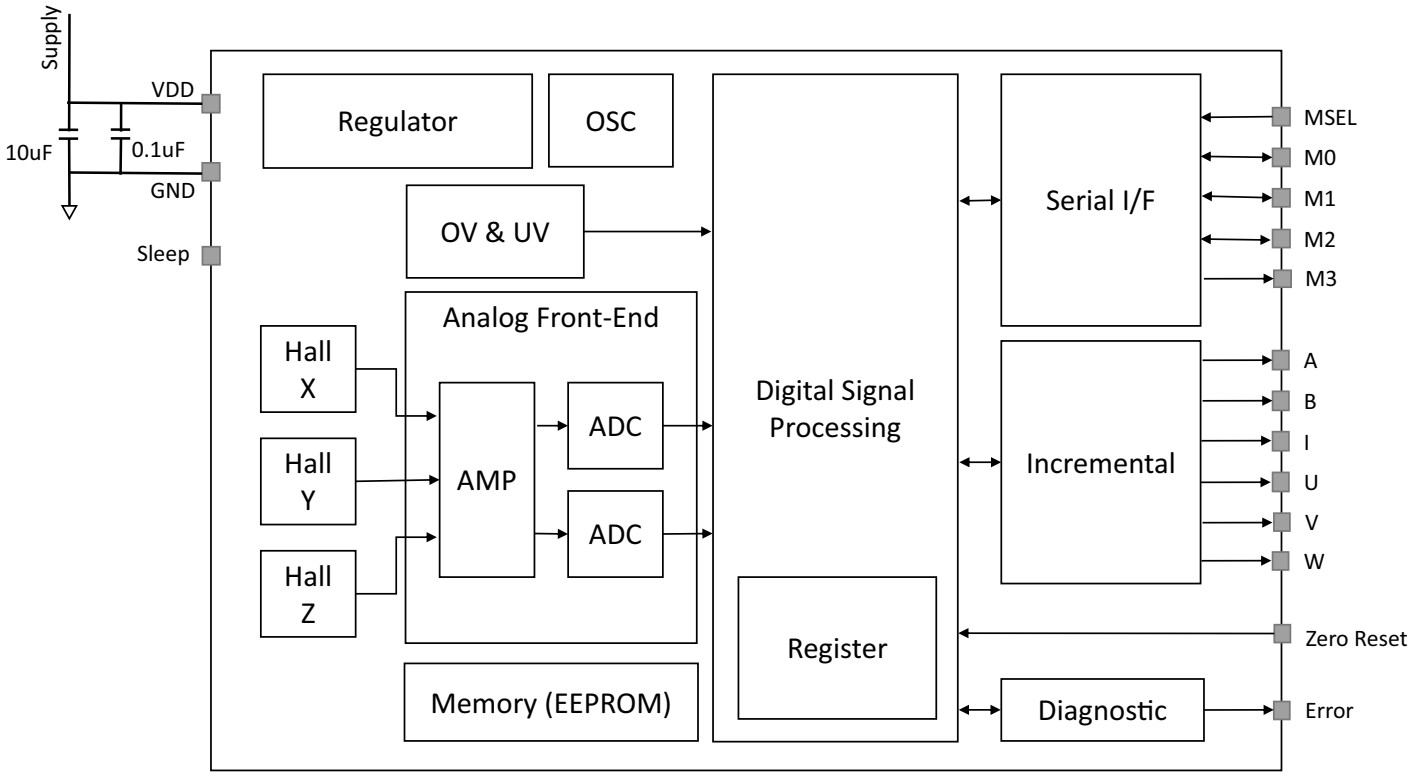
The AEAT-9955-Q32 allows users to configure a zero reset position. The following is the calibration procedure.

Via SPI Register

1. Stop the encoder to the motor system at the desired location.
2. Once it is stationary, write value 8'h8 to address 0x12 to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2] address 0x22.
   – 10 : Calibration Pass
   – 11 : Calibration Fail
4. Write value 8'h0 to address 0x12 to exit the calibration sequence.
5. The offset value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write value 8'h4 to address 0x12.
   – To return to operation mode, write value 8'h0 to address to 0x12.

AEAT-9955-Q32 Circuit Diagram

Figure 1: Recommended Circuit Diagram for the AEAT-9955-Q32

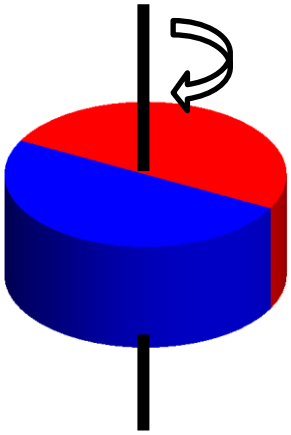


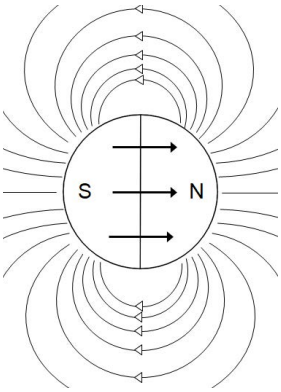
NOTE: Connect the 10-µF and 100-nF capacitors as close as possible to the individually assigned power and ground pins.

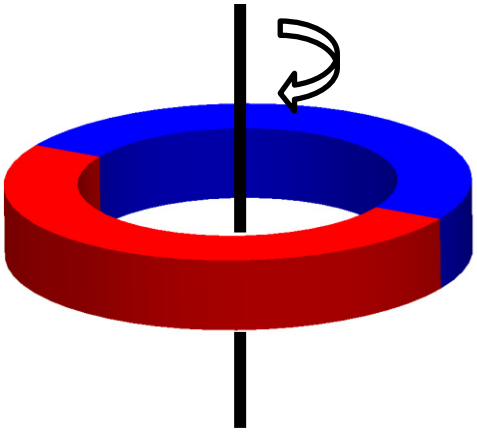
Recommended Magnetic Input Specifications

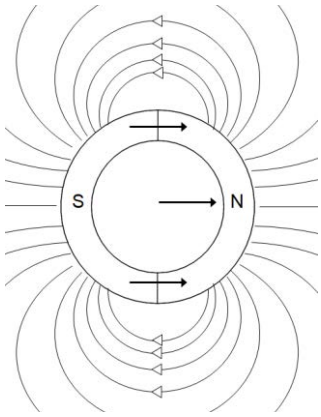
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter Disc magnet Ring magnet ID /OD	d	 4 —	 6 ID,15 OD,25	 — —	 mm mm mm	Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized and one pole pair.
Thickness Disc magnet Ring magnet	t	 — 2	 2.5 6	 — —	 mm mm	
Magnetic input field magnitude On-axis (disc magnet) Off-axis (ring magnet)	Bpk	 45 30	 — —	 100 150	 mT mT	Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet displacement radius	R_m	—	—	0.25	mm	Displacement between the magnet axis and the device center.
Recommended magnet material and temperature drift	—	—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Diametrically Magnetized Magnet





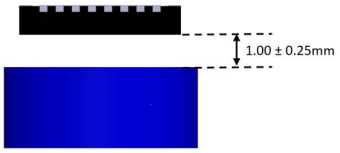
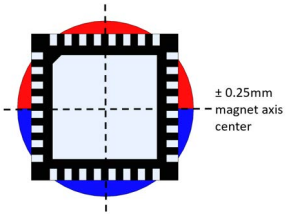
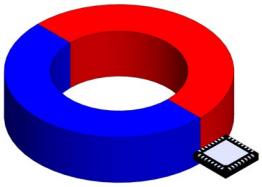
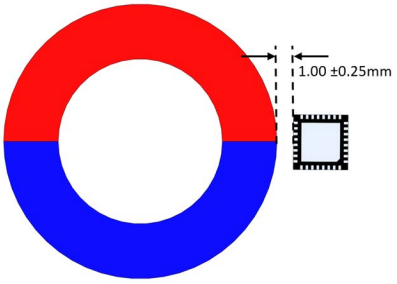
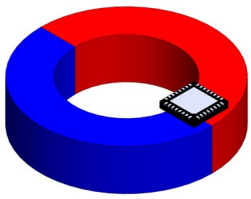
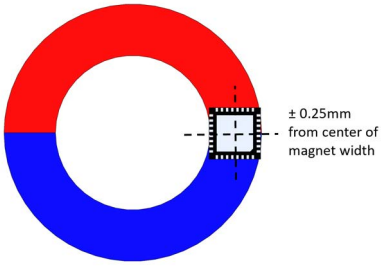
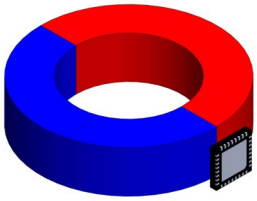
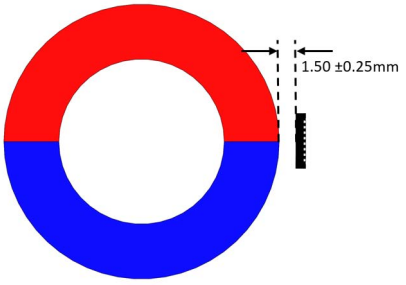




Magnet and IC Package Placement

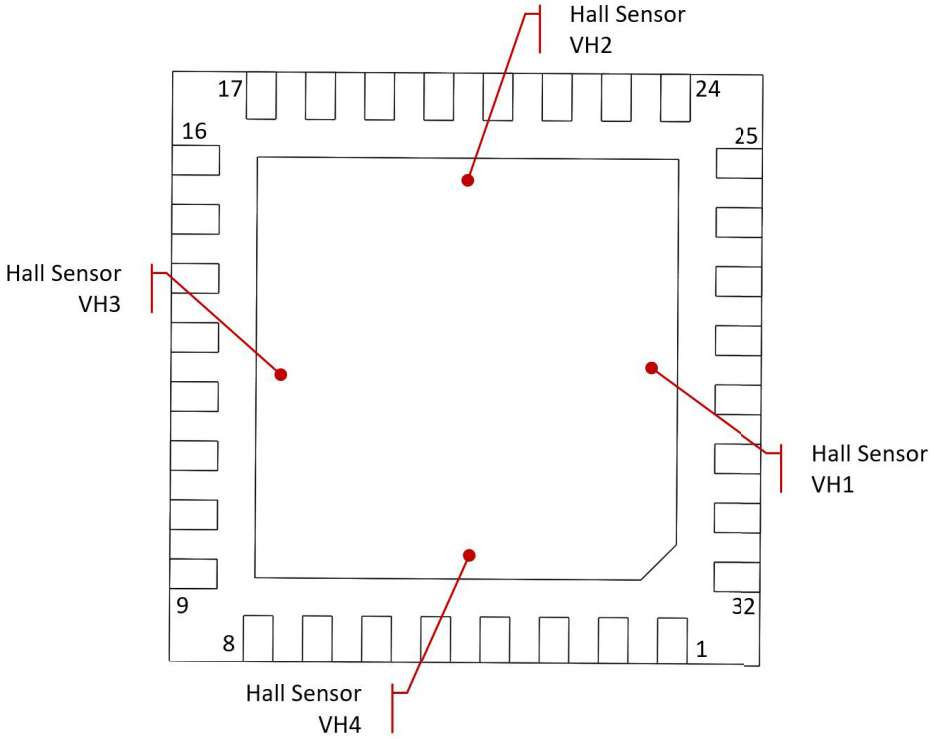
The AEAT-9955 multi-axis capability comes from multiple integrated Hall devices that allow flexibility on the sensor mounting with respect to the magnet. Generally, the shaft end configuration senses the vertical field (Z component perpendicular to the chip surface), and the rest of the configuration senses the horizontal field (X and Y components parallel to the chip surface).

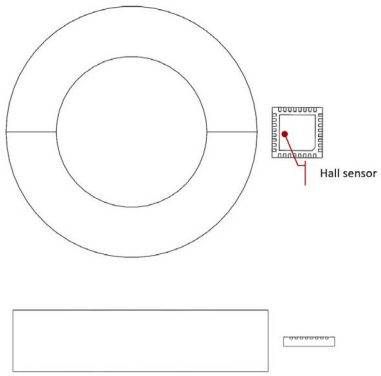
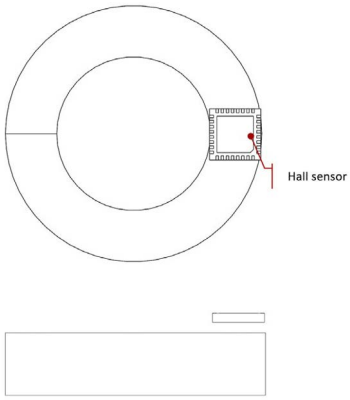
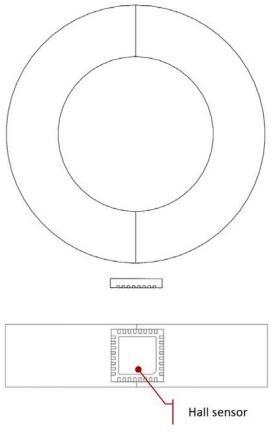
The nominal mounting tolerance is indicated the following table.

Configuration	Gap Tolerance	X-Y Tolerance
Shaft End 		
Side Shaft 		
Axial 		
Radial 		

Off-Axis Sensing Orientation

The off-axis configuration is sensed via the vertical Hall element. Each axis requires a specific vertical Hall orientation to be configured. Multiple vertical Hall sensors are built in to provide flexibility in the mounting configuration. The vertical Hall selections are available in the Customer Configuration 0 registers.



Side-Shaft	Axial	Radial
 Hall sensor facing the magnet OD	 Hall sensor facing the magnet OD	 Hall sensor tangent with the magnet OD

Serial Interface Format

The AEAT-9955 serial interface hosts up to 10 different protocols for position output and memory access. The protocol is configurable with the combination of the physical I/O MSEL and M0 and memory settings PSEL, SPI4[0], and SPI4[1]. The default factory setting is all zeros, which is either SPI3 or SPI4-16a depending on the MSEL state. The output pin can be configured to high impedance mode for multi slave connection or bus connection.

All protocol selection can be switched during operation.

MATS Table

Mode / Pin	SPI3	SSI3a	SSI3b	SSI2a	SSI2b	SPI4-16a	SPI4-16b	SPI4-16c	SPI4-8	PWM
MSEL	0	0	0	0	0	1	1	1	1	1
PSEL	x	0	1	0	1	0	0	0	0	1
SPI4[1]	x	x	x	x	x	0	0	1	1	x
SPI4[0]	x	x	x	x	x	0	1	0	1	x
M0	0	1	1	1	1	NCS	NCS	NCS	NCS	-
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	MOSI	MOSI	-
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	SCK	SCK	-
M3	DO	DO	DO	DO	DO	MISO	MISO	MISO	MISO	PWM

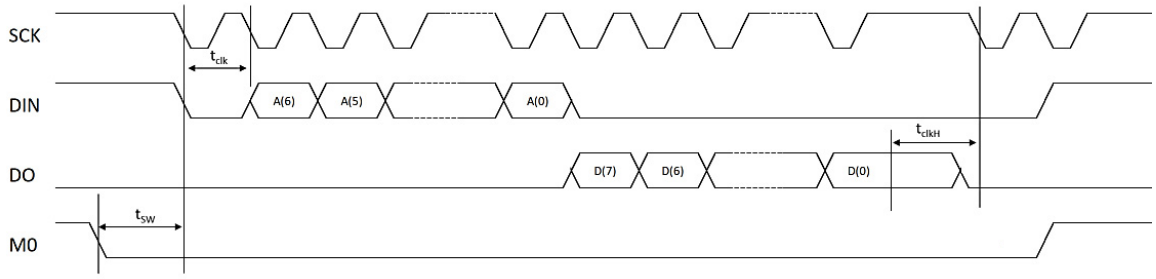
NOTE: PSEL, SPI4[1], and SPI4[0] are configured through memory. MSEL and M0 are configured through I/O pads.

Serial Peripheral Interface (SPI3)

SPI3 protocols allow access to memory read write only. Assert 0 on the MSEL and M0 pin to configure it. The SPI is implemented with CPOL=0 and CPHA=0; data is propagated on the clock falling edge.

- M1 → SPI_Data Input (DIN) signal for the SPI protocol, input to the AEAT-9955.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9955.
- M3 → SPI_Data Output (DO) signal for the SPI protocol, output from the AEAT-9955.

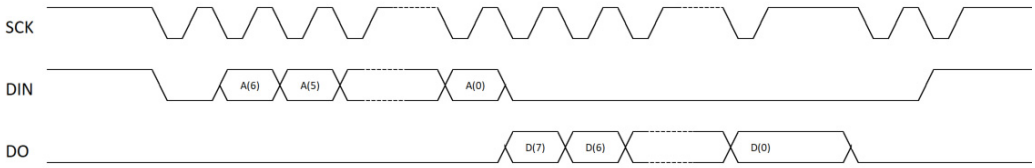
SPI3 Timing Diagram



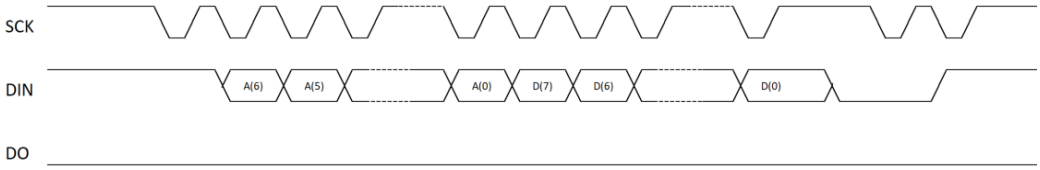
Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between the SCn falling edge and the CLK rising edge	1	—	—	µs
t_{clk}	Serial clock period	—	—	100	ns
t_{clkH}	CLK high time after the end of the last clock period	300	—	—	ns

NOTE: The user should read back data to confirm that it has been written successfully.

SPI3 Read



SPI3 Write



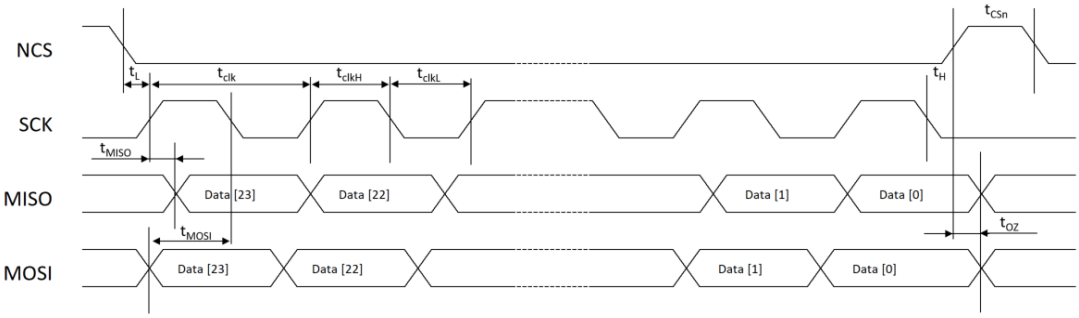
Serial Peripheral Interface (SPI4)

The SPI protocol uses four pins from the AEAT-9955. These four pins are shared between the UVW, SSI, and SPI protocols. To select the SPI4 protocol, assert 1 on the MSEL pin.

SPI4 protocols allow the user to access memory read or write and position data. It uses CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for the SPI protocol, input to the AEAT-9955.
- M1 → SPI_Data Input (MOSI) signal for the SPI protocol, input to the AEAT-9955.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9955.
- M3 → SPI_Data Output (MISO) signal for the SPI protocol, output from the AEAT-9955.

SPI4 Timing Diagram



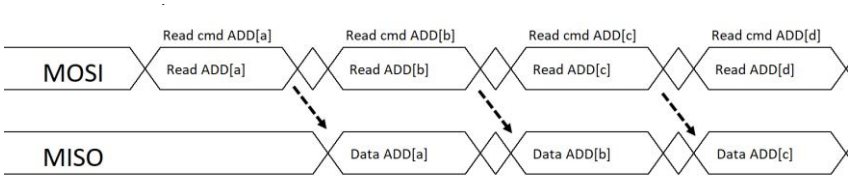
Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between the SCn falling edge and the CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	100	—	—	ns
t_{clkL}	Low period of the serial clock	50	—	—	ns

Symbol	Description	Min.	Typ.	Max.	Unit
t_{clkH}	High period of the serial clock	50	—	—	ns
t_H	Time between the last falling edge of CLK and the rising edge of CSn	$t_{clk}/2$	—	—	ns
t_{CSn}	High time of CS between two transmissions	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	CLK edge to data output valid	—	51	—	ns

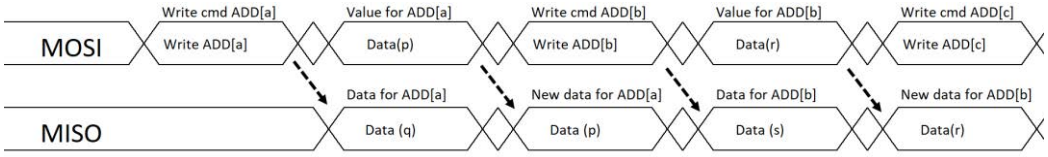
NOTE: The user should read back data to confirm that it has been written successfully.

SPI4 Command and Data Frame

SPI4 Read Sequence



SPI4 Write Sequence



SPI-4(A) 16-Bit (Parity)

By default, the chip is configured to SPI4 16-bit selection; PSEL = 0, SPI4[1] = 0, SPI4[0] = 0 in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Peripheral to Controller (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Peripheral to Controller (pos 10b)					P	EF	Pos[9:0]										0	0	0	0
Peripheral to Controller (pos 11b)					P	EF	Pos[10:0]											0	0	0
Peripheral to Controller (pos 12b)					P	EF	Pos[11:0]												0	0
Peripheral to Controller (pos 13b)					P	EF	Pos[12:0]													0
Peripheral to Controller (pos 14b)					P	EF	Pos[13:0]													
Peripheral to Controller (pos 15b)				P	EF	Pos[14:0]														
Peripheral to Controller (pos 16b)			P	EF	Pos[15:0]															
Peripheral to Controller (pos 17b)		P	EF	Pos[16:0]																
Peripheral to Controller (pos 18b)	P	EF	Pos[17:0]																	

P: Parity
EF: Error Flag
RW: Read = 1, Write = 0

SPI4-(B) 24-Bit (CRC)

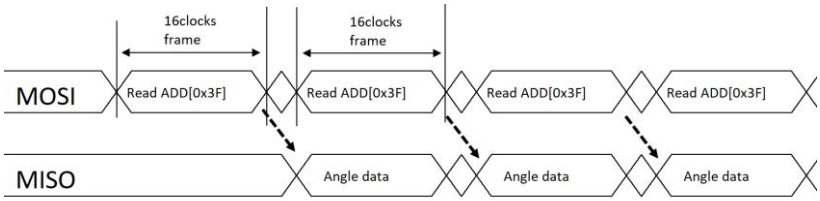
To configure the chip to SPI4 24-bit selection, set PSEL = 0, SPI4[1] = 0, SPI4[0] = 1 in the register setting.

	Data Format																								
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Peripheral to Controller (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Peripheral to Controller (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Peripheral to Controller (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Peripheral to Controller (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Peripheral to Controller (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Peripheral to Controller (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Peripheral to Controller (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Peripheral to Controller (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Peripheral to Controller (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

W: Warning
E: Error
RW: Read = 1, Write = 0

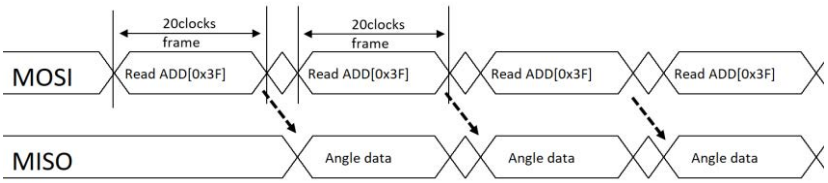
Position Read

Absolute position data can be obtained by sending a read command to address 0x3F.



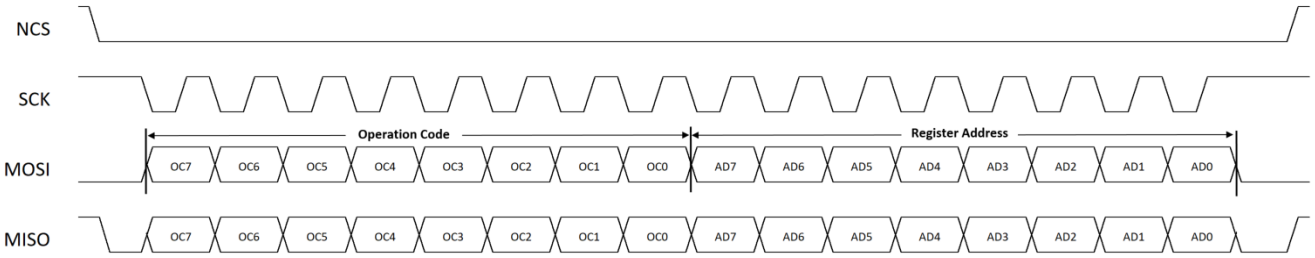
In the event of higher single-turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Example: 18bit + 2bit (parity and error)



SPI4-8

To configure the chip to SPI4 24-bit selection, set PSEL = 0, SPI4[1] = 1, SPI4[0] = 1 in the register setting.

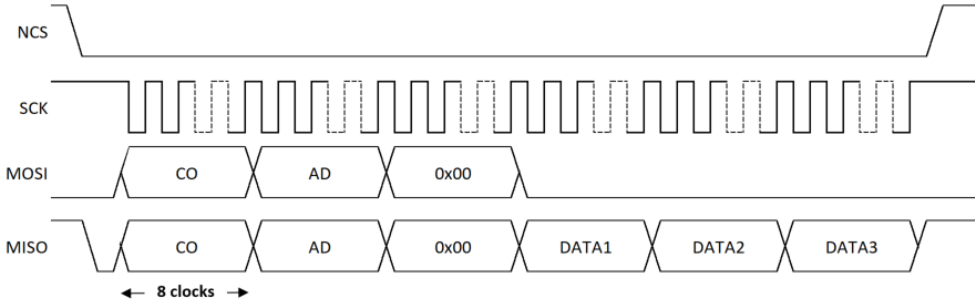


When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.

The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over specific operation code (OC).

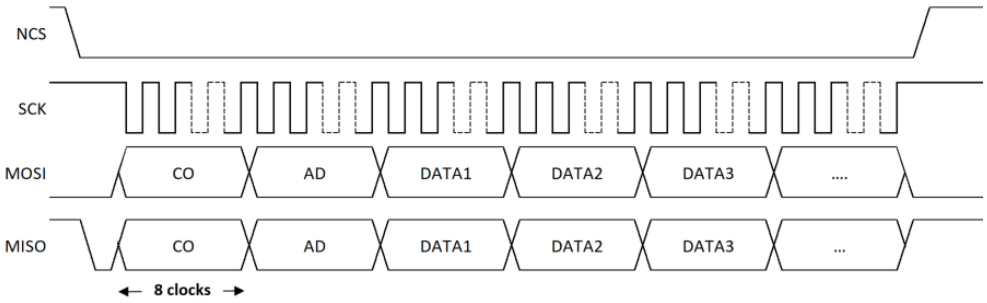
Register Read (OC=0x81'h)

This operation is used to read data from the internal register of the chip. It can be performed consecutively starting from any register address. The data continues to be transmitted as long the clock (SCK) is sent and the chip select (NCS) remains active.



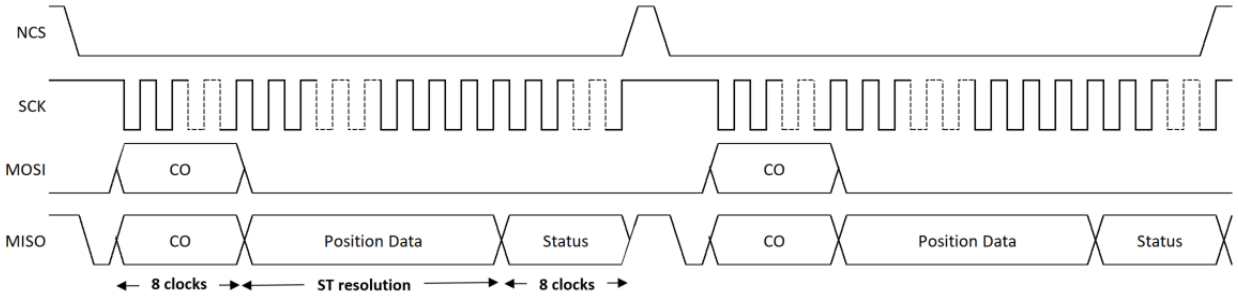
Register Write (OC=0xCF'h)

This operation is used to write data into the internal register of the chip. It can be performed consecutively starting from any register address.The subsequent data byte is written into the next register address (AD+1), while the NCS signal stays active. Complete written data is transmitted back via MISO.

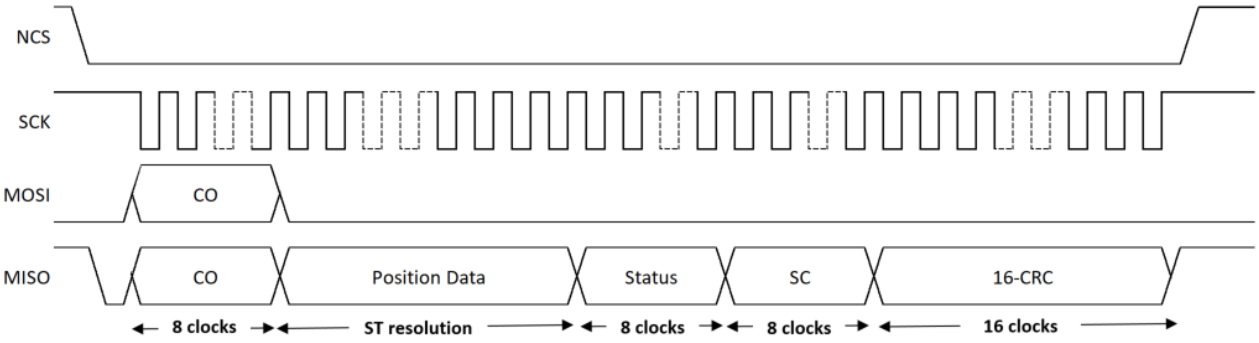


Position Read (OC=0xA6'h)

Read the absolute position by sending the operation code, and the data will be transmitted on the MISO line. The position data consists of the single-turn position data length and status byte. The position data length follows the single-turn resolution setting.



For safety format, there are additional bytes: sequence counter (SC) and CRC.



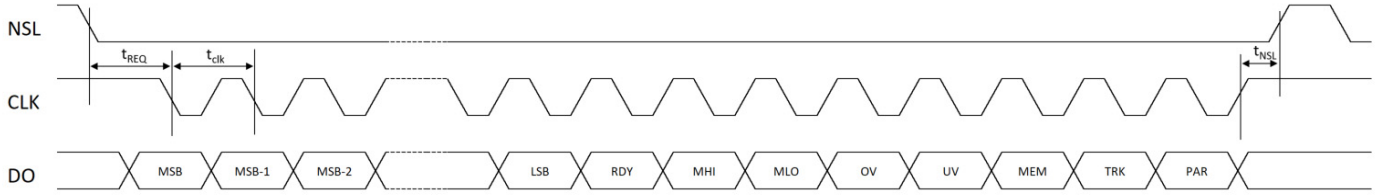
Serial Synchronous Interface 3-Wire (SSI3)

The SSI3 protocol uses three pins from the AEAT-9955. These three pins are shared between the UVW, SSI, and SPI protocols. To activate the SSI3 protocol, assert 0 on the MSEL pin and assert 1 on the M0 pin.

- M1 → SSI_NSL Input (NSL) signal for the SSI protocol, input to the AEAT-9955.
- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9955.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9955.

It is available in two options per PSEL register setting.

SSI Protocol Timing Diagram. Default: Data Output with 3-Wire SSI to 10-MHz Clock Rates

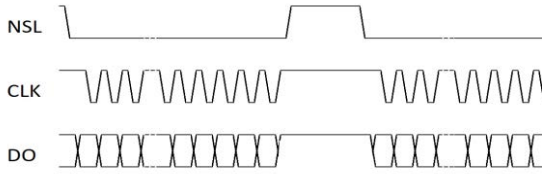


Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	SSI_SPI_SEL switch time	1	—	—	µs
t_{REQ}	SCL high time between the NSL falling edge and the first SCL falling edge	300	—	—	ns
t_{NSL}	NSL high time between two successive SSI reads	200	—	—	ns

SSI-3(A)

By default, the chip is configured to SSI-3(A) selection; PSEL = 0 in the register setting.

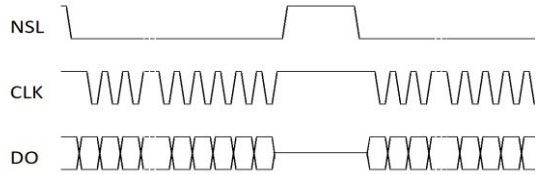
The DO pin is held at a high state once the NSL pin is high.



SSI-3(B)

To configure the chip to SSI-3(B) selection, set PSEL = 1 in the register setting.

The DO pin is at a tristate (high-impedance) state once the NSL pin is high.



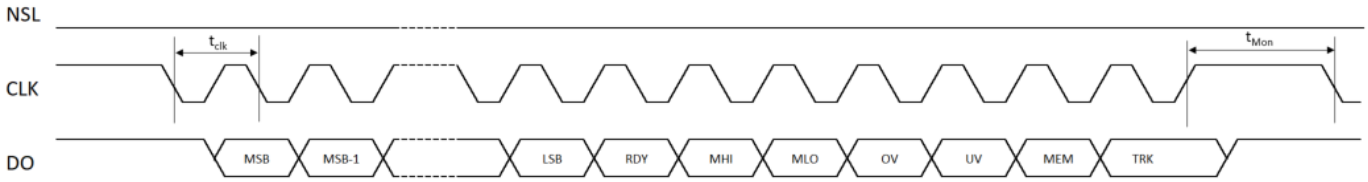
Serial Synchronous Interface 2-Wire (SSI2)

The SSI2 protocol uses two pins from the AEAT-9955. These two pins are shared between the SSI and SPI protocols. To activate the SSI2 protocol, assert 0 on the MSEL and M1 pins and assert 1 on the M0 pin upon power-up.

- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9955.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9955.

Depending on the PSEL setting, it can be configured as SSI2(A) Ring Mode or SSI2(B) No Ring Mode.

Data is latched on the first CLK falling edge and is transmitted on the next falling edge.

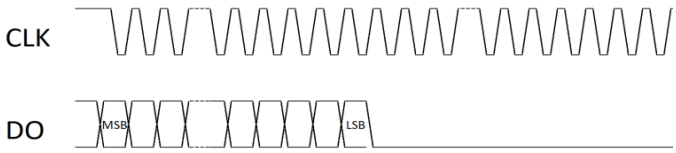


Symbol	Description	Min.	Typ.	Max.	Unit
t_{Clk}	NSL low time after the rising edge of the last clock period for an SSI read	250	—	$t_M/2$	ns
t_M	NSL high time between two successive SSI reads	—	16.5	18.0	µs

SSI-2(A)

By default, the chip is configured to SSI-2(A) selection; PSEL = 0 in the register setting.

Outputs single data position and remains low after LSB until the next monoflop (t_M) expires.

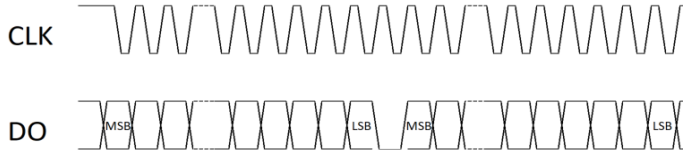


SSI-2(B)

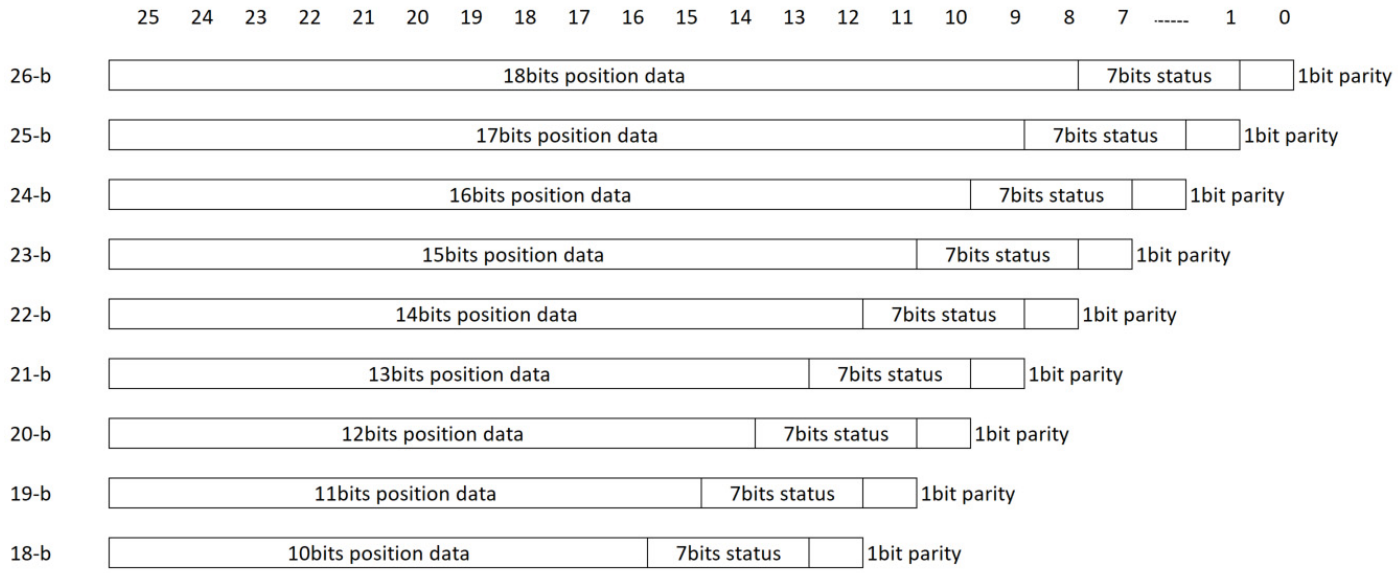
To configure the chip to SSI-2(B) selection, set PSEL = 1 in the register setting.

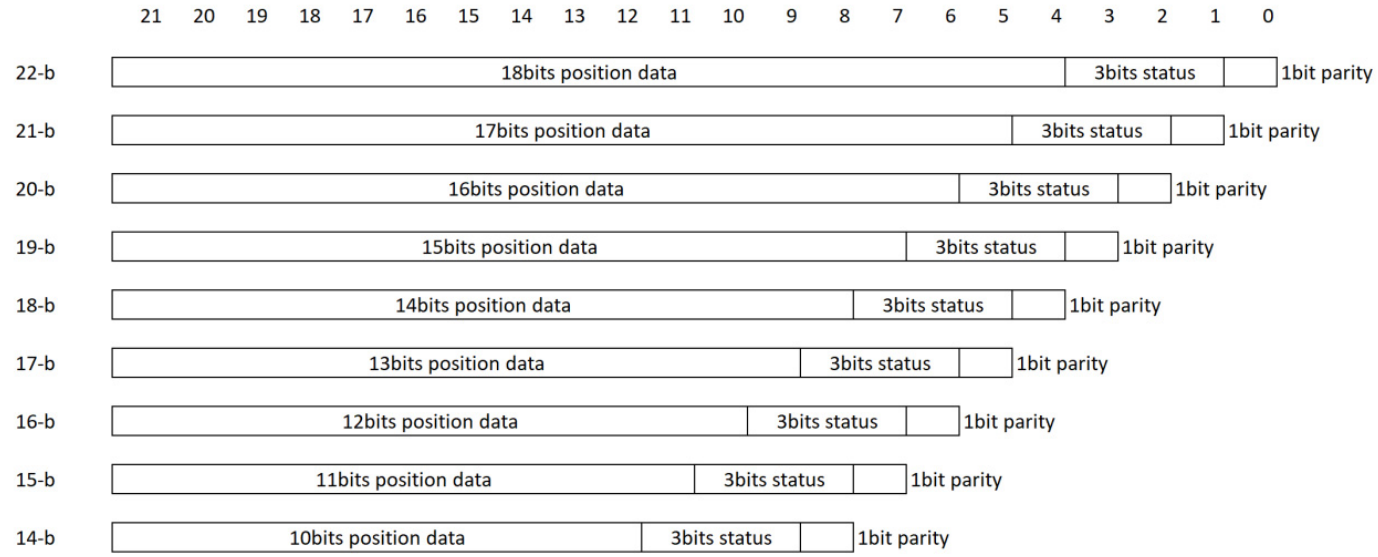
The same position data can be continuously output by sending clock train, and the data is separated by a single low pulse.

Data will be refreshed when the next monoflop (t_M) expires.



SSI READ Data Format





NOTE:

- 7-b status: {Ready, MHI, MLO, OV, UV, Mem, Trck}
- See Status and Alarm for more details.

Safety and Non-safety Protocol Format

The position serial interface is available in Safety and Non-safety format; applicable for SSI3, SSI2, and SPI-8.

Position (n-bit)	Status / Alarm (7-bit)							Parity (1-bit)
Position[(n-1):0]	READY	MHI	MLO	OV	UV	MEM	TRK	parity

Position (n-bit)	Status / Alarm (8-bit)							SC (8-bit)	CRC (8/16-bit)
Position[(n-1):0]	Status[1:0] (1)	MHI	MLO	OV	UV	MEM	TRK	SC [7:0] (2)	CRC [7/15:0] (3)

NOTE:

1. 2-bit status to indicate the safety status:
   - Status = 2b'00 – Encoder not ready.
   - Status = 2b'01 – Encoder not ready, Force test failed.
   - Status = 2b'10 – Encoder not ready.
   - Status = 2b'11 – Encoder not ready, Force test passed.
2. SC denotes as "Sequence Count" or life counter that automatically increments on every position transmission. The counting starts from 1 to 255, and the initial value upon power-up is configurable.
3. CRC poly 0x1021 or 0x1D, initial value is configurable (0x0000, 5555, AAAA, FFFF).

Status and Alarm

The error bit is triggered if Magnet High (MHI), Magnet Low (MLO), Memory Error (MEM), or communication error.

Details of the error bit are available in the following register address.

Address	bit							
	7	6	5	4	3	2	1	0
0x21	RDY	MHI	MLO	OV	UV	MEM	TRK	

- **Ready:** The chip is ready, and the ready value is 1.
- **Parity:** 1-b parity is even parity.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is set high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is set low consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Memory Error (MEM) Error:** This indicates that memory corruption has occurred. When this is set high, perform a power-cycle to reload the memory. The value for this alarm is represented as 1.
- **Tracker (TRK) Error:** This indicates that the angular error has exceeded 5° within 5 ms. When this is set high consistently, perform a power-cycle to re-initialize the sensor. The value for this alarm is represented as 1.

Power Modes

The AEAT-9955 is designed with two power modes:

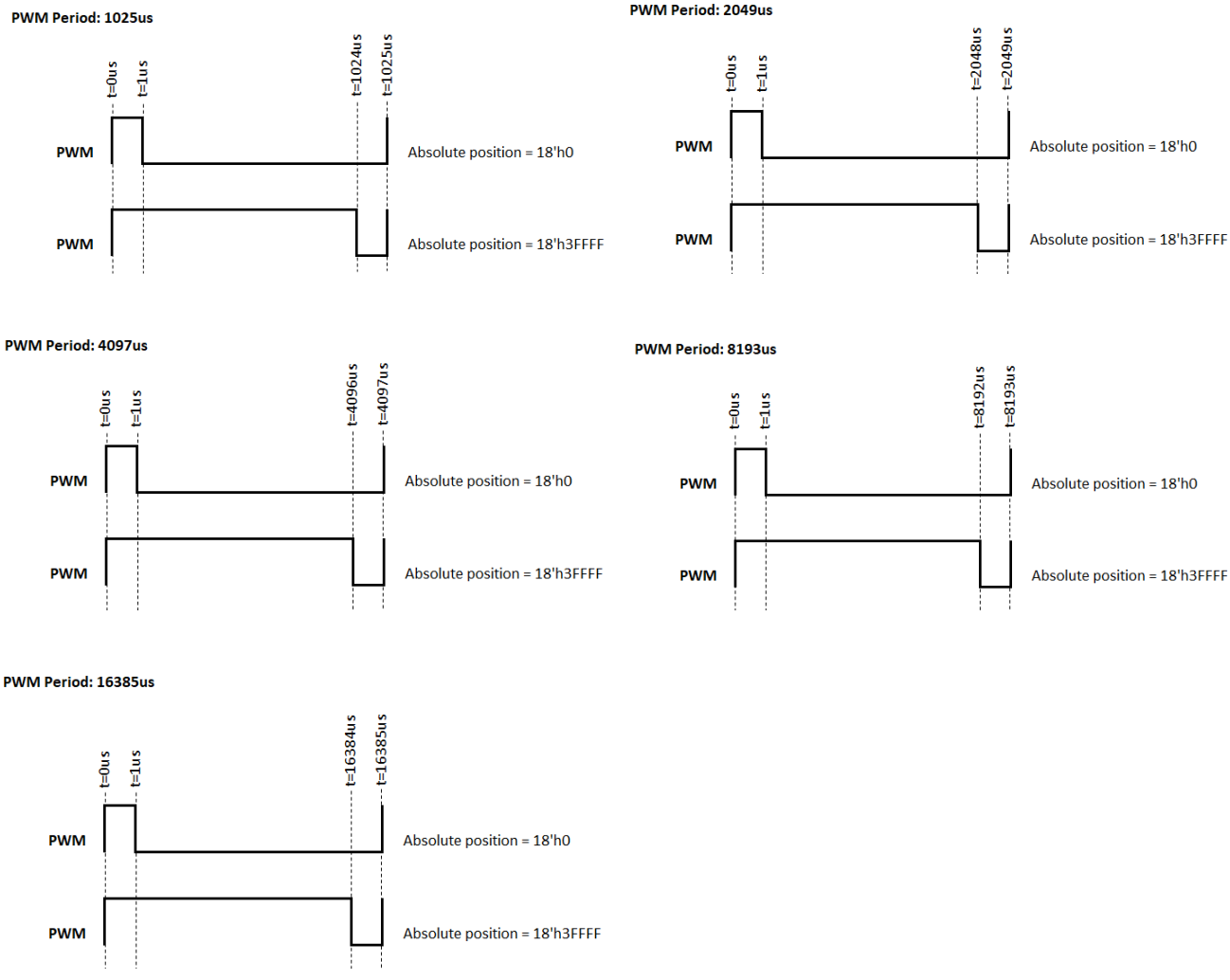
- **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}.
- **Sleep Mode** powers down the chip front-end and digital processing blocks, leaving only the detection block to track on user input with low current consumption, IDD_{IDLE}.

PWM

The PWM protocol uses one output pin (W_PWM) from the AEAT-9955. Note that the W_PWM pin is shared between the UVW and PWM protocols. The PWM signals are configurable to have a period of 1025, 2049, 4097, 8193, or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

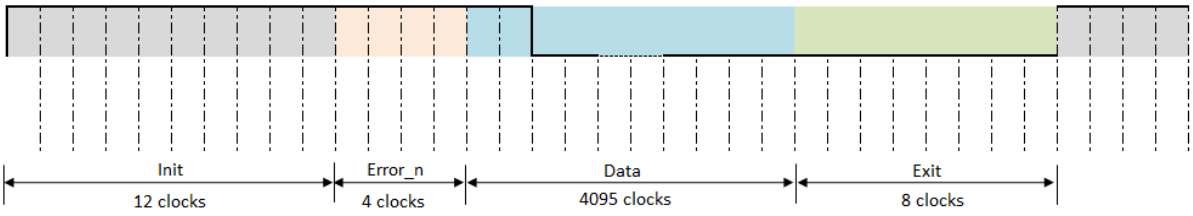
PWM Period: 1025, 2049, 4097, 8193, 16385 µs



The PWM protocol is also available with Init, Error_n, and Exit along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PMW Period: 4119 µs



Incremental Output Format

The AEAT-9955 provides ABI and UVW signals to indicate the incremental position of the motor.

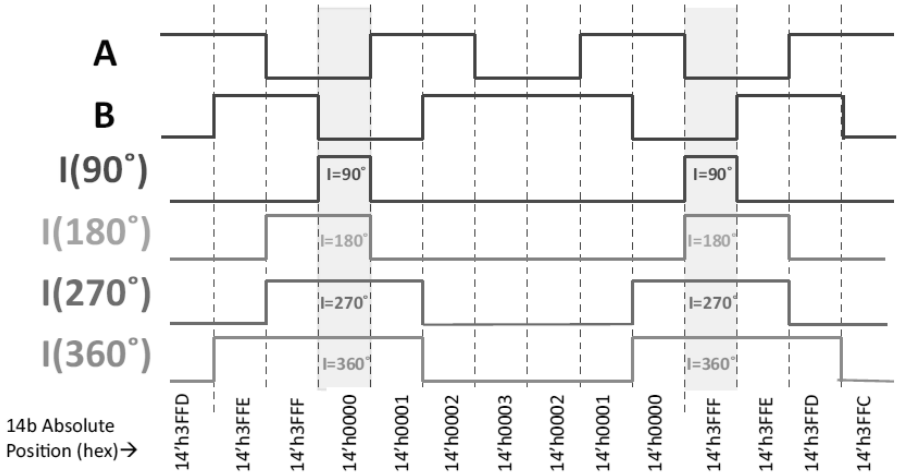
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

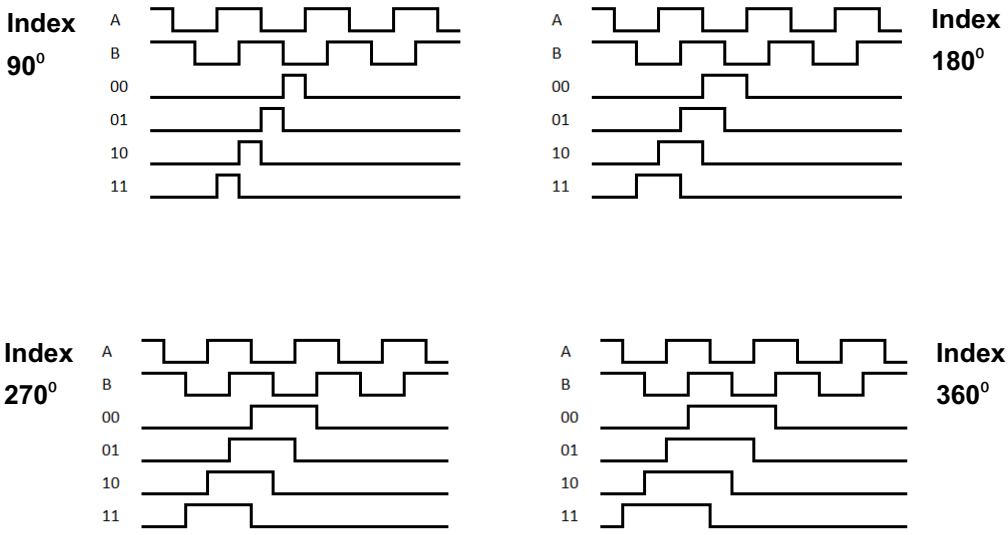
- Programmable CPR: 1 to 20,000 CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)
- Programmable I-state: 90, 180, 270, or 360 electrical degrees (edeg)

Figure 2: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming the User Sets Hysteresis at 0.02 Mechanical Degrees

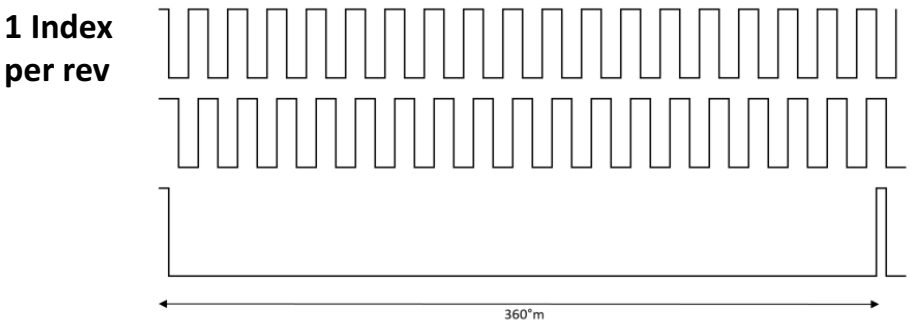


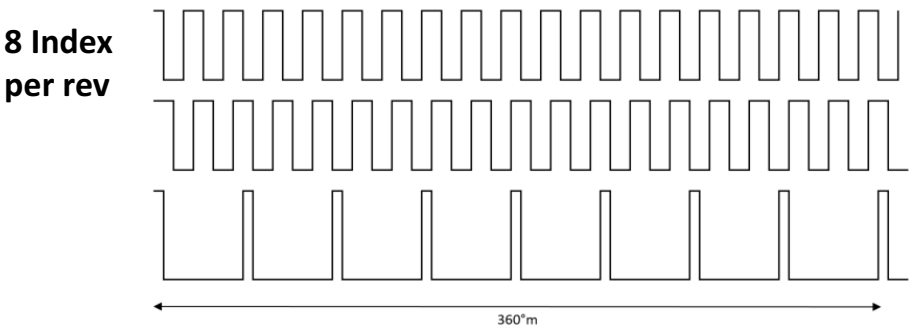
The index position is configurable among the incremental states.

The index signal rises high once per turn at the absolute zero position.

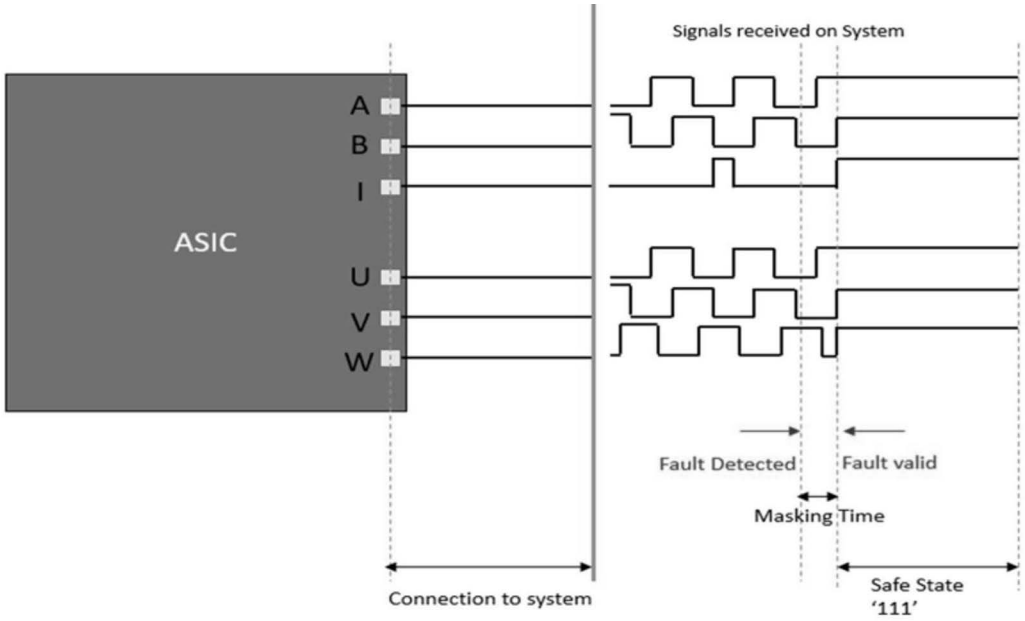


The number of indexes per revolutions is configurable from 1 pulse up to 128 pulses.





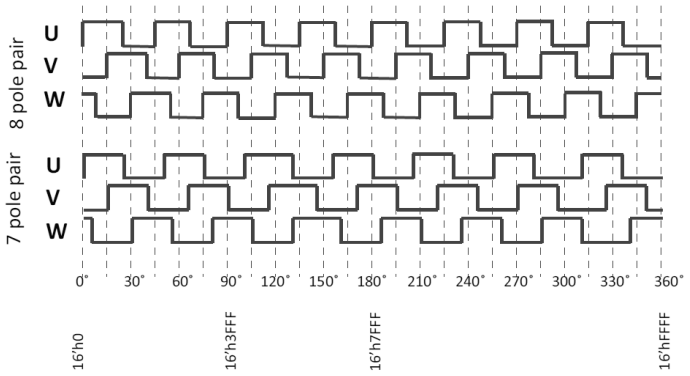
Under safety mode, the incremental ABI and commutation output UVW assert to High State.

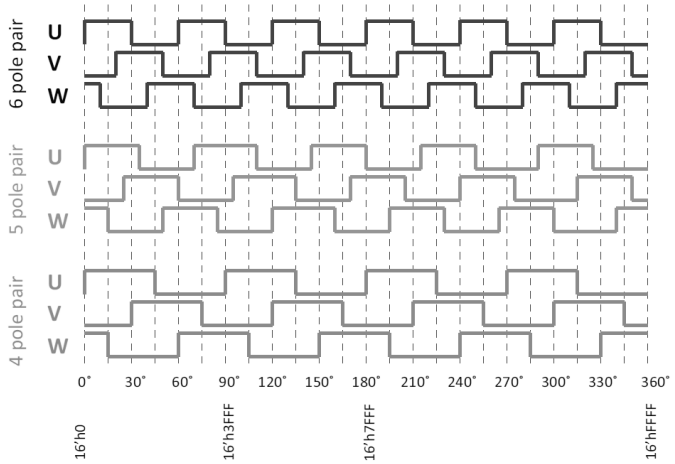


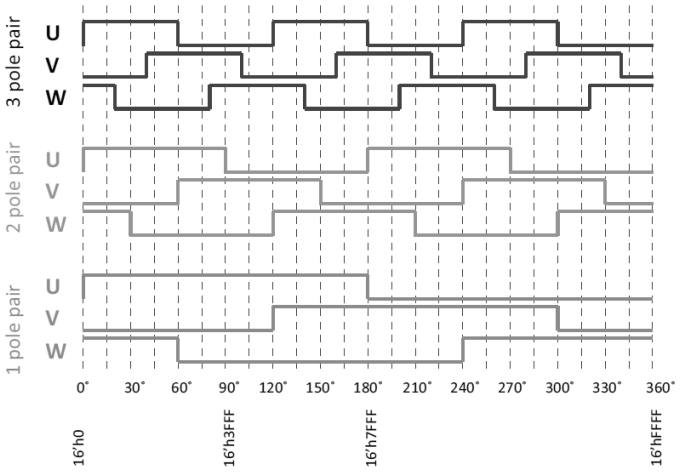
UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that the W_PWM pin is shared between the UVW and PWM protocols.

The AEAT-9955 can configure pole pairs from 1 to 32 (equivalent to 2 to 64 poles).

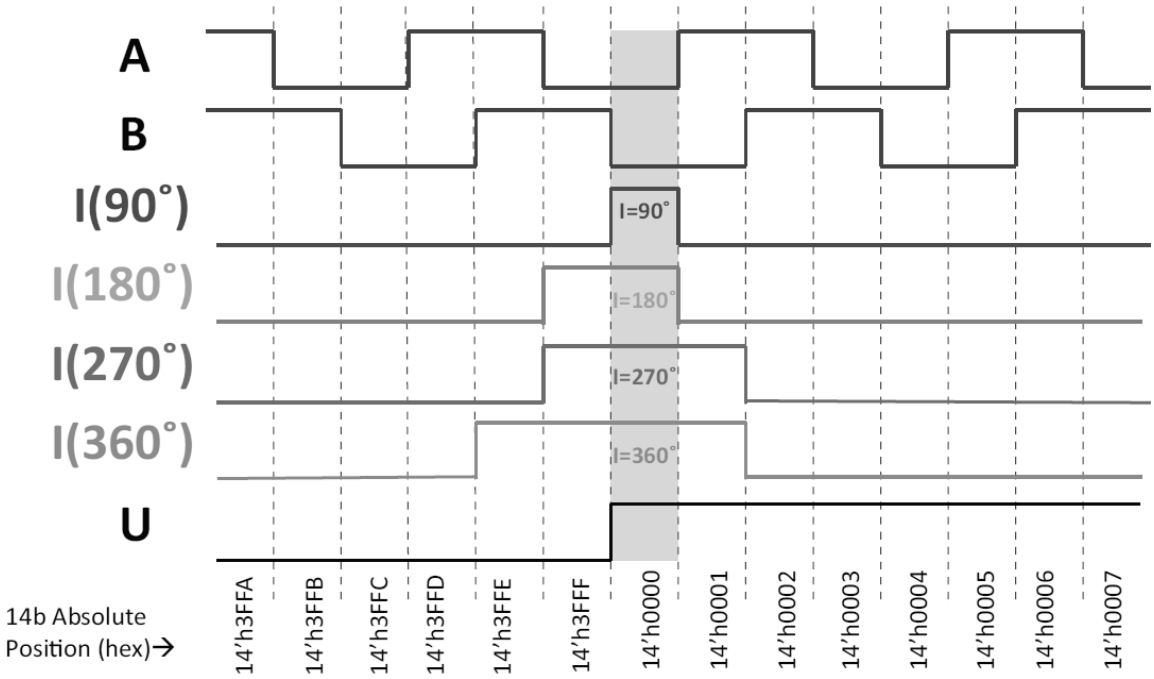






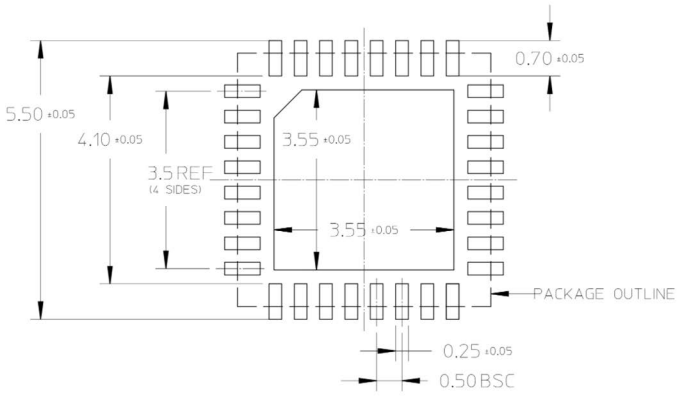
Note that signal U from the UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 3: U-to-I Tagging



Recommended PCB Land Pattern (in mm)

Land Pattern Dimensions and Tolerance



Recommended Lead-Free Solder Reflow Temperature Profile