Bipolar Transistors
Thermal Stability and Design

Description

This document describes the thermal stability and thermal design of bipolar transistors.

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1. Thermal stability and thermal design for transistor circuits

As described in Chapter 1, one of the characteristics of transistors and other semiconductor devices is that the electrical characteristics are very sensitive to temperature. Therefore, when creating a circuit design, it is necessary to consider changes in the operating point due to changes in temperature.

1.1. Temperature characteristics of transistors

(1) Thermal stability

The performance stability factor S is defined by:

$$S = \frac{\partial I_C}{\partial I_{CBO}} \quad \cdots\cdots (1\text{–}1)$$

This equation represents a change in the collector current I_C in response to a change in the collector cut-off current due to a change in temperature. The transistor parameters with the greatest temperature dependence are the cut-off current I_{CBO} (I_{CEO}) and the base-emitter voltage V_{BE}. These parameters are expressed as a function of temperature:

$$I_{CBO(T_X)} = I_{CBO(T_O)}\, e^{K(T_X - T_O)} \quad \cdots\cdots (1\text{–}2)$$

$$I_E = I_{CBO}\, e^{\frac{q V_{BE}}{k T}} \quad \cdots\cdots (1\text{–}3)$$

T_O : Reference temperature (K)
T_X : Temperature to be found (K)
K : Temperature coefficient, which is generally 0.07/ °C to 0.08/ °C for silicon transistors
q : Elementary charge (1.602×10^{-19} C)
k : Boltzmann constant (1.38×10^{-23} J/K)
T : Absolute temperature (K)

Let the power dissipation applied to a junction be P_C. Then, a change in P_C, $\Delta P_{C(1)}$, due to some reason causes a junction temperature change of $\Delta P_{C(1)} R_{th(j\text{-}a)}$. This causes changes in I_{CBO} and V_{BE} (ΔI_{CBO} and ΔV_{BE}), which in turn cause changes of S I_{CBO} and g_m ΔV_{BE} in the collector current respectively. (The transconductance g_m of the transistor is defined as $g_m = \partial I_C / \partial V_{BE}$.)

If the variation in the power dissipation caused by these changes, $P_{C(2)}$, is greater than $\Delta P_{C(1)}$, the junction temperature continues to increase. It is therefore necessary to keep

the power dissipation due to ΔI_{CBO} and ΔV_{BE}, $P_{C(2)}$, below $P_{C(1)}$.

Hence, it is considered that a transistor is stable when the following condition is met:

$$\Delta P_{C(1)} \geqq V_C \left(S \, \Delta I_{CBO} + g_m \, \Delta V_{BE} \right) \quad \cdots\cdots (1\text{–}4)$$

where, V_C is collector voltage.

Equation 1-4 can be restated as:

$$V_C \, S \, \frac{\Delta I_{CBO}}{\Delta P_C} + V_C \, gm \, \frac{\Delta V_{BE}}{\Delta P_C} \leqq 1 \quad \cdots\cdots (1\text{–}5)$$

As ΔT is considered to be equal to $\Delta P_C R_{th(j\text{-}a)}$, differentiating Equation 1-2 with respect to P_C gives:

$$\frac{\Delta I_{CBO}}{\Delta P_C} = \frac{\Delta I_{CBO}}{\Delta T} \, \frac{\Delta T}{\Delta P_C} = K \, R_{th(j\text{-}a)} \, I_{CBO(T_0)} \, e^{K \left(T_X - T_0 + P_C R_{th(j\text{-}a)} \right)} \quad \cdots\cdots (1\text{–}6)$$

From Equation 1-3, the temperature characteristics of V_{BE} that provide a constant I_E can be calculated as follows:

$$\frac{\Delta V_{BE}}{\Delta T} \approx \frac{k \, K \, T}{q} \approx -2.0 \times 10^{-3} \ V/°C \quad \cdots\cdots (1\text{–}7)$$

* $\Delta V_{BE}/\Delta T$ is normally calculated to be -1.8 to -2.2 mV/ °C depending on the bias condition of the transistor. In general, -2 mV/ °C is used as a typical temperature coefficient. The temperature coefficient of a Darlington transistor is twice as great as this value (-4.0 to -4.5 mV/ °C).

Hence:

$$\frac{\Delta V_{BE}}{\Delta P_C} = \frac{\Delta V_{BE}}{\Delta T} \, \frac{\Delta T}{\Delta P_C} \approx -2.0 \times 10^{-3} \times R_{th(j\text{-}a)} \quad \cdots\cdots (1\text{–}8)$$

Substituting Equations 1-6 and 1-8 into Equation 1-5 gives:

$$V_C \, S \, K \, R_{th(j\text{-}a)} \, I_{CBO(T_O)} \, e^{K \left(T_X - T_O + P_C R_{th(j\text{-}a)} \right)} - 2.0 \times 10^{-3} \, R_{th(j\text{-}a)} \, V_C \, gm \leqq 1 \quad \cdots\cdots (1\text{–}9)$$

$$T_X - T_O + P_C \, R_{th(j\text{-}a)} \geqq T_{jmax} - T_O$$

A transistor circuit is considered stable if Equation 1-9 is satisfied. However, this equation is too complicated to be of practical use. When changes in I_C in the definition of S in response to changes in V_{BE} are taken into consideration, the second term of Equation 1-9 can be ignored in practice. Therefore, Equation 1-9 can be simplified to:

$$V_C \, S \, K \, R_{th\,(j-a)} \, I_{CBO\,(To)} \, e^{K\,(Tx - To + P_C R_{th\,(j-a)})} \leqq 1 \quad \cdots\cdots (1\text{–}10)$$

$$Tx - To + P_C R_{th\,(j-a)} \geqq T_{jmax} - To$$

The critical voltage V_{crit} is defined as:

$$V_{crit} = \frac{1}{S \, K \, R_{th\,(j-a)} \, I_{CBO\,(To)}} \quad \cdots\cdots (1\text{–}11)$$

Substituting Equation 1-11 into Equation 1-10 gives:

$$\frac{V_C}{V_{crit}} \, e^{K\,(Tx - To + P_C R_{th\,(j-a)})} \leqq 1 \quad \cdots\cdots (1\text{–}12)$$

Let K be 0.08 and the reference temperature T_o (ambient temperature) be 25 °C. Then, Equation 1-12 can be restated as:

$$P_C \, R_{th(j-a)} + T - 25 \leqq 29 \ln \frac{V_C}{V_{crit}} \quad \cdots\cdots (1\text{–}13)$$

Therefore, Equation 1-11 and Equation 1-13 represent the conditions that a transistor circuit must satisfy to maintain stability.

(2) Stability factors for bias circuits

Figure 1.1 shows the stability factors for several bias circuits. (a), (b), and (c) are typical bias circuits whereas (d) is a bias circuit in which the DC resistance of the input transformer cannot be ignored.

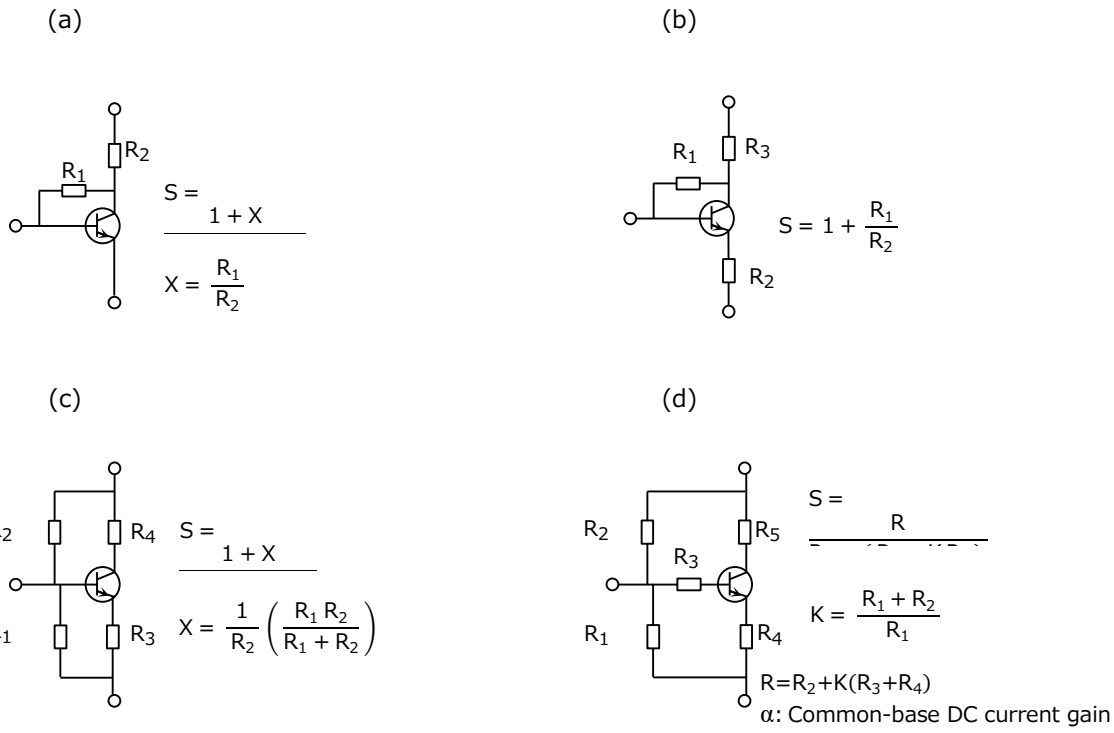


Figure 1.1 Stability factors for bias circuits

Generally, it is preferable for a stability factor to be small. However, a reduction in the stability factor increases DC dissipation, causing efficiency to deteriorate. Since reducing the stability factor causes an increase in DC dissipation, a temperature-compensating device is generally used to improve the thermal stability of the output-stage bias circuit.

The use of a temperature-compensating device makes it possible to freely select a thermal stability level. Thermistors and varistors are commonly used as temperature-compensating devices. For how to use these devices, refer to the respective technical documents.

1.2. Thermal design

(1) Maximum allowable collector power dissipation and equivalent thermal circuit

When the bias circuit is sufficiently thermally stable, the maximum collector power dissipation ($P_{C(max)}$) of a transistor can be expressed as follows in terms of the ambient temperature T_a, the transistor's maximum junction temperature $T_{j(max)}$, and the total thermal resistance from the junction to the ambient $R_{th(j-a)}$:

$$P_{C\,max\,(T_a)} = \frac{T_{j\,max} - T_a}{R_{th\,(j-a)}} \quad , \quad P_{C\,max\,(Tc)} = \frac{T_{j\,max} - T_C}{R_{th\,(j-c)}} \qquad \cdots\cdots (1\text{–}14)$$

A heat flow can be modeled by analogy to an electrical circuit. Using this model, the heat flow from the junction of a transistor to the ambient air is expressed using thermal resistances and thermal capacitances. Figure 1.2 shows an equivalent thermal circuit in a thermally steady state.

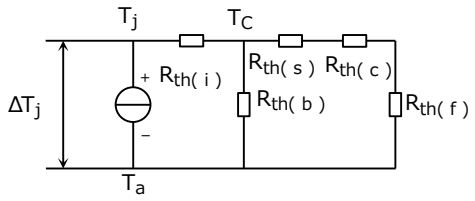


Figure 1.2 Equivalent thermal circuit

$R_{th(i)}$: Junction-to-case thermal resistance
$R_{th(b)}$: Case-to-ambient thermal resistance
$R_{th(s)}$: Thermal resistance of an insulation plate
$R_{th(c)}$: Contact thermal resistance between case and heat sink
$R_{th(f)}$: Thermal resistance of a heat sink

From the equivalent circuit of Figure 1.2, the junction-to-ambient thermal resistance $R_{th(j-a)}$ can be calculated as follows:

$$R_{th\,(j-a)} = R_{th\,(i)} + \frac{R_{th\,(b)}\left(R_{th\,(s)} + R_{th\,(c)} + R_{th\,(f)}\right)}{R_{th\,(b)} + R_{th\,(s)} + R_{th\,(c)} + R_{th\,(f)}} \qquad \cdots\cdots (1\text{–}15)$$

Since no heat sink is generally used for transistors with medium or lower output, $R_{th(j-a)}$ can be calculated as:

$$R_{th\,(j-a)} = R_{th\,(i)} + R_{th\,(b)} \qquad \cdots\cdots (1\text{–}16)$$

The datasheets for low- or medium-output transistors show their maximum allowable collector power dissipation at an ambient temperature (T_a) of 25 °C. This is calculated as follows from $R_{th(j-a)}$ given by Equation 1-16 and $T_{j(max)}$.

$$P_{Cmax\,(Ta\,=\,25\,°C)} = \frac{T_{j\,max} - 25}{R_{th\,(j-a)}} \qquad \cdots\cdots (1\text{–}17)$$

The case-to-ambient thermal resistance $R_{th(b)}$ varies with the material and shape of the case. Generally, $R_{th(b)}$ is significantly larger than $R_{th(i)}$, $R_{th(c)}$, $R_{th(s)}$, and $R_{th(f)}$. Therefore, Equation 1-15 can be simplified to:

$$R_{th(j-a)} = R_{th(i)} + R_{th(c)} + R_{th(s)} + R_{th(f)} \quad \cdots\cdots (1\text{–}18)$$

Equation 1-18 can be used to create a thermal design that satisfies the maximum rating requirement for DC dissipation. When transistors are used in a switching circuit, great care is required to ensure that the peak T_j value does not exceed $T_{j(max)}$.

(2) Pulse response of junction temperature

Generally, the thermal impedance of a transistor is modeled as a distributed constant circuit as shown in Figure 1.3.

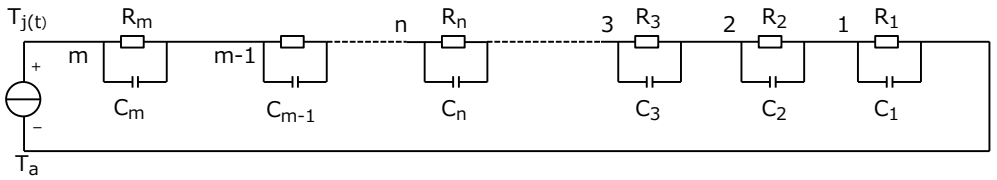


Figure 1.3 Circuit of transient thermal impedance

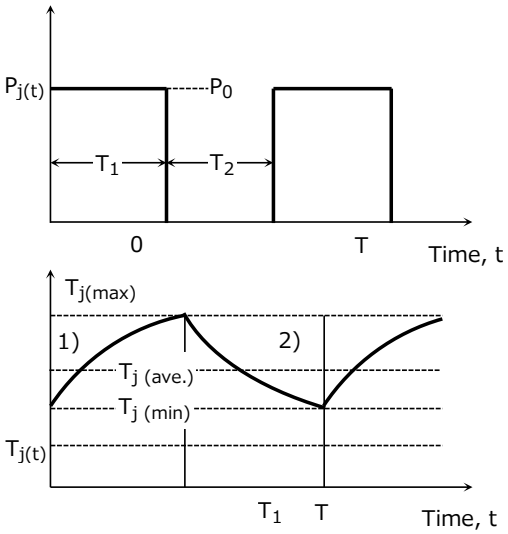


Figure 1.4 Temperature change when pulse loss is applied

When the pulse dissipation $P_{j(t)}$ shown in Figure 1.4 is applied to the circuit of Figure 1.3, a change in junction temperature $T_{j(t)}$ that appears at the mth parallel RC circuit under stable thermal conditions can be calculated as follows:

1) In the region where $P_{j(t)} = P_0$:

$$T_{j(t)} = \sum_{n-1}^{m} \{ (P_0 R_n) - T_{n(min)} \} \left\{ 1 - e^{\left(\frac{-t}{C_n R_n} \right)} \right\} + T_{n(min)}$$

2) In the region where $P_{j(t)} = 0$:

$$T_{j(t)} = \sum^{m} \left\{ T_{n(min)} e^{\left(\frac{-t}{C_n R_n} \right)} \right\}$$

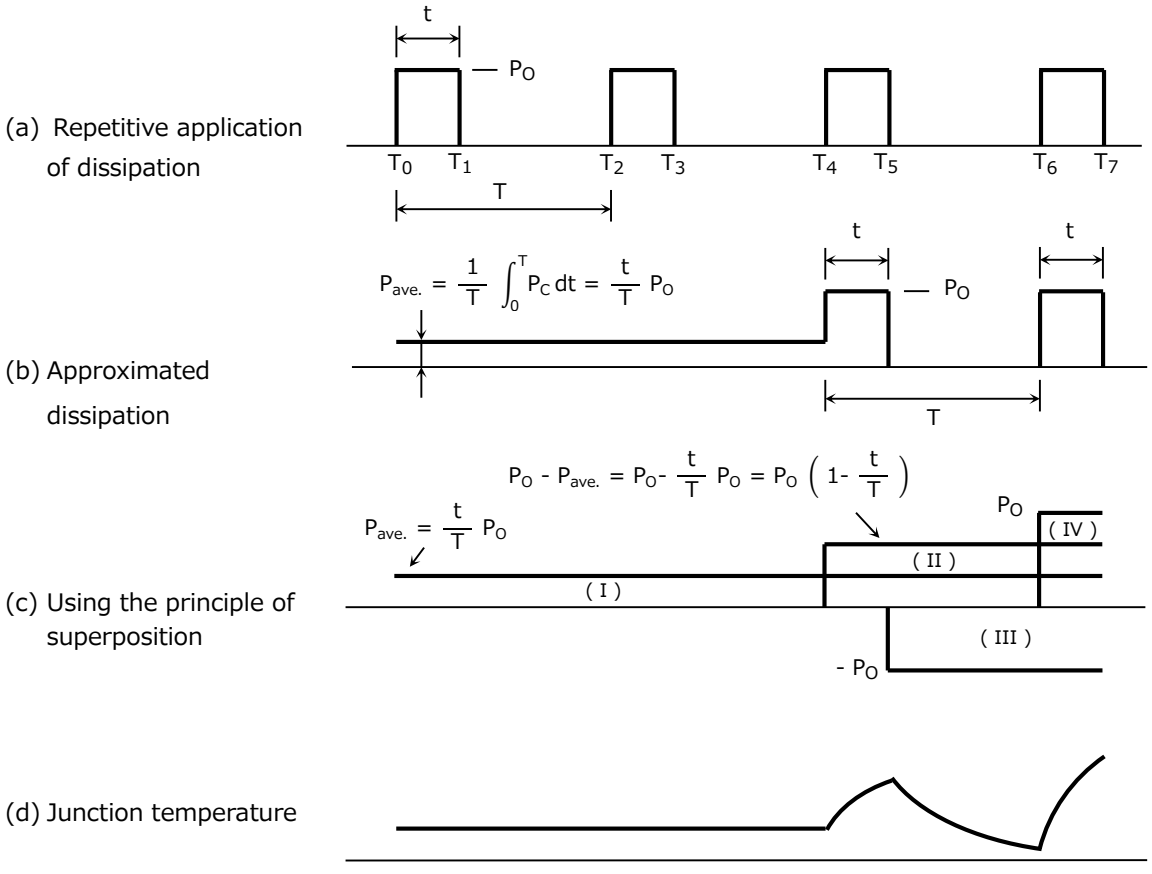
For typical transistors, the actual $P_{j(t)}$ value can be approximated by substituting 4 for n. However, if the C and R values are indefinite, it is difficult to calculate T_j. Therefore, $T_{j(max)}$ is generally calculated using transient thermal impedance as follows:

Figure 1.5 shows an example of typical transient thermal impedance characteristics.

Suppose that a single rectangular pulse (with a pulse width of t and a peak value of P_0) is applied. From the Figure, we read the transient thermal impedance at a pulse width of t, and then use Equation 1-21 to calculate $T_{j(max)}$.

$$T_{j(max)} = r_{th(t)} P_O + T_a \quad \cdots\cdots (1\text{–}21)$$

When a repetitive pulse train with a cyclic period of T is applied as shown in Figure 1.4, T_{jpeak} is given by Equation 1-22 using the principle of superposition.



$$\Delta T_{j(I)} = P_O \frac{t}{T} R_{th(j-a)}$$

$$\Delta T_{j(II)} = P_O \left(1 - \frac{t}{T} \right) r_{th(T+t)}$$

$$\Delta T_{j(III)} = - P_O \, r_{th(T)}$$

$$\Delta T_{j(IV)} = P_O \, r_{th(t)}$$

$$T_{j(max)} = P_O \left[\frac{t}{T} R_{th(j-a)} + \left(1 + \frac{t}{T} \right) r_{th(T+t)} - r_{th(T)} + r_{th(t)} \right] + T_a$$

..... (1–22)

Equation 1-22 is applicable only to the thermally limited region of the SOA where no current concentration occurs due to secondary breakdown.

Great care should be exercised in the thermal design for a pulsed power application to ensure that $T_{j(max)}$ given by Equation 1-22 does not exceed the maximum rated junction temperature of the transistor.

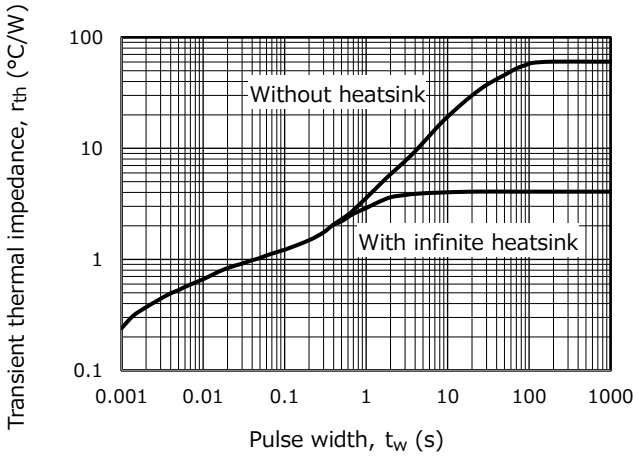


Figure 1.5 Example of transient thermal impedance

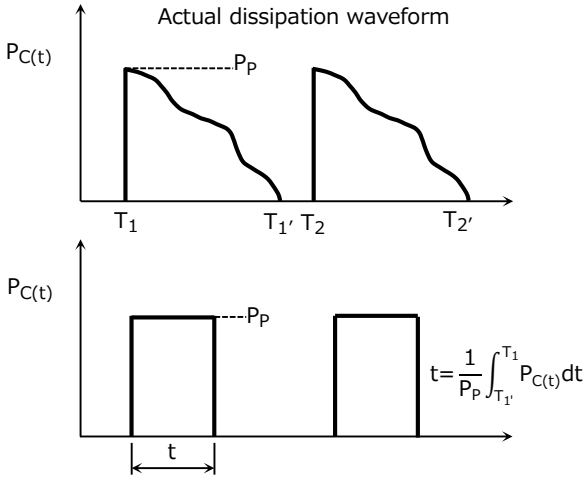


Figure 1.6 The approximation to a square waveform of the loss waveform

The above description assumes that a rectangular waveform is applied to a transistor. However, for actual transistor applications, a rectangular $P_{j(t)}$ waveform is seldom used.

Therefore, in order to estimate T_{jpeak} using Equation 1-22, a power dissipation waveform should be approximated to a rectangular wave as shown in Figure 1.6.

Sine and triangular waves can be approximated to rectangular waves as shown in Figure 1.7.

T_o obtain a rectangle with an area equal to a half-sine or triangle area, multiply the peak value of P_P by 0.7 in the case of (a) and (b), and multiply the pulse width by 0.91 for (a) and by 0.71 for (b).

In the case of (c) and (d), use the same peak value of P_P, and multiply the pulse width by 0.63 for (c) and by 0.5 for (d).

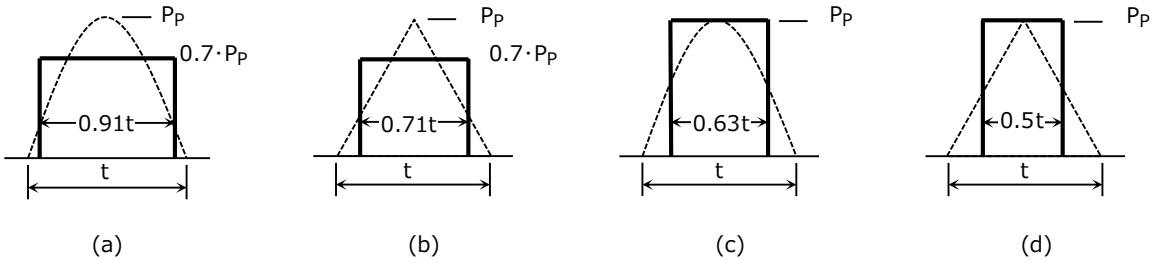


Figure 1.7 The method to approximate a sine wave and a triangular wave loss waveform to a square waveform

1.3. Thermal resistance

The thermal resistance values shown in the equivalent thermal circuit of Figure 1.2 can be explained as follows:

(1) Junction-to-case thermal resistance (internal thermal resistance): $R_{th(i)}$

The internal thermal resistance $R_{th(i)}$ from the junction of a transistor to the case depends on the structure and material of the transistor and differs from transistor to transistor.

To measure internal thermal resistance, the case of the transistor must be cooled to maintain a constant temperature. When the case temperature T_C is held at 25 °C, the maximum allowable power dissipation, $P_{C(max)}$, of a transistor can be calculated using Equation (1-23):

$$P_{C\,max} = \frac{T_{j\,max} - T_C}{R_{th\,(i)}} = \frac{T_{j\,max} - 25}{R_{th\,(i)}} \quad (W) \qquad \cdots\cdots (1\text{-}23)$$

In the datasheets for high-power transistors, the maximum allowable collector power dissipation $P_{C(max)}$ is specified either at T_C = 25 °C or assuming the use of an infinite heat sink. $P_{C(max)}$ is determined by the internal thermal resistance of the transistor as indicated by Equation 1-23.

(2) Contact thermal resistance: $R_{th(c)}$

Contact thermal resistance $R_{th(c)}$ varies according to the condition of the contact surface between the case of a transistor and a heat sink. This condition is greatly affected by factors such as the evenness, coarseness, and area of contact, as well as the tightening of the transistor onto the heat sink. The influence of the coarseness and unevenness of the contact surface can be reduced by applying silicone grease or attaching silicone rubber.

(3) Insulation plate's thermal resistance: $R_{th(s)}$

If it is necessary to provide electrical insulation between a transistor and a heat sink, an insulation plate must be inserted between them. The thermal resistance of this insulation plate $R_{th(s)}$ varies with the materials, thickness, and area of the plate and is not negligible.

For packages insulated by mold resin, the thermal resistance specified for a transistor includes the insulator's thermal resistance $R_{th(s)}$.

(4) Heat sink's thermal resistance: $R_{th(f)}$

The thermal resistance of a heat sink can be considered as the distributed thermal resistance of a heat path from the surface of a heat sink to the ambient air. The thermal resistance of a heat sink depends on the condition of the ambient, a difference in temperature between the heat sink and the ambient air, and the effective area of the heat sink. It is difficult to mathematically express $R_{th(f)}$. At present, $R_{th(f)}$ is obtained by measurement. Figure 1.8 shows an example of thermal resistance data measured for a transistor standing vertically at the center of a heat sink.

Various heat sinks are available from many vendors. Optimal heat sinks should be selected, referring to their technical datasheets.

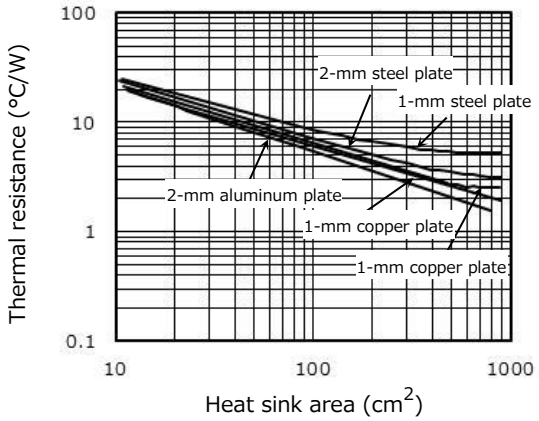


Figure 1.8 Heat sink surface area vs. thermal resistance

1.4. Example of thermal design calculation

This section provides examples of calculation for thermal design. The given constants or the constants that need to be found are as follows:

(a) $R_{th(i)}$ and $T_{j(max)}$ of the transistor

(b) Collector power dissipation of the transistor: P_C

(c) Ambient temperature: Ta

(d) Thermal resistance of a heat sink: $R_{th(f)}$

Example 1: Let's calculate the thermal resistance required for a heat sink when the $R_{th(i)}$, $T_{j(max)}$, and P_C of a transistor and the ambient temperature are predefined.

Suppose that the transistor is used at a collector power dissipation (P_C) of 15 W and an ambient temperature (T_a) of 60 °C.

The conditions given are $P_{C(max)}$ = 80 W (at T_C = 25 °C) , $T_{j(max)}$ = 150 °C, P_C = 15 W, and T_a = 60 °C. Suppose that the sum of the thermal resistance of an insulating plate and silicone grease is $R_{th(c)} + R_{th(s)}$ = 0.8 °C/W.

From Equation 1-17 and Equation 1-23,

$$R_{th(i)} = \frac{T_{j\,max} - T_C}{P_{C\,max}} = \frac{150 - 25}{80} \approx 1.6\ °C/W$$

$$R_{th(j-a)} = \frac{T_{j\,max} - T_a}{P_C} = \frac{150 - 60}{15} = 6\ °C/W$$

From Equation (1-18),

$$R_{th(f)} = R_{th(j-a)} - (R_{th(i)} + R_{th(C)} + R_{th(s)}) \approx 6 - (1.6 + 0.8) = 3.6\ °C/W$$

Therefore, a heat sink with a thermal resistance less than 3.6 °C/W is required. Figure 1.8 shows that when we use a heat sink made of a 2-mm aluminum plate, a heat sink with an area of 200 cm^2 is required. Therefore, an aluminum heat sink measuring 140 × 140 × 2 mm is suitable.

Example 2: Let's calculate the maximum allowable collector power dissipation of a transistor when the $R_{th\ (i)}$ and $T_{j(max)}$ of the transistor, the ambient temperature, and the thermal resistance of a heat sink are predefined.

Suppose that a transistor is attached to an aluminum heat sink with the size of 100 × 100 × 2 mm using an insulating plate and silicone grease and that the transistor is used at an ambient temperature (T_a) of 60 °C. The conditions given are P_C = 20 W (at T_C = 25 °C), $T_{j(max)}$ = 150 °C, and T_a = 60 °C. From Figure 2.8, $R_{th\ (f)}$ = 5.4 °C/ W. Suppose that $R_{th(c)} + R_{th(s)}$ = 0.6 °C/ W.

From Equation (1-23),

$$R_{th\,(i)} = \frac{T_{j\ max} - 25}{P_{C\ max}} = \frac{150 - 25}{20} = 6.25 \quad °C / W$$

From Equation (1-18),

$$R_{th\,(j-a)} = R_{th\,(i)} + R_{th\,(C)} + R_{th\,(s)} + R_{th\,(f)} = 6.25 + 0.6 + 5.4 = 12.25 \quad °C / W$$

From Equation (1-14),

$$P_C = \frac{T_{j\,max} - T_a}{R_{th\,(j-a)}} = \frac{150 - 60}{12.25} \approx 7.3 \quad W$$

Example 3: Let's calculate the maximum operating ambient temperature when the $R_{th\ (i)}$, $T_{j(max)}$, and P_C of a transistor and the thermal resistance of a heat sink are predefined.

Suppose that a transistor is attached to an aluminum heat sink with the size of 100 × 100 × 2 mm using an insulating plate and silicone grease. Also suppose that a transistor operates at a collector power dissipation of 15 W. The conditions given are $P_{C(max)}$= 150 W (at T_C = 25 °C) and $T_{j(max)}$ = 150 °C. From Figure 1.8, $R_{th\ (f)}$ = 5.4 °C/ W; hence, P_C = 15 W. $R_{th(c)} + R_{th(s)}$ = 0.7 °C/ W.

From Equation (1-23),

$$R_{th\ (i)} = \frac{T_{j\ max} - T_C}{P_{C\ max}} = \frac{150 - 25}{150} \approx 0.83\ °C / W$$

From Equation (1-18),

$$R_{th\ (j-a)} = R_{th\ (i)} + R_{th(C)} + R_{th(s)} + R_{th(f)} = 0.83 + 0.7 + 5.4 \approx 6.9\ °C / W$$

From Equation (1-14),

$$T_a = T_{j\ max} - R_{th\ (j-a)} P_C = 150 - 6.9 \times 15 \approx 46.5\ °C$$

Therefore, the maximum operating ambient temperature is 46.5 °C.

1.5. Thermal design taking reliability into consideration

In addition to thermal stability and the thermal design considerations described above, reliability should be taken into account.

For industrial and other applications requiring many transistors, their maximum ratings should be derated, considering reliability.

Since the useful life of a transistor decreases exponentially with its junction temperature, reliability can be increased by derating the maximum ratings with respect to junction temperature (although the benefit of derating depends on the type of transistor). It is therefore necessary to minimize the junction temperature (i.e., the sum of the ambient temperature and a temperature rise caused by the power applied), particularly for applications requiring high reliability.

In addition, if transistors are exposed to sudden changes in junction temperature when a system is turned on and off, their internal lead bonds could suffer thermal fatigue damage owing to repeated on-off cycles. To prevent this problem, their junction temperature as well as changes in junction temperature should be considered when derating transistors.

The following is an example of thermal design calculation, considering reliability.

Example 4: Let's calculate the size of a heat sink required when the collector power dissipation and ambient temperature are predefined.

Suppose that the transistor operates at a collector power dissipation of 3 W and an ambient temperature of up to 55 °C. The conditions given are $P_{C(max)}$ = 25 W (at T_C = 25 °C) and $T_{j(max)}$ = 150 °C.

From Equation (1-23),

$$R_{th\,(i)} = \frac{T_{j\,max} - T_C}{P_{C\,max}} = \frac{150 - 25}{25} = 5 \quad °C / W$$

To achieve high reliability, let's derate the maximum operating junction temperature by 50 °C:

$$T_{j\,(opr)\,max} = 150 - 50 = 100 \quad °C$$

From Equation (1-14),

$$R_{th\,(j-a)} = \frac{T_{j\,(opr)\,max} - T_{a\,(max)}}{P_C} = \frac{100 - 55}{3} = 15 \quad °C / W$$

Suppose that $R_{th(c)} + R_{th(s)}$ = 0.6 °C/ W. Then, from Equation 1-18:

$$R_{th(f)} = R_{th(j-a)} - (R_{th(i)} + R_{th(c)} + R_{th(s)}) = 15 - (5 + 0.6) = 9.4\ °C/W$$

Therefore, a heat sink with a thermal resistance of less than 9.4 °C/ W is required.

From Figure 1.8, an aluminum heat sink with the size of 65 × 65 × 2 mm is suitable.

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