Benefits of a Point-of-Use Clock for Jitter Optimization

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Most electronics introduced today contain a large amount of digital circuitry. Digital circuits rely on a repeating trigger signal to instigate each subsequent action in their process. This is the clock signal. Clocks are required for each circuit with digital content in the system. Clock Generators are chips that output these necessary signals. This set of clock signals is often referred to as the clock tree.

Renesas is the largest vendor of clock generation devices today. Clock vendors, such as Renesas, specify the jitter performance which customers can achieve at the output of individual devices which comprise a clock tree. Clock vendors are not able to specify the level of jitter our customers can expect to achieve at the end points of their clock trees. Board level design choices have a significant impact on noise at the input of the devices being clocked.

Something which can be particularly challenging to predict and manage is the amount of noise which gets imposed on a clock trace as it travels across a board from the final clock device to the destination device, i.e. its point-of-use (PoU). It is this fundamental challenge that makes a system architecture which places the final clock chip very close to the PoU sensible.

There are plenty of devices on the market that offer wide fanout with very good performance (150 fs jitter or less), which act as the primary clock source (PCS) and can provide every clock signal for a complex, network-synchronized system. The 8A34001 from Renesas is an example of such a clock device. It features 12 differential outputs from up to 8 different frequency domains, relying on up to 8 different reference inputs. For systems needing more and/or better clock signals, designers will add buffers or additional clock generators and/or jitter attenuators. The RC32504 is a high performance jitter attenuator in a very small (4x4mm) package making it an excellent fit for such systems.

Even those systems which don't need more clock signals than the 8A34001 provides may find the RC32504 to be a valuable tool. If the noise imposed by routing the clock across the board results in a signal that is too noisy at the PoU, the RC32504 can solve that problem. The RC32504 requires minimal external circuitry and is 1/3 the size of similar devices, making it much easier to place very near the PoU.

In many systems, only a subset of the clocking signals need to meet very stringent (<100 fs) jitter levels. It is becoming common in such systems to place one of these PoU jitter attenuators very near those devices demanding the ultimate performance, while simply routing signals from the primary reference clock (PRC) to the other devices with less demanding jitter needs.

Where wide fanout of high performance, low jitter clocks is required, the system designer will be confronted by a choice. Devices exist which fanout as many as 12 clean clock signals. These devices are in significantly larger (9x9) packages. Utilizing 3 of the RC32504 instead uses 40% less board space, and

allows the designer to place the clean clock source much closer to at least two of those devices, thereby optimizing the jitter at the PoU.

Another intriguing use case has emerged at customers in the form of the following scenario: You are building a board with devices (PHY, MAC, etc) that call for very low jitter signals. You budget the jitter across your timing tree. It looks achievable, but very tight. The RC32504 can help. Proactively place them at the point of use, but design the board such that you are able to not populate the RC32504 socket if the signals are clean enough. If you do need some localized jitter clean up, you don't need to re-spin the board, just populate the socket and you are good to go. At 4x4mm in size, the amount of board space you are dedicating to this safety net is minimal.