

Power Management IC designed for “NXP®i.MX 8M mini”

## BD71847AMWV Platform Design Guide

### 1. Introduction

BD71847AMWV is a Power Management Integrated Circuit (PMIC) available in 56-QFN package and dedicated to the application powered by 5V input. PMIC includes six Buck converters, six LDOs, one internal load switch and crystal oscillator driver for RTC clock. These functions are designed to support the specific power requirements from NXP i.MX 8M mini platform to achieve the required performance for cost-sensitive applications.

The below figure is the outline of the power map between PMIC and i.MX 8M mini SoC, showing that all voltage rails required by SoC are satisfied.

“BD71847AMWV Platform Design Guide” provides the guideline for designing PCB including recommendation for the PCB layer stack up, the components placement and the PCB routings.

To reduce the risk that comes from PCB layout or parts placement, the guideline is strongly recommended to be applied to the PCB design.

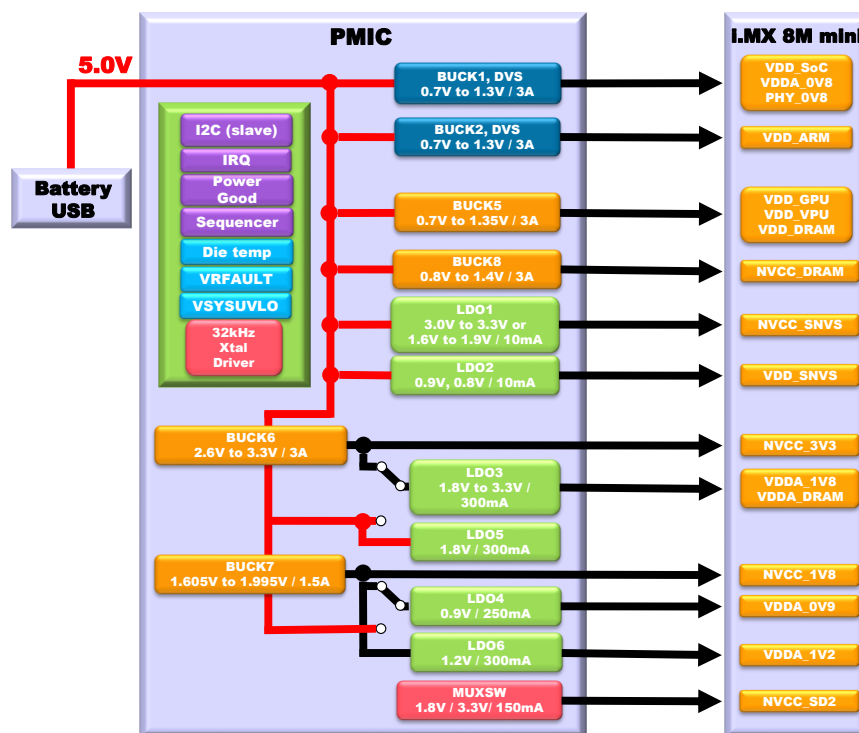


Figure 1.1 The system power map

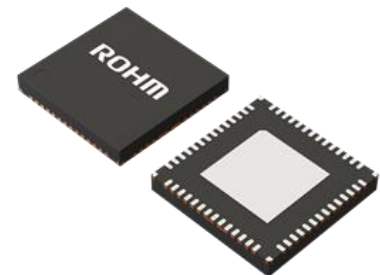


Figure 1.2 The package image

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## 2. Revision History

Table 2.1 Revision History

Revision Number	Description	Revision Date
1p0	Initial release	Mar. 7 <sup>th</sup> , 2019
1p1	Changed the comment for pull up source of PWRON_B	Mar. 11 <sup>th</sup> , 2019

### 3. Features

#### 3.1. Terminologies

Table 3.1 Acronyms, Conventions and Terminologies

Term	Definition
BOM	Bill Of Materials
PMIC	Power Management Integrated Circuit
FET	Field Effect Transistor
I2C	Inter-Integrated Circuit
IRQ	Interrupt ReQuest
LDO	Low Drop-Out Regulator
OCP	Over Current Protection
OVP	Over Voltage Protection
SoC	System-On-a-Chip

#### 3.2. Reference Documents

Table 3.2 Reference Documents

Document
BD71847AMWV Datasheet Rev.001.pdf
BD71847AMWV Reference Schematic Rev.1p0.pdf
BD71847AMWV Reference BOM Rev1p0.xlsx
BD71847AMWV Reference Layout Rev.1p0.brd
BD71847AMWV_Reference_Layout_Both_Surfaces_Rev1p0.brd
BD71847AMWV Schematic Guideline Rev1p1.xlsx

Note: For the customers requesting the smaller application area, ROHM provides the reference layout data of BD71847AMWV\_Reference\_Layout\_Both\_Surfaces\_Rev1p0.brd where all input and output capacitors for each VR are placed at bottom layer. When you need to place some parts at bottom layer because of the limited area, it can be referred to.

### 3.3. PMIC futures

BD71847AMWV supply the power required by SoC and peripheral devices for NXP i.MX 8M mini platform.

Once PMIC powered up, it can be controlled by I2C interface to determine the internal register settings.

The followings explain the features incorporated in the IC.

#### Voltage Rails

- 8ch low power consumption Buck Convertors with Integrated BUCK FETs
  - Buck1: 0.7V – 1.3V / 10mV step (DVS),  $I_{\text{OMAX}} = 3.0\text{A}$
  - Buck2: 0.7V – 1.3V / 10mV step (DVS),  $I_{\text{OMAX}} = 3.0\text{A}$
  - Buck5: 0.7V – 1.35V / 8 steps,  $I_{\text{OMAX}} = 3.0\text{A}$
  - Buck6: 3.0V – 3.3V / 100mV step,  $I_{\text{OMAX}} = 3.0\text{A}$
  - Buck7: 1.605V – 1.995V / 8 steps,  $I_{\text{OMAX}} = 1.5\text{A}$
  - Buck8: 0.8V – 1.4V / 10mV step,  $I_{\text{OMAX}} = 3.0\text{A}$
- 7ch LDO Regulator
  - LDO1: 3.0V – 3.3V / 1.6V – 1.9V,  $I_{\text{OMAX}} = 10\text{mA}$
  - LDO2: 0.9V / 0.8V,  $I_{\text{OMAX}} = 10\text{mA}$
  - LDO3: 1.8V – 3.3V,  $I_{\text{OMAX}} = 300\text{mA}$
  - LDO4: 0.9V – 1.8V,  $I_{\text{OMAX}} = 250\text{mA}$
  - LDO5: 1.8V – 3.3V,  $I_{\text{OMAX}} = 300\text{mA}$
  - LDO6: 0.9V – 1.8V,  $I_{\text{OMAX}} = 300\text{mA}$
- 1ch Internal General Switch
  - Mux Switch: 1.8V/3.3V,  $I_{\text{OMAX}} = 150\text{mA}$

#### Serial Interface

- I2C interface provides access to configuration registers.

#### Crystal Oscillator Driver

- 32.768kHz Crystal Oscillator Driver is included.

## 4. General Design Considerations

This chapter provides general PCB design guidelines such as BD71847AMWV general parts placement.

### 4.1. Package Dimension of BD71847AMWV

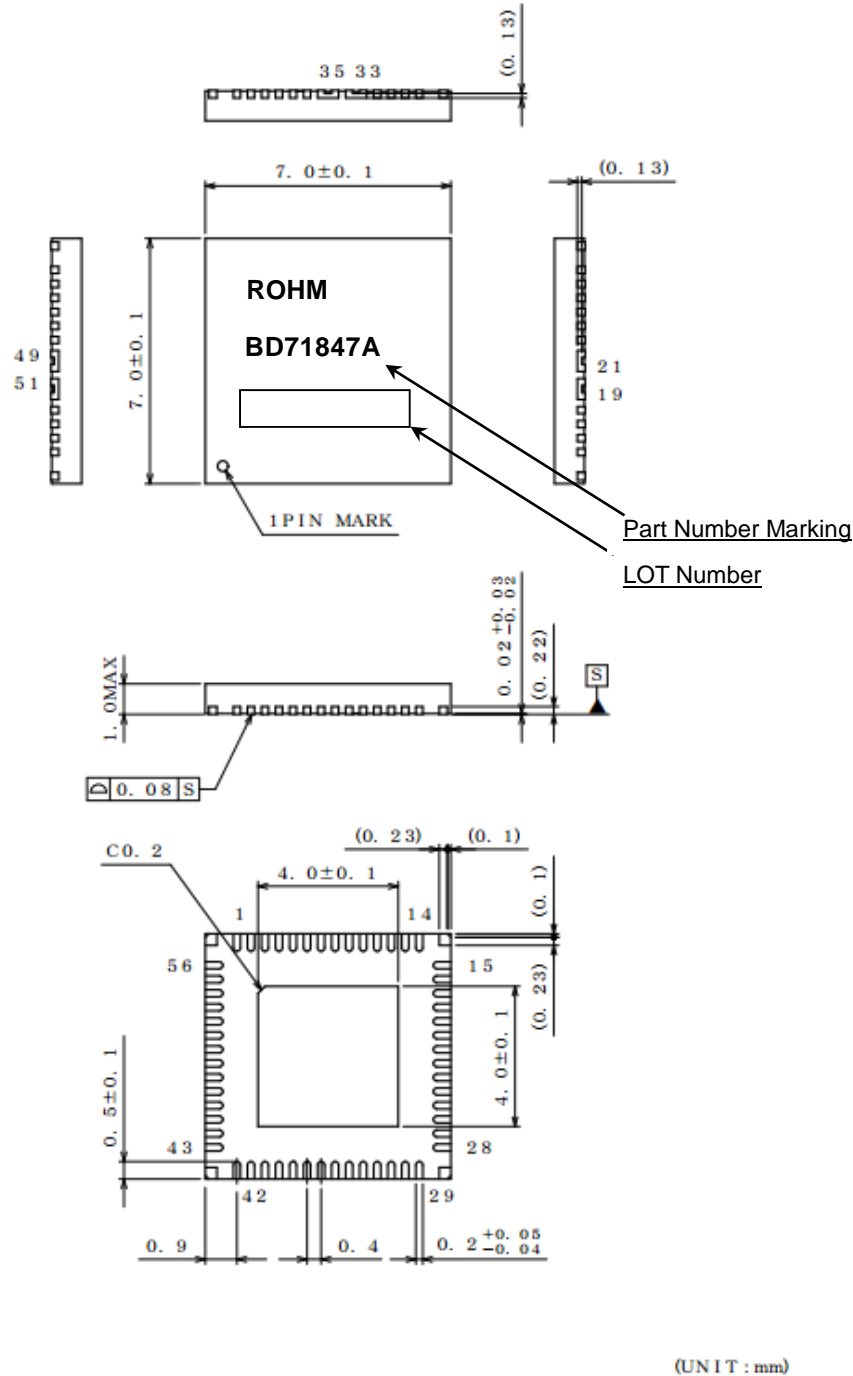


Figure 4.1 The package dimension of BD71847AMWV

## 4.2. Pin Configuration

The pin configuration of BD71847AMWV is designed and it will result in the effective routings between PMIC and SoC, memory device and other components.

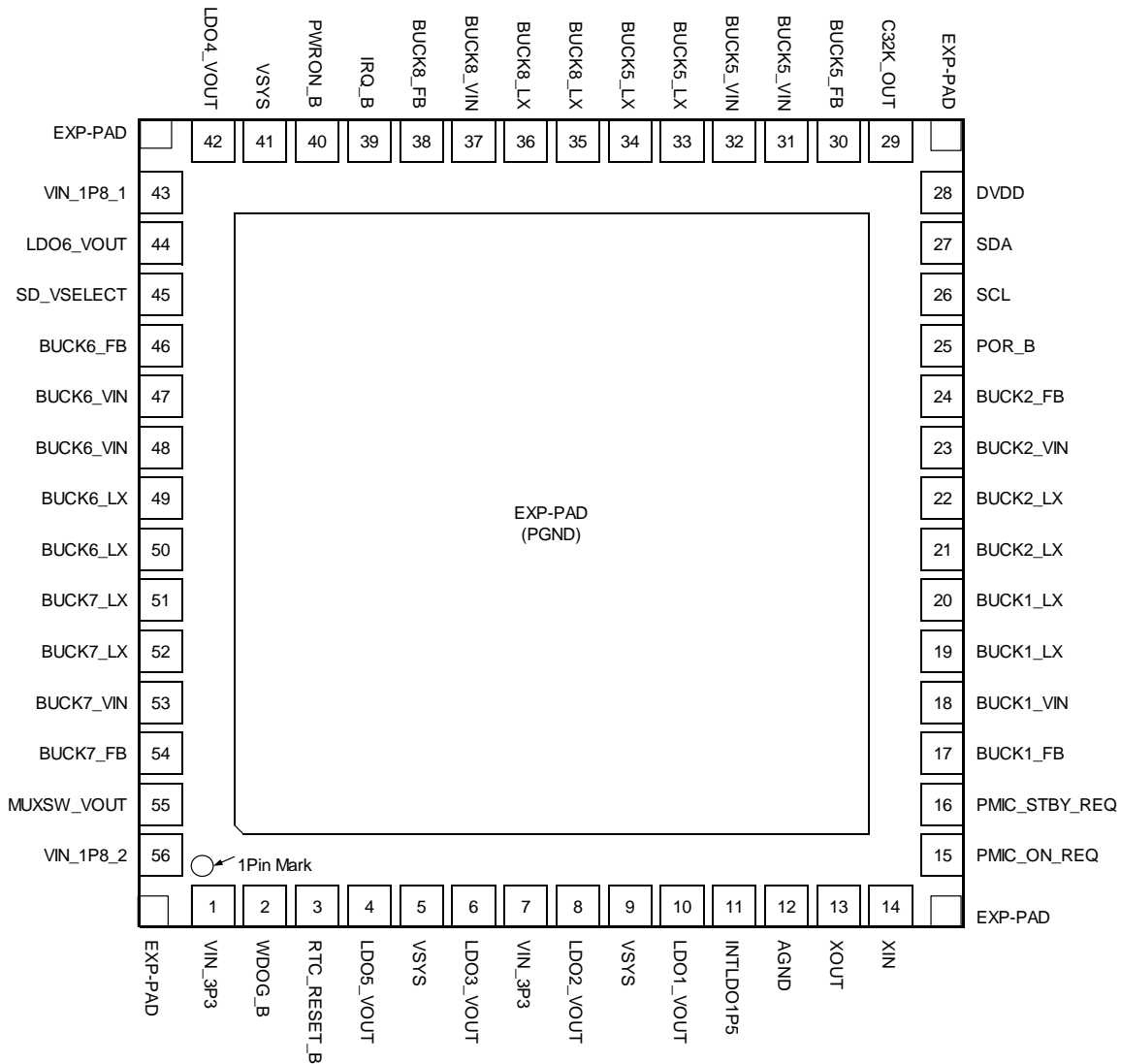


Figure 4.2 BD71847AMWV pin configuration

Note: EXP-PAD is the power GND for PMIC so it should be soldered to GND plane.

EXP-PADs assigned to 4 corners are also the same potentials with EXP-PAD.



### 4.3. General Stack-up Recommendations

Type-3 and 6 layers PCB technology are used for BD71847AMWV ROHM's EVM.

The following general stack-up is strongly recommended to be applied to all the routings on the PCB.

- Surface plane layers are recommended to apply 1.9 Mils thick copper.
- Internal plane layers are recommended to apply 1.2 Mils thick copper.
- It is recommended I2C signals to have the reference versus solid planes over the length of their routing and not to cross plane splits. Ground should be the ideal reference.
- The extra area in each layers should be filled with as much ground or other power rails as possible.  
There should not be any large free areas with no metal for each layer because of the improvement for heat dissipation. Large metal area also reduces stray resistance and inductance.

### 4.4. 6-layer Board Stack-up

BD71847AMWV ROHM's EVM uses Type 3 PCB technology and Figure 4.3 shows the 6-layer PCB stack-up.

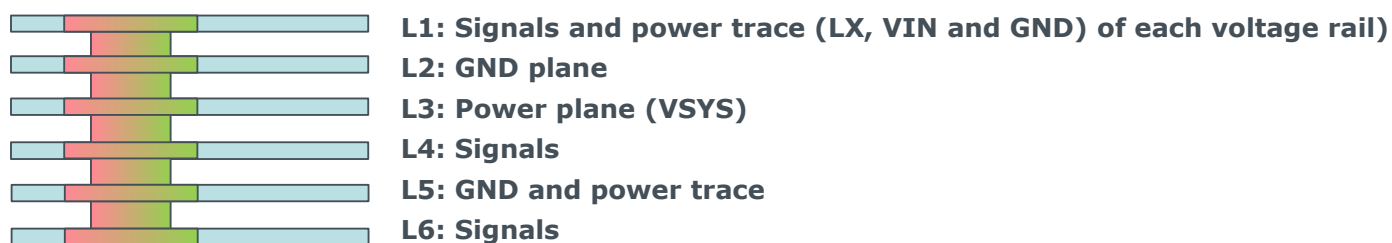


Figure 4.3 6-layers PCB stack-up

### 4.5. Via Guidelines

This section explains proper via-drill, pad, and anti-pad size.

Note:  
Improper drill, pad, and anti-pad size may cause some troubles on the PCB cost, reliability, manufacturability, and electrical characteristics.

Type-3 PCB technology employs plated through-hole (PTH) vias for breakout routing. The dimension of PTH vias may vary as necessary. Table 4.1 shows the recommended via dimension used for the breakout areas of BD71847AMWV. Figure 4.4 shows the image of PTH vias.

Table 4.1 Dimension example for PTH

Via type	Hole size	Pad size	Anti-Pad size
Plated through-hole (PTH)	300μm	600μm	900μm

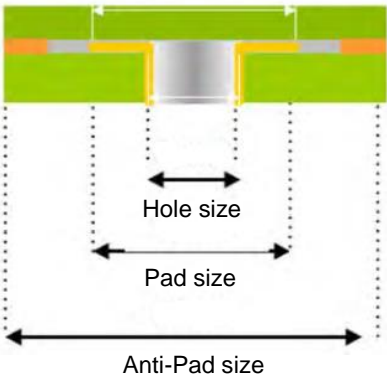


Figure 4.4 The image of PTH vias

#### 4.6. Placement of PTHs underneath the exposed pad

When the distance between the edge of metal mask of the exposed pad and PTH is close, the solder may get on the resist then the PTH and exposed pad of BD71847AMWV will be shorted. To avoid the soldering issue, it is highly recommended to keep the positions of PTHs away from the edge of the exposed pad by 500 $\mu$ m or more, and PTHs should be placed not to disrupt the current flows between each GND of the output capacitors and the exposed pad.

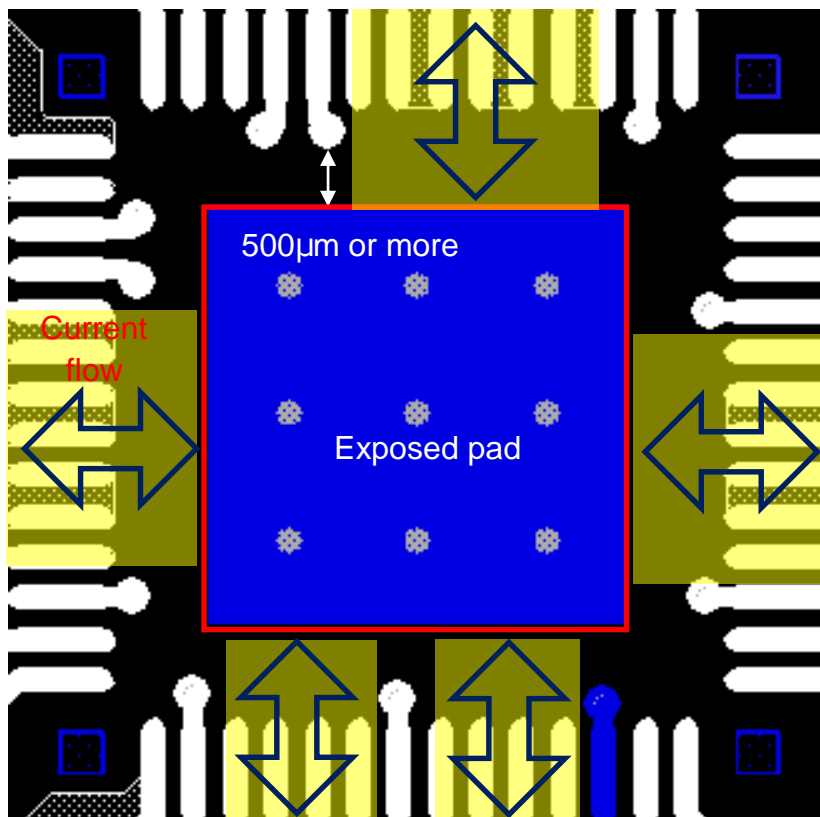


Figure 4.5 The clearance between PTH and the exposed pad

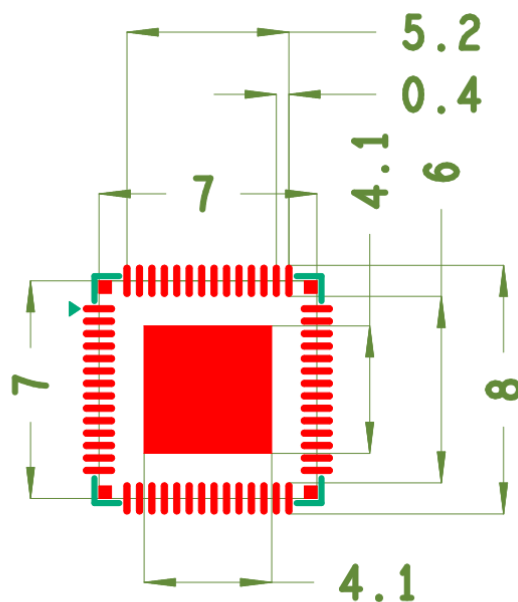
##### Note

The spaces for the current flows between GNDs of each output capacitor and exposed pad for PMIC PGND should be ensured. So it is recommended that the numbers of PTHs disturbing the current flows should be secured.

#### 4.7. The footprint of PMIC (BD71847AMWV)

To realize the layout of Figure 4.5, we used the dimension data as the footprint for PMIC.

It makes it possible to put some vias at the area between each pad and exposed pad.



**Pad Size: 0.2x1.0**

Figure 4.6 The dimension of the footprint (unit [mm])

## 4.8. Outline of PCB layout

For understanding the outline of ROHM's reference layout, the layout data for Layer 1(Top Layer) to 6 (Bottom layer) are shown in Figure 4.7 to Figure 4.12.

The layout is designed, supposing the position of the SoC as Figure 4.7

(1st pin of SoC is positioned at lower right.)

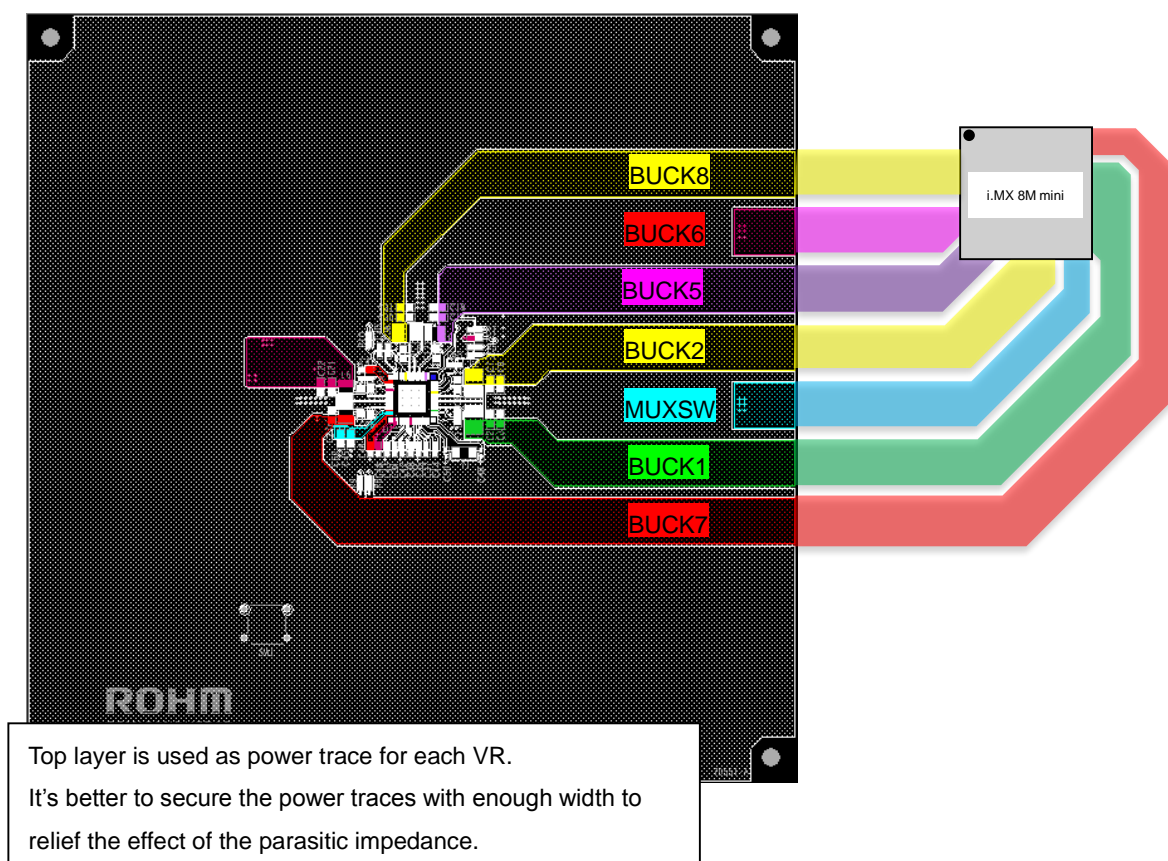


Figure 4.7 BD71847AMWV Reference Board Outline (Top Layer)



Figure 4.8 BD71847AMWV Reference Board Outline (Layer 2)

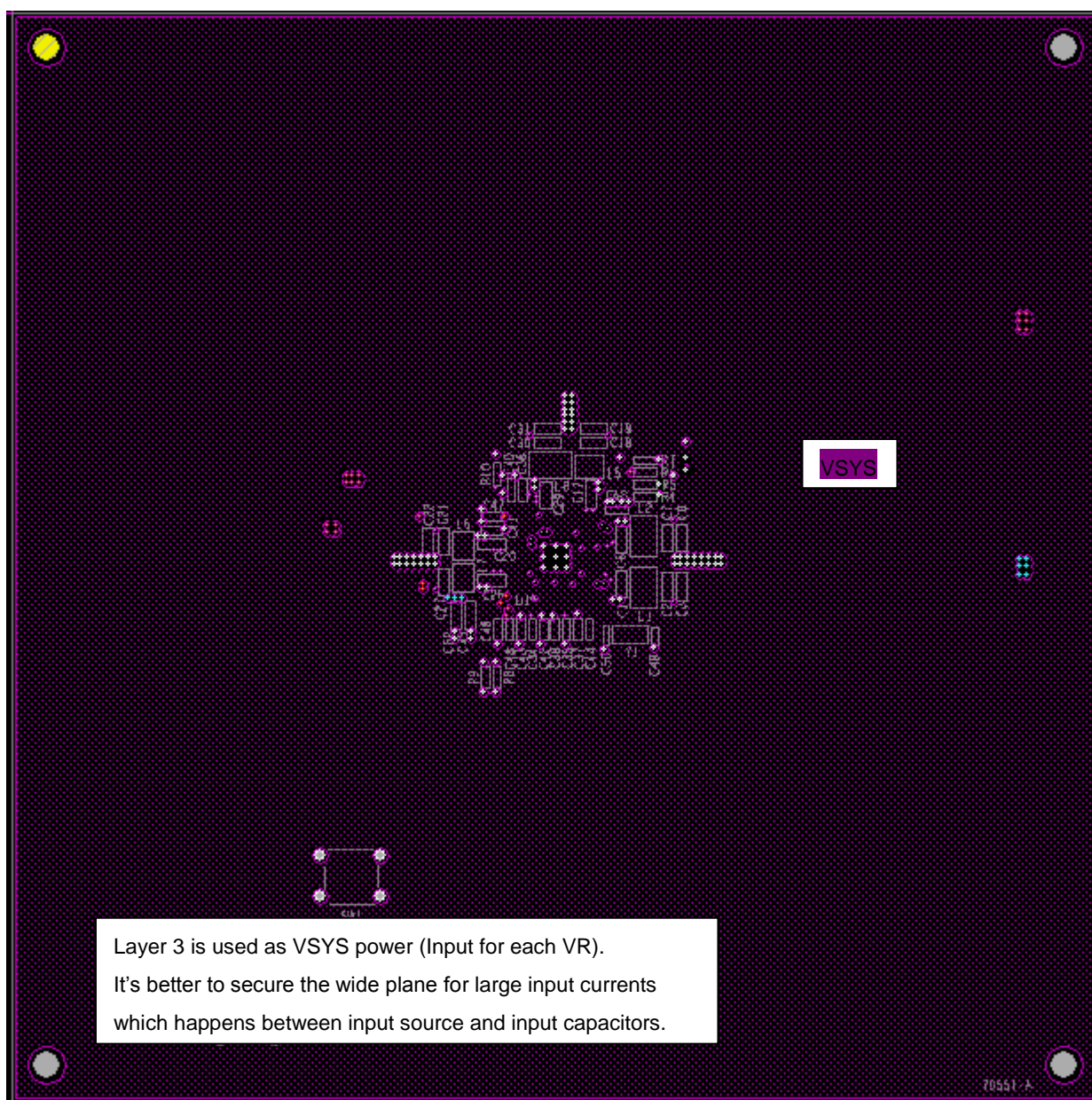


Figure 4.9 BD71847AMWV Reference Board Outline (Layer 3)



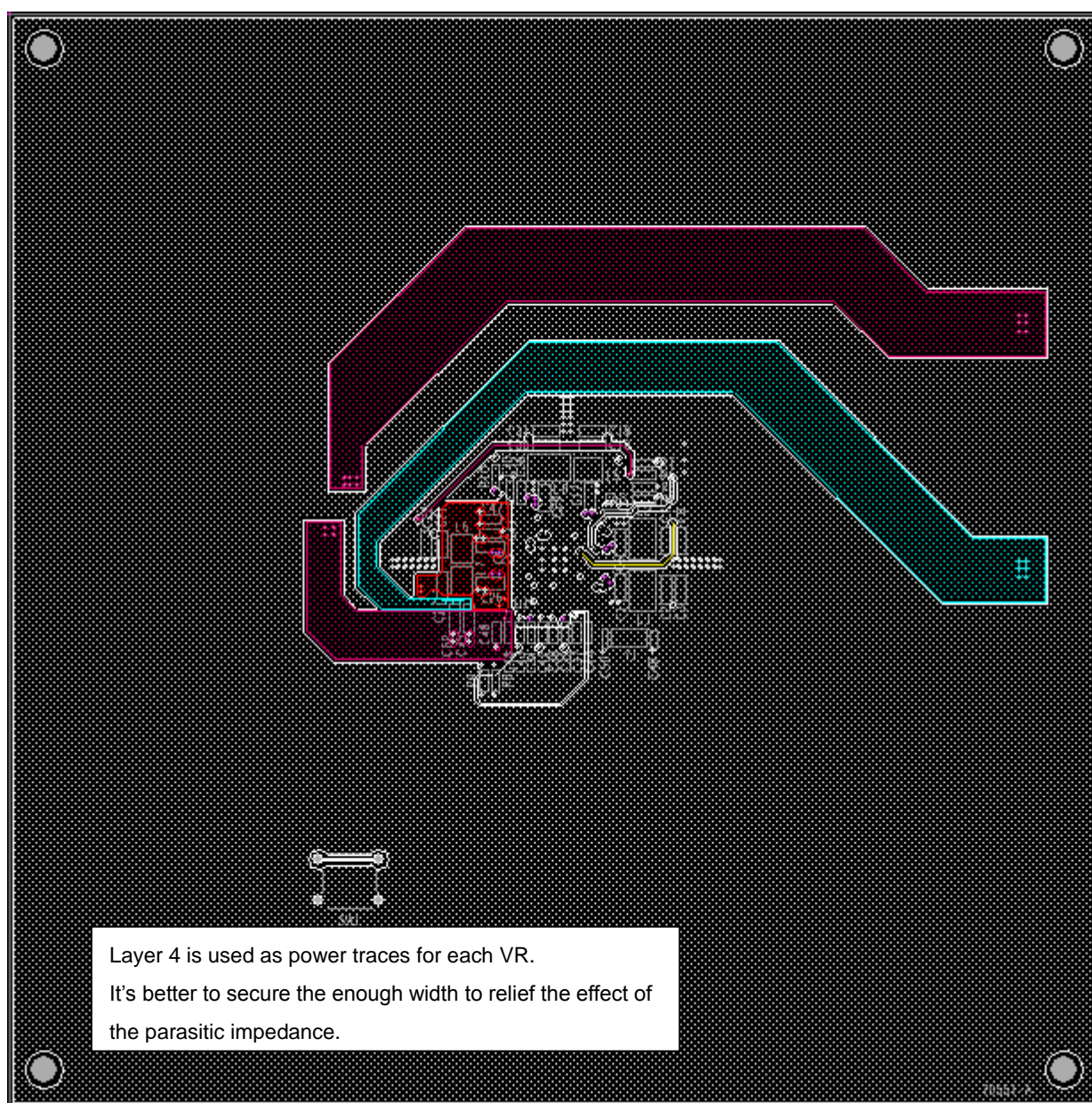


Figure 4.10 BD71847AMWV Reference Board Outline (Layer 4)



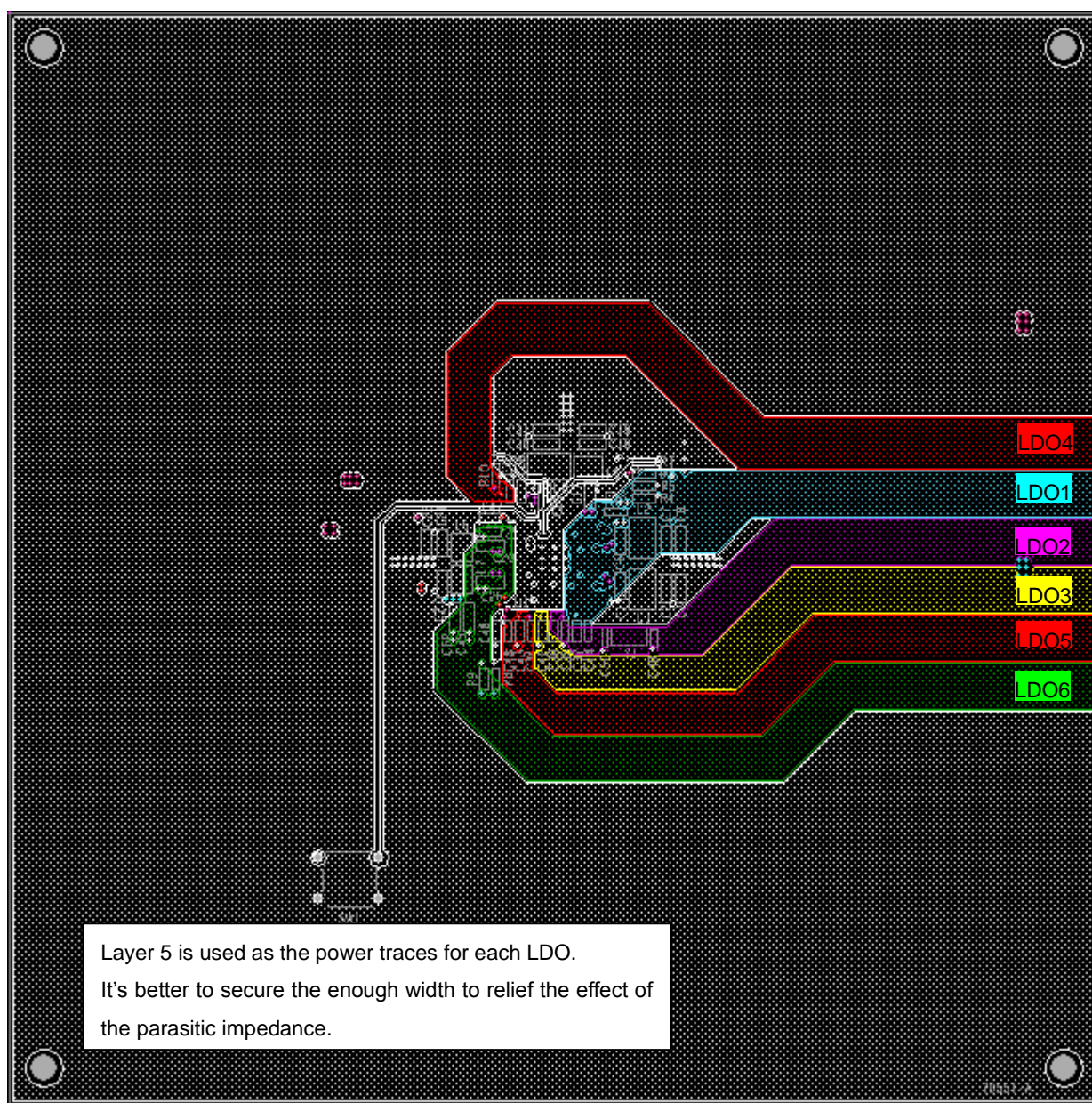


Figure 4.11 BD71847AMWV Reference Board Outline (Layer 5)

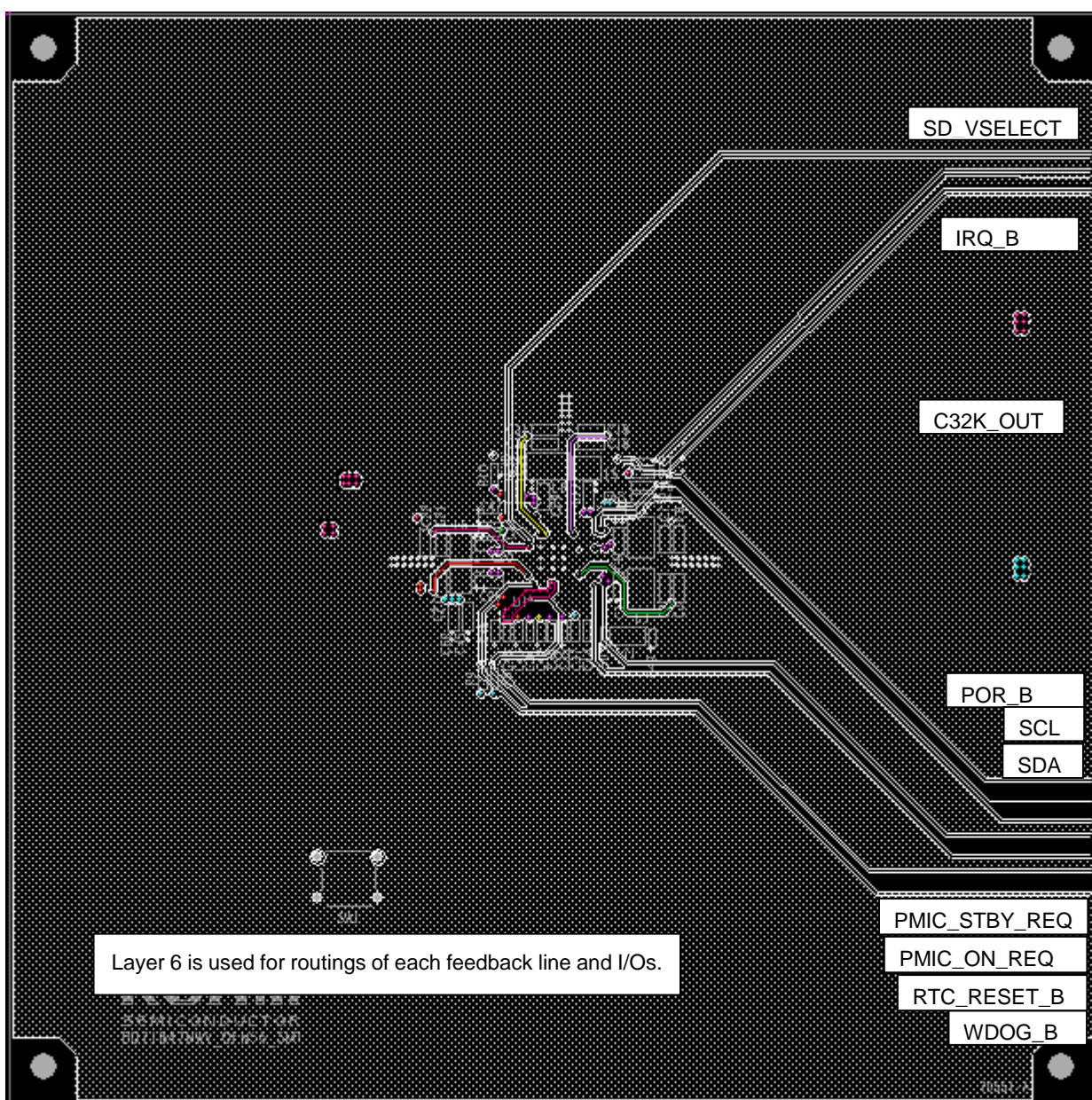


Figure 4.12 BD71847AMWV Reference Board Outline (Layer 6)

## 5. Platform Power Delivery Guidelines

BD71847AMWV is the PMIC that incorporates single BUCK regulators, LDOs, and the internal load switch. It is essential to follow the guidelines to ensure the stable power delivery to the SoC and the system.

### 5.1. Platform Power Delivery

Figure 5.1 shows the voltages BD71847AMWV provides to the SoC and other devices in the system and the information of the maximum currents for each VR are summarized in Table 5.1.

Table 5.1 The Maximum Design Powers for BUCK convertors, LDOs, and the Load Switch

Voltage Rail	Type	Input Voltage	Default Output Voltage [V]	Max Current [mA]	Over Current Protection Min [mA]
BUCK1	Buck	VSYS	0.7 – 1.3	3000	4500
BUCK2	Buck	VSYS	0.7 – 1.3	3000	4500
BUCK5	Buck	VSYS	0.7 – 1.35	3000	4500
BUCK6	Buck	VSYS	2.6 – 3.3	3000	4500
BUCK7	Buck	VSYS	1.605 – 1.995	1500	3000
BUCK8	Buck	VSYS	0.8 – 1.4	3000	4500
LDO1	LDO	VSYS	1.6 – 1.9	10	20
LDO2	LDO	VSYS	0.9 / 0.8	10	20
LDO3	LDO	BUCK6 / VSYS	1.8 – 3.3	300	390
LDO4	LDO	BUCK7 / VSYS	0.9 – 1.8	250	325
LDO5	LDO	BUCK6	1.8 – 3.3	300	340
LDO6	LDO	BUCK7	0.9 – 1.8	300	340
MUXSW	Load Switch	1.8V / 3.3V	1.8 / 3.3	150	-

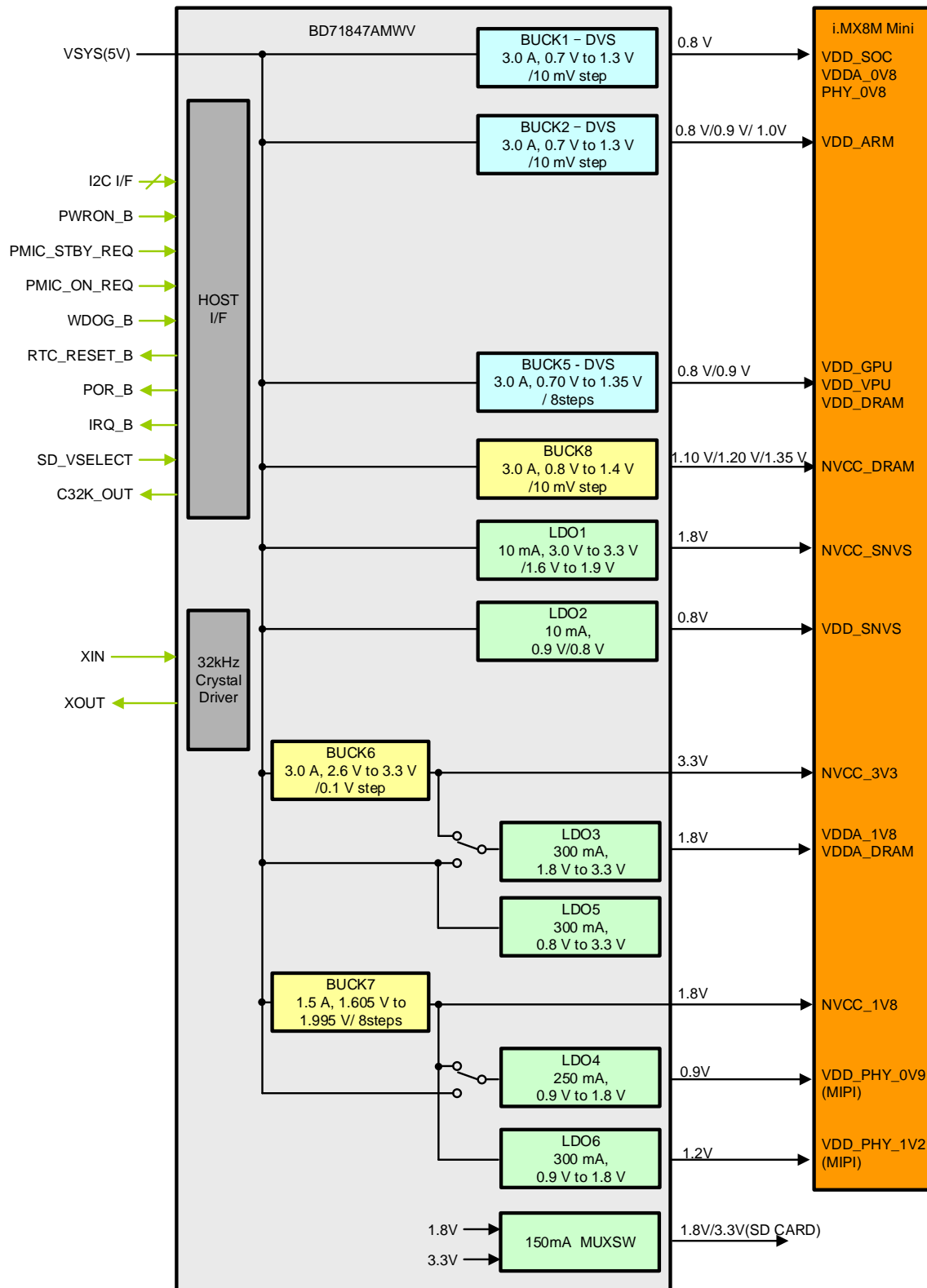


Figure 5.1 BD71847AMWV Power Delivery Map

## 5.2. General Layout Guideline

This section explains the guideline about the layout for voltage regulators. The voltage rails with higher I<sub>omax</sub> current especially for BUCK converters should be carefully designed not to transmit the unwanted interference caused by switching noises to other signals with high impedance.

And IR drop caused by large switching currents often influence the violation of the stability for the input level for each buck converter so the design for each input should be taken care. It is highly recommended to follow the all guidelines in this section.

### 5.2.1. Overall Component Placement

Figure 5.2 shows the overall parts placement. The figure shows the positions of the components needed to be put closely to PMIC. It is strongly recommended that the components controlling the higher currents like input / output capacitors and inductors are placed in priority to any other components to guarantee the stabilities of each VR.

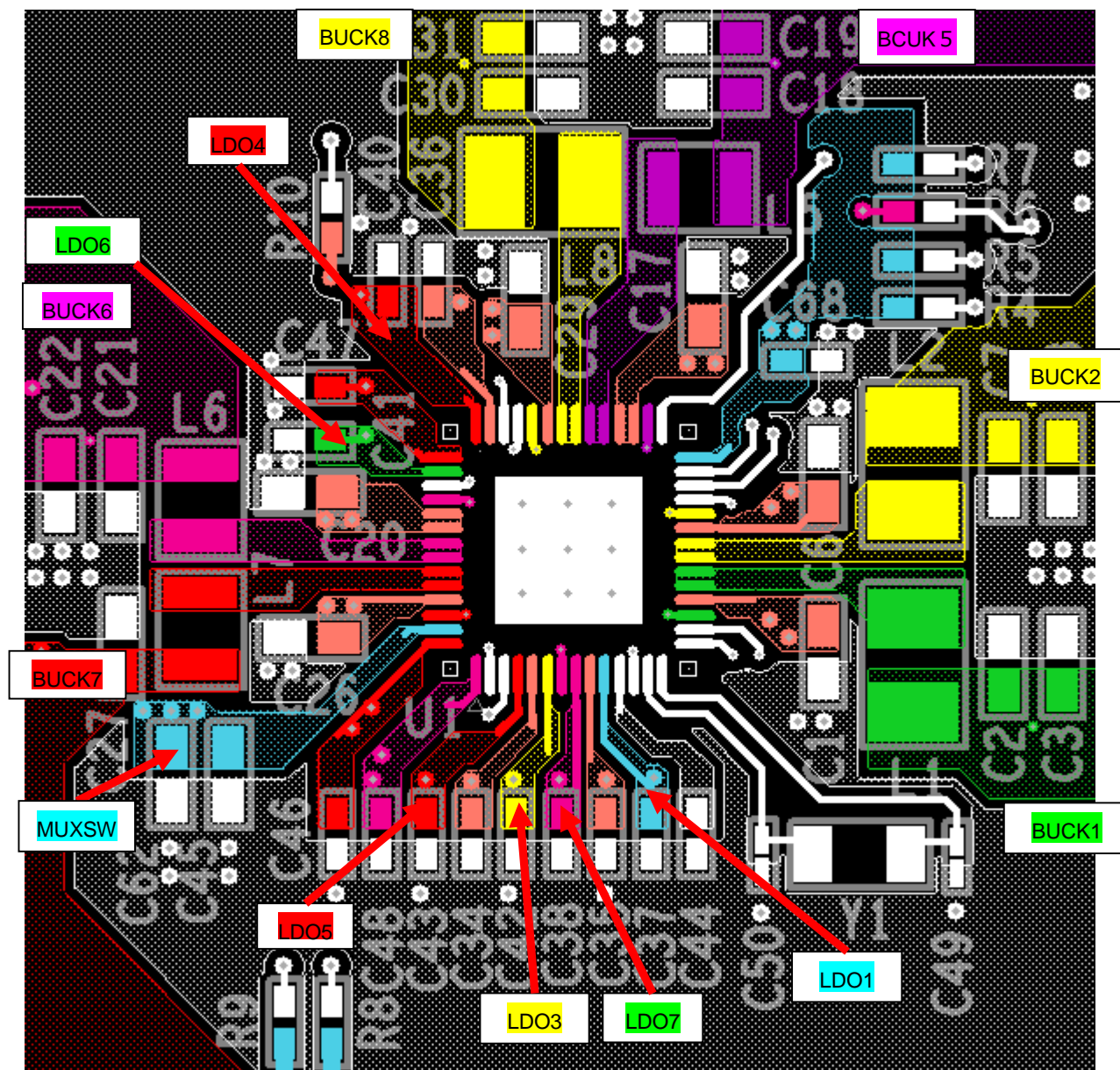


Figure 5.2 Overall component placement example



### 5.2.2. Large Current Loop

There are 2 high-pulsing current flow loops in the BUCK convertor system.

#### Loop1

When Tr2 turns ON, the loop starts from the input capacitor, to VIN terminal, to LX terminal, to L (inductor), to output capacitors, and then returns to the input capacitor through GND.

#### Loop2

When Tr1 turns ON, the loop starts from Tr1, to L (inductor), to output capacitors, and then returns to Tr1 through GND.

To reduce the noise and improve efficiency, please minimize the impedance of the each loop.

Figure 5.3 shows the current loops to be designed carefully.

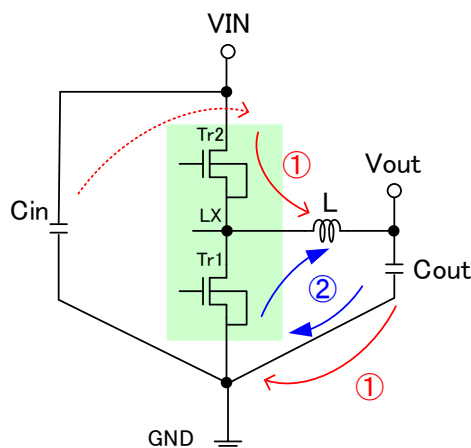


Figure 5.3 BUCK Converter Large Current Loops

As Figure 5.4 shows, the patterns which handle the heavy currents should be routed as much shortly and widely as possible to suppress the effect of the parasitic impedance coming from PCB layout, especially the node with drastic shift in current or voltage level such as VIN (input voltage) and power ground (GND). Two vias with the diameter of 300 $\mu$ m are used for input and GND for each input capacitor to make the impedance lower.

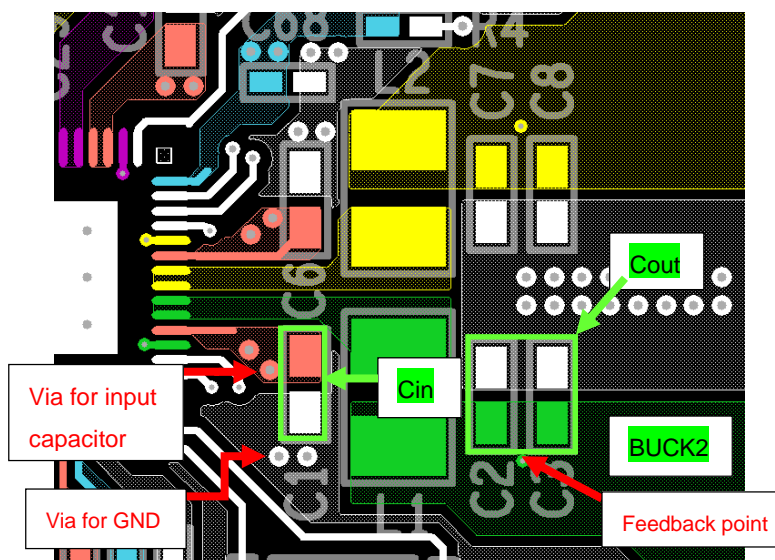


Figure 5.4 Example of parts placement and routings for BUCK2 at the top layer

### 5.2.3. Power GND

Power ground for BUCK Converters (exposed pad) is the noisy ground because of the current loops indicated in the previous section. Thus, the power ground should take an area as large as possible to keep the impedance low and reduce the swing of ground voltage level.

### 5.2.4. VSYS (Power supply for BD71847AMWV analog circuit)

BUCK X\_VIN (X is 1, 2, 3... and 8) of each VR's input should be connected to VSYS plane directly to minimize the parasitic and common impedance effects.

The enough numbers of vias for input capacitors should be used and the decoupling capacitors should be placed as close to PMIC as possible. The reference layout (BD71847AMWV reference layout) can be referred to for your reference.

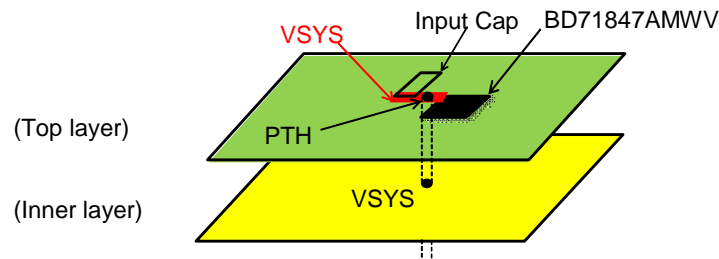


Figure 5.5 Layout for BUCK X\_VIN and VSYS

### 5.2.5. Other Signal Pattern Precautions

Make sure to leave adequate space between noisy lines of voltage rail and serial interface (I2C).

### 5.2.6. Feedback Sense Lines

Feedback sense lines (e.g., BUCK1\_FB, BUCK2\_FB etc.) should be routed to monitor the accurate output voltages for each voltage rail. In order to avoid the effects of IR drop and switching noise, please make sure that the feedback sense lines are independently routed from the point near output capacitors.

As the method for voltage sensing, "Local sensing" is recommended in all VRs.

In addition, these lines are interfered by noisy lines since these sense lines are high impedance nodes. Please don't route these sense lines by overlapping with or in parallel with noisy lines such as LX, SCL and SDA.

Drastic voltage shift in feedback lines result in unexpected voltage violations.

### 5.2.7. AGND layout

AGND is recommended not to be connected to PGND for PMIC (exposed pad) directly to avoid noise effect. It's better to short AGND to a GND at inner GND plane (stable GND) through PTH.

The reference layout as above can be referred to.

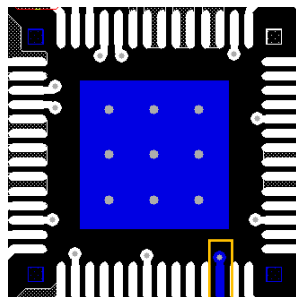


Figure 5.6 Connection between Power GND and Analog GND



### 5.3. BUCK Convertors

In this section, application circuits for each voltage rail are explained.

For more detail information, the document of “BD71847AMWV schematic check list” can be referred to.

#### 5.3.1. BUCK1 (VDD\_SOC)

BUCK1 is a high-efficiency buck converter which converts VSYS (2.7V to 5.5V) voltage to a regulated voltage.

This VR can dynamically change its output voltage setting using the I2C interface. BUCK1 output voltage range is from 0.7V to 1.3V by 10mV step.

##### 5.3.1.1. Schematic Example

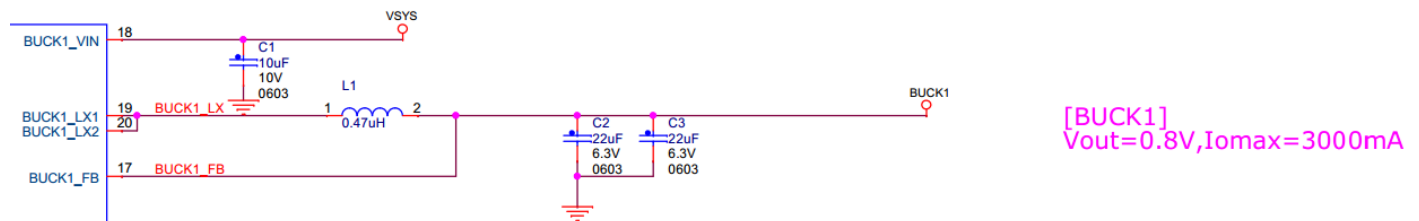


Figure 5.7 BUCK1 Schematic Example

##### 5.3.1.2. Schematic checklist

Table 5.2 BUCK1 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>Buck1 (VDD_SOC)</b>			
BUCK1_VIN[1:0]	I	<p>Connect to the 5V power supply in the system.</p> <p>As a decoupling capacitor, use <b>one 10µF</b>.</p> <p>Select the input capacitor with the capacitance <math>\geq 3.5\mu\text{F}</math> including the DC bias effect at VSYS=5.0V.</p> <p>&lt;The recommended part of capacitor is shown below.&gt;  A.LMK107BBJ106MALT, size:1608, capacitance: 10µF, tolerance:10V</p>	
BUCK1_LX[1:0]	O	<p>Connect to BUCK1 via the inductor.</p> <p>Connect <b>one 0.47µH</b> <math>\pm 20\%</math> inductors to BUCK1_LX0 and 1.</p> <p>Select the inductor to be used according to board area and cost restrictions.</p> <p>&lt;The recommended part of inductor is shown below.&gt;  A.HMLE32251E-R47MSR, size : 3225 , Rated DC Current : 7.2A  B.MEKK2016HR47M, size : 2016 , Rated DC Current : 4.7A  C.DFE252012P-R47M=P2, size : 2520 , Rated DC Current : 4A</p> <p>As output capacitors, use <b>two 22µF</b> capacitors.</p> <p>Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.</p> <p>&lt;The recommended part of 22µF capacitor is shown below.&gt;  A.GRM188R60J226MEA0D, size:1608, capacitance: 22µF, tolerance:6.3V  B.JMK107BBJ226MA, size:1608, capacitance: 22µF, tolerance: 6.3V</p>	
BUCK1_FB	I	Connect to the sense pin of BUCK1_FB to near output capacitors.	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.

### 5.3.1.3. Parts placement for each decoupling capacitor

About the parts placement for each capacitor around BUCK1, the below reference layout can be referred to.

BUCK1\_FB should be connected to near output capacitors.

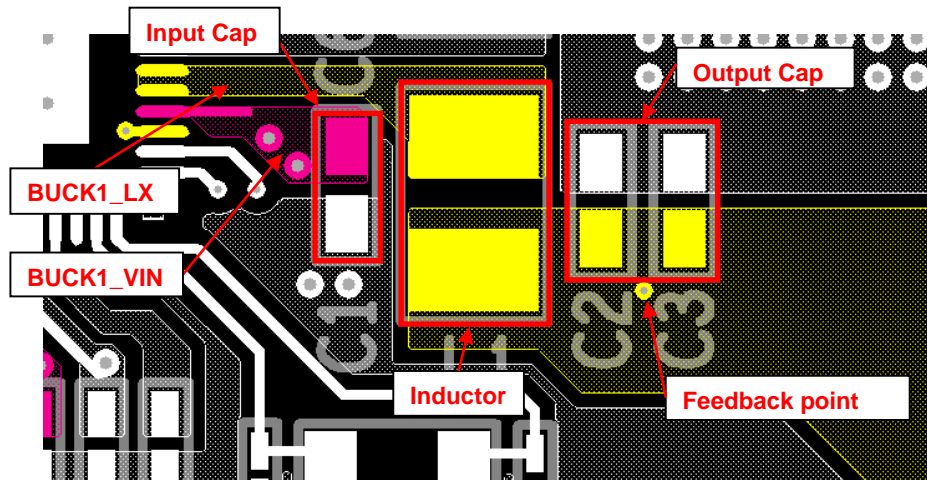


Figure 5.8 BUCK1 Layout Example (Top Layer)

### 5.3.2. BUCK2 (VDD\_ARM)

BUCK2 is a high-efficiency buck converter which converts V<sub>SY</sub>S (2.7V to 5.5V) voltage to a regulated voltage. This VR can dynamically change its output voltage setting using the I2C interface. BUCK2 output voltage range is from 0.7V to 1.3V by 10mV step.

#### 5.3.2.1. Schematic Example

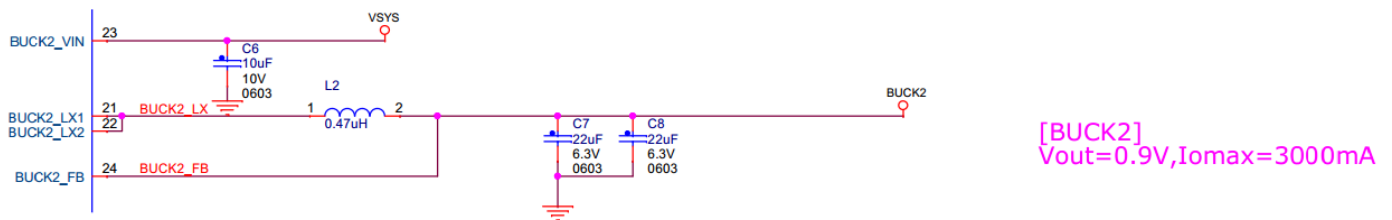


Figure 5.9 BUCK2 Schematic Example

### 5.3.2.2. Schematic checklist

Table 5.3 BUCK2 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>BUCK2 (VDD_ARM)</b>			
BUCK2_VIN[1:0]	I	Connect to the 5V power supply in the system. As a decoupling capacitor, use <b>one 10μF</b> . Select the input capacitor with the capacitance $\geq 3.5\mu\text{F}$ including the DC bias effect at VSYS=5.0V. <The recommended part of capacitor is shown below.> A.LMK107BBJ106MALT, size:1608, capacitance: 10μF, tolerance:10V	
BUCK2_LX[1:0]	O	Connect to BUCK2 via the inductor. Connect <b>one 0.47μH ±20%</b> inductors to BUCK2_LX0 and 1. Select the inductor to be used according to board area and cost restrictions. <The recommended part of inductor is shown below.> A.HMLE32251E-R47MSR, size: 3225 , Rated DC Current : 7.2A B.MEKK2016HR47M, size : 2016 , Rated DC Current : 4.7A C.DFE252012P-R47M=P2, size : 2520 , Rated DC Current : 4A As output capacitors, use <b>two 22μF</b> capacitors. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV. <The recommended part of 22μF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22μF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22μF, tolerance: 6.3V	
BUCK2_FB	I	Connect to the sense pin of BUCK2_FB to near output capacitors.	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.

### 5.3.2.3. Layout Example

About the parts placement for each capacitor around BUCK2, the below reference layout can be referred to.

BUCK2\_FB should be connected to near output capacitors.

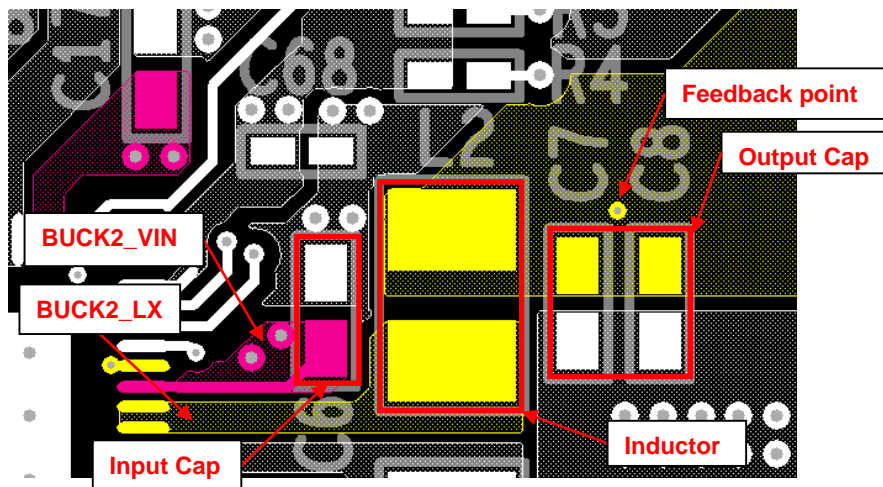


Figure 5.10 BUCK2 Layout Example (Top Layer)

### 5.3.3. BUCK5 (VDD\_DRAM)

BUCK5 is a high-efficiency buck converter which converts VSYS (2.7V to 5.5V) voltage to a regulated voltage. BUCK5 output voltage is programmable by the register and its range is from 0.7V to 1.35V.

#### 5.3.3.1. Schematic Example

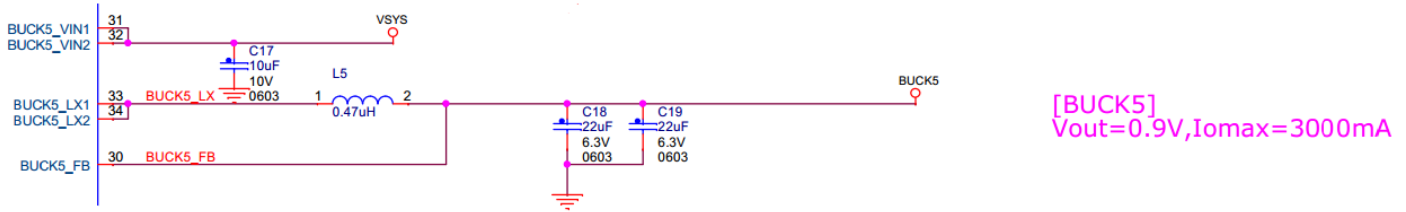


Figure 5.11 BUCK5 Schematic Example

#### 5.3.3.2. Schematic Checklist

Table 5.4 BUCK5 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
<b>BUCK5 (VDD_DRAM)</b>			
BUCK5_VIN[1:0]	I	Connect to the 5V power supply in the system. As a decoupling capacitor, use <b>one 10µF</b> . Select the input capacitor with the capacitance $\geq 3.5\mu\text{F}$ including the DC bias effect at VSYS=5.0V.  <The recommended part of capacitor is shown below.> A.LMK107BBJ106MALT, size:1608, capacitance: 10µF, tolerance:10V	
BUCK5_LX[1:0]	O	Connect to BUCK5 via the inductor. Connect <b>one 0.47µH ±20%</b> inductors to BUCK5_LX[1:0]. Select the inductor to be used according to board area and cost restrictions.  <The recommended part of inductor is shown below.> A.MEKK2016HR47M, size : 2016 , Rated DC Current : 4.7A B.DFE252012P-R47M=P2, size : 2520 , Rated DC Current : 4A	
BUCK5_FB	I	As output capacitors, use <b>two 22µF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of 22µF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22µF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22µF, tolerance: 6.3V	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.

### 5.3.3.3. Layout Example

About the parts placement for each capacitor around BUCK5, the below reference layout can be referred to. BUCK5\_FB should be connected to near output capacitors.

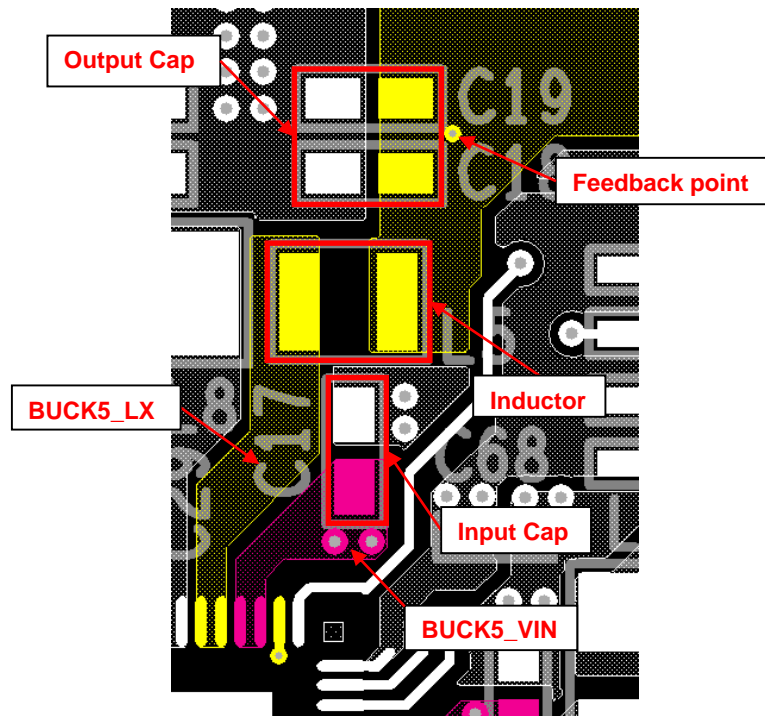


Figure 5.12 BUCK5 Layout Example (Top Layer)

### 5.3.4. BUCK6 (NVCC\_3P3)

BUCK6 is a high-efficiency buck converter which converts VSYS (2.7V to 5.5V) voltage to a regulated voltage. BUCK6 output voltage is programmable by the register and its range is from 3.0V to 3.3V by 100mV step.

#### 5.3.4.1. Schematic Example

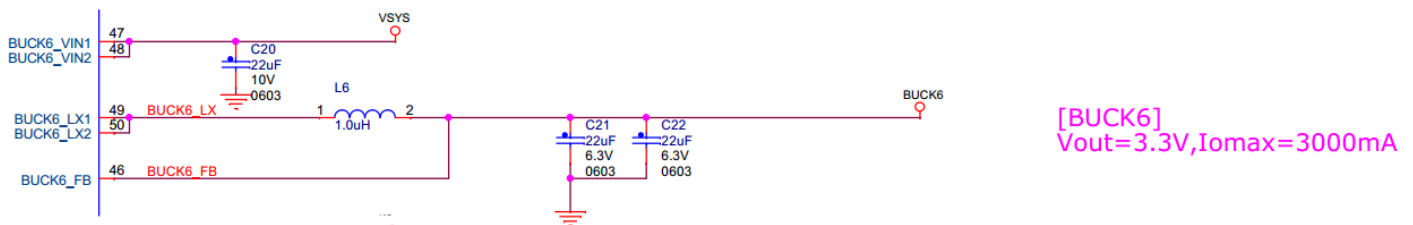


Figure 5.13 BUCK6 Schematic Example

### 5.3.4.2. Schematic Checklist

Table 5.5 BUCK6 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
<b>BUCK6 (NVCC_3P3)</b>			
BUCK6_VIN[1:0]	I	Connect to the 5V power supply in the system.	
		As a decoupling capacitor, use <b>one 22μF</b> . Select the input capacitor with the capacitance $\geq 7.7\mu\text{F}$ including the DC bias effect at $V_{\text{SYS}}=5.0\text{V}$ .	
		<The recommended part of capacitor is shown below.> A.LMK107BBJ226MA-T, size:1608, capacitance: 22μF, tolerance:10V	
BUCK6_LX[1:0]	O	Connect to BUCK6 via the inductor.	
		Connect <b>one 1.0μH ±20%</b> inductors to BUCK6_LX[1:0]. Select the inductor to be used according to board area and cost restrictions.	
		<The recommended part of inductor is shown below.> A.MEKK2016H1R0M, size: 2016 , Rated DC Current : 3.5A B.DFE252012P-1R0M=P2, size : 2520 , Rated DC Current : 3.2A	
BUCK6_FB	I	As output capacitors, use <b>two 22μF</b> capacitors. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.	
		<The recommended part of 22μF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22μF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22μF, tolerance: 6.3V	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.

### 5.3.4.3. Layout Example

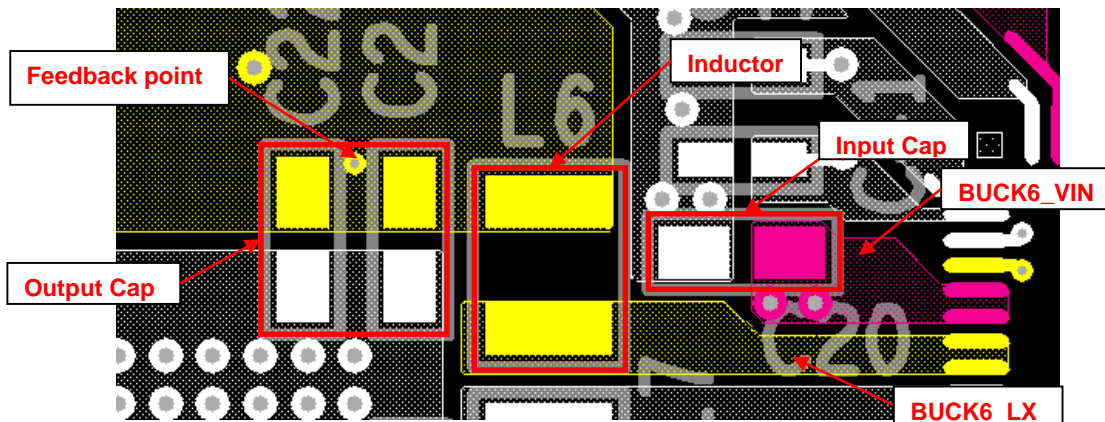


Figure 5.14 BUCK6 Layout Example (Top Layer)

### 5.3.5. BUCK7 (NVCC\_1V8)

VBUCK7 is a high-efficiency buck converter which converts VSYS (2.7V to 5.5V) voltage to a regulated voltage. BUCK7 output voltage is programmable by the register and its range is from 1.6V to 2.0V by eight steps.

#### 5.3.5.1. Schematic Example

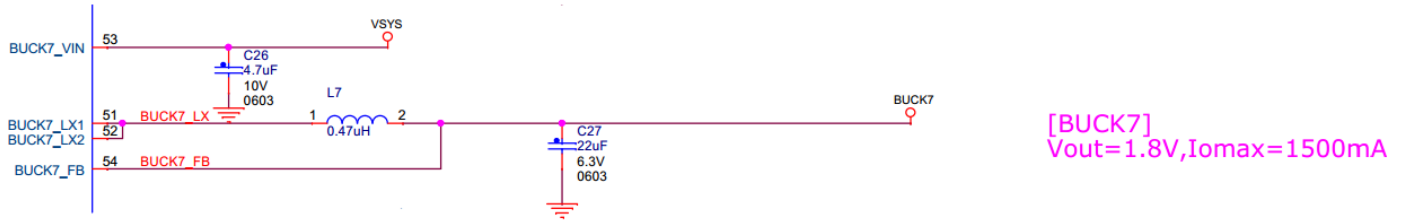


Figure 5.15 BUCK7 Schematic Example

#### 5.3.5.2. Schematic Checklist

Table 5.6 BUCK7 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
<b>BUCK7 (NVCC_1V8)</b>			
BUCK7_VIN	I	Connect to the 5V power supply in the system.	
		As a decoupling capacitor, use <b>one 4.7µF</b> . Select the input capacitor with the capacitance $\geq 1.88\mu\text{F}$ including the DC bias effect at VSYS=5.0V.  <The recommended part of capacitor is shown below.> A.LMK107BJ475MA, size:1608, capacitance: 4.7µF, tolerance:10V	
BUCK7_LX	O	Connect to BUCK7 via the inductor.	
		Connect <b>one 0.47µH</b> $\pm 20\%$ inductors to BUCK7_LX. Select the inductor to be used according to board area and cost restrictions.  <The recommended part of inductor is shown below.> A.MEKK2016HR47M, size : 2016 , Rated DC Current : 4.7A B.DFE252012P-R47M=P2, size : 2520 , Rated DC Current : 4A	
BUCK7_FB	I	As output capacitors, use <b>one 22µF</b> capacitor.	
		Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of 22µF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22µF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22µF, tolerance: 6.3V	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.



### 5.3.5.3. Layout Example

About the parts placement for each capacitor around BUCK7, the below reference layout can be referred to.

BUCK7\_FB should be connected to near output capacitors.

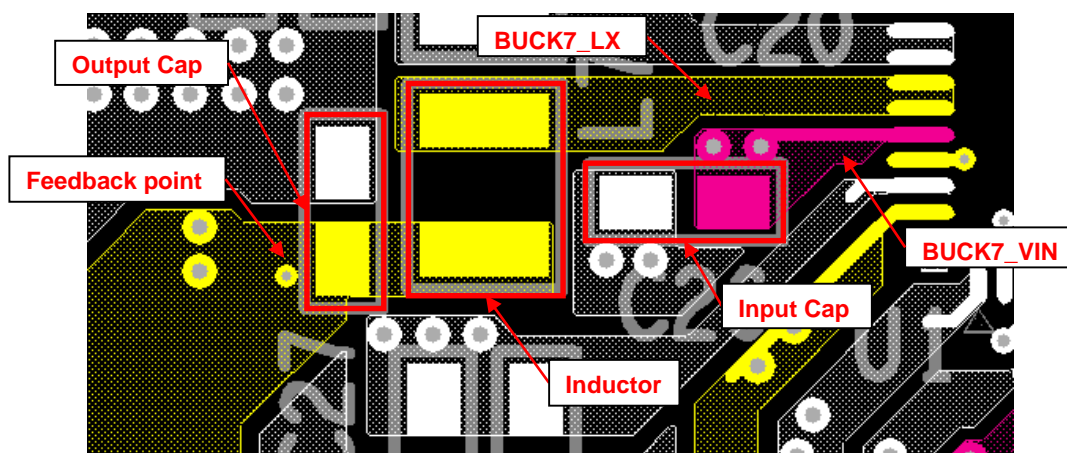


Figure 5.16 BUCK7 Layout Example (Top Layer)



### 5.3.6. BUCK8 (NVCC\_DRAM)

BUCK8 is a high-efficiency buck converter which converts VSYS (2.7V to 5.5V) voltage to a regulated voltage. BUCK8 output voltage is programmable by the register and its range is from 0.8V to 1.4V by 10mV step.

#### 5.3.6.1. Schematic Example

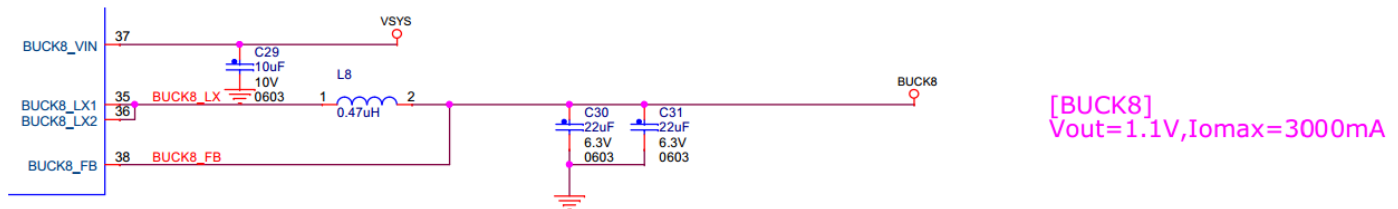


Figure 5.17 BUCK8 Schematic Example

#### 5.3.6.2. Schematic Checklist

Table 5.7 BUCK8 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
<b>BUCK8 (NVCC_DRAM)</b>			
BUCK8_VIN[1:0]	I	Connect to the 5V power supply in the system. As a decoupling capacitor, use <b>one 10μF</b> . Select the input capacitor with the capacitance $\geq 3.5\mu\text{F}$ including the DC bias effect at VSYS=5.0V.  <The recommended part of capacitor is shown below.> A.LMK107BBJ106MALT, size:1608, capacitance: 10μF, tolerance:10V	
BUCK8_LX[1:0]	O	Connect to BUCK8 via the inductor. Connect <b>one 0.47μH</b> $\pm 20\%$ inductors to BUCK8_LX0 and 1. Select the inductor to be used according to board area and cost restrictions.  <The recommended part of inductor is shown below.> A.HMLE32251E-R47MSR, size: 3225 , Rated DC Current : 7.2A B.MEKK2016HR47M, size : 2016 , Rated DC Current : 4.7A C.DFE252012P-R47M=P2, size : 2520 , Rated DC Current : 4A	
BUCK8_FB	I	As output capacitors, use <b>two 22μF</b> capacitors. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of 22μF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22μF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22μF, tolerance: 6.3V	

Note: Some dummy pads for output capacitors should be prepared like the reference schematic for the fine tuning in the actual board.

### 5.3.6.3. Layout Example

About the parts placement for each capacitor around BUCK8, the below reference layout can be referred to.

BUCK8\_FB should be connected to near output capacitors.

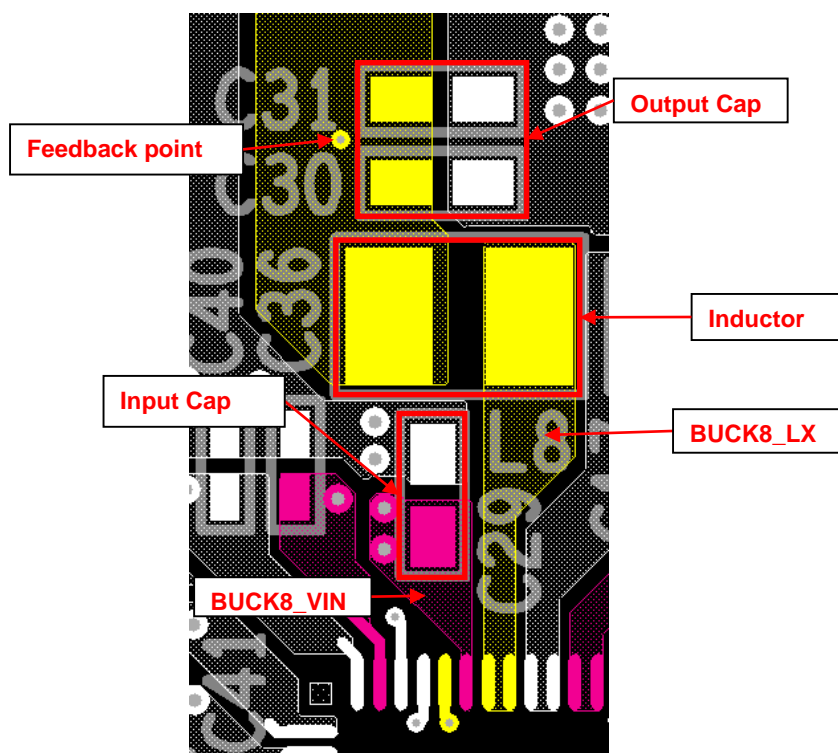


Figure 5.18 BUCK8 Layout Example (Top Layer)

## 5.4. LDOs

### 5.4.1. LDO1 (NVCC\_SNVS)

LDO1 converts V<sub>SYS</sub> (2.7V to 5.5V) voltage to a regulated voltage.

LDO1 output voltage is programmable by the register and its range is from 3.0V to 3.3V or 1.6V to 1.9V by 100mV step.

LDO1 should be used as the input for DVDD and pull up voltages for IRQ\_B, RTC\_RESET\_B, WDOG\_B and I2C interface.

### 5.4.2. LDO2 (VDD\_SNVS)

LDO2 converts V<sub>SYS</sub> (2.7V to 5.5V) voltage to a regulated voltage.

LDO2 output voltage is programmable and can be selected between 0.8V and 0.9V by the register.

### 5.4.3. LDO3 (VDDA\_1V8/VDDA\_DRAM)

LDO3 converts V<sub>SYS</sub> (2.7V to 5.5V) voltage to a regulated voltage when BUCK6 is OFF.

After BUCK6 is ON, the input source will be changed from V<sub>SYS</sub> to BUCK6 automatically.

LDO3 output voltage is programmable and its voltage range is from 1.8V to 3.3V by 100mV step.

### 5.4.4. LDO4 (VDDA\_0V9)

LDO4 converts V<sub>SYS</sub> (2.7V to 5.5V) voltage to a regulated voltage when BUCK7 is OFF.

After BUCK7 is ON, the input source will be changed from V<sub>SYS</sub> to BUCK7 automatically.

LDO4 output voltage is programmable and its voltage range is from 0.9V to 1.8V by 100mV step.

### 5.4.5. LDO5 (No use)

LDO5 converts BUCK6 voltage to the regulated voltage.

LDO5 output voltage is programmable and its voltage range is from 1.8V to 3.3V by 100mV step.

This LDO is OFF state as the default setting.

### 5.4.6. LDO6 (VDDA\_1V2)

LDO6 converts BUCK7 voltage to the regulated voltage.

LDO6 output voltage is programmable and its voltage range is from 0.9V to 1.8V by 100mV step.

### 5.4.7. Schematic Examples

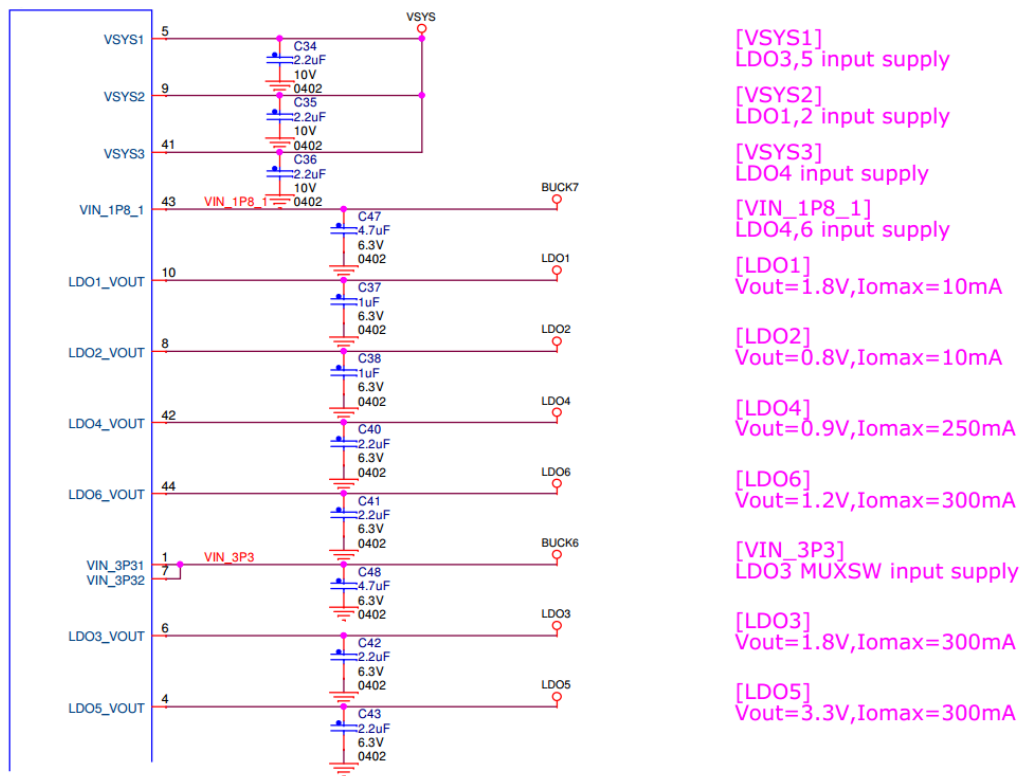


Figure 5.19 LDO1 to 6 Schematic Example

#### 5.4.7.1. Schematic Checklist

Table 5.8 LDO1-7 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>LDO1 (NVCC_SNVS) : Vout = 3.0V-3.3V / 1.6V-1.9V , Iomax=10mA</b>			
LDO1	O	As the output capacitor, use <b>one 1μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ105MV-F, size:1005, capacitance: 1.0μF, tolerance:6.3V	
<b>LDO2 (VDD_SNVS) : Vout = 0.9V / 0.8V , Iomax=10mA</b>			
LDO2	O	As the output capacitor, use <b>one 1μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ105MV-F, size:1005, capacitance: 1.0μF, tolerance:6.3V	
<b>LDO3 (VDDA_DRAM) : Vout = 1.8V - 3.3V, Iomax=300mA</b>			
LDO3	O	As the output capacitor, use <b>one 2.2μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ225MV-F, size:1005, capacitance: 2.2μF, tolerance:6.3V	

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>LDO4 (VDDA_0P9) : Vout = 0.9V - 1.8V, Iomax=250mA</b>			
LDO4	O	As the output capacitor, use <b>one 2.2μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ225MV-F, size:1005, capacitance: 2.2μF, tolerance:6.3V	
<b>LDO5 (1.8V PHY) : Vout = 1.8 - 3.3V, Iomax=300mA</b>			
LDO5	O	As the output capacitor, use <b>one 2.2μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ225MV-F, size:1005, capacitance: 2.2μF, tolerance:6.3V	
<b>LDO6 (1.2V PHY) : Vout = 0.9V - 1.8V, Iomax=300mA</b>			
LDO6	O	As the output capacitor, use <b>one 2.2μF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ225MV-F, size:1005, capacitance: 2.2μF, tolerance:6.3V	
<b>Inputs for LDOs</b>			
VSYS1	I	As the input capacitor, use <b>one 2.2μF</b> capacitor.  <The recommended part of capacitor is shown below.> A.GRM155R61A225KE95, size:1005, capacitance: 2.2μF, tolerance:10V	
VSYS2	I	As the input capacitor, use <b>one 2.2μF</b> capacitor.  <The recommended part of capacitor is shown below.> A.GRM155R61A225KE95, size:1005, capacitance: 2.2μF, tolerance:10V	
VSYS3	I	As the input capacitor, use <b>one 2.2μF</b> capacitor.  <The recommended part of capacitor is shown below.> A.GRM155R61A225KE95, size:1005, capacitance: 2.2μF, tolerance:10V	
VIN_1P8_1	I	The input for LDO4, 6 and connect to BUCK7. As the input capacitor, use <b>one 4.7μF</b> capacitor.  <The recommended part of capacitor is shown below.> A.JMK105BBJ475MV-F, size:1005, capacitance: 4.7μF, tolerance:6.3V	
VIN_3P3	I	The input for LDO3, 5, MUXSW and connect to BUCK6. As the input capacitor, use <b>one 4.7μF</b> capacitor.  <The recommended part of capacitor is shown below.> A.JMK105BBJ475MV-F, size:1005, capacitance: 4.7μF, tolerance:6.3V	

## 5.5. Load SW

### 5.5.1. MUXSW (NVCC\_SD2)

VMUXSW is the internal load switch for SD card power.

MUXSW output voltage supports 1.8V and 3.3V which are determined by the setting of SD\_VSELECT.

#### 5.5.1.1. Schematic Examples

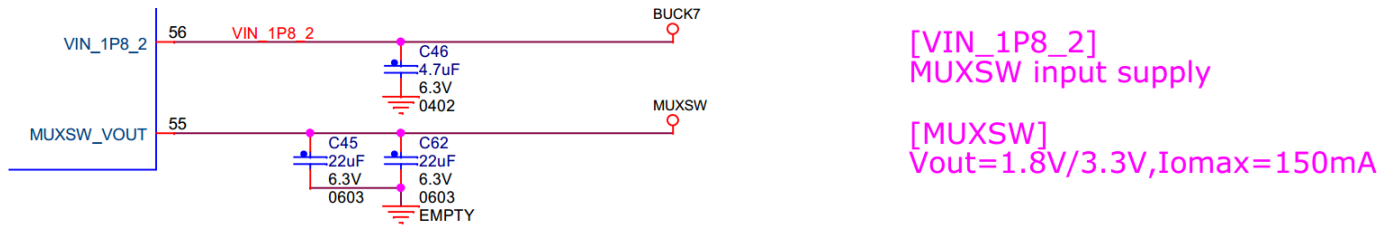


Figure 5.20 MUXSW Schematic Example

#### 5.5.1.2. Schematic Checklist

Table 5.9 MUXSW schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>MUXSW : Vout = 1.8V / 3.3V, Iomax=150mA</b>			
VIN_1P8_2	I	The input for MUXSW and connect to BUCK7. As the input capacitor, use <b>one 4.7µF</b> capacitor.  <The recommended part of capacitor is shown below.> A.JMK105BBJ475MV-F, size:1005, capacitance: 4.7µF, tolerance:6.3V	
MUXSW_VOUT[1:0]	O	As the output capacitor, use <b>one 22µF</b> capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of 22µF capacitor is shown below.> A.GRM188R60J226MEA0D, size:1608, capacitance: 22µF, tolerance:6.3V B.JMK107BBJ226MA, size:1608, capacitance: 22µF, tolerance: 6.3V	

Note: According to the setting of SD\_VSELECT by SoC, the output of MUXSW is determined.

When SD\_VSELECT = 0V, "3.3V mode" is selected and VIN\_3P3 is used as the input.

When SD\_VSELECT = DVDD, "1.8V mode" is selected and VIN\_1P8\_2 is used as the input.

## 5.6. Crystal Oscillator Driver

### 5.6.1. XIN / XOUT / C32K\_OUT

BD71847AMWV has the crystal oscillator driver for 32.768 kHz for RTC in SoC internally.

The external load capacitors of C49 and C50 shown in the Figure 5.25 are set to 18pF and this value was determined after fine tuning the specific parameters for the crystal of ST3215SB32768H5HPWAA (Load capacitance is 12.5pF) together with ROHM's evaluation board.

So it is ideal to confirm the valid capacitance value supported by the crystal supplier finely since the peripheral environment around the crystal including the crystal part number itself should be different from the condition in ROHM's evaluation.

#### 5.6.1.1. Schematic Examples

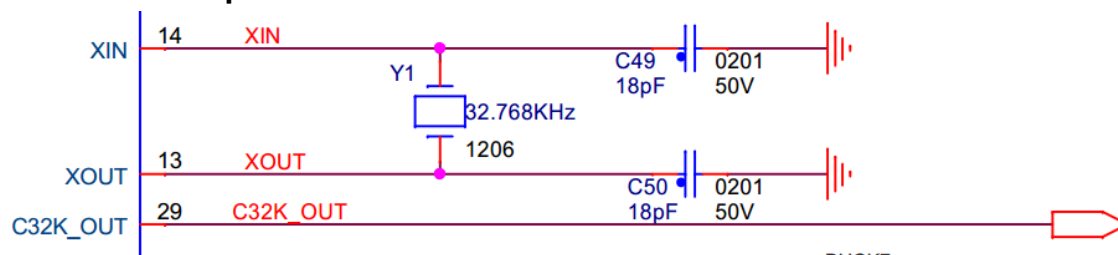


Figure 5.21 Crystal Oscillator Driver Schematic Example

#### 5.6.1.2. Schematic Checklist

Table 5.10 Schematic checklist of crystal oscillator driver

Pin Names	Dir.	Notes (Unit of parts size : mm)	Check
<b>Crystal Oscillator Driver</b>			
XIN	I	As the load capacitor, use <b>one 18pF</b> capacitor. (Refer to comment for other part.) <The recommended part of capacitor is shown below.> A.UMK063CH180JT-F, size:0603, capacitance: 18pF, tolerance:50V	
XOUT	O	As the load capacitor, use <b>one 18pF</b> capacitor. (Refer to comment for other part.) <The recommended part of capacitor is shown below.> A.UMK063CH180JT-F, size:0603, capacitance: 18pF, tolerance:50V	
C32K_OUT		Connect to SoC	

Note: As the crystal oscillator for RTC clock circuit, 32.768 kHz and 12.5pF (KYOCERA) is used together with BD71847AMWV evaluation board. 18pF is the value based on the test result for ST3215SB32768H5HPWAA in our evaluation board.

It is recommended to tune the load capacitance finely in the actual set to guarantee the stable oscillation.

<The recommended part of capacitor is shown below.>

A. ST3215SB32768H5HPWAA, size:3215, Load capacitance: 12.5pF

B. WMRAG32K76CS1C00R0, size:0906, capacitance: 8pF

For B part, load capacitance for XIN and XOUT is **3pF** after matching test in our evaluation board.

### 5.6.1.3. Layout Example

Crystal oscillator driver circuit is extremely sensitive to external environment like parasitic capacitance due to the long wirings for XIN and XOUT. So it is recommended to position the Crystal oscillator part near PMIC to shorten the length of the wirings.

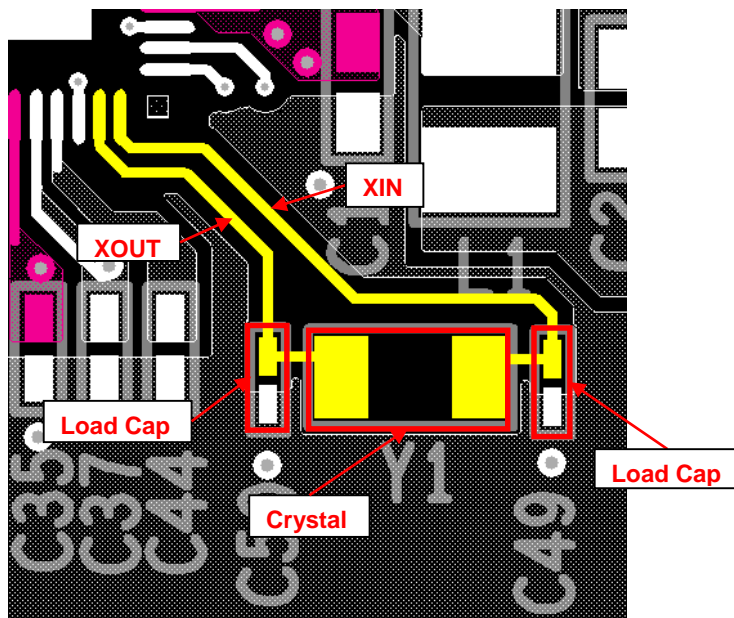


Figure 5.22 XIN / XOUT Layout Example (Top Layer)



## 5.7. Interfaces

I2C interface is selected for the communication between PMIC and SoC.

### 5.7.1. I2C

Table 5.11 Schematic checklist of I2C

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
<b>I2C</b>						
DVDD	I	-	-	-	The input power source for C32K_OUT and I2C interface. Capacitor for decoupling, use <b>one 1.0μF ± 20%</b> (size : 1005, capacitance : 1.0μF, tolerance : 6.3V)	
SCL	I	DVDD	Pulled up to DVDD with 1kohm	-	Connect to SoC (Note) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	
SDA	I/O	DVDD	Pulled up to DVDD with 1kohm	-	Connect to SoC (Note) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	

Note: Recommended to use LDO1 (NVCC\_SNVS) as power source for DVDD.

If DVDD is not used as the pull up voltage for SCL and SDA, it's recommended to use NVCC\_I2C in SoC as the pull up voltage.

## 5.7.2. System Control – Reset, Power, and Control Signals

Table 5.12 Schematic checklist of System Control – Reset, Power, and Control Signals

Pin Names	Dir.	Expected Signal Voltage Level	Expected System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
<b>System Control - Reset, Power, and Control Signals</b>						
PWRON_B	I	VSYS	Pulled up to VSYS or LDO1 (NVCC_SNVs_1V8) with 100kohm	Pulled up to VSYS or LDO1 (NVCC_SNVs_1V8) with 100kohm	Connect to Power Button LDO1 (NVCC_SNVs_1V8) can be used as a pull up source when OTP is the default setting.	
POR_B	O	BUCK7 Refer to Notes	Pulled up to BUCK7 with 10kohm	NC	Connect to SoC (Note1) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	
IRQ_B	O	DVDD Refer to Notes	Pulled up to DVDD with 10kohm	NC	Connect to SoC (Note2) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	
RTC_RESET_B	O	DVDD Refer to Notes	Pulled up to DVDD with 10kohm	NC	Connect to SoC (Note3) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	
PMIC_STBY_REQ	I	DVDD Refer to Notes	-	-	Connect to SoC (Note4)	
PMIC_ON_REQ	I	DVDD Refer to Notes	-	-	Connect to SoC (Note4)	
WDOG_B	I	DVDD Refer to Notes	Pulled up to DVDD with 10kohm	Pulled up to DVDD with 10kohm	Connect to SoC (Note2) If pull up resistor is prepared within SoC, the additional pull up resistor is not needed.	
SD_VSELECT	I	DVDD Refer to Notes	-	GND	Connect to SoC (Note5)	

Note1: The source for pull up should be BUCK7 to avoid a leakage current. POR\_B keeps L level until PMIC\_ON\_REQ is issued by SoC and POR\_B is de-asserted during the power sequence.

Note2: If the power source for NVCC\_GPIO1 in SoC is different from the voltage of DVDD in PMIC, the pull up voltage is set to NVCC\_GPIO1.

Note3: If DVDD is different from the voltage of NVCC\_SNVs in SoC, the pull up voltage is set to NVCC\_SNVs.

Note4: This signal comes from SoC so the signal voltage level depends on the power source for NVCC\_SNVs.

Note5: The voltage level depends on the power source for NVCC\_GPIO1 which is the power source for GPIO in SoC.

### 5.7.3. MISC

Table 5.13 Schematic checklist of MISC

Pin Names	Dir.	Signal Voltage Level	Notes	Check
<b>MISC</b>				
INTLDO1P5	O	INTLDO1P5	As the output capacitor, use one 1.0 $\mu$ F capacitor. Select the output capacitors within the capacitance range defined in the datasheet of BD71847AMWV.  <The recommended part of capacitor is shown below.> A.JMK105BJ105MV-F, size:1005, capacitance: 1.0 $\mu$ F, tolerance:6.3V	
AGND	-	GND	Connect to PGND at inner GND plane	
EXP-PADs (PGND0~4)	-	GND	Connect to the inner GND plane with lower impedance or solder to the land pattern on the board.	

Note: The package has one pad at bottom and four corner pads to fix the position of the part.

These pads are shorted internally and it is recommended to solder these pads to the board.

## 6. Reference Board Layout For Limited Application Area

For the products with the limitation of the application area, parts need to be mounted at top and bottom layers.

In such situation, power GND and input layout should be kindly taken care.

As the reference data, ROHM provides "BD71847AMWV\_Reference\_Layout\_Both\_Surface\_Rev1p0.brd".

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