transphorm

Application Note 0009

Recommended External Circuitry for Transphorm GaN FETs

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Part I: Introduction

Transphorm GaN FETs provide significant advantages over silicon (Si) superjunction MOSFETs by offering lower gate charge (Qg), faster switching speeds, and lower body-diode reverse recovery charge (Qrr). GaN FETs exhibit in-circuit switching speeds much higher than that of the current Si technologies. The inherent rapid switching of GaN devices reduces current/voltage cross-over power losses, enabling high frequency operation while simultaneously achieving high efficiency.

However, the accompanying high di/dt transient during switching, combined with parasitic inductances, generates noise voltages in the circuit. This noise can interfere with the gate and the driver of the device, and, in the worst case, creates sustained oscillation that must be prevented for safe operation of the circuit. This application note provides guidance on how to eliminate oscillation and how to achieve high switching current with a controlled di/dt.

Part II: Solutions to Suppress Oscillation

To avoid sustained oscillation, it is important to minimize noise generation, to minimize noise feedback, and to damp the ringing energy resulting from the high current/voltage transients. This can be achieved with the recommendations outlined below using a half-bridge switching circuit in Figure 1 as an example.

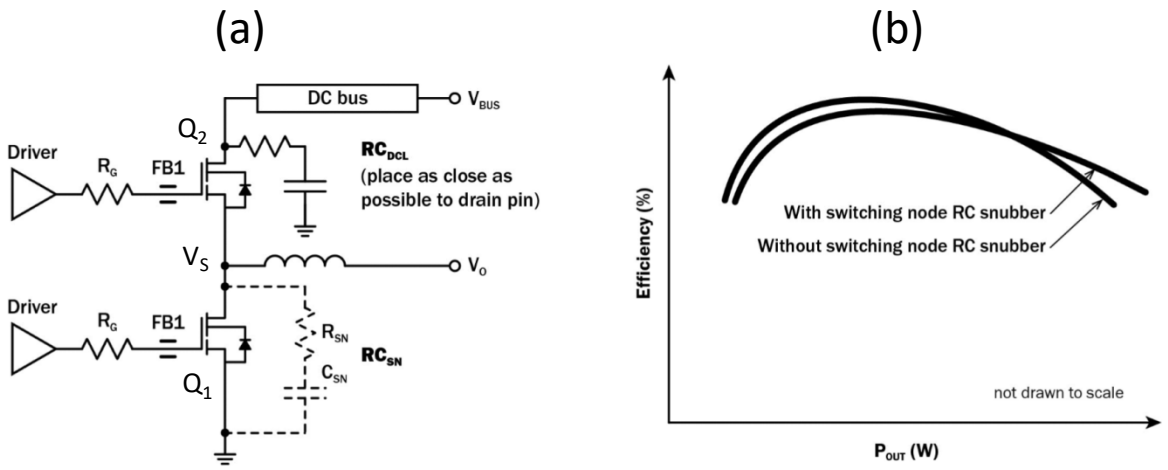


Figure 1. a) Half-bridge switching circuit and b) Efficiency vs. output power

1) Optimize the PCB layout to minimize external parasitic inductances and associated feedback. Use a large area ground plane for an overall low-noise base potential. Arrange the gate drive circuit on one side and the output circuit on the other side to minimize noise feedback from the output loop to the input loop. Place the driver circuit close to the gate of the device. Shorten the power loop by arranging the high-side and low-side devices close-by.

2) Use a gate ferrite bead [FB1 in **Figure 1(a)**] to prevent the high-frequency noise from entering the driver and logic circuits. This bead should be mounted close to the Gate lead of the device. NOTE: This is required even for single-ended non-half-bridge designs. The specification of the recommended gate ferrite beads are listed in Transphorm's GaN FET datasheets and also summarized in **Table 2**. The TO247 package includes a built-in gate ferrite bead for our Gen III devices but has been moved to the outside for our latest Gen IV (G4) devices. Please refer to page three of the datasheet to verify its position.

3) Use a DC-link RC snubber [RC_{DCL} in Figure 1(a)]. The DC rail or DC-link, when decoupled with a low-ESR fast capacitor, can be considered a high-Q C-L network at high frequencies (with "L" being the feed inductance of the DC bus). This can interact with the devices at voltage/current transients and lead to ringing. Adding an RC snubber across the DC-link close to the drain pin of the high-side device can effectively absorb the ringing energy, suppressing potential oscillation. This effect is shown in **Figure 2** where the high-frequency ringing at 25A turn-off is substantially damped with the RC_{DCL}. Since this snubber is not inserted at the switching node, it does not add switching loss to the circuit. NOTE: This is recommended even for single-ended non-half-bridge designs. *The practical values of the RC_{DCL} can be 2 sets of 6-10Ω/0.5W SMD resistors in series with a 10nF/600-1000V ceramic SMD cap, or 1 set of 3-4Ω/1W resistors in series with a 10-20nF/600-1000V cap if space is limited.*

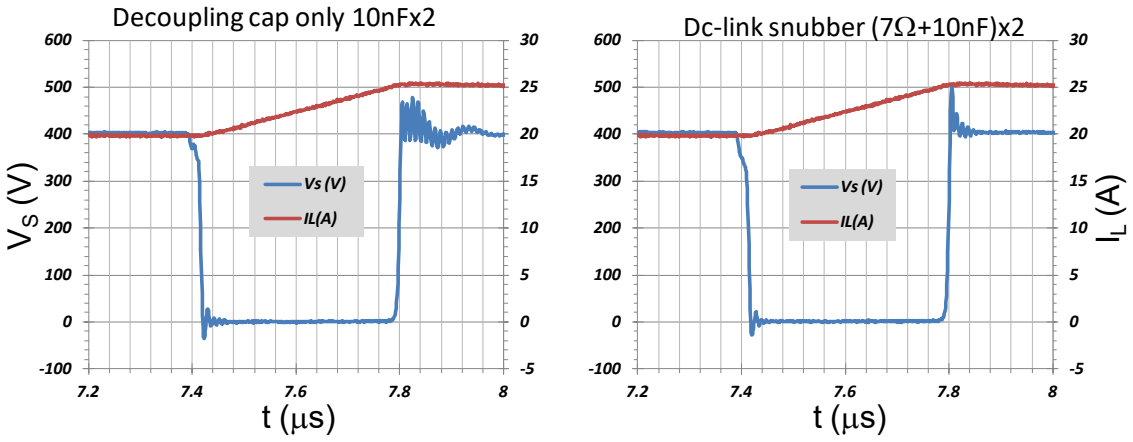


Figure 2. Half-bridge inductive switching waveforms with decoupling capacitor only and with DC-link snubber (RC_{DCL}) (Devices: TP65H050WS)

4) Adding a switching-node RC snubber [RC_{SN} in **Figure 1(a)**] can further reduce high-frequency ringing and help control di/dt transients at high operation currents. The effect of the RC_{SN} on switching waveform at a switching current >50A is shown in **Figure 3**. Unlike the RC_{DCL}, the capacitance of the RC_{SN} does increase switching loss. The recommended snubber parameters with little degradation in efficiency are given in the datasheet and are summarized in **Table 2**.

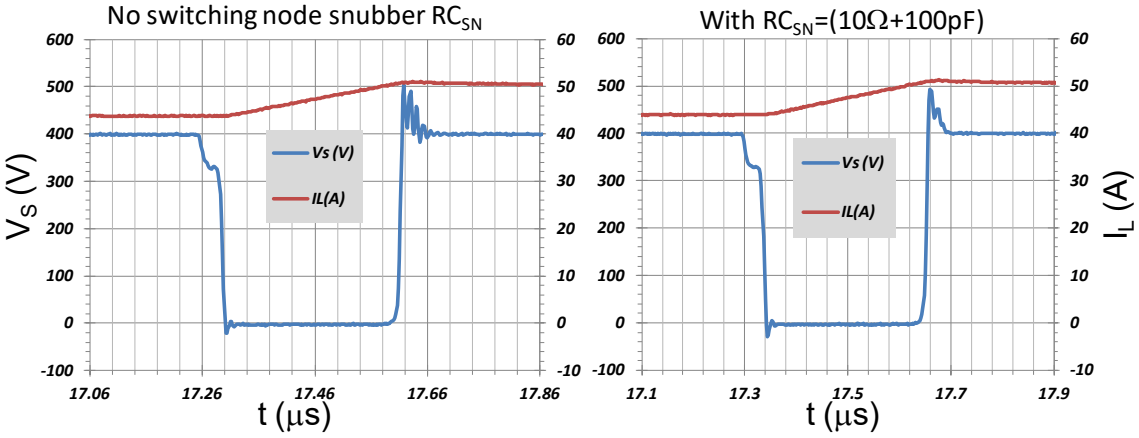


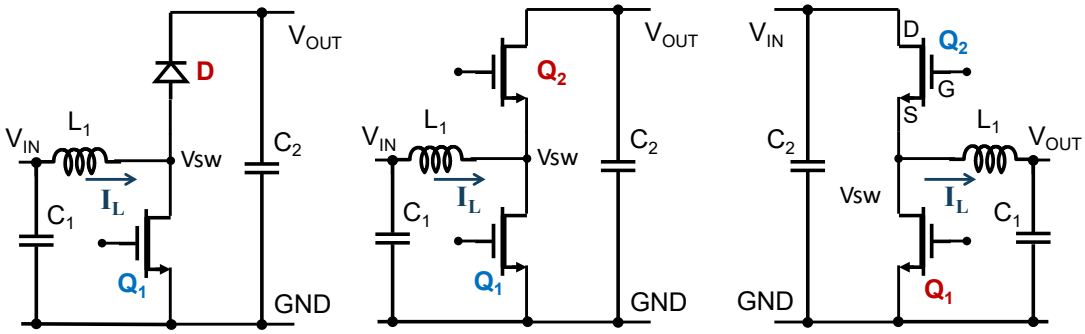
Figure 3. Effect of switching node snubber RC_{SN} on half-bridge inductive switching waveforms (Devices: TP65H035WS).

Part III: The di/dt Limits of GaN Switching Devices & Solutions for High-current Operation

Transphorm GaN FETs are designed for the highest robustness and reliability within the technology boundaries today. These devices can operate to their full voltage rating and at extremely high di/dt levels in normal operation mode (forward conduction when current enters the Drain). However, when used as a free-wheeling device in reverse conduction mode (current enters the Source when the Gate is off), there are di/dt limits beyond which the performance can be negatively affected. Although these reverse conduction di/dt limits in the range of 1200~3800 A/μs (depending on device & stress duration) are much greater than that of typical superjunction devices at ~60A/us, care must be taken for best performance at high current levels since the di/dt value is a strong function of switching current.

It is important to note that this di/dt limit only applies to the device acting as a free-wheeling diode (FWD) and only applies to the duration when the FWD transitions from blocking voltage to reverse conducting current. Three cases are illustrated in **Figure 4**; the affected devices are the ones functioning as an FWD during dead-time when the inductor current commutates from the main switch to the reverse current of the FWD.

1) A boost converter that uses an SiC diode as the rectifier device – Not affected.
2) A synchronous boost that uses a GaN FET as the FWD –Q_2 affected.
3) A synchronous buck that uses a GaN FET as the FWD – Q_1 affected.



1) Boost converter
Q_1 di/dt limit: No

2) Boost converter
Q_1 di/dt limit: No
Q_2 di/dt limit: Yes

3) Buck converter
Q_1 di/dt limit: Yes
Q_2 di/dt limit: No

Figure 4. Identifying the device affected by the di/dt limit in three popular circuits: (1) boost converter, (2) synchronous boost converter, and (3) buck converter.

The maximum di/dt stress happens when the main switch [Q_1 in **Figure 4** (2) or Q_2 in **Figure 4** (3)] turns off and the inductor current redirects to the FWD instantly. The higher the turn-off current, the higher the reverse conduction di/dt. The reverse conduction di/dt limits and associated maximum (turn-off) switching current values are listed in the datasheet. The example for TP65H035WS is shown in **Table 1**. The $(di/dt)_{RDMC}$ and I_{RDMC1} values are for constant repetitive switching operation such as in a DC to DC converter, while I_{RDMC2} applies to DC to AC or AC to DC conversion circuits when the peak current switching is much lower than the average switching current. The $(di/dt)_{RDMT}$ and I_{RDMC} values are for transient and continuous transient conditions respectively such as in the event of power-line-disturbance (PLD) in a PFC (when one AC input cycle is missing, which forces the circuit to operate at a much higher current in the next cycle to make up for the energy loss).

Symbol	Parameter	Min	Typ	Max	Unit
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [b]	–	–	1800	A/µs
I_{RDMC1}	Reverse diode switching current, repetitive (dc) [c, e]	–	–	28	A
I_{RDMC2}	Reverse diode switching current, repetitive (ac) [c, e]	–	–	35	A
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]	–	–	3800	A/µs
I_{RDMT}	Reverse diode switching current, transient [d,e]	–	–	45	A

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Continuous switching operation
c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
d. ≤300 pulses per second for a total duration ≤20 minutes
e. I_{RDM} values can be increased by increasing R_G and C_{SN} on page 3

Table 1. TP65H035WS reverse diode conduction di/dt limits and associated max switching current when using the recommended R_G and RC_{SN}.

Note that the reverse diode switching current limits were obtained with the recommended circuit parameters [**Figure 1(a)** and **Table 2**]. The gate resistor R_G is important to control the di/dt and the addition of a switching node snubber RC_{SN} offers further improvements when operation current is high. The effect of RC_{SN} is shown in **Figure 1(b)**: a slight reduction in low-load efficiency, but a significant enhancement at high load. In applications with operation current below 70 percent of the maximum rating or when an Rg is equal to or higher than the recommended value, the RC_{SN} can be omitted. On the other hand, one can further increase the R_G value if the operation current is higher than the maximum I_{RDM}'s in the datasheet. In all situations, care has to be taken to ensure junction temperature of the devices do not exceeding maximum rating.

Part IV: Additional Design Notes

1) Circuit and Layout Recommendations

- As GaN FETs switch extremely fast, we recommend using a driver(s) with sufficient Common Mode Transient Immunity (CMTI) so as not to cause disruption between the secondary and primary side of isolated drivers when in operation.
- When using the GaN FETs in a half bridge configuration, we recommend using an integrated half bridge gate driver(s) that offers overlap protection to prevent outputs VOA and VOB from being high at the same time, such as the Skyworks Si823x series.
- Place the RC_{DCL} as close as possible to the drain pin of the high-side GaN FET and ground it to the large ground plane.
- SMD mounting is recommended for all snubber components.
- A Gate resistor (R_G) is required for all devices.
- Gate ferrite beads (FB1) are only required for TO-220 and PQFN devices; depending on the generation TO-247 devices have built-in ferrite beads (Gen III) where Gen IV (datasheet "G4" designation) use an external ferrite bead. Always review page three of datasheets to get the latest design recommendations.
- If the device is being driven at >70 percent of the rated I_{RDM} values or a smaller than recommended gate resistor is used, then a switching node RC snubber (RC_{SN}) is recommended in addition to the required DC-link RC snubber (RC_{DCL}).

- The gate ferrite bead and gate resistor prevent oscillation and reduce excessive di/dt when the GaN device is used in a half-bridge topology.
- The RC_{DCL} reduces the voltage ringing due to device interaction with the bypass network.
- The RC_{SN} slightly reduces light and medium load efficiency with the benefit of increased output power.
- The RC_{SN} implementation in a half-bridge has the advantage of allowing a higher peak turn-off switching current due to the reduction of the di/dt seen by the freewheeling device as the main conducting device turns off.

2) Required and Recommended External Components for Single Gate Resistor Designs

Device Gate Drive Recommendations for Half Bridge Topologies								
Specifications	GaN FET Devices							
	TP65H015G5WS	TP65H035G4WS/QS	TP65H035WS	TP65H050G4WS/BS/QS	TP65H050WS	TP65H070LDG/LSG	TP65H150G4LSG	TP65H300G4LSG
	TO-247	TO-247/TOLL	TO-247	TO-247/TO-263/TOLL	TO-247	PQFN	PQFN	PQFN
Gate Voltage Drive	0V, 12 V	0V, 12 V	0V, 12V	0V, 12V	0V, 12V	0V, 12V	0V, 12V	0V, 12V
Recommended Gate Resistor (R_G)	15Ω	30Ω	30Ω	45Ω	45Ω	50-70Ω	60-70Ω	30-60Ω
Recommended Gate Resistor (R_G) for 2x to 2.5x Irms Topology: AC to DC or DC to AC		47Ω @ 45Apk	47Ω @ 45Apk	47Ω @ 33Apk	47Ω @ 33Apk	TBD	TBD	TBD
DC Link Snubber (RC_{DCL})	[10pF, 3.3Ω] x 3	[4.7nF, 5Ω] x 2	[10nF, 8Ω] x 2	[4.7nF, 8Ω] x 2	[10nF, 8Ω] x 2	[10nF, 10Ω] x 2	[4.7 - 10nF, 5Ω]	[4.7 - 10nF, 5Ω]
Ferrite Bead Gate (FB1) @ 100 MHz	80-120Ω	200-270Ω	Internal	200-300Ω	Internal	240Ω	240Ω	240Ω
Recommended RC_{SN}	[100pF, 10Ω] x 3	[100pF, 10Ω]	[200pF, 5Ω]	[200pF, 5Ω]	[100pF, 10Ω]	[68pF, 15Ω]	[22pF, 15Ω]	[22pF, 15Ω]
Datasheet Specification di/dt Maximums								
Specifications	GaN FET Devices							
	TP65H015G5WS	TP65H035G4WS	TP65H035WS	TP65H050G4WS/BS	TP65H050WS	TP65H070LDG/LSG	TP65H150G4LSG	TP65H300G4LSG
	TO-247	TO-247	TO-247	TO-247/TO-263	TO-247	PQFN	PQFN	PQFN
Reverse diode max (di/dt), repetitive (A/µs) -di/dt_{RDMC}	3500	3200	1800	2500	1600	1200	1200	1200
Reverse diode max swiching current, dc-dc repetative (A) - I_{RDMC1}	--	--	28	--	24	18	--	--
Reverse diode max swiching current, ac repetative (A) - I_{RDMC2}	--	--	35	--	28	23	--	--
Reverse diode max (di/dt), transient (A/µs) - di/dt_{RDMT}	--	--	3800	--	3000	2600	--	--
Reverse diode max swiching current, transient (A) - I_{RDMT}	--	--	45	--	36	28	--	--
When -3V ~ -5V turn-off is used, Rg can increase by 1.5x to 1.8x.								

Table 2. Recommended components for half-bridge circuit in Figure 1(a).

3) To Verify GaN FET Stable Operation

To verify adequate operational margin without oscillation, as a minimum observe the V_{DS} waveforms at the turn-on and turn-off switching edges at the application's maximum drain current. This may occur during start-up or at the application's maximum load step. A double-pulse or multi-pulse test is highly recommended utilizing the actual layout, with current levels at or greater than 120 percent of the application's anticipated peak current. Verify that the ringing on the V_{DS} waveform at the transition edges is adequately damped. See design guide DG004: Multi-pulse Testing for GaN Layout Verification.

4) Recommended Driving Gate Resistance using a single R_G or dual $R_{G(on)}$ and $R_{G(off)}$

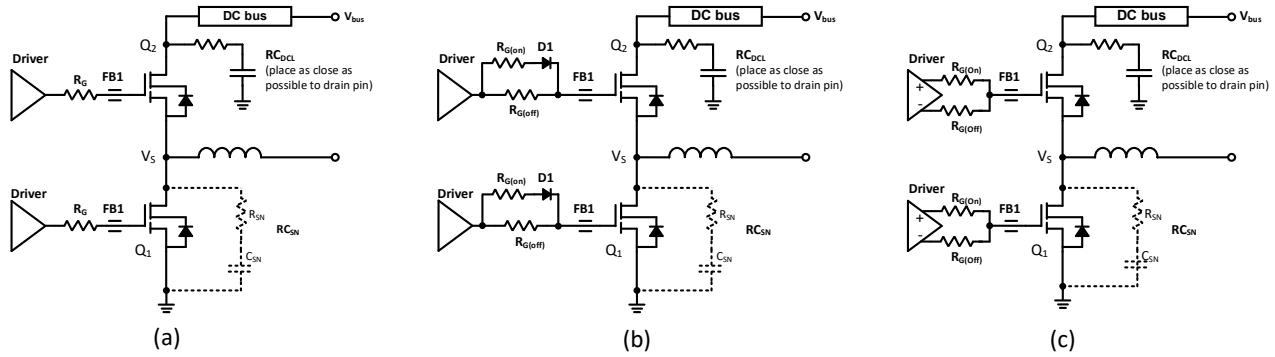


Figure 5. Driving circuits: (a) Single output driver with a single Rg, (b) single output driver with different turn-on and turn-off Rg, and (c) dual output driver with different turn-on and turn-off Rg.

The driver circuits with different configurations of driver and gate resistor are shown in Figure 5. A proper gate resistor is effective to limit the switching di/dt and keep the switching stable. As described in part III, the di/dt limit only applies to the device acting as a free-wheeling diode (FWD), i.e. the turn-off switching speed of the active device should be controlled, and only large turn-off Rg should be chosen but turn-on Rg can be small to reduce the turn-on power loss. The separate turn-on and turn-off Rg can be achieved using a Schottky diode in series with a Rg1 resistor paralleling with a Rg2 resistor, as shown in Figure 5 (b). It should be noticed that the direction of diode is different from that in the gate driving circuit of Si MOSFET. The equivalent turn-on Rg_on is Rg1*Rg2/(Rg1+Rg2), and turn-off Rg value is same with Rg2. It is convenient to configure the turn-on and turn-off Rg when a dual output driver IC is used, as shown in Figure 5 (c). Although there is no di/dt limit for turn-on, a proper turn-on Rg should be carefully selected to avoid cross-talk issues in high-speed switching half bridge circuit using 3 pin TO-220 and TO-247 packaged devices. The recommended equivalent gate resistor values for different GaN devices are listed in Table 3. For improving noise immunity during turn-off, a -3V gate drive voltage can be considered but the turn off Rg should be increased to maintain the same di/dt and turn-on Rg can be reduced to keep same turn-on switching speed.

Device Gate Drive Recommendations for Half Bridge Topologies							
Specifications	**GaN FET Devices**						
	TP65H015G5WS	**TP65H035G4WS/QS**	**TP65H035WS**	**TP65H050G4WS/BS/QS**	**TP65H050WS/QS**	**TP65H070LDG/LSG**	**TP65H150G4PS/LSG**
	TO-247	**TO-247/TOLL**	**TO-247**	**TO-247/TO-263/TOLL**	**TO-247**	**PQFN**	**TO-220/PQFN**
Gate Voltage Drive	**0V, 12 V**	**0V, 12 V**	**0V, 12V**	**0V, 12V**	**0V, 12V**	**0V, 12V**	**0V, 12V**
Recommended Gate Resistor $R_{G(on)}$	5Ω	22Ω	30Ω	30Ω	33Ω	33Ω	22 to 30Ω
Recommended Gate Resistor $R_{G(off)}$	15Ω	47Ω	47Ω	47Ω	47Ω	47 to 56Ω	33 to 47 Ω
Recommended Gate Resistor (R_G) for 2x to 2.5x Irms Topology: AC to DC or DC to AC	TBD	47Ω @ 45Apk	47Ω @ 45Apk	47Ω @ 33Apk	47Ω @ 33Apk	TBD	TBD
Gate Voltage Drive	**-3V, 12 V**	**-3V, 12 V**	**-3V, 12 V**	**-3V, 12 V**	**-3V, 12 V**	**-3V, 12 V**	**-3V, 12 V**
Recommended Gate Resistor $R_{G(on)}$	15Ω	18Ω	25 to 30Ω	25 to 30Ω	25 to 30Ω	22 to 30Ω	18-25Ω
Recommended Gate Resistor $R_{G(off)}$	TBD	47Ω to 56Ω	47 to 56Ω	47 to 56Ω	47 to 56Ω	47 to 56Ω	33 to 47Ω