

REVISION	DESCRIPTION	DATE	APPROVED

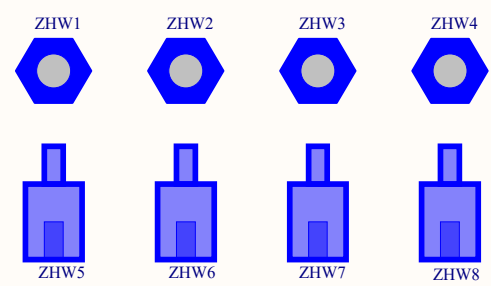
Note: Items in this schematic may be inconsistent with the Alif PCB Layout Guidelines, AAPN0036. If a discrepancy is seen between the schematic and AAPN0036, AAPN0036 takes precedence.

Revision History:

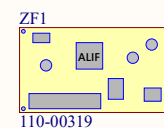
REV	DATE	Description:
A	04-SEP-2025	Initial Release, taken from 120-00319-B Replacing JLOB E1 with CMSIS DAP E1C E1C Supports 3 UARTS, SEUART, UART2 and UART4

Required 2.54mm Shunts:

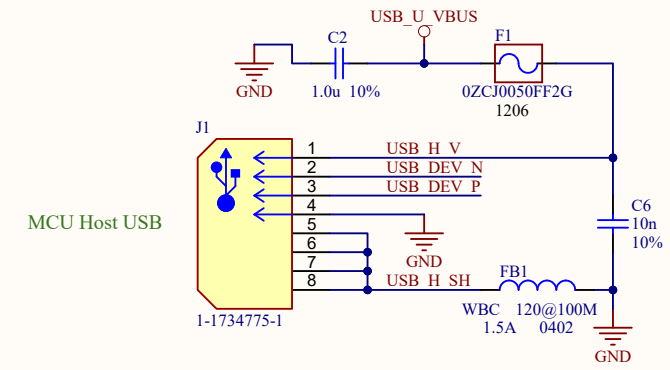
JP1	VDD_3V3_USB Current Measurement (* shunted)
JP2-1 JP2-2	VDD_MAIN = 1.8V (* shunted)
JP2-2 JP2-3	VDD_MAIN = 3.3V
JP3	VDDIO Current Measurement (* shunted)
JP4-1 JP4-2	FLEXIO = 1.8V (* shunted)
JP4-2 JP4-3	FLEXIO = 3.3V
JP5-1 JP5-2	VBATT = VDD_MAIN (* default)
JP5-2 JP5-3	VBATT = 3.3V / Coin Cell
JP7-1 JP7-2	Click Board Power = 1.8V
JP7-3 JP7-4	Click Board Power = 3.3V (* default)
JP7-5 JP7-6	Click Board Power = 5.0V



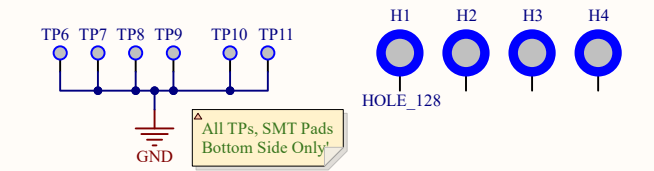
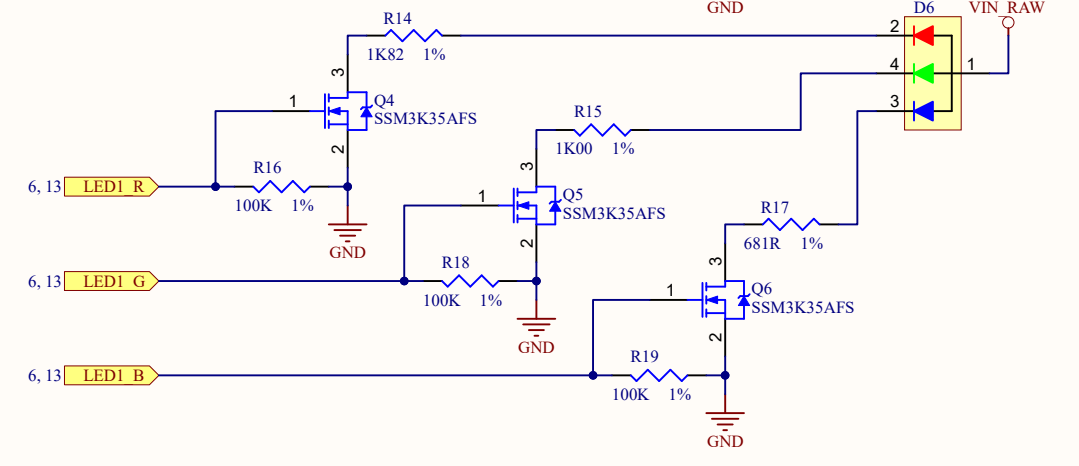
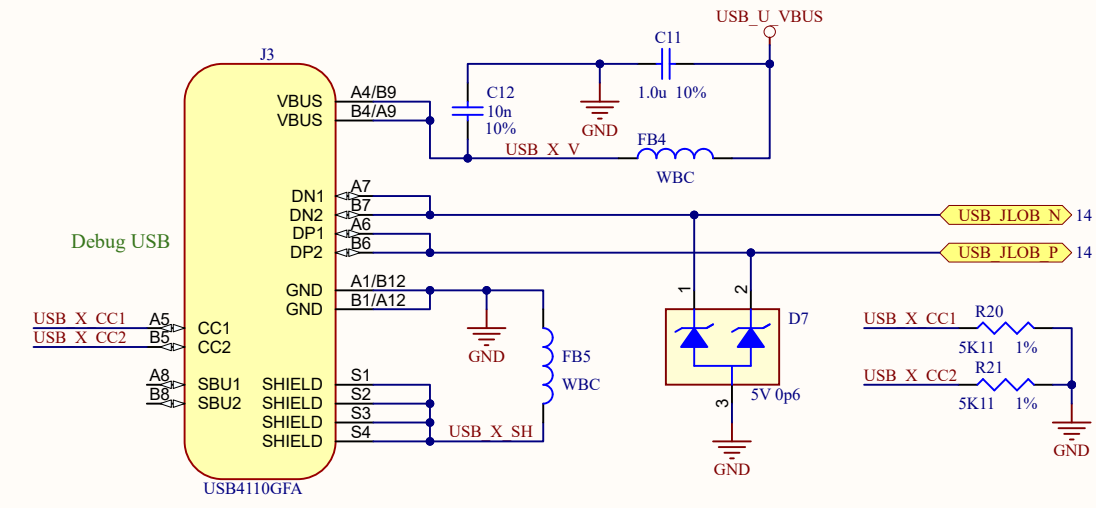
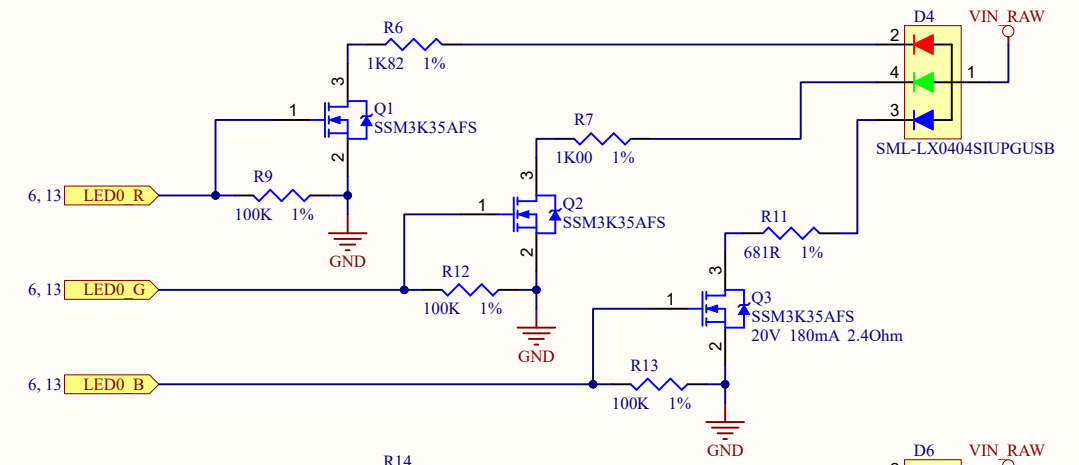
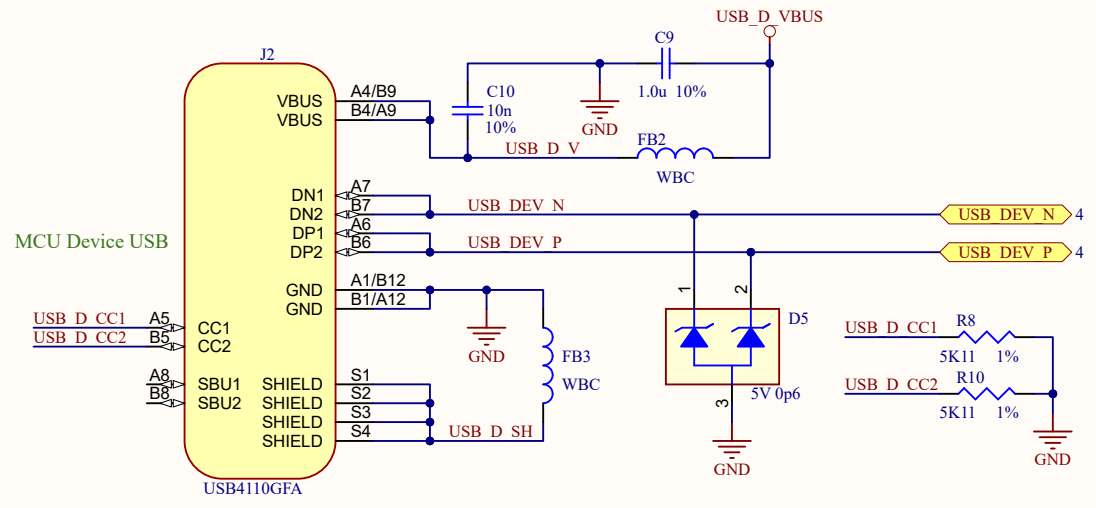
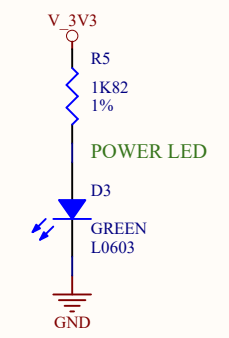
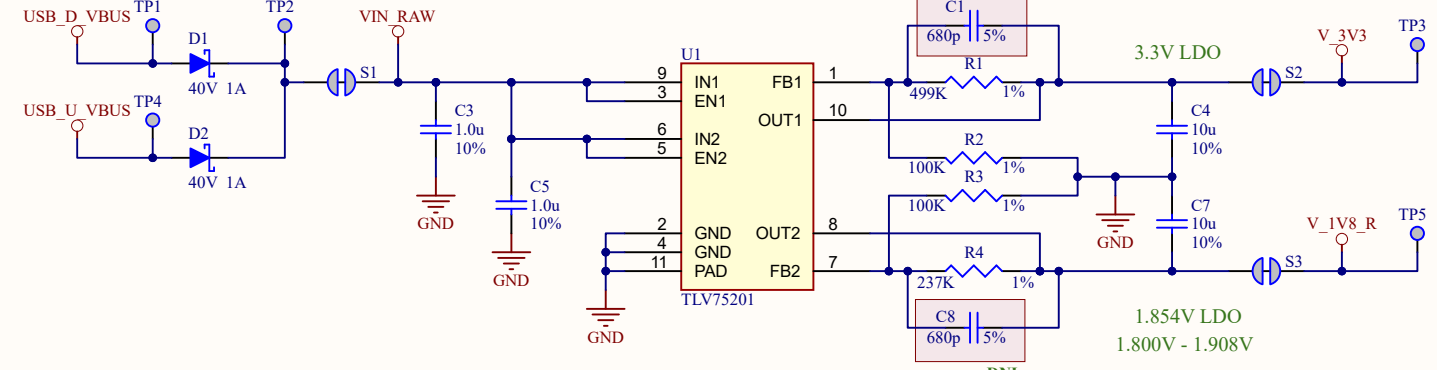
Nylon Mounting Hardware (H1 - H4)



APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00319			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00319	EAGLE DEV KIT				
ASSY DWG: 120-00319	SIZE: B	CAGE CODE: none	DWG NO.: 220-00319	REV: B	
FAB DWG: 210-00319	SCALE: none	FILE NAME: 1-RevisionHistory.SchDoc	SHEET: 1	OF: 15	
PCB DWG: 110-00319					



USB Host only gets power from Debug USB

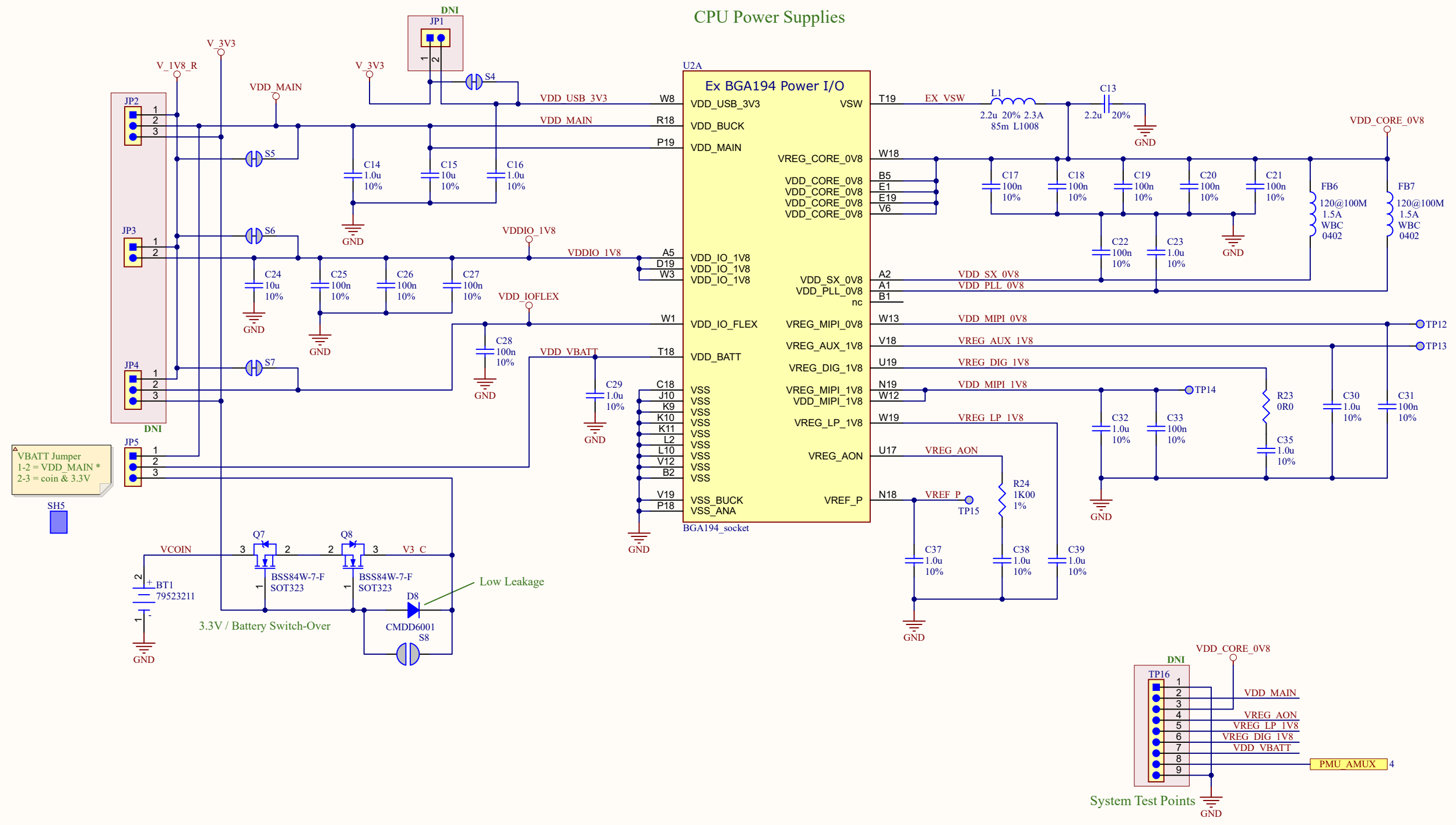


All TPs, SMT Pads Bottom Side Only!

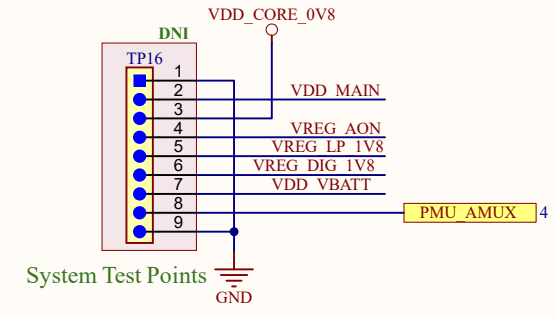
APPROVALS	DATE	PROJECT		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA		
ENG: K Braun	--/--	00319				
DSN: K Braun	--/--		TITLE			
CHK: n/a	--/--		EAGLE DEV KIT			
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ASSY DWG: 120-00319			SCALE: none	FILE NAME	2-PowerInput.SchDoc	SHEET 2 OF 15
FAB DWG: 210-00319						
PCB DWG: 110-00319						

REVISION	DESCRIPTION	DATE	APPROVED

CPU Power Supplies

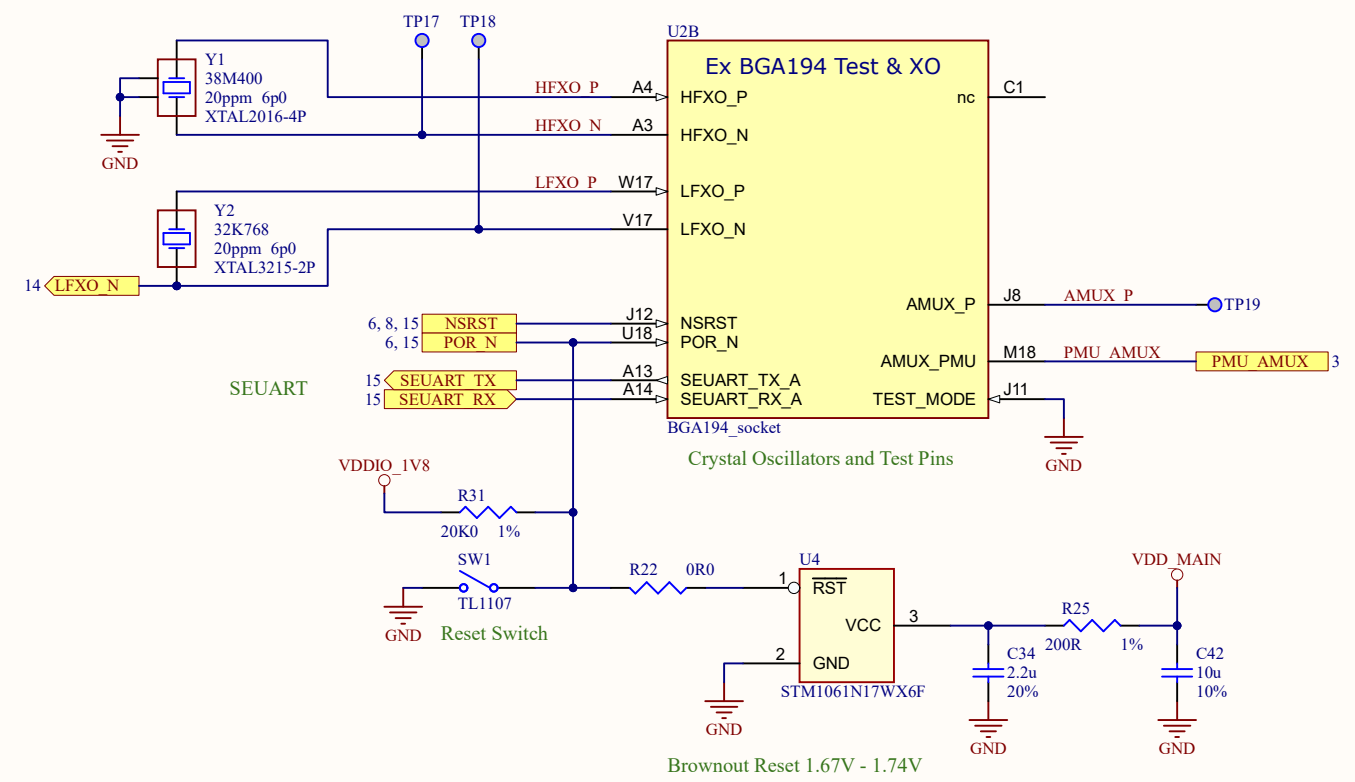
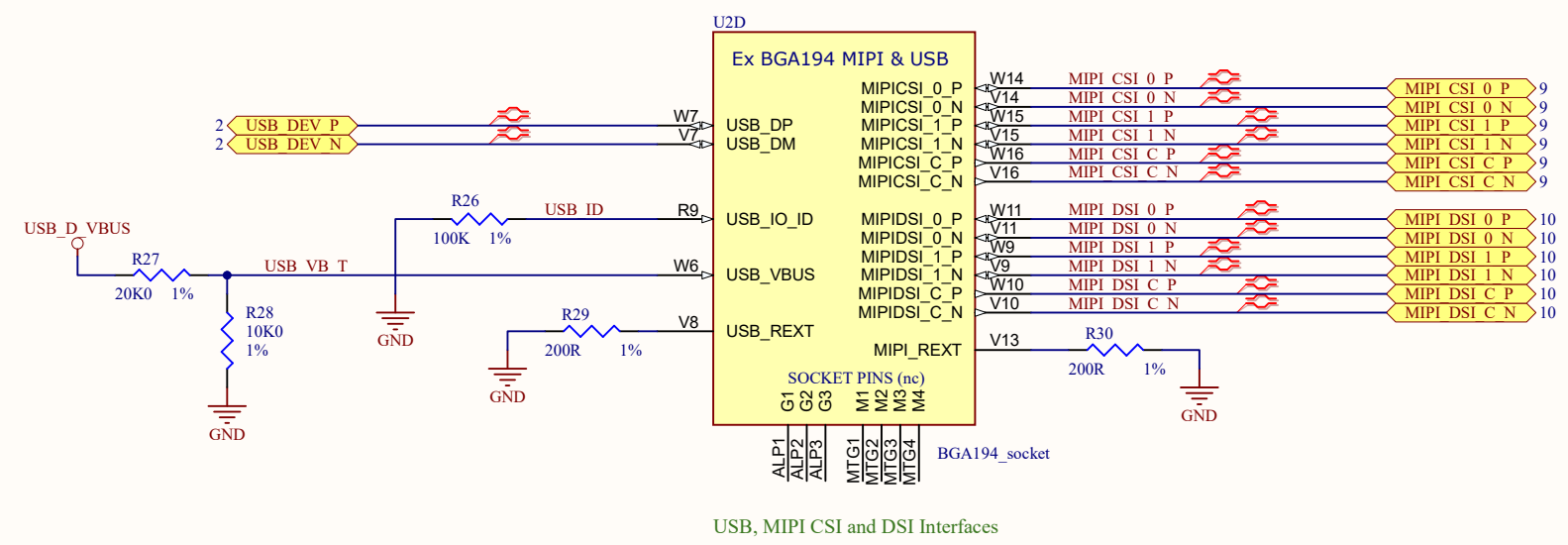


VBATT Jumper
1-2 = VDD_MAIN *
2-3 = coin & 3.3V



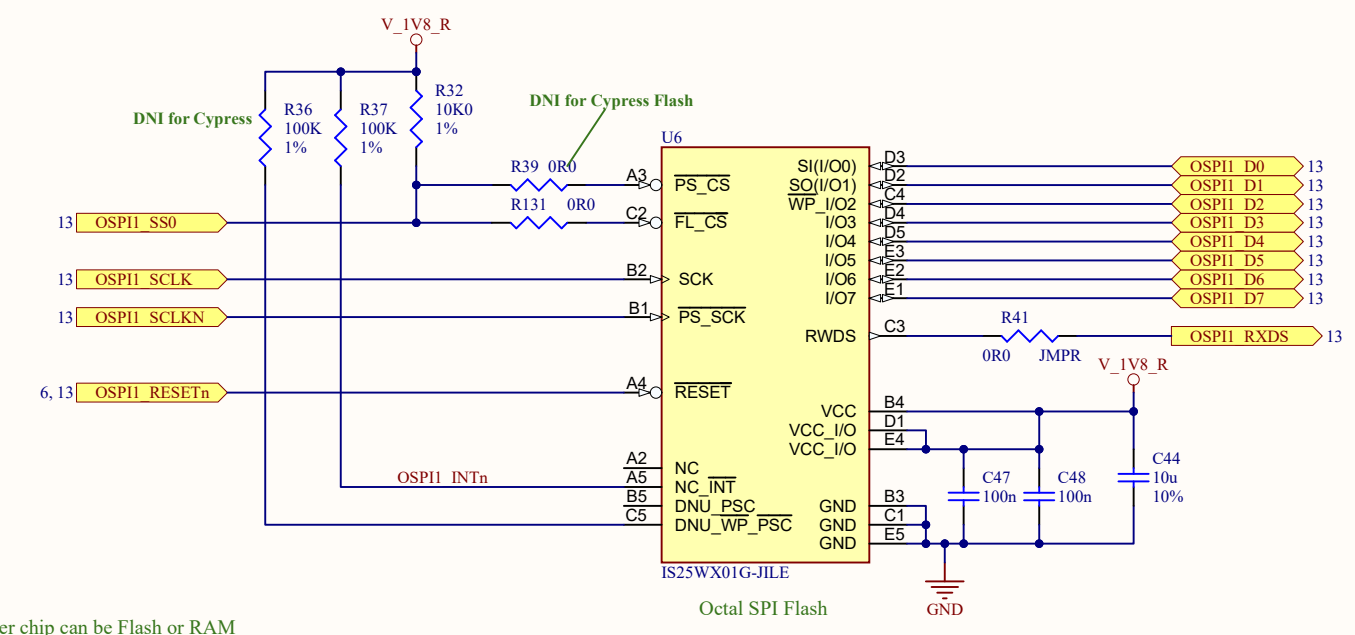
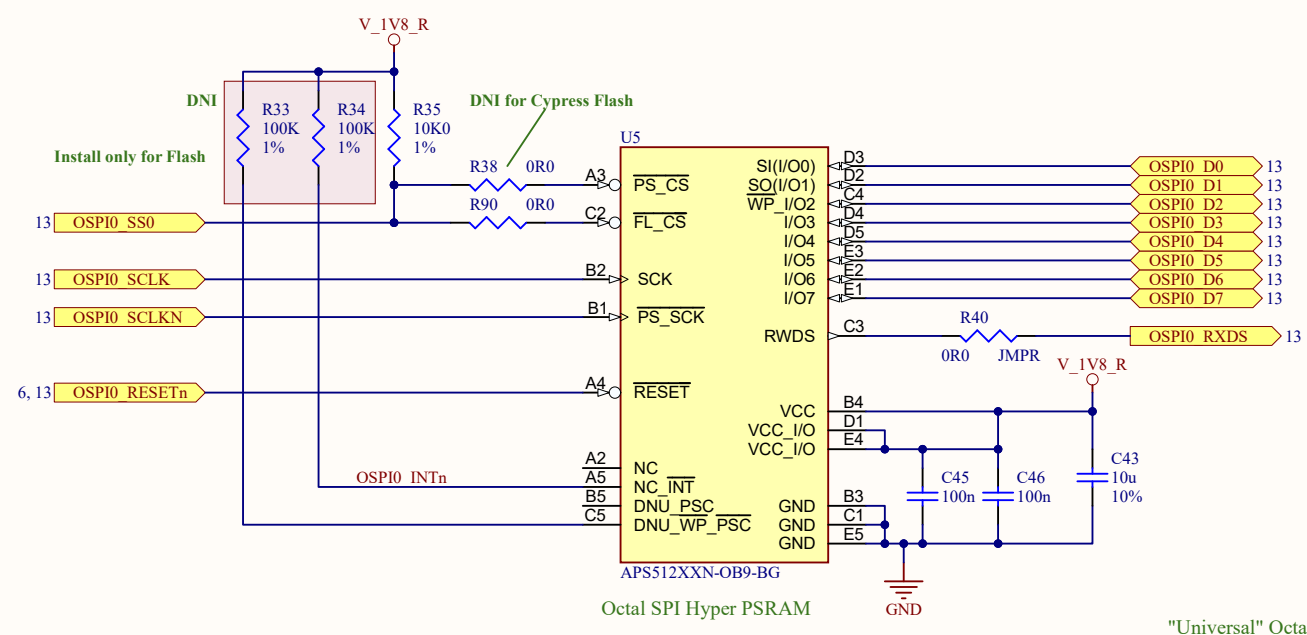
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
ENG: K Braun	--/--	00319	Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
DSN: K Braun	--/--		TITLE	
CHK: n/a	--/--		EAGLE DEV KIT	
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.
BOM: 250-00319		B	none	220-00319
ASSY DWG: 120-00319		SCALE	FILE NAME	REV
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PCB DWG: 110-00319				

REVISION	DESCRIPTION	DATE	APPROVED

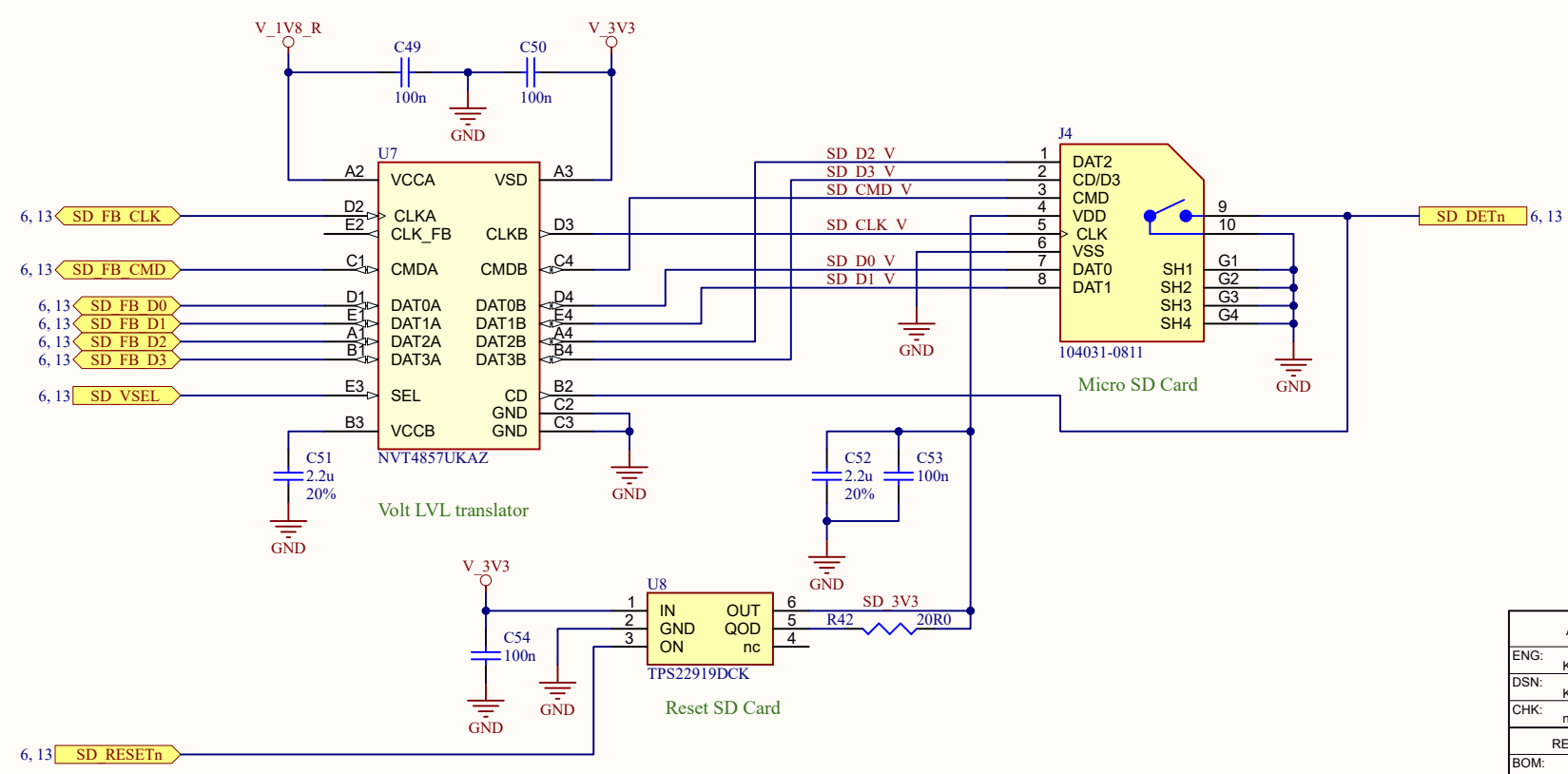


APPROVALS	DATE	PROJECT			Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00319			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00319	EAGLE DEV KIT				
ASSY DWG: 120-00319	SIZE	CAGE CODE	DWG NO.	REV	
FAB DWG: 210-00319	B	none	220-00319	B	
PCB DWG: 110-00319	SCALE: none	FILE NAME	4-CPUMipiXo.SchDoc	SHEET	4 OF 15

REVISION	DESCRIPTION	DATE	APPROVED



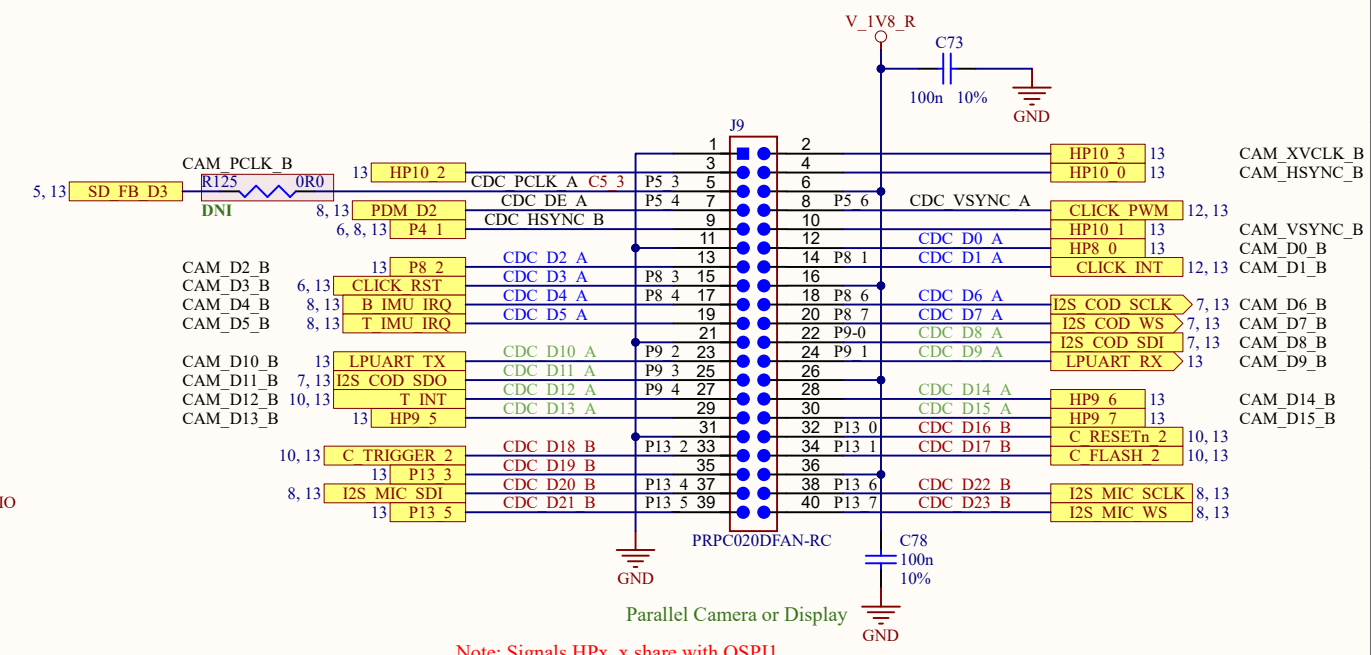
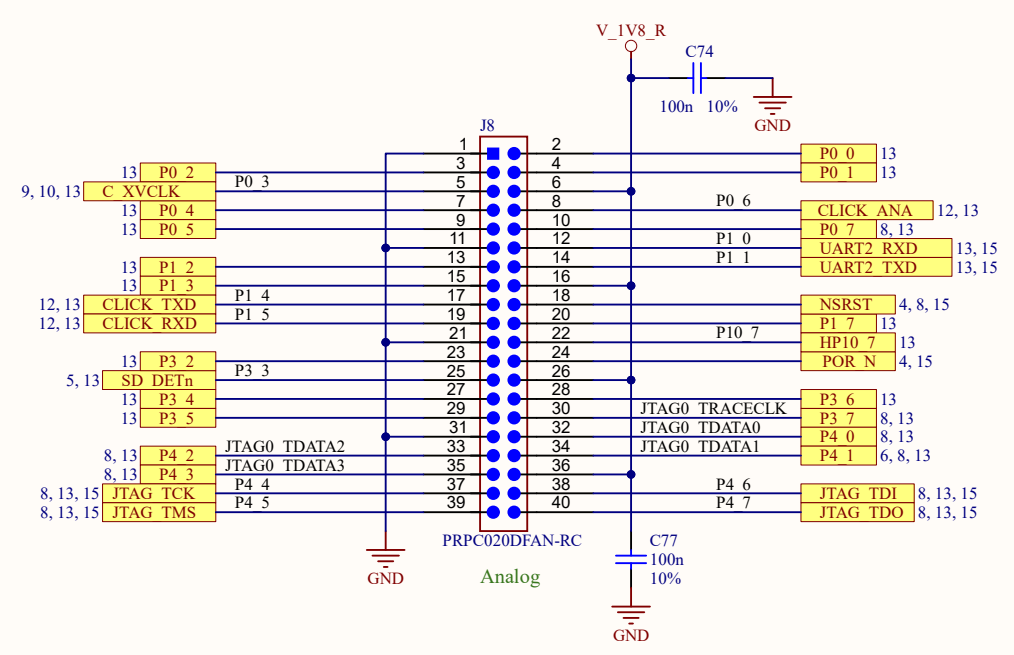
"Universal" Octal SPI Devices. Either chip can be Flash or RAM



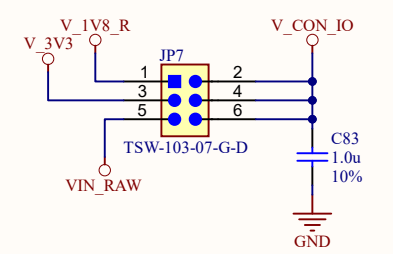
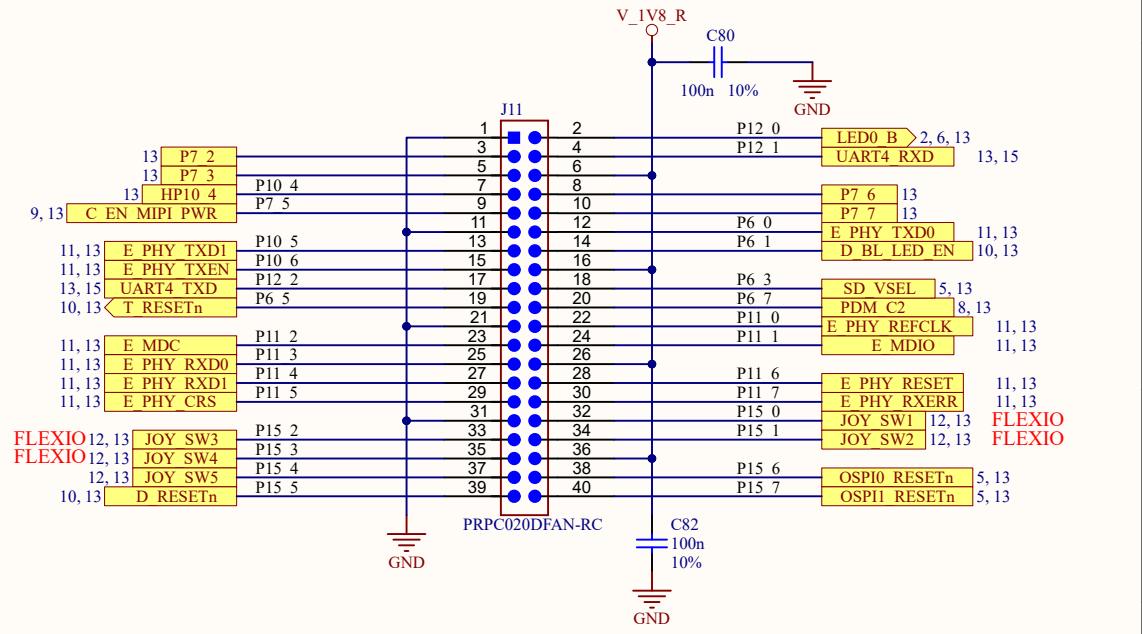
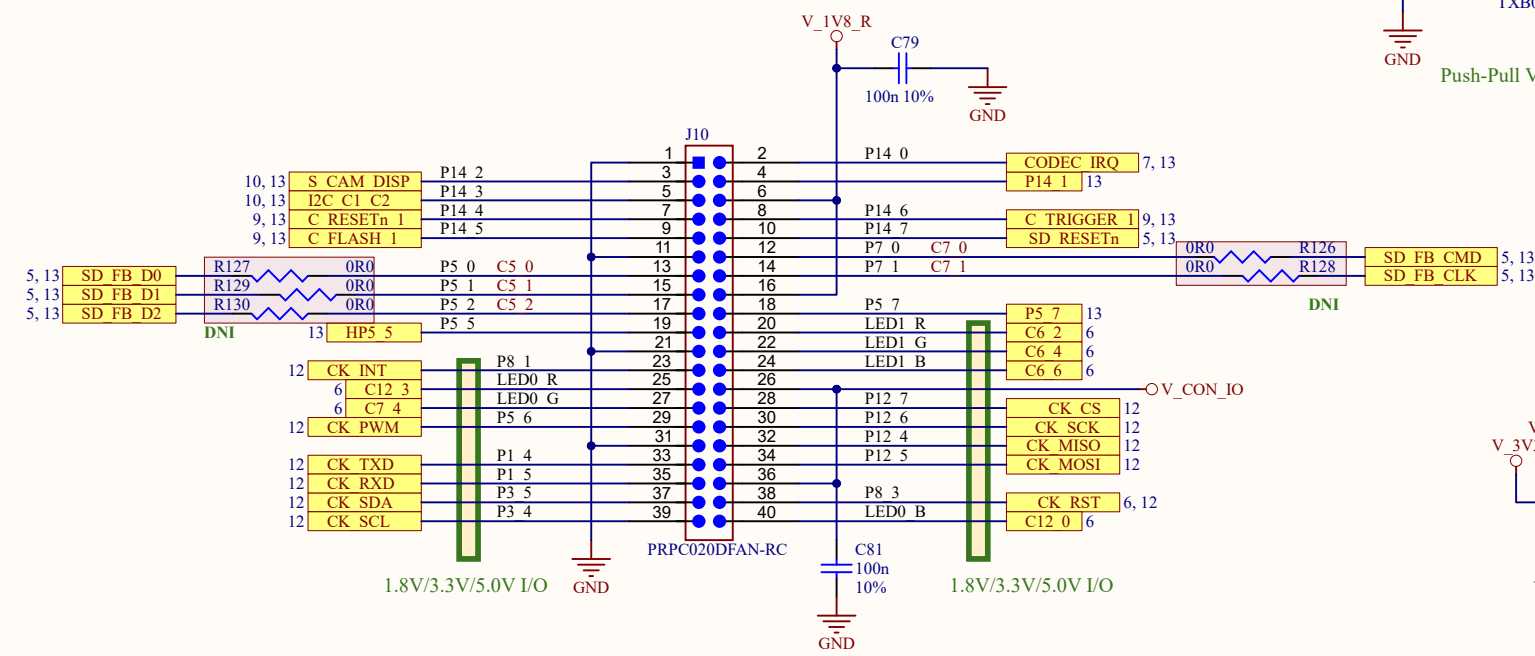
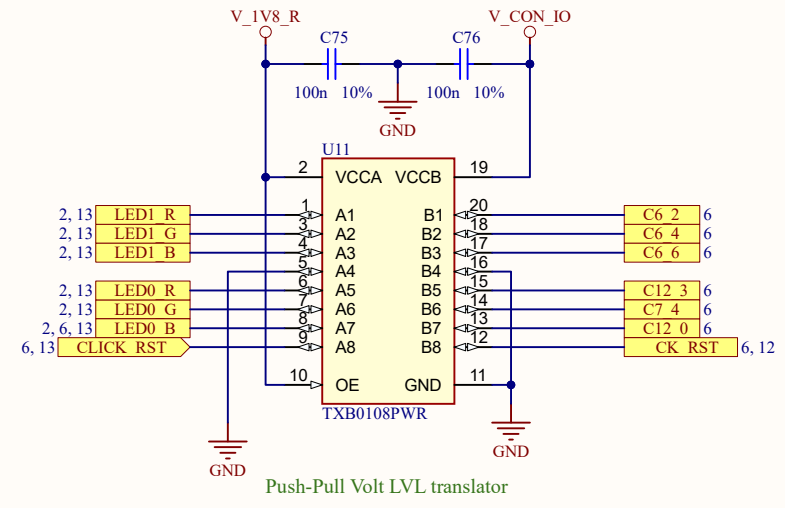
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
ENG: K Braun	--/--	00319	Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
DSN: K Braun	--/--			
CHK: n/a	--/--			
REFERENCE DOCUMENTS			TITLE	
BOM: 250-00319			EAGLE DEV KIT	
ASSY DWG: 120-00319	SIZE: B	CAGE CODE: none	DWG NO.: 220-00319	REV: B
FAB DWG: 210-00319	SCALE: none	FILE NAME: 5-Memory.SchDoc	SHEET 5 OF 15	
PCB DWG: 110-00319				

DWG. NO. 220-00319
REV. 5

REVISION	DESCRIPTION	DATE	APPROVED



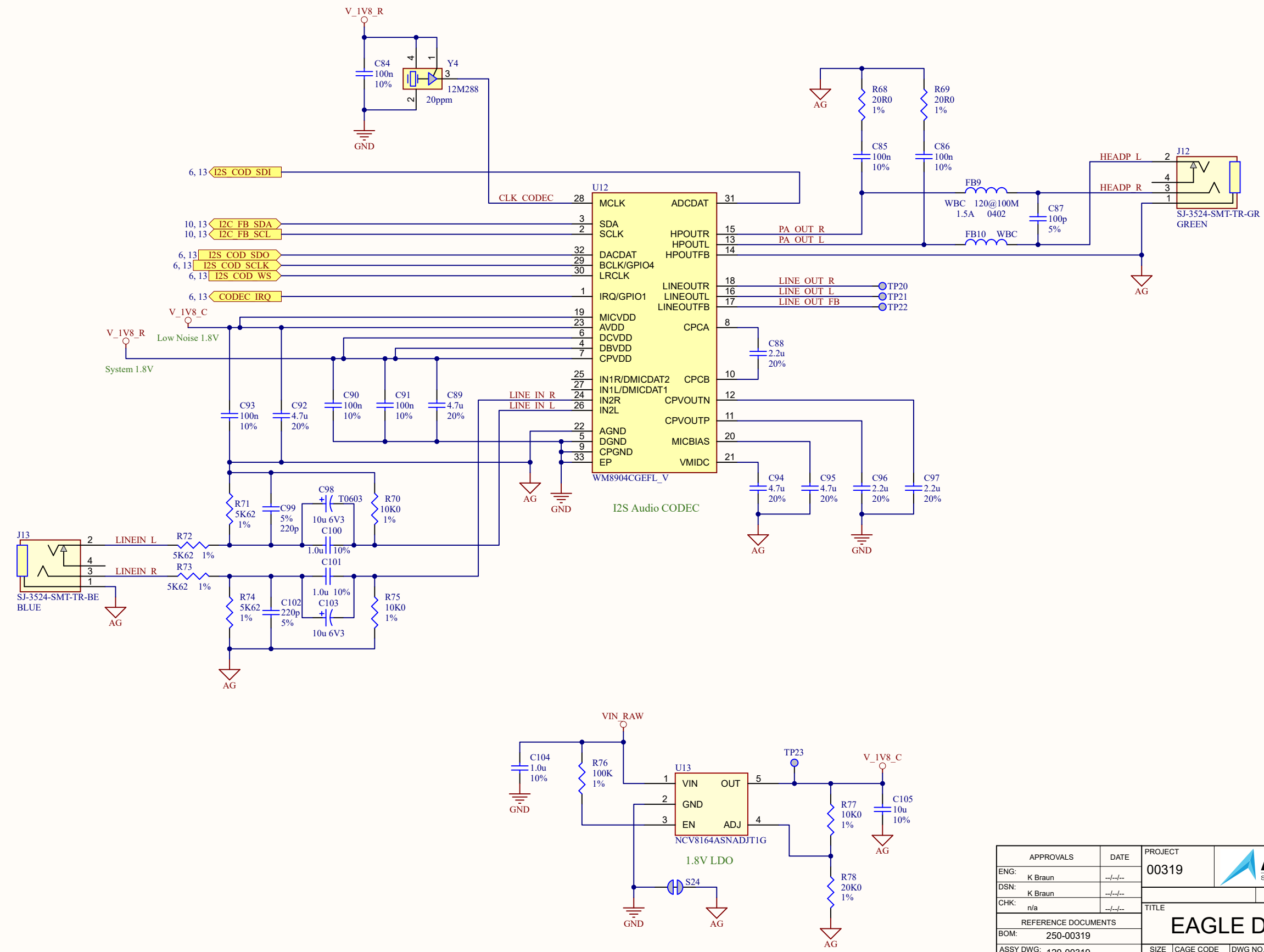
Note: Signals HPx_x share with OSP11
Shunts need to be soldered before signal(s) is/are available



Connector I/O Voltage
1-2 = 1.8V
3-4 = 3.3V
5-6 = 5.0V

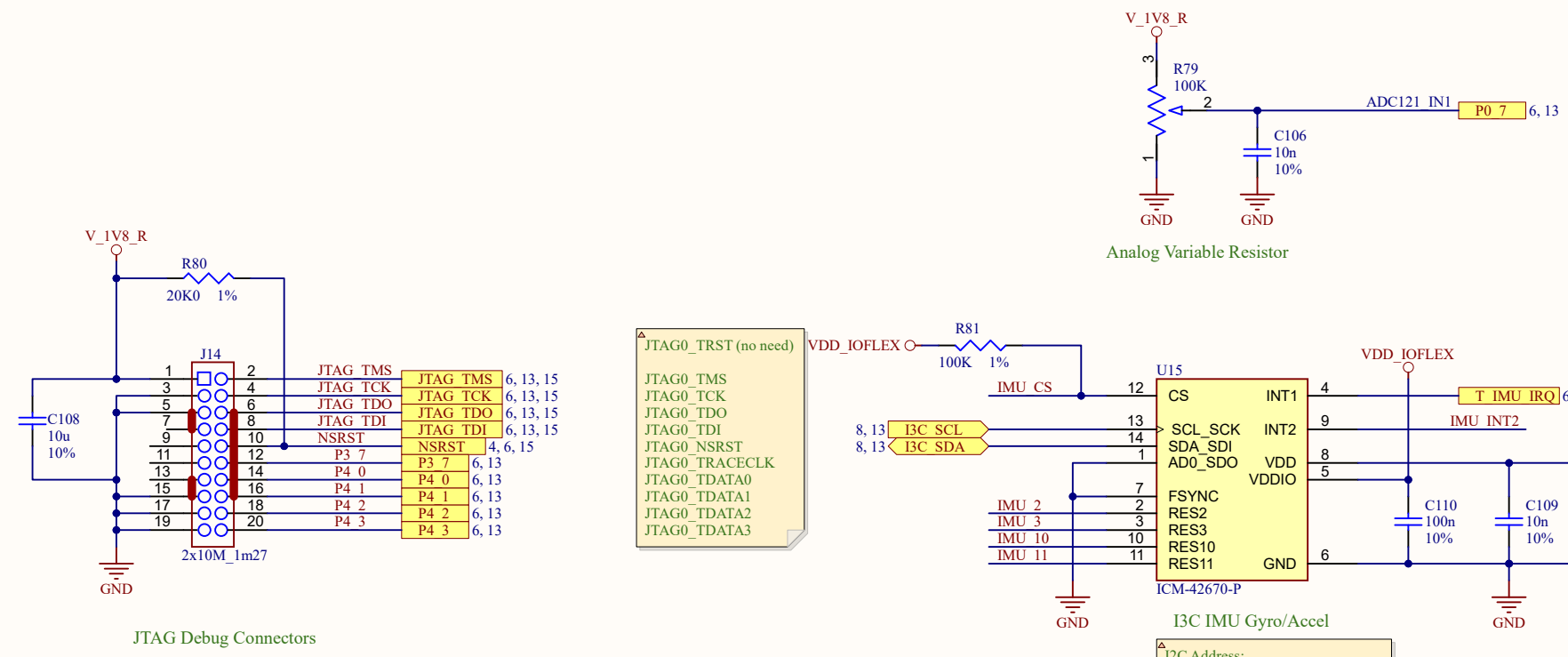
APPROVALS	DATE	PROJECT		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00319		
DSN: K Braun	--/--		EAGLE DEV KIT	
CHK: n/a	--/--			
REFERENCE DOCUMENTS			TITLE	
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ASSY DWG: 120-00319	SCALE: none	FILE NAME: 6-IO Headers.SchDoc	SHEET 6 OF 15	
FAB DWG: 210-00319				
PCB DWG: 110-00319				

REVISION	DESCRIPTION	DATE	APPROVED



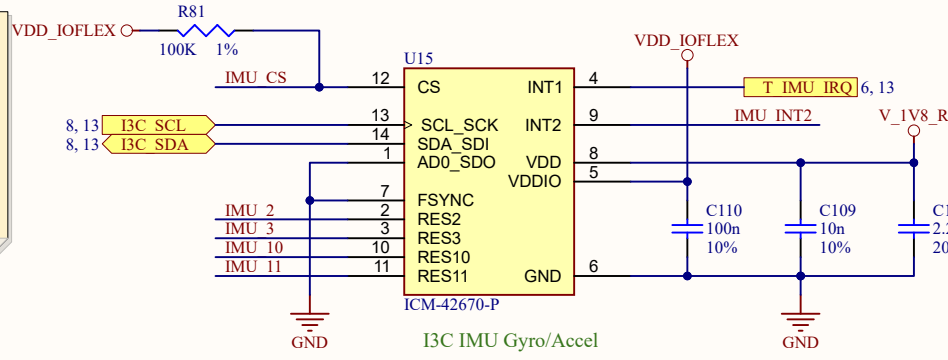
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
ENG: K Braun	--/--	00319	Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
DSN: K Braun	--/--		TITLE	
CHK: n/a	--/--		EAGLE DEV KIT	
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG. NO.
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ASSY DWG: 120-00319		SCALE: none	FILE NAME	7-CODEC.SchDoc
FAB DWG: 210-00319				SHEET 7 OF 15
PCB DWG: 110-00319				

REVISION	DESCRIPTION	DATE	APPROVED

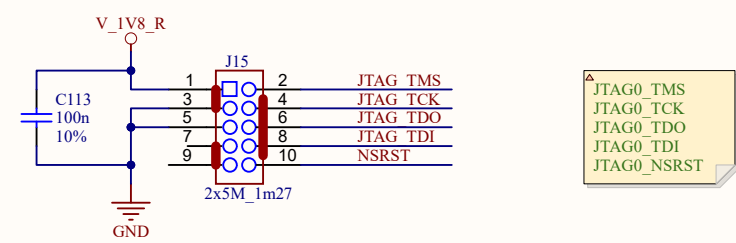
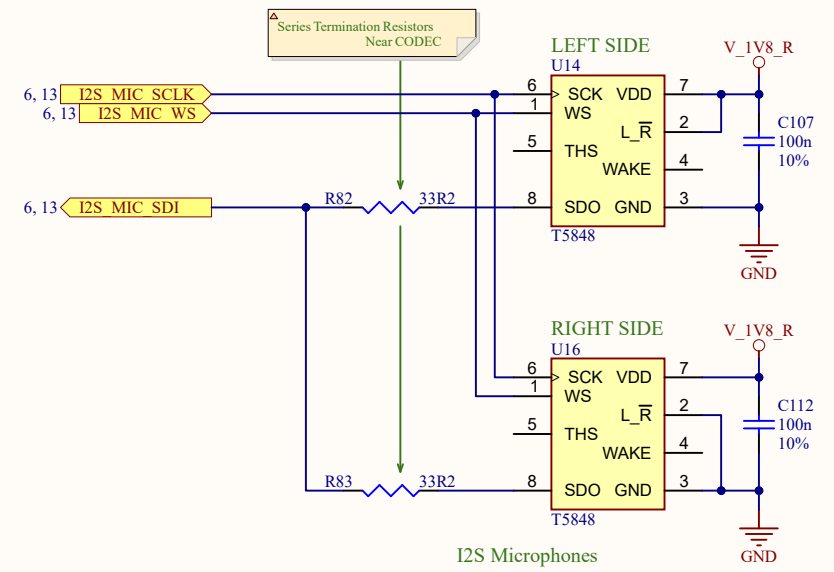


JTAG0_TRST (no need)

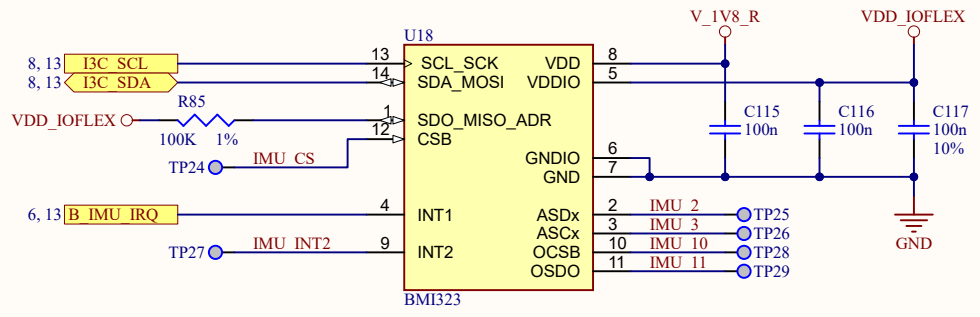
JTAG0_TMS
JTAG0_TCK
JTAG0_TDO
JTAG0_TDI
JTAG0_NSRST
JTAG0_TRACECLK
JTAG0_TDATA0
JTAG0_TDATA1
JTAG0_TDATA2
JTAG0_TDATA3



I2C Address:
AD0
0 7-bit = 0x68, 8-bit = 0xD0*
1 7-bit = 0x69, 8-bit = 0xD2



JTAG0_TMS
JTAG0_TCK
JTAG0_TDO
JTAG0_TDI
JTAG0_NSRST



I2C Address:
SDO_MISO_ADR
0 7-bit = 0x68, 8-bit = 0xD0
1 7-bit = 0x69, 8-bit = 0xD2*

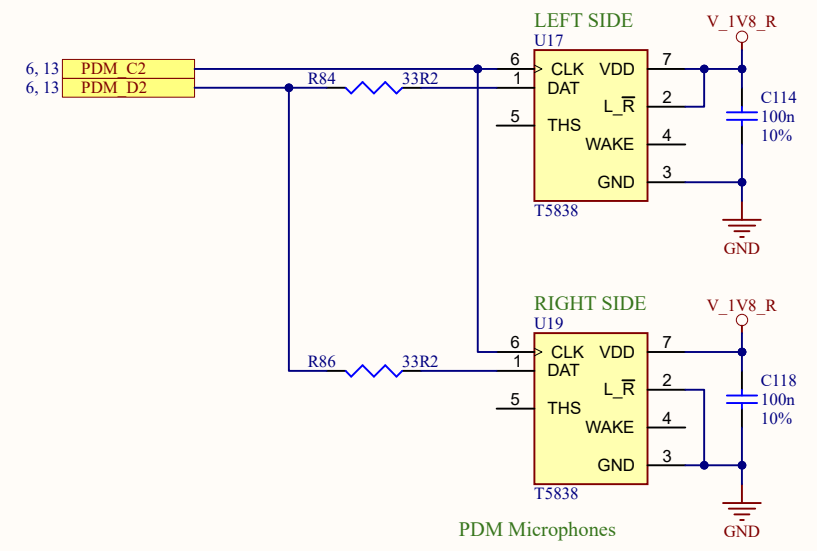
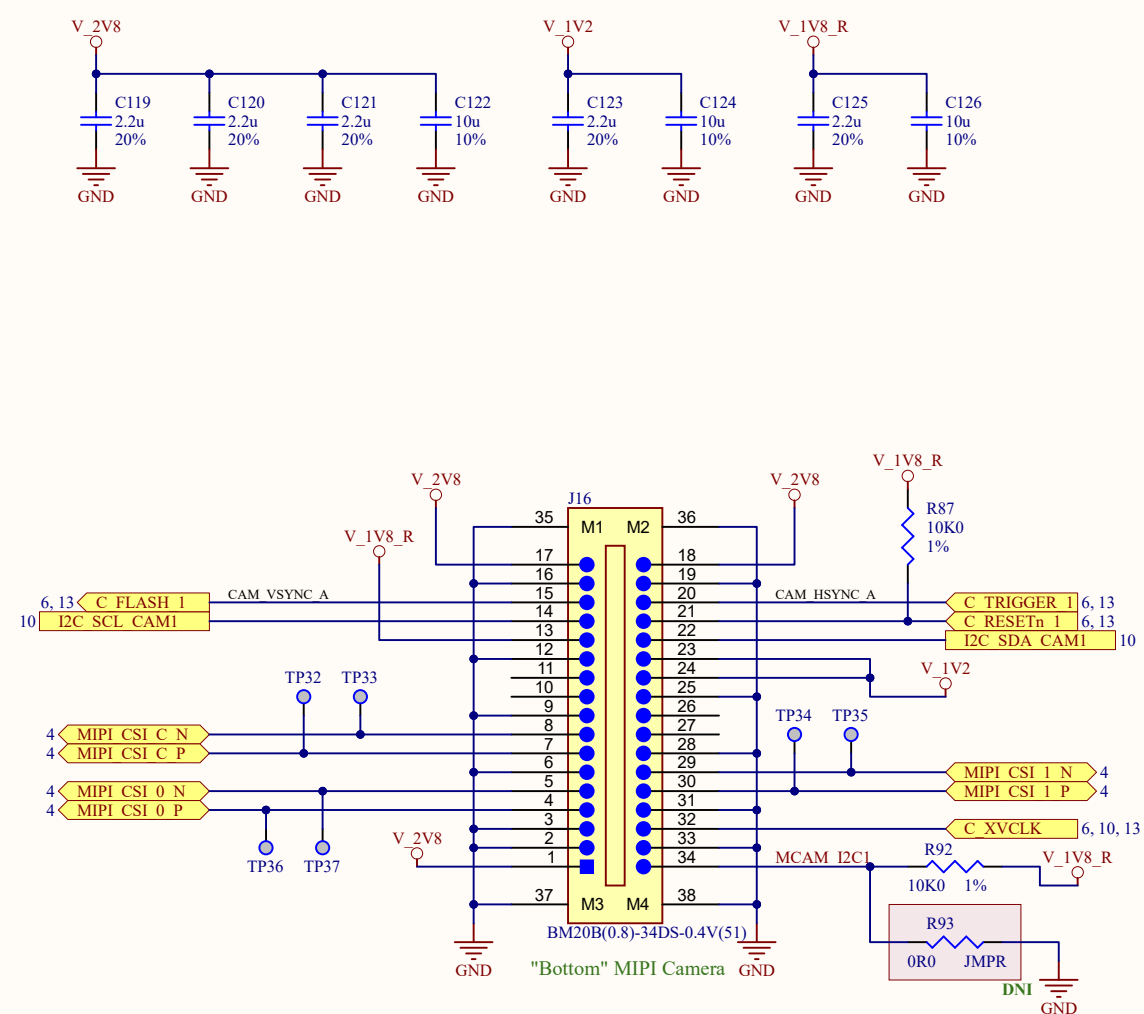
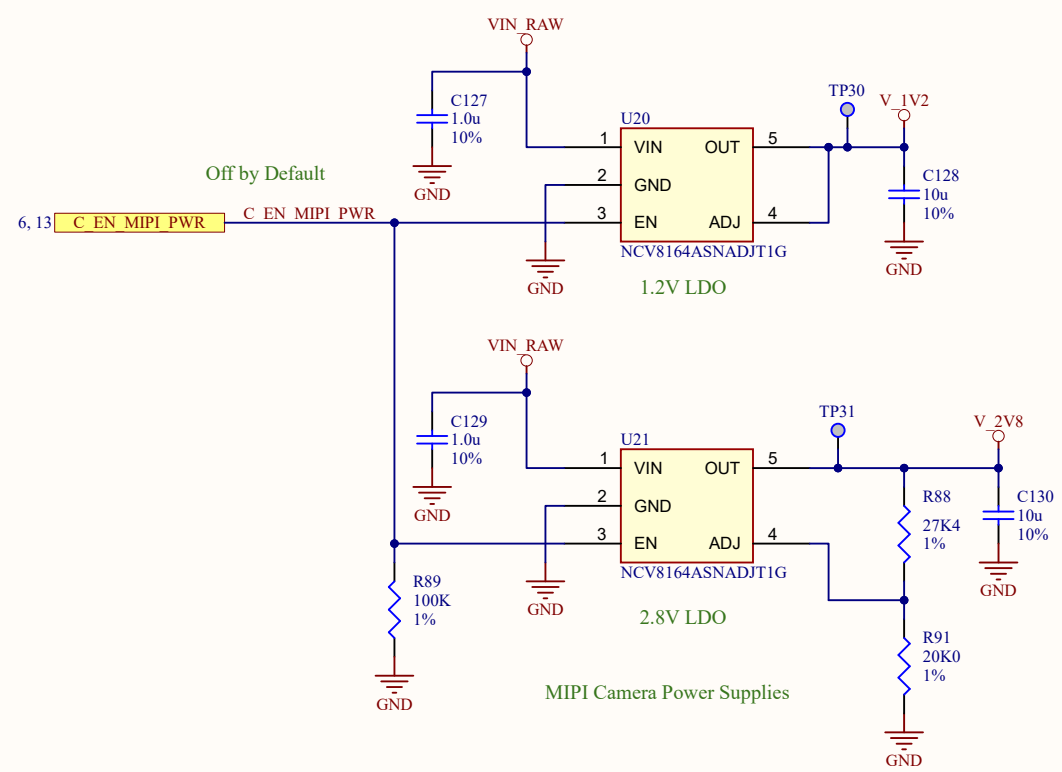


Table 29: Mapping of the secondary interface pins

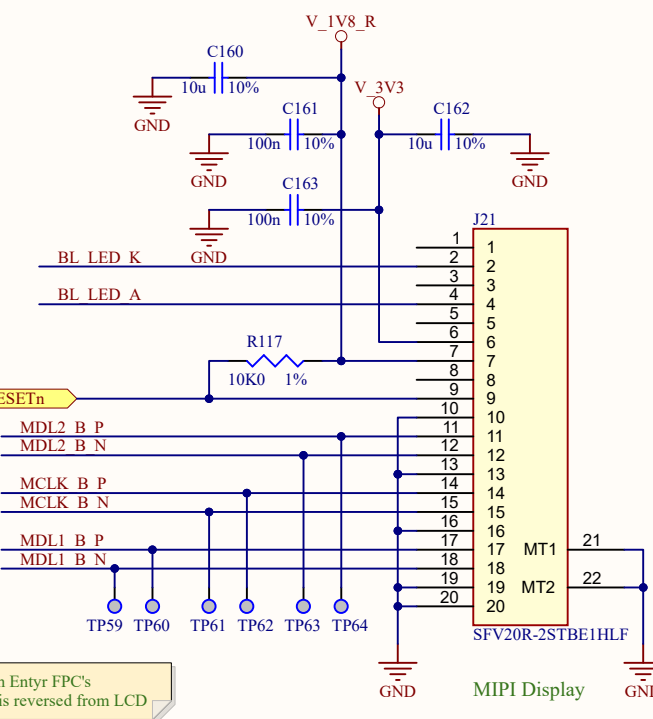
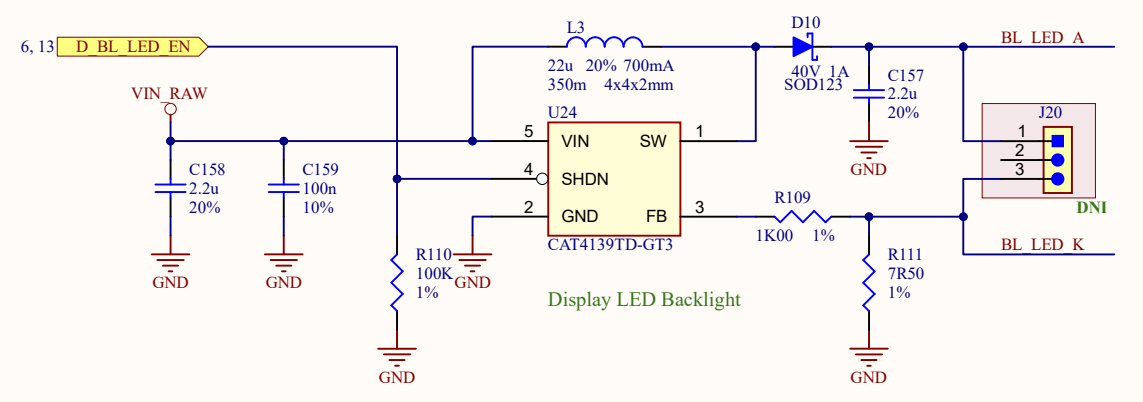
Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I2C
2	ASDx	Digital I/O	Secondary Magnetometer interface	MOSI	SISO	SDA
3	ASCx	Digital I/O	Secondary Magnetometer interface	SCK	SCK	SCL
10	OCSB	Digital in	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital out	Secondary OIS interface	MISO	DNC	DNC

APPROVALS	DATE	PROJECT		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
ENG: K Braun	--/--	00319			
DSN: K Braun	--/--		EAGLE DEV KIT		
CHK: n/a	--/--				
REFERENCE DOCUMENTS			TITLE		
BOM: 250-00319	ASSY DWG: 120-00319		SIZE: B	CAGE CODE: none	DWG NO.: 220-00319
FAB DWG: 210-00319		SCALE: none		FILE NAME: 8-SensorsAndJTAG.SchDoc	REV: B
PCB DWG: 110-00319		SHEET: 8		OF: 15	

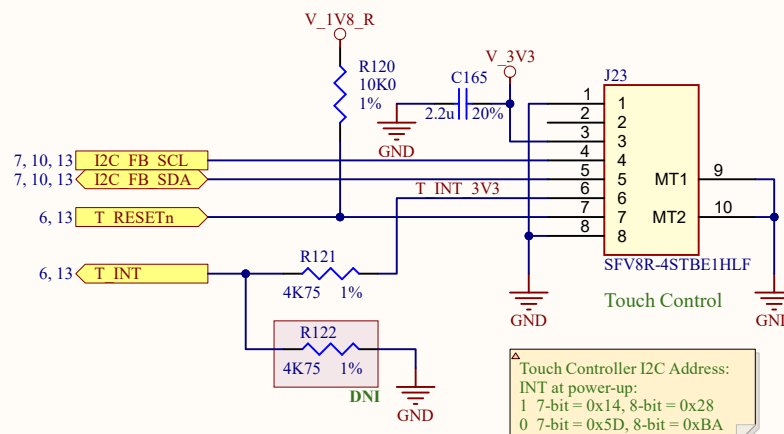


^aOV5765 MIPI Camera I2C Address Option (Pin 34):
 1.8V: 7-bit = 0x10 (J16 - bottom connector)
 GND: 7-bit = 0x36 (J22 - top connector)
 MT9M114 MIPI Camera I2C Address Option
 1.8V: 7-bit = 0x5D (bottom connector)
 GND: 7-bit = 0x48 (top connector)
 ARX030 MIPI Camera I2C Address Option
 1.8V: 7-bit = 0x36 (bottom connector)
 GND: 7-bit = 0x36 (top connector) - same T&B

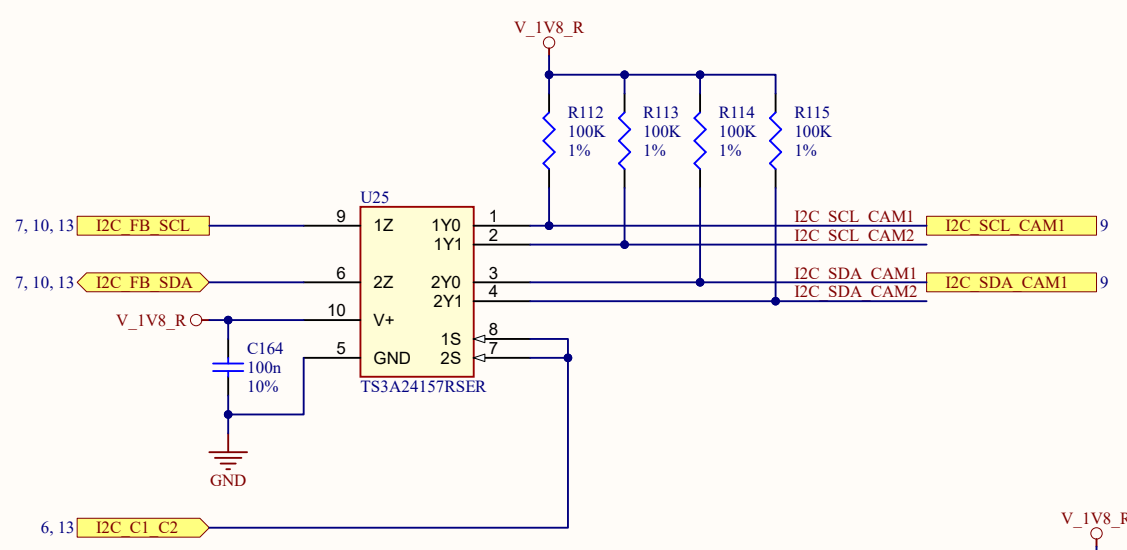
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00319			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00319	EAGLE DEV KIT				
ASSY DWG: 120-00319	SIZE	CAGE CODE	DWG NO.	REV	
FAB DWG: 210-00319	B	none	220-00319	B	
PCB DWG: 110-00319	SCALE: none	FILE NAME	9-MIPI 1.SchDoc	SHEET	9 OF 15



With Bottom Entry FPC's - Pin order is reversed from LCD

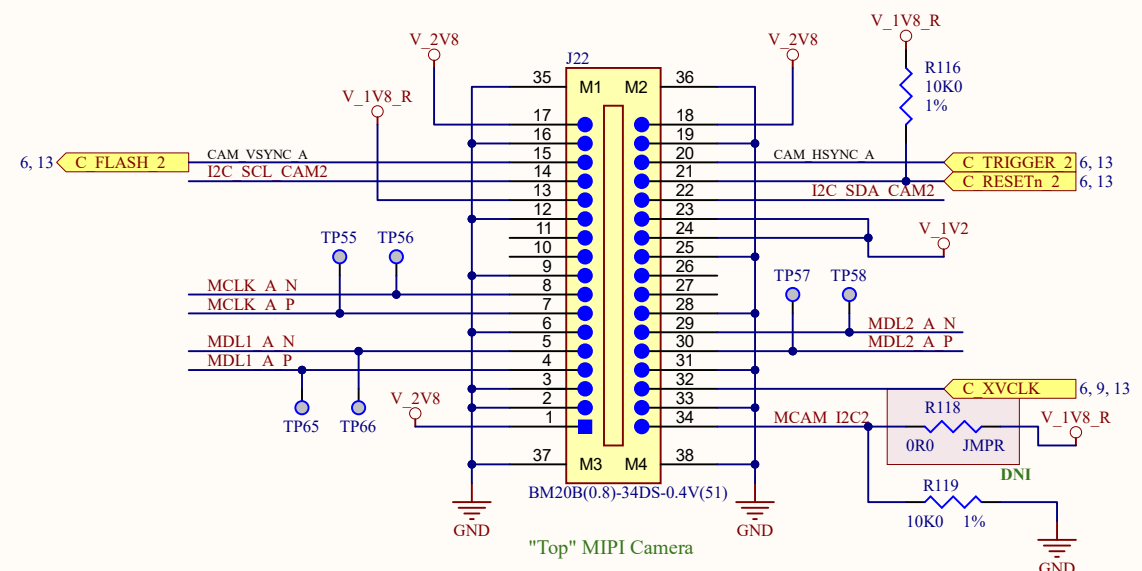


Touch Controller I2C Address:
INT at power-up:
1 7-bit = 0x14, 8-bit = 0x28
0 7-bit = 0x5D, 8-bit = 0xBA

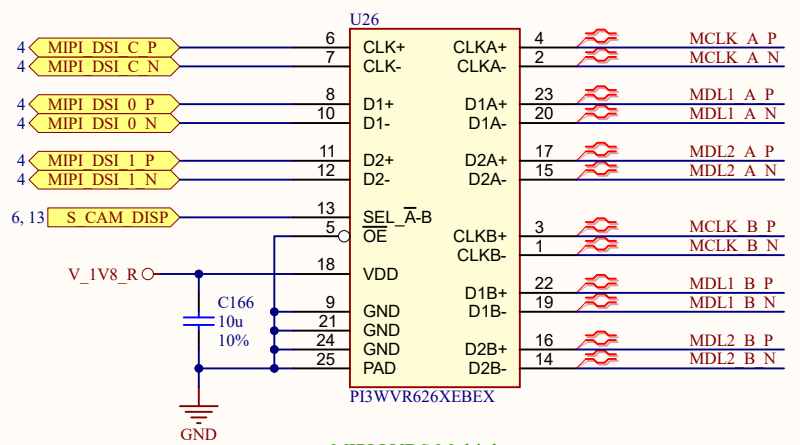


MIPI Camera I2C Multiplexer:
Some cameras do not have changeable I2C addresses. If both cameras are used at the same time, an I2C address conflict will occur. This mux picks a single camera to access.

I2C_C1_C2 : 0 = Cam 1, 1 = Cam 2



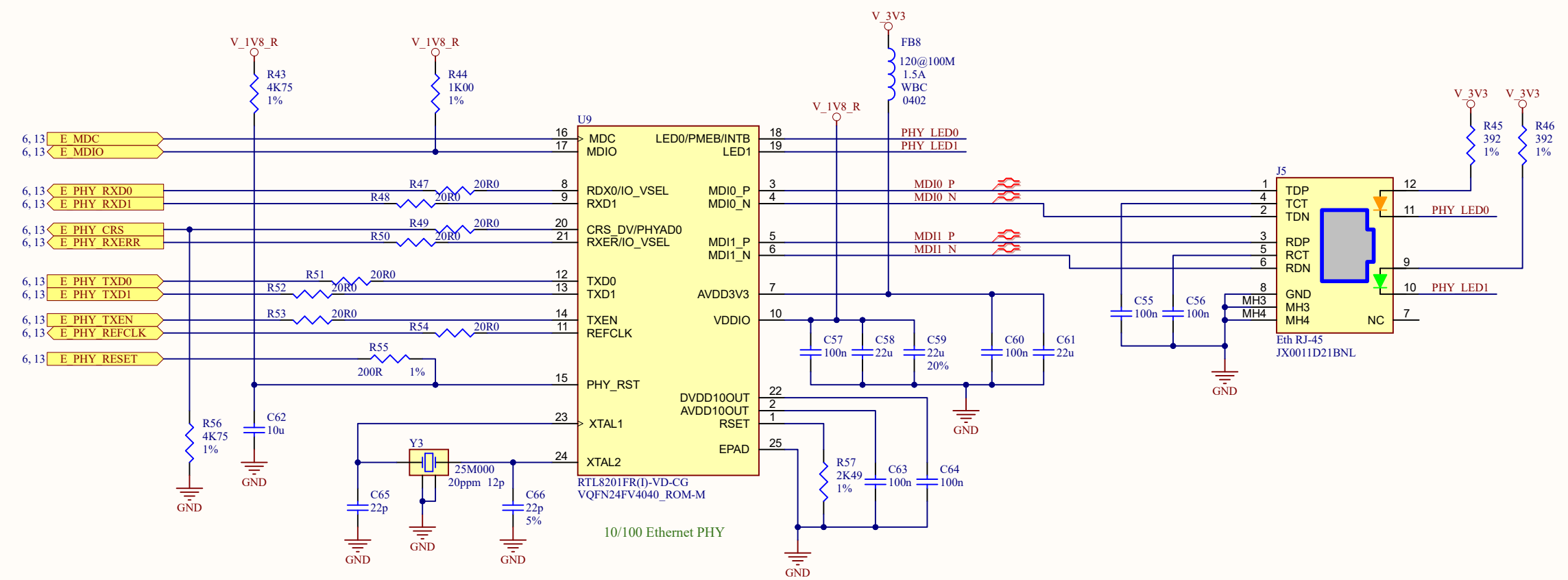
"Top" MIPI Camera



MIPI LVDS Multiplexer
S_CAM_DISP : 0 = CSI, 1 = DSI

APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
ENG: K Braun	--/--	00319	Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
DSN: K Braun	--/--			
CHK: n/a	--/--			
REFERENCE DOCUMENTS			TITLE	
BOM: 250-00319			EAGLE DEV KIT	
ASSY DWG: 120-00319	SIZE: B	CAGE CODE: none	DWG NO.: 220-00319	REV: B
FAB DWG: 210-00319	SCALE: none	FILE NAME: 10-MIPI_2.SchDoc		
PCB DWG: 110-00319			SHEET: 10	OF: 15

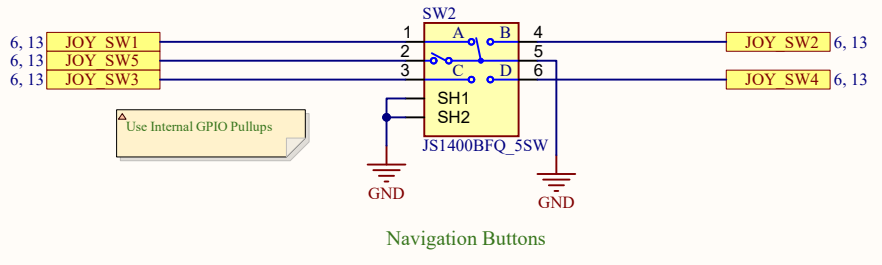
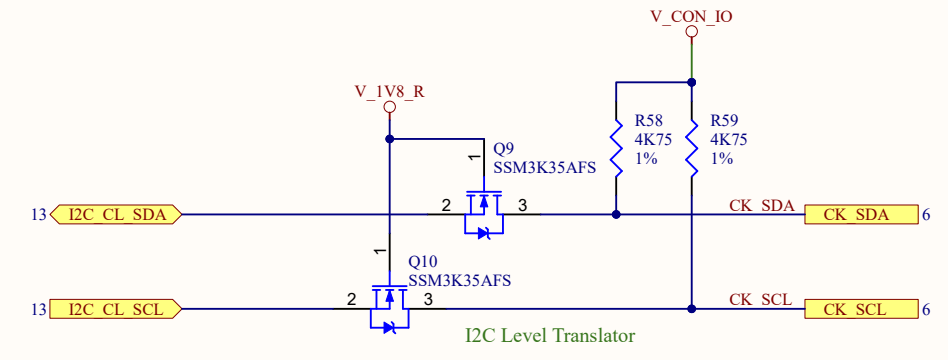
REVISION	DESCRIPTION	DATE	APPROVED



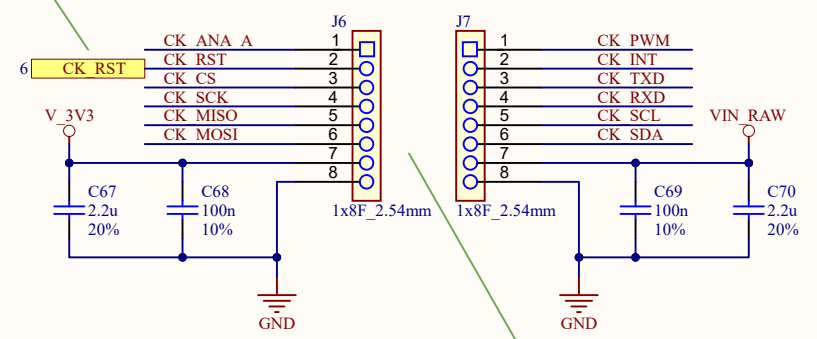
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00319			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00319		EAGLE DEV KIT			
ASSY DWG: 120-00319		SIZE	CAGE CODE	DWG NO.	REV
FAB DWG: 210-00319		B	none	220-00319	B
PCB DWG: 110-00319		SCALE: none	FILE NAME	11-Ethernet.SchDoc	SHEET 11 OF 15

DWG NO. 220-00319
REV/SHT B / 11

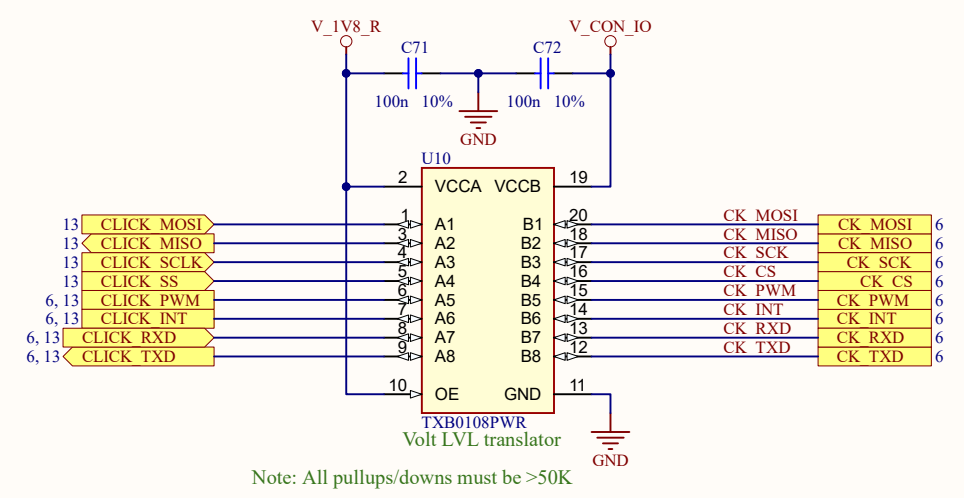
REVISION	DESCRIPTION	DATE	APPROVED



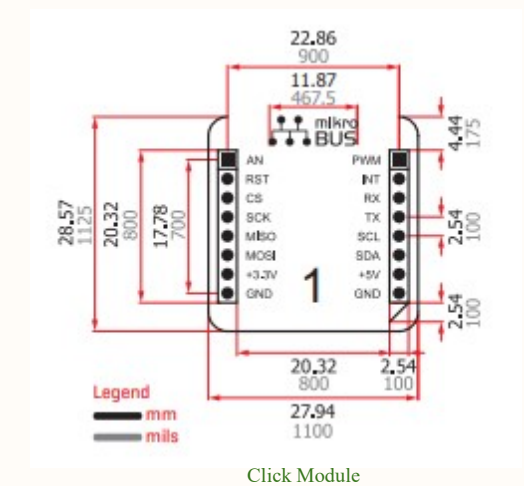
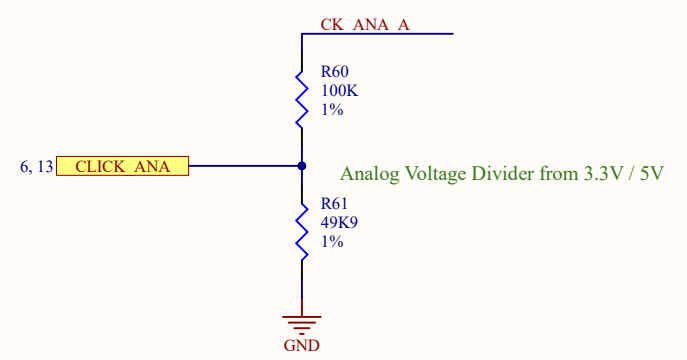
LVL translator on "Headers" page



Layout in accordance to Click Module

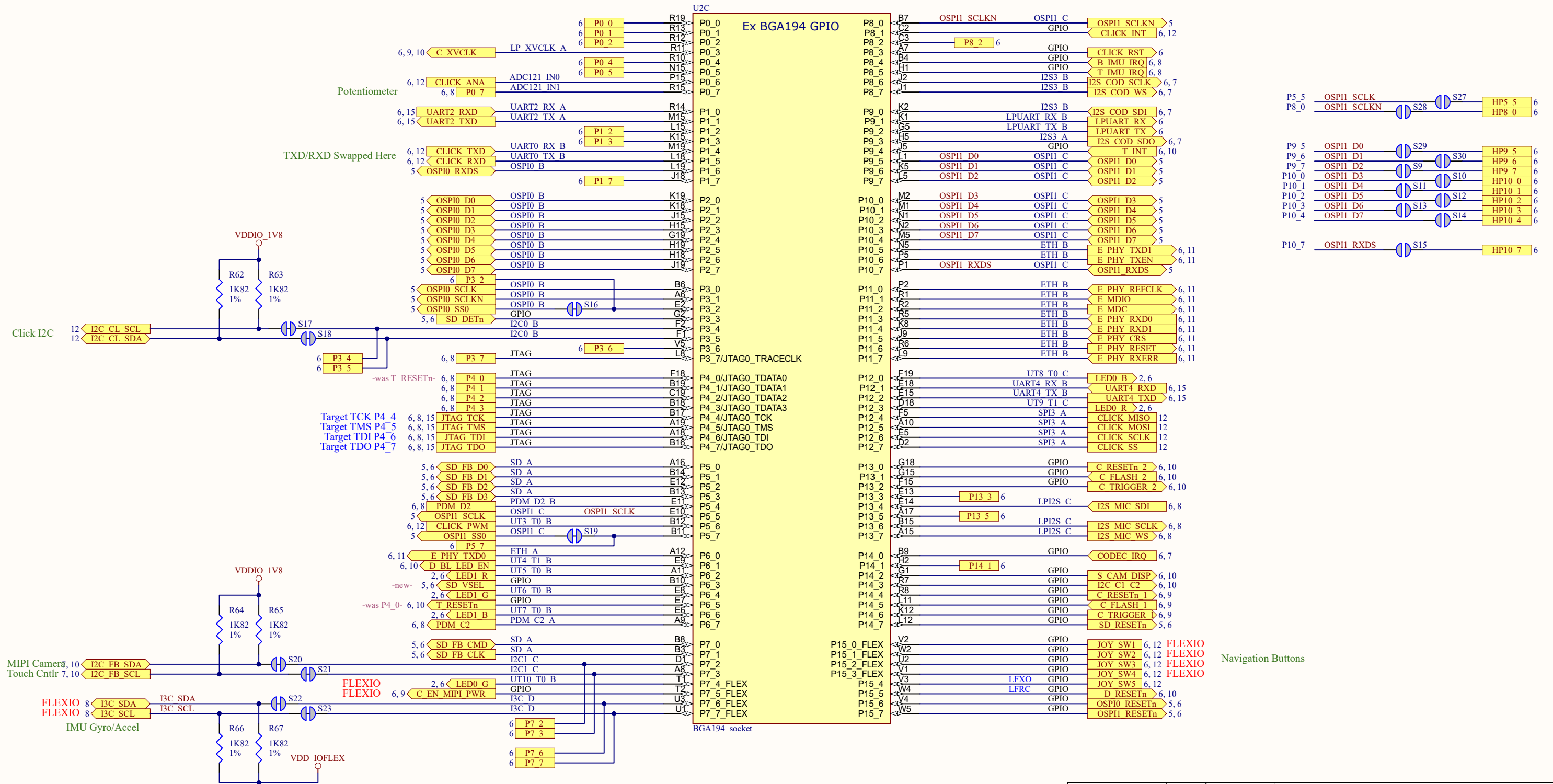


Note: All pullups/downs must be >50K



APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
ENG: K Braun	--/--	00319	Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA	
DSN: K Braun	--/--		TITLE	
CHK: n/a	--/--		EAGLE DEV KIT	
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.
BOM: 250-00319		B	none	220-00319
ASSY DWG: 120-00319		SCALE:	FILE NAME	REV
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PCB DWG: 110-00319		SHEET 12 OF 15		

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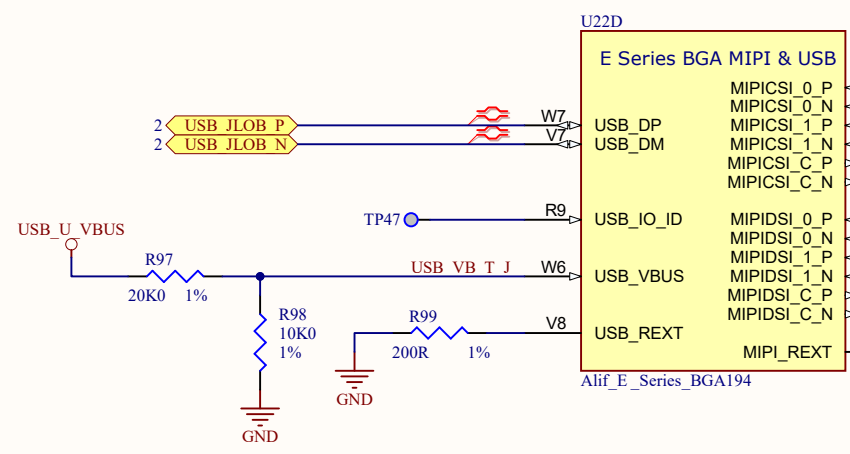
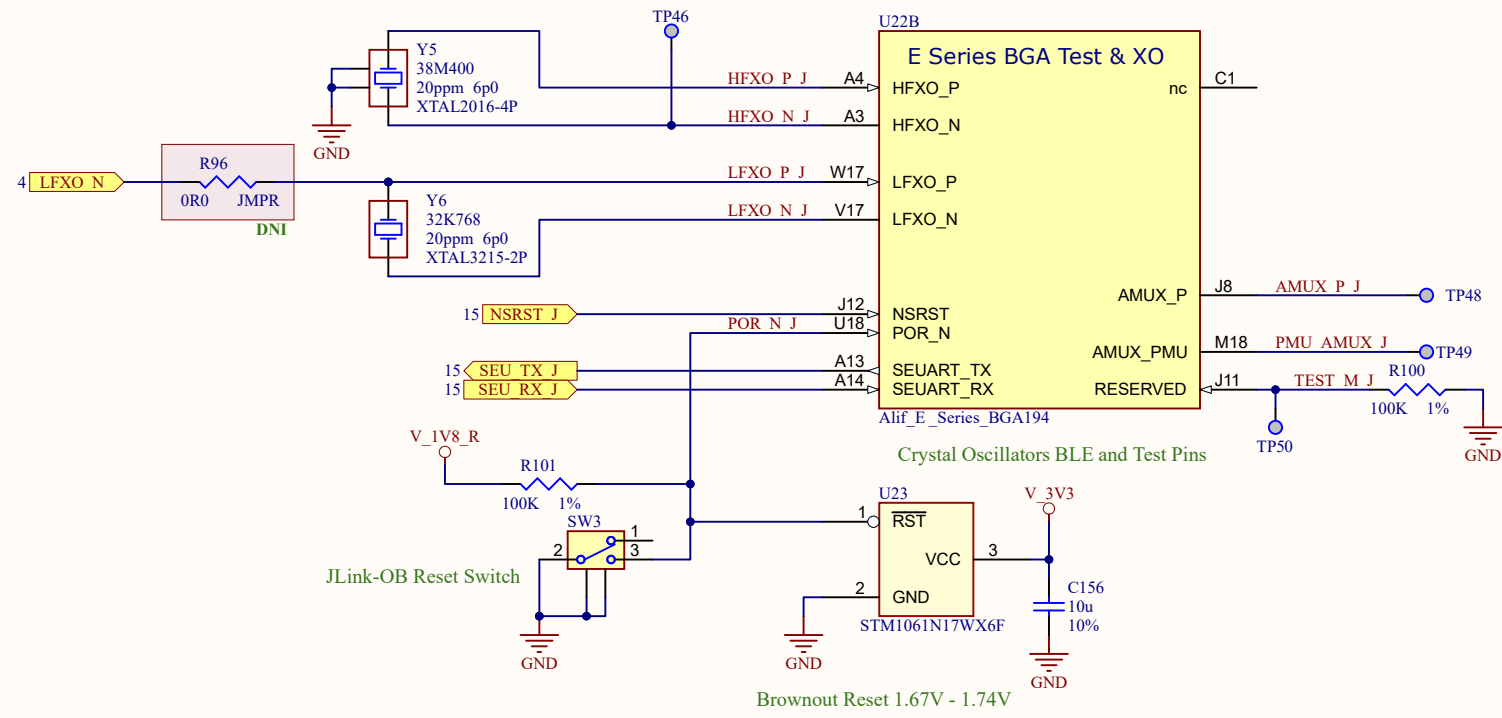
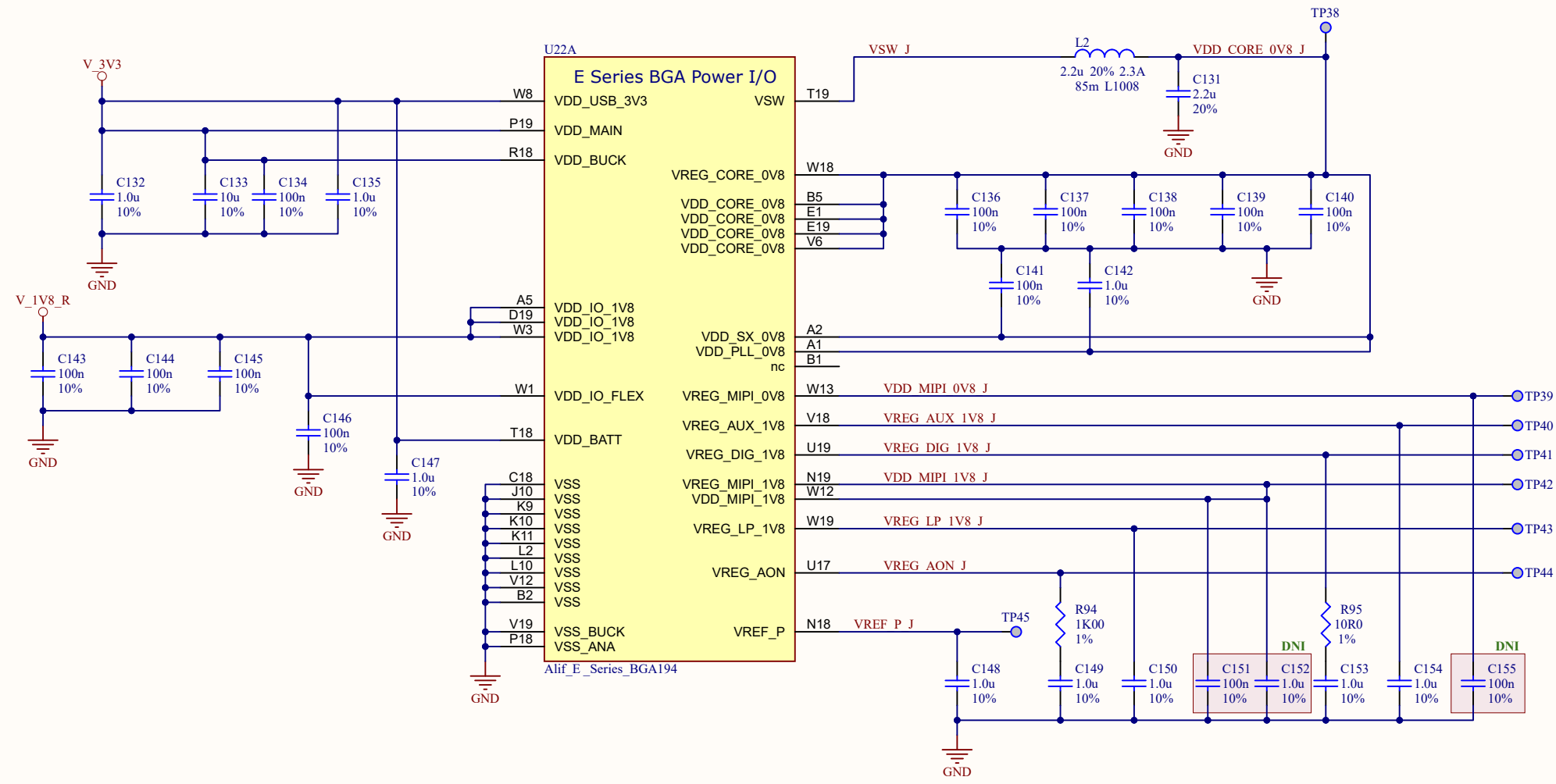


Navigation Buttons

APPROVALS	DATE	PROJECT	<p>Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA</p>
ENG: K Braun	--/--	00319	
DSN: K Braun	--/--		
CHK: n/a	--/--		
REFERENCE DOCUMENTS			TITLE
BOM: 250-00319	EAGLE DEV KIT		
ASSY DWG: 120-00319	SIZE	CAGE CODE	DWG NO.
FAB DWG: 210-00319	B	none	220-00319
PCB DWG: 110-00319	SCALE: none	FILE NAME	13-CPU_GPIO.SchDoc
			SHEET 13 OF 15

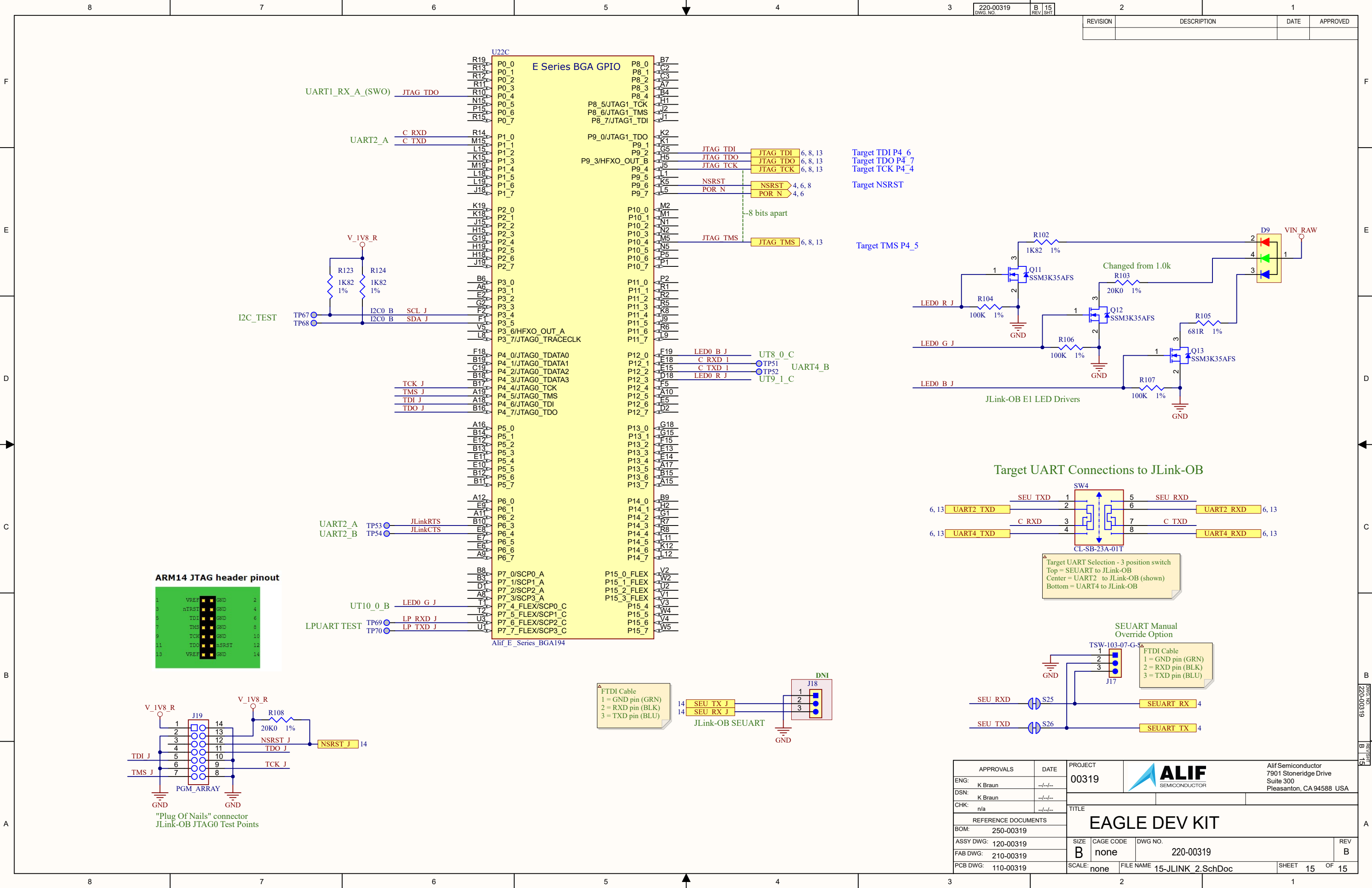
JLink-OB E1 CPU Power Supplies

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA		
ENG: K Braun	--/--	00319				
DSN: K Braun	--/--		EAGLE DEV KIT			
CHK: n/a	--/--					
REFERENCE DOCUMENTS			SIZE	CAGE CODE	DWG NO.	REV
BOM: 250-00319			B	none	220-00319	B
ASSY DWG: 120-00319			SCALE: none	FILE NAME	14-JLINK_1.SchDoc	SHEET 14 OF 15
FAB DWG: 210-00319						
PCB DWG: 110-00319						

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA		
ENG: K Braun	--/--	00319	EAGLE DEV KIT				
DSN: K Braun	--/--						
CHK: n/a	--/--						
REFERENCE DOCUMENTS							
BOM: 250-00319	ASSY DWG: 120-00319	FAB DWG: 210-00319	PCB DWG: 110-00319	SIZE: B	CAGE CODE: none	DWG NO.: 220-00319	REV: B
TITLE			SCALE: none	FILE NAME: 15-JLINK_2.SchDoc	SHEET: 15 OF 15		

DWG. NO. 220-00319 REV. SHT B 15