Agilex™ 5 FPGAs and SoCs Device Overview

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2024.01.12

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1. Overview of the Intel Agilex® 5 FPGAs and SoCs

The Intel Agilex® 5 FPGA product family extends the innovations of the Intel Agilex FPGA portfolio to midrange FPGA applications. The Intel Agilex 5 FPGAs and SoCs serve a broad range of applications that require high performance, lower power consumption, smaller form factor, and lower logic densities.

- First enhanced DSP with AI Tensor block in the industry—delivers high-efficiency artificial intelligence (AI) and digital signal processing (DSP)
- First asymmetric applications processor system in the FPGA industry—a combination of a dual-core Arm* Cortex*-A76 and a dual-core Arm Cortex-A55 processors enables you to optimize the performance and power efficiency of processing workloads
- Monolithic die architecture—provides higher system integration and lower power with smaller form factor packages
- Advanced connectivity features:
  - High-speed GTS transceivers up to 28.1 Gbps
  - PCI Express* (PCIe*) 4.0 ×8 support
  - DDR external memory interface up to 4,000 Mbps DDR5
  - General purpose I/Os supporting voltages from 1.0 V to 3.3 V

The Intel Agilex 5 FPGA product family delivers on average 50% higher fabric performance and up to 42% lower total power consumption compared to previous generation Intel® FPGAs. To achieve this improvement, the product family leverages these key innovations and techniques:

- Advanced Intel 7 technology
- Second generation Intel Hyperflex® FPGA architecture
- High level of system integration
- SmartVID and fixed low core voltage device options
- Power islands, power gating, and other power reduction techniques

These capabilities and advanced features make the Intel Agilex 5 FPGA product family ideal for midrange FPGA applications across the edge and core. The applications span across many segments including wireless and wireline communications, video and broadcast equipments, industrial, test and measurement, medical electronics, data centers, and defense.

Note: The information contained in this document is preliminary and subject to change.

Related Information

Intel Agilex 5 FPGA and SoC FPGA on the Intel website
Provides the latest information about Intel Agilex 5 devices.

1.1. Key Features and Innovations in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs tier consists of the performance-optimized D-Series FPGAs and the power-optimized E-Series FPGAs.

Table 1. Intel Agilex 5 FPGAs and SoCs Series

Feature and Innovation	D-Series FPGA	E-Series FPGA	
		Device Group A	Device Group B
Process technology	Intel 7		
Architecture	Monolithic die		
Packaging	Variable Pitch BGA (VPBGA) package with minimum ball pitch of 0.65 mm(1) for smaller form factor and to help reduce the number of PCB layers	VPBGA package with minimum ball pitch of 0.65 mm(1) for smaller form factor and to help reduce the number of PCB layers	• VPBGA package with minimum ball pitch of 0.65 mm(1) for smaller form factor and to help reduce the number of PCB layers • Rectangular package and standard pattern ball array with smaller ball pitch of 0.5 mm for smaller form factor
Core fabric	Second generation Intel Hyperflex core fabric		
Logic elements	103 thousand to 644 thousand	138 thousand to 656 thousand	50 thousand to 656 thousand
On-chip RAM	MLAB and M20K		
	69 Mb	38 Mb	38 Mb
Variable precision DSP	Industry-leading digital signal processing (DSP) support with up to 38 TFLOPS		
AI Tensor block	Yes		
Clocking and PLL	• Programmable clock tree synthesis for flexible, low power, and low skew clocking • I/O PLL supports integer mode with precise frequency synthesis for general purpose I/O, external memory interfaces, LVDS, and fabric usage • Transmit PLL (TX PLL) supports fractional synthesis and ultra-low jitter with LC tank-based PLL for transceiver usage.		
General Purpose I/Os	• 1.0 V to 1.3 V high-speed I/O (HSIO) • 1.8 V to 3.3 V high-voltage I/O (HVIO)		
MIPI* D-PHY* v2.5	Up to 3.5 Gbps(2) per lane	Up to 3.5 Gbps(2) per lane	Up to 2.5 Gbps(3) per lane
External memory interface	Fourth generation scalable integrated hard memory controllers and PHY		
	• 3,200 Mbps DDR4 • 4,000 Mbps DDR5 • 4,267 Mbps LPDDR4 • 4,267 Mbps LPDDR5	• 2,667 Mbps DDR4 • 3,600 Mbps DDR5 • 3,733 Mbps LPDDR4 • 3,733 Mbps LPDDR5	• 2,400 Mbps DDR4 • 2,667 Mbps LPDDR4 • 2,400 Mbps LPDDR5
Cryptography	SDM supports Advanced Encryption Standard (AES)		
Transceiver hard IPs	• Multiple Gigabit Ethernet (GbE) network interface connectivity in one device • PCS and PCIe hard IPs free up valuable core logic resources, save power, and increase your productivity		

continued...

(1) 0.65 mm is the minimum ball pitch and is not meant for signal trace routing. The VPBGA design meets the 0.8 mm design rules and the use of standard plated through hole (PTH) via.

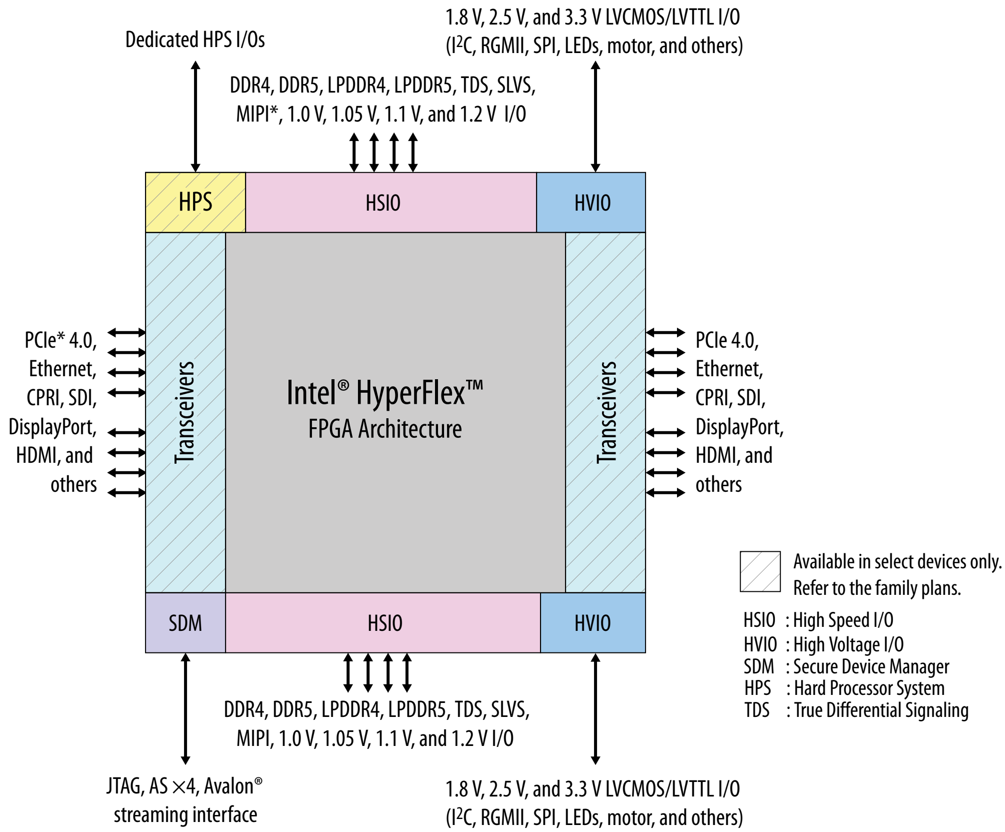
Feature and Innovation	D-Series FPGA	E-Series FPGA	
		Device Group A	Device Group B
	• Hardened 10 and 25 GbE media access control (MAC), physical coding sublayer (PCS), and forward error correction (FEC) with IEEE 1588 support • Up to 28.1 Gbps non-return-to-zero (NRZ) • Up to PCIe 4.0 ×8	• Hardened 10 and 25 GbE MAC, PCS, and FEC with IEEE 1588 support • Up to 28.1 Gbps NRZ • PCIe 4.0 ×4	• Hardened 10 GbE MAC, PCS, and FEC with IEEE 1588 support • Up to 17.16 Gbps NRZ • Up to PCIe 4.0 ×4
SDM	Dedicated secure device manager (SDM) that: • Manages FPGA configuration process and all security features • Performs authenticated FPGA configuration and HPS boot • Supports FPGA bitstream encryption, secure key provisioning, and physically unclonable function (PUF) key storage • Manages runtime sensors and supports active tamper detection and responses • Supports platform attestation using the security protocol and data model (SPDM) protocol • Provides access to hardened cryptographic engines as a service		
HPS (SoCs only)	Hard processor system (HPS) with embedded multicore Arm processors: • Dual-core 64-bit Arm Cortex-A76 up to 1.8 GHz • Dual-core 64-bit Arm Cortex-A55 up to 1.5 GHz		
Power saving	Comprehensive set of advanced power saving features that deliver up to 40% lower power compared to previous generation high-performance FPGAs		

(2) Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel.

(3) Up to 2.5 Gbps for standard reference and long reference channels.

1.2. Intel Agilex 5 FPGAs and SoCs Block Diagram

Figure 1. Intel Agilex 5 FPGAs and SoCs Block Diagram



Related Information

Intel Agilex 5 FPGAs and SoCs Family Plan on page 13

1.3. Intel Agilex 5 FPGAs and SoCs Summary of Features

The Intel Agilex 5 FPGAs and SoCs share the same high performance core fabric and common features.

Table 2. Feature Summary

<table>
<tr><th>Feature</th><th colspan="3">Description</th></tr>
<tr><td rowspan="2">Packaging</td><td colspan="3">• Multiple devices with identical package footprints allows seamless migration across different device densities
• Variable Pitch BGA (VPBGA) package design with minimum ball pitch of 0.65 mm[4] for smaller package form factor and to help reduce the number of PCB layers</td></tr>
<tr><td>E-Series</td><td colspan="2">0.5 mm ball pitch package option for small form-factor with more I/O counts</td></tr>
<tr><td>High performance core fabric</td><td colspan="3">• Second Generation Intel Hyperflex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks
• Enhanced adaptive logic module (ALM)
• Improved multi-track routing architecture reduces congestion and improves compile times
• Hierarchical core clocking architecture with programmable clock tree synthesis
• Fine-grained partial reconfiguration</td></tr>
<tr><td>Internal memory blocks</td><td colspan="3">• Multi-level on-chip memory hierarchy
• M20K—20 kilobits with hard error correction code (ECC) support
• MLAB—640-bit distributed LUTRAM</td></tr>
<tr><td>Variable precision DSP blocks</td><td colspan="3">• Variable precision DSP blocks with hard IEEE 754-compliant floating-point units, including support for:
— Single-precision FP32 (32-bit arithmetic)
— Half-precision FP16 (16-bit arithmetic) and FP19 (19-bit arithmetic) floating point modes
— Tensor floating point FP19 floating point modes
— BFLOAT16 floating-point format
• High-performance AI Tensor blocks:
— Enables high-performance compute density of FPGA fabric Tera Operations Per Second (TOPS)
— Up to 57 INT8 TOPS for AI workloads
— Hardware programmable for AI with customized workloads
— Supports push-button flow from industry standard frameworks, such as TensorFlow*, to FPGA bitstream
• Every DSP block supports INT16 complex multiplication mode
• Supports signal processing with precision ranging from 9×9 up to 54×54
• Native 27×27, 18×19, and 9×9 multiplication modes
• 64-bit accumulator and cascade for systolic 200 GbE finite impulse responses (FIRs)
• Internal coefficient memory banks
• Pre-adder/subtractor improves efficiency
• 2× additional pipeline register increases performance and reduces power consumption</td></tr>
<tr><td rowspan="3">Core clock networks</td><td colspan="3">• Programmable clock tree synthesis—backwards compatible with global, regional and peripheral clock networks
• Synthesize clocks where needed only—minimizes dynamic power
• 800 MHz LVDS interface clocking—supports 1,600 Mbps LVDS interface through the 1.3 V TDS standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards</td></tr>
<tr><td>D-Series</td><td colspan="2">2,000 MHz external memory interface clocking, supports 4,000 Mbps DDR5 interface</td></tr>
<tr><td>E-Series</td><td>Device Group A</td><td>1,800 MHz external memory interface clocking, supports 3,600 Mbps DDR5 interface</td></tr>
</table>

continued...

[4] 0.65 mm is the minimum ball pitch and is not meant for signal trace routing. The VPBGA design meets the 0.8 mm design rules and the use of standard plated through hole (PTH) via.

<table>
<tr><th colspan="2">Feature</th><th colspan="3">Description</th></tr>
<tr><td colspan="2"></td><td></td><td>Device Group B</td><td>1,200 MHz external memory interface clocking, supports 2,400 Mbps DDR4 interface</td></tr>
<tr><td rowspan="9">General purpose I/Os</td><td rowspan="3">General</td><td colspan="3">• 1.6 Gbps 1.3 V TDS standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards
• 1.0 V, 1.05 V, 1.1 V, and 1.2 V single-ended LVCMOS interfacing
• 1.8 V, 2.5 V, and 3.3 V single-ended LVCMOS/LVTTL I/O
• On-chip termination (OCT)</td></tr>
<tr><td>D-Series</td><td colspan="2">Over 400 total GPIOs available</td></tr>
<tr><td>E-Series</td><td colspan="2">Over 500 total GPIOs available</td></tr>
<tr><td rowspan="3">External memory interface
(Hard IP)</td><td>D-Series</td><td colspan="2">• 2,000 MHz (4,000 Mbps) DDR5 external memory interface
• 2,133 MHz (4,267 Mbps) LPDDR5 external memory interface
• 1,600 MHz (3,200 Mbps) DDR4 external memory interface
• 2,133 MHz (4,267 Mbps) LPDDR4/4X external memory interface</td></tr>
<tr><td rowspan="2">E-Series</td><td>Device Group A</td><td>• 1,800 MHz (3,600 Mbps) DDR5 external memory interface
• 1,867 MHz (3,733 Mbps) LPDDR5 external memory interface
• 1,333 MHz (2,667 Mbps) DDR4 external memory interface
• 1,867 MHz (3,733 Mbps) LPDDR4 external memory interface</td></tr>
<tr><td>Device Group B</td><td>• 1,200 MHz (2,400 Mbps) DDR4 external memory interface
• 1,333 MHz (2,667 Mbps) LPDDR4 external memory interface
• 1,200 MHz (2,400 Mbps) LPDDR5 external memory interface</td></tr>
<tr><td rowspan="3">MIPI</td><td>D-Series</td><td colspan="2">MIPI D-PHY v2.5 at up to 3.5 Gbps(5) per lane</td></tr>
<tr><td rowspan="2">E-Series</td><td>Device Group A</td><td>MIPI D-PHY v2.5 at up to 3.5 Gbps(5) per lane</td></tr>
<tr><td>Device Group B</td><td>MIPI D-PHY v2.5 at up to 2.5 Gbps(6) per lane</td></tr>
<tr><td rowspan="3">Phase locked loops (PLL)</td><td>I/O PLL</td><td colspan="3">• Integer PLLs adjacent to general purpose I/Os
• Precision frequency synthesis
• Clock delay compensation
• Zero-delay buffering
• Support external memory and LVDS-compatible interface</td></tr>
<tr><td>Transmit PLLs (TX PLLs)</td><td colspan="3">• Precise fractional synthesis
• Ultra low jitter with LC tank-based PLL
• Supports transceiver interfaces</td></tr>
<tr><td>System PLL</td><td colspan="3">• One System PLL per GTS transceiver bank
• Integer mode
• Precision frequency synthesis
• Supports transceiver-to-fabric interface
• You can repurpose the System PLL for core usage if it is not used by the GTS transceiver</td></tr>
<tr><td colspan="2">Memory controller support</td><td colspan="3">Multiple hard IP instantiations in each device</td></tr>
<tr><td colspan="5" align="right">continued...</td></tr>
</table>

(5) Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel.

(6) Up to 2.5 Gbps for standard reference and long reference channels.

Feature		Description		
		D-Series	• DDR4 hard memory controller • LPDDR4/4X hard memory controller • DDR5 hard memory controller • LPDDR5 hard memory controller	
		E-Series	Device Group A	• DDR4 hard memory controller • LPDDR4 hard memory controller • DDR5 hard memory controller • LPDDR5 hard memory controller
			Device Group B	• DDR4 hard memory controller • LPDDR4 hard memory controller • LPDDR5 hard memory controller
Transceivers	PCIe	PCIe rates up to PCIe 4.0, 16 Gbps NRZ		
	Networking	• Insertion loss compliant to 802.3bj and CEI 25G-LR standards • Oversampling capability for data rates below 1 Gbps • SFP+ optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic reconfiguration of individual GTS transceiver channels • On-chip instrumentation (Intel Quartus® Prime Eye Viewer with non-destructive eye height and destructive eye width margining)		
		D-Series	Continuous operating range of 1 Gbps to 28.1 Gbps NRZ	
		E-Series	Device Group A	Continuous operating range of 1 Gbps to 28.1 Gbps NRZ
			Device Group B	Continuous operating range of 1 Gbps to 17.16 Gbps NRZ
Transceiver hard IP	PCIe	• Multiple hard IP instantiations in each device • TLP bypass feature • Single-root I/O virtualization (SR-IOV) • Precise time management		
		D-Series	• Up to PCIe 4.0 ×8 EP and RP • Port bifurcation support: 4×8 root port or endpoint, or (4×4)+(4×4) root port or endpoint	
		E-Series	• Up to PCIe 4.0 ×4 EP and RP • 6 × 4 endpoint or root ports	
	Other protocols	• CPRI and fibre channel • CR/KR (AN/LT) • 1588 PTP • MAC, PCS, and FEC bypass options		
		D-Series	Ethernet IP configuration: 16× 10 or 25 GbE MAC, PCS, and FEC	
		E-Series	Device Group A	Ethernet IP configuration: 6 × 10 or 25 GbE MAC, PCS, and FEC
			Device Group B	Ethernet IP configuration: 6 × 10 GbE MAC, PCS, and FEC
Configuration		• Dedicated SDM • Software-programmable device configuration • Serial flash interface • Configuration from parallel flash through external host		

continued...

Feature	Description
	• Fine-grained partial reconfiguration of core fabric—add or remove system logic while the device is operating • Dynamic reconfiguration of GTS transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators • PUF service • Platform attestation • Anti-tamper features • Configuration via protocol (CvP) using PCIe 1.0, 2.0, 3.0, or 4.0
Functional safety	• Functional Safety Data Package (FSDP) • Improved FPGA diagnostic measures enable use of Intel Agilex 5 FPGAs in safety-critical applications
Software and tools	• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • New compile innovations in each Intel oneAPI release • Transceiver toolkit • Platform Designer IP integration tool • Intel DSP Builder for Intel FPGAs advanced blockset • Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA)

1.4. Additional Features for Intel Agilex 5 SoCs

In addition to the common features of the Intel Agilex 5 FPGAs and SoCs, the Intel Agilex 5 SoCs provide additional features.

Table 3. Features Specific to Intel Agilex 5 SoCs

SoC Subsystem	Feature	Description
HPS	Multiprocessor unit core	• Multicore Arm processors, including dual-core Arm Cortex-A76 MPCore and dual-core Arm Cortex-A55 MPCore processors, with Arm CoreSight* debug and trace technology • Scalar floating-point unit supporting single and double precision • Arm Neon* technology media processing engine for each processor
	System controllers	• System memory management unit (SMMU) • Cache coherency unit (CCU)
	Cache	• Arm Cortex-A76: — Level 1 cache per core: • 64 kilobytes (KB) L1 instruction cache with parity • 64 KB L1 data cache with ECC — Level 2 cache per core: Unified 256 KB L2 data and instructions cache with ECC • Arm Cortex-A55: — Level 1 cache per core: • 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC — Level 2 cache per core: Unified 128 KB L2 data and instructions cache with ECC • Shared level 3 cache: 2 megabytes (MB) L3 cache
	On-chip memory	512 KB on-chip RAM
	Direct memory access (DMA)	Eight-channel DMA controller

continued...

SoC Subsystem	Feature	Description
	Ethernet MAC (TSN)	• Three 10 Mbps/100 Mbps/1 Gbps/2.5 Gbps Ethernet MACs with integrated DMA and Time-Sensitive Networking (TSN) support • 1 Gbps and 2.5 Gbps (2.5 Gbps requires soft paths to the transceivers)
	USB	• One USB 2.0 On-The-Go (OTG) with integrated DMA • One USB 3.1 Gen 1
	UART	Two UART 16550-compatible controllers
	Serial peripheral interface (SPI) controller	Four SPI (two masters and two slaves)
	I^2C	Five I^2C controllers
	I^3C	Two I^3C controllers
	SD/SDIO/eMMC controller	• SD/eMMC devices up to version 5.1 • SD devices up to version 6.1 • SDIO devices up to version 4.1
	NAND flash controller	• One ONFI 1.x and 2.x • 8 bit and 16 bit support • Compatible with Toggle 1.x and 2.x specifications
	GPIO	Maximum of 48 software-programmable GPIOs
	Timers	• Four general-purpose timers • Five watchdog timers
SDM		• Secure boot • AES encryption • Secure Hash Algorithms (SHA) and Elliptic Curve Digital Signature Algorithm (ECDSA) authentications
External memory interface		Hard memory controllers: • D-Series—DDR4, DDR5, LPDDR4, and LPDDR5 • E-Series: — Device Group A—DDR4, DDR5, LPDDR4, and LPDDR5 — Device Group B—DDR4, LPDDR4, and LPDDR5

2. Intel Agilex 5 FPGAs and SoCs Family Plan

The Intel Agilex 5 FPGAs and SoCs are available as D-Series and E-Series FPGAs with different features to fit your application requirements.

Note:

- The tables in the following sections are preliminary and subject to change.
- The resource counts vary by package options.
- The performance specifications vary by speed grades.
- The HPS and GTS transceivers are available only for specific ordering part numbers.

Related Information

Intel Agilex 5 FPGAs and SoCs Family Plan on page 13

2.1. Intel Agilex 5 FPGAs and SoCs D-Series

Table 4. D-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device	Logic Element	M20K		MLAB		DSP	
		Count	Size (Mb)	Count	Size (Mb)	18×19 Multiplier	Peak INT8 (TOPS [7])
A5D 010	103,250	534	10.43	1,780	1.09	552	8.48
A5D 025	254,054	1,281	25.02	3,420	2.09	1,472	22.61
A5D 031	318,600	1,602	31.29	5,400	3.30	1,840	28.26
A5D 051	515,070	2.563	50.06	8,440	5.15	2,944	45.22
A5D 064	644,280	3,204	62.58	10,920	6.67	3,680	56.22

(7) Tera Operations Per Second

Table 5. D-Series FPGA Family Plan—I/Os and Interfaces

The values in this table are maximum resources or performance.

Device	HVIO (1.8 V–3.3 V)	HSIO (1.0 V–1.3 V)	PLL Count		1.3 V LVDS Pairs at 1.6 Gbps	External Memory Interface		MIPI D-PHY Interface
			I/O PLL	Fabric-Feeding I/O PLL(8)		DDR4 (×64)	DDR4, DDR5, LPDDR4,LPDDR5 (×32)	
A5D 010	60	384	8	11	192	2	4	28
A5D 025	60	384	8	11	192	2	4	28
A5D 031	60	384	8	11	192	2	4	28
A5D 051	60	384	8	15	192	2	4	28
A5D 064	60	384	8	15	192	2	4	28

Table 6. D-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device	Transceiver 28.1 Gbps Max. Rate	PCIe 4.0 Instance		10/25 Gigabit Ethernet (MAC & PCS)	HPS	
		×4	×8		Processor	Cache Size
A5D 010	16	4	2	8	• Dual core Arm Cortex-A76 up to 1.8 GHz • Dual core Arm Cortex-A55 up to 1.5 GHz	• Shared: 2 MB L3 • Cortex-A76: — 64 KB L1 — 256 KB L2 • Cortex-A55: — 32 KB L1 — 128 KB L2
A5D 025	16	4	2	8		
A5D 031	16	4	2	8		
A5D 051	24	6	3	12		
A5D 064	32	8	4	16		

Related Information

Variable Pitch BGA (VPBGA) Package Design of Intel Agilex 5 FPGAs and SoCs on page 41

2.2. Intel Agilex 5 FPGAs and SoCs E-Series

Table 7. E-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device Group Type	Device	Logic Element	M20K		MLAB		DSP	
			Count	Size (Mb)	Count	Size (Mb)	18×19 Multipliers	Peak INT8 (TOPS(9))
Device Group A	A5E 013A	138,060	358	6.99	2,340	1.43	376	5.78
	A5E 028A	282,256	716	13.98	4.784	2.92	752	11.55

continued...

(8) The fabric-feeding I/O PLL counts include the System PLL in the GTS transceiver banks. You can use the System PLL for core fabric usage if you do not use it for the transceiver.

(9) Tera Operations Per Second

Device Group Type	Device	Logic Element	M20K		MLAB		DSP	
			Count	Size (Mb)	Count	Size (Mb)	18×19 Multipliers	Peak INT8 (TOPS(9))
	A5E 043A	434,240	1,050	20.51	6,720	4.10	1,128	17.33
	A5E 052A	523,920	1,288	25.16	8,440	5.15	1,352	20.78
	A5E 065A	656,080	1,611	31.46	11,120	6.79	1,692	25.99
Device Group B	A5E 005B	50,445	130	2.54	850	0.52	130	1.70
	A5E 007B	69,030	179	3.50	1,170	0.71	188	2.46
	A5E 008B	85,196	229	4.47	1,780	1.09	232	3.05
	A5E 013B	138,060	358	6.99	2,340	1.43	376	4.93
	A5E 028B	282,256	716	13.98	4,784	2.92	752	9.85
	A5E 043B	434,240	1,050	20.51	6,720	4.10	1,128	14.78
	A5E 052B	523,920	1,288	25.16	8,440	5.15	1,352	17.72
	A5E 065B	656,080	1,611	31.46	11,120	6.79	1,692	22.17

Table 8. E-Series FPGA Family Plan—I/Os and Interfaces

The values in this table are maximum resources or performance.

Device Group Type	Device	HVIO (1.8 V–3.3 V)	HSIO (1.0 V–1.3 V)	PLL Count		1.3 V LVDS Pairs at 1.6 Gbps	DDR4, DDR5(10), LPDDR4, LPDDR5 Interface (×32)	MIPI D-PHY Interface
				I/O PLL	Fabric-Feeding I/O PLL(11)			
Device Group A	A5E 013A	200	192	4	8	96	2	14
	A5E 028A	200	192	4	10	96	2	14
	A5E 043A	120	384	8	13	192	4	28
	A5E 065A	120	384	8	13	192	4	28
	A5E 052A	120	384	8	13	192	4	28
Device Group B	A5E 005B	160	96	2	5	48	1	7
	A5E 007B	160	96	2	5	48	1	7
	A5E 008B	200	192	4	8	96	2	14
	A5E 013B	200	192	4	8	96	2	14
	A5E 028B	200	192	4	10	96	2	14

continued...

(9) Tera Operations Per Second

(10) Applicable only to E-Series Device Group A FPGAs.

(11) The fabric-feeding I/O PLL counts include the System PLL in the GTS transceiver banks. You can use the System PLL for core fabric usage if you do not use it for the transceiver.

Device Group Type	Device	HVIO (1.8 V–3.3 V)	HSIO (1.0 V–1.3 V)	PLL Count		1.3 V LVDS Pairs at 1.6 Gbps	DDR4, DDR5[10], LPDDR4, LPDDR5 Interface (×32)	MIPI D-PHY Interface
				I/O PLL	Fabric-Feeding I/O PLL[11]			
	A5E 043B	120	384	8	13	192	4	28
	A5E 052B	120	384	8	13	192	4	28
	A5E 065B	120	384	8	13	192	4	28

Table 9. E-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device Group Type	Device	Transceiver[12]	PCIe 4.0 ×4	Gigabit Ethernet[13] (MAC & PCS)	HPS	
					Processor	Cache Size
Device Group A	A5E 013A	4	1	1	• Dual core Arm Cortex-A76 up to 1.8 GHz • Dual core Arm Cortex-A55 up to 1.5 GHz	• Shared: 2 MB L3 • Cortex-A76: — 64 KB L1 — 256 KB L2 • Cortex-A55: — 32 KB L1 — 128 KB L2
	A5E 028A	12	3	3		
	A5E 052A	24	6	4		
	A5E 065A	24	6	6		
	A5E 043A	16	4	4		
Device Group B	A5E 005B	—	—	—	—	—
	A5E 007B	—	—	—	—	—
	A5E 008B	4	1	1	• Dual core Arm Cortex-A76 up to 1.4 GHz • Dual core Arm Cortex-A55 up to 1.25 GHz	• Shared: 2 MB L3 • Cortex-A76: — 64 KB L1 — 256 KB L2 • Cortex-A55: — 32 KB L1 — 128 KB L2
	A5E 013B	4	1	1		
	A5E 028B	12	3	3		
	A5E 043B	16	4	4		
	A5E 052B	24	6	6		
	A5E 065B	24	6	6		

(10) Applicable only to E-Series Device Group A FPGAs.

(11) The fabric-feeding I/O PLL counts include the System PLL in the GTS transceiver banks. You can use the System PLL for core fabric usage if you do not use it for the transceiver.

(12) E-Series Device Group A FPGAs: 28.1 Gbps maximum rate. E-Series Device Group B FPGAs: 17.16 Gbps maximum rate.

(13) E-Series Device Group A FPGAs: 10/25 GbE. E-Series Device Group B FPGAs: 10 GbE.

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2.3. Intel Agilex 5 FPGAs and SoCs Package Options

In the following figures:

- The arrows indicate the package migration paths. The shades represent the devices included in each path.
- To achieve full I/O migration across devices in the same migration path, restrict I/Os and transceivers utilization to match the device with the lowest I/O and transceiver counts.
- For more information about the device migration path, refer to the *AN 979: Intel Agilex 5 FPGAs and SoCs Device Migration Guidelines: E-Series* (Intel RDC item #784351) application note.

Figure 2. Package Options, Migrations, and I/O Pins—D-Series

Series	Device	Package Key: HVIO / HSIO / LVDS / Transceivers	
		Minimum Ball Pitch: 0.65 mm Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA	
		B23A 820-pin VPBGA 23 mm × 23 mm	**B32A** 1610-pin VPBGA 32 mm × 32 mm
D-Series	A5D 010	60 / 192 / 96 / 8	60 / 384 / 192 / 16
	A5D 025	60 / 192 / 96 / 8	60 / 384 / 192 / 16
	A5D 031	60 / 192 / 96 / 8	60 / 384 / 192 / 16
	A5D 051		60 / 384 / 192 / 24
	A5D 064		60 / 384 / 192 / 32

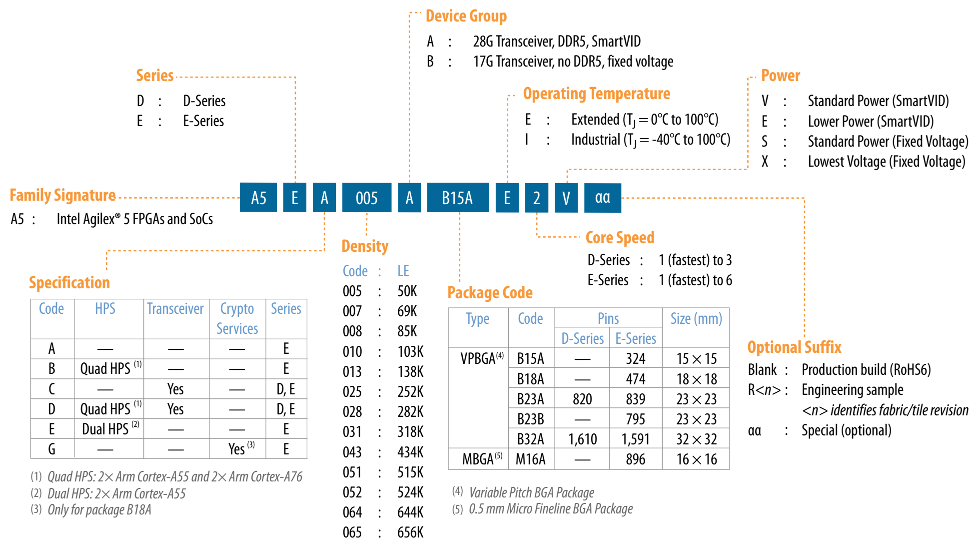
Figure 3. Package Options, Migrations, and I/O Pins—E-Series

Series		Device	Package Key: HVIO / HSIO / LVDS / Transceivers					
			Ball Pitch: 0.5 mm Grid Array Pattern: Standard MBGA: Micro Fineline BGA	Minimum Ball Pitch: 0.65 mm Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA				
			M16A 896-pin MBGA 16 mm × 16 mm	**B15A** 324-pin VPBGA 15 mm × 15 mm	**B18A** 474-pin VPBGA 18 mm × 18 mm	**B23B** 795-pin VPBGA 23 mm × 23 mm	**B23A** 839-pin VPBGA 23 mm × 23 mm	**B32A** 1591-pin VPBGA 32 mm × 32 mm
E-Series	Device Group A	A5E 013A					120 / 96 / 48 / 4	200 / 192 / 96 / 4
		A5E 028A					120 / 96 / 48 / 12	200 / 192 / 96 / 12
		A5E 043A					120 / 96 / 48 / 12	120 / 384 / 192 / 16
		A5E 052A					120 / 96 / 48 / 12	120 / 384 / 192 / 24
		A5E 065A					120 / 96 / 48 / 12	120 / 384 / 192 / 24
	Device Group B	A5E 005B		80 / 62 / 31 / 0	160 / 48 / 24 / 0	160 / 96 / 48 / 0		
		A5E 007B		80 / 62 / 31 / 0	160 / 48 / 24 / 0	160 / 96 / 48 / 0		
		A5E 008B	40 / 192 / 96 / 4			160 / 192 / 96 / 0	120 / 96 / 48 / 4	200 / 192 / 96 / 4
		A5E 013B	40 / 192 / 96 / 4			160 / 192 / 96 / 0	120 / 96 / 48 / 4	200 / 192 / 96 / 4
		A5E 028B	40 / 192 / 96 / 8			160 / 192 / 96 / 0	120 / 96 / 48 / 12	200 / 192 / 96 / 12
		A5E 043B					120 / 96 / 48 / 12	120 / 384 / 192 / 16
		A5E 052B					120 / 96 / 48 / 12	120 / 384 / 192 / 24
		A5E 065B					120 / 96 / 48 / 12	120 / 384 / 192 / 24

Note: For the VPBGA packages, 0.65 mm is the minimum ball pitch and is not meant for signal trace routing. The VPBGA design meets the 0.8 mm design rules and the use of standard plated through hole (PTH) via.

2.4. Available Options

Figure 4. Intel Agilex 5 FPGAs and SoCs Ordering Part Number



3. Second Generation Intel Hyperflex Core Architecture

The Intel Agilex 5 FPGAs and SoCs are based on a core fabric featuring the second generation Intel Hyperflex core architecture.

Table 10. Advantages of the Intel Hyperflex Core Architecture

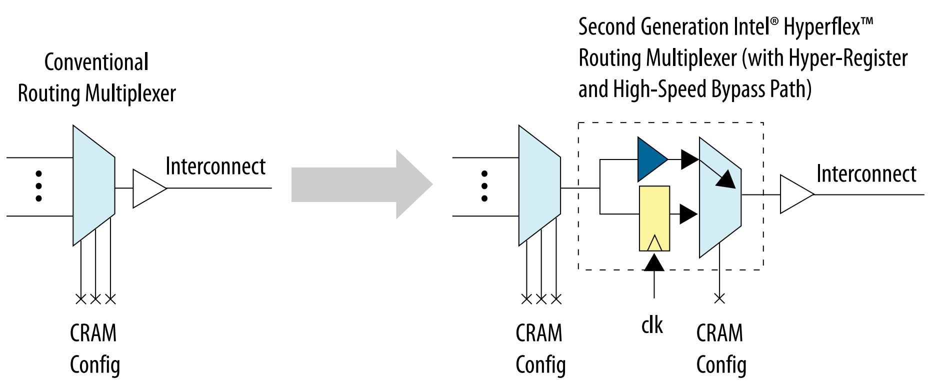
This table lists some of the advantages of the Intel Hyperflex core architecture.

Advantage	Description
Higher throughput	Delivers, on average, 50% higher core clock frequency performance in designs from previous generation high-end FPGAs to obtain throughput breakthroughs.
Improved power efficiency	Uses reduced IP size to consolidate designs that previously spanned multiple devices into a single device. This consolidation reduces power requirement by up to 42% compared to Intel Stratix® 10 FPGAs.
Greater design functionality	Uses faster clock frequency to reduce bus widths and reduce IP size. The reduced bus widths and IP size free up additional FPGA resources to add greater functionality.
Increased designer productivity	Boosts performance with less routing congestion and fewer design iterations using the Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure.

Additional to traditional ALM user registers, the Intel Hyperflex core architecture adds bypassable registers called Hyper-Registers:

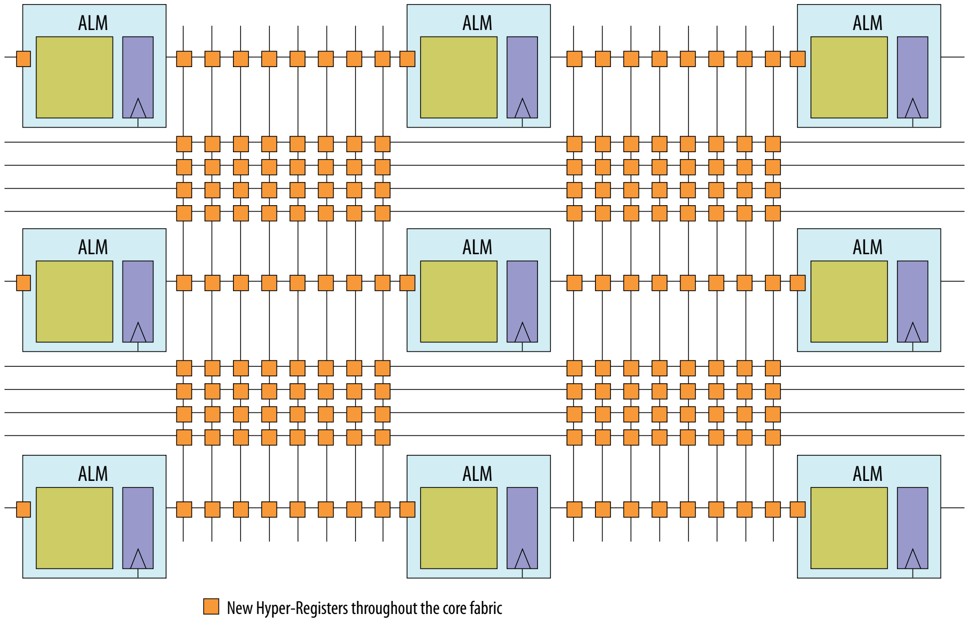
- Distributed throughout the FPGA fabric.
- Available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 5. Bypassable Hyper-Register



In the second generation Intel Hyperflex core architecture, Intel optimized the number of registers to improve timing closure time and fabric area utilization.

Figure 6. Intel Hyperflex Core Architecture



The Hyper-Registers enable you to achieve core performance increases using key design techniques. If you implement these design techniques, the Hyper-Aware design tools automatically utilizes the Hyper-Registers to achieve maximum core clock frequency:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero-latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

4. Adaptive Logic Module in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs use an enhanced adaptive logic module (ALM) similar to the previous generation Intel FPGAs such as Intel Arria® 10 and Intel Stratix 10 FPGAs. The enhanced ALM allows for efficient implementation of logic functions and easy IP conversion between Intel Agilex 5 FPGAs and Intel Arria 10 and Intel Stratix 10 FPGAs.

Figure 7. ALM Block Diagram

This figure shows the ALM with 8-input fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

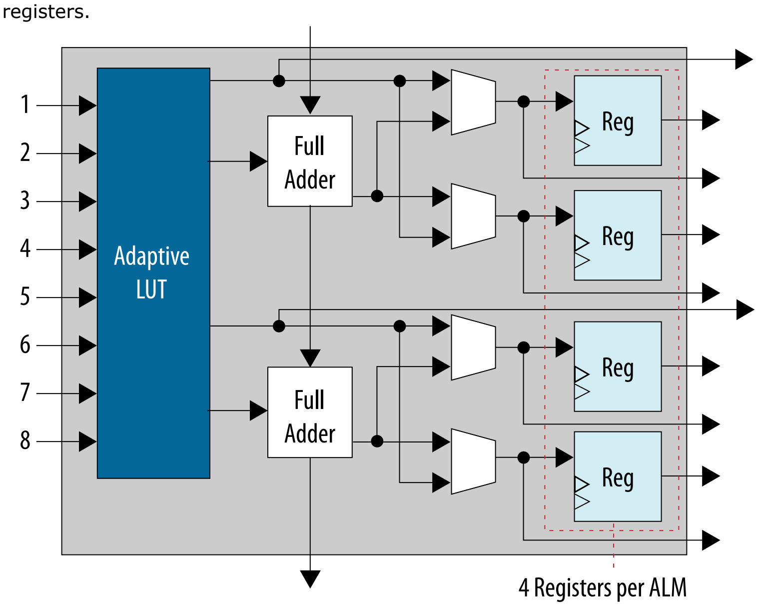


Table 11. Key Features and Capabilities of the ALM

Key Feature	Capability
High register count	Together with the second generation Intel Hyperflex architecture, the four registers per 8-input fracturable LUT enables maximized core performance at very high core logic utilization.
ALM operating modes	Optimize core logic utilization by implementing an extended 7-input logic function, a single 6-input logic function, or two smaller independent functions (for example, two 4-input functions).
Two clock sources	Two clock sources per ALM generate two normal clocks and two delayed clocks to drive the ALM registers, resulting in more clock domains and time-borrowing capability.

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Key Feature	Capability
Additional LUT outputs	Additional fast 6-LUT and 5-LUT outputs for combinatorial functions improve critical path for logic cascade.
Improved register packing	The improved register packing, including 5-input LUT with two packed register paths, results in more efficient usage of the fabric area and improved critical path.
Latch mode support	The ALM supports latch mode in the address latch enable.

The Intel Quartus Prime software capitalizes on the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as the software automatically maps legacy designs into the ALM architecture of the Intel Agilex 5 FPGAs and SoCs.

5. Internal Embedded Memory in Intel Agilex 5 FPGAs and SoCs

The embedded memory blocks in Intel Agilex 5 FPGAs and SoCs are similar to the embedded memory of previous generation Intel FPGAs.

Table 12. Embedded Memory Block Types and Features for Intel Agilex 5 FPGAs and SoCs

Feature	MLAB	M20K
Usage	For wide and shallow memory configurations	For supporting larger memory configurations
Block size	640 bits	20 kilobits
Configurations	• 64×10 (emulated) • 32×20	• 2,048×10 (or ×8) • 1,024×20 (or ×16) • 512×40 (or ×32)
Hard ECC	—	Yes
Modes	Single-port RAM, dual-port RAM, FIFO, ROM, and shift register	

6. Variable-Precision DSP in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs are the first midrange or edge-centric FPGAs with an AI tensor block, making it the ideal choice for edge AI applications.

For INT8 operations in a single DSP block, the Intel Agilex 5 FPGAs and SoCs improve peak theoretical TOPS:

- D-Series—up to 2.5 times than Intel Stratix 10 FPGAs
- E-Series—up to 37 times than Cyclone® V FPGAs

Through a large increase in arithmetic density(14), the Intel Agilex 5 FPGAs and SoCs fit more multipliers and accumulators in the same footprint of a standard DSP block.

The Intel FPGA AI Suite (Intel FPGA AI) supports the new AI features. The Intel FPGA AI Suite enables push-button flow from industry standard frameworks—such as Caffe, PyTorch*, and TensorFlow—to FPGA bitstream.

Additionally, the Intel Agilex 5 FPGAs and SoCs also carry over the variable-precision DSP architecture from previous Intel FPGAs with hard fixed point and IEEE 754-compliant floating point capabilities.

In fixed point mode, you can configure the DSP blocks to support signal processing with precisions from 9×9 up to 54×54:

- Increased 9×9 multipliers count, with three 9×9 multipliers for every 18×19 multiplier
- A pipeline register increases the maximum DSP block operating frequency and reduces the power consumption
- Dynamically switch multiplier inputs through `scanin` and `chainout` signals
- Compile each DSP block independently as six 9×9, dual 18×19, or single 27×27 multiply-accumulate.

The variable-precision DSP supports floating point addition, multiplication, multiply-add, and multiply-accumulate:

- Single-precision 32-bit arithmetic FP32 floating point mode
- Half-precision 16-bit arithmetic FP16 and FP19 floating point modes, and BFLOAT16 floating point format

With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to efficiently implement even higher-precision DSP functions.

(14) Arithmetic density is a measure of how many dot products can fit into a 1 mm^2 of silicon on any given process node.

Table 13. Variable-Precision DSP Block Configurations in Intel Agilex 5 FPGAs and SoCs

This table lists the way Intel Agilex 5 FPGAs and SoCs accommodate the different precisions within a DSP block or by utilizing multiple DSP blocks.

Multiplier	DSP Block Resource Usage	Expected Application
9×9 bits	One-sixth of a variable-precision DSP block (One DSP block can support six 9×9)	Low-precision fixed point
18×19 bits	Half of a variable-precision DSP block	Medium-precision fixed point
27×27 bits	One variable-precision DSP block	High-precision fixed point
19×36 bits	One variable-precision DSP block with external adder	Fixed point fast Fourier transform (FFT)
36×36 bits	Two variable-precision DSP blocks with external adder	Very high-precision fixed point
54×54 bits	Four variable-precision DSP blocks with external adder	Double-precision fixed point
Half-precision floating point	One variable-precision DSP block (Contains adder for two FP16, FP19, or BFLOAT16 multipliers with one accumulator)	Half-precision floating point
Single-precision floating point	One variable-precision DSP block (Contains one FP32 multipliers with one accumulator)	Single-precision floating point
AI tensor block	Two sums of ten INT8×INT8 multipliers tensor fixed-point and floating-point computation	Tensor dot products of 10-element vectors computation
Complex multiplication mode	One variable-precision DSP block (16×16 ± 16×16)	INT16 complex multiplication

7. Core Clock Network in Intel Agilex 5 FPGAs and SoCs

Intel Agilex 5 FPGAs and SoCs use programmable clock tree synthesis for its core clocking function.

Programmable clock tree synthesis uses dedicated clock tree routing and switching circuits. These dedicated circuits enable the Intel Quartus Prime software to create the exact clock trees that your design requires.

Advantages of using programmable clock tree synthesis:

- Minimizes clock tree insertion delay
- Reduces dynamic power dissipation in the clock tree
- Allows greater flexibility of clocking in the core
- Maintains backwards compatibility with legacy global and regional clocking schemes

Features of the core clock network of Intel Agilex 5 FPGAs and SoCs:

- Supports the second-generation Intel Hyperflex core architecture
- Supports the hard memory controllers(15) for:
  - DDR4—up to 3,200 Mbps
  - DDR5—up to 4,000 Mbps
  - LPDDR4—up to 4,267 Mbps
  - LPDDR5—up to 4,267 Mbps
- Supported by dedicated clock input pins and integer I/O PLLs

Related Information

- Key Features and Innovations in Intel Agilex 5 FPGAs and SoCs on page 5
- Intel Agilex 5 FPGAs and SoCs Summary of Features on page 7

(15) Each Intel Agilex 5 FPGA series has different hard memory controller support. For more information, refer to the related information.

8. General Purpose I/Os in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs are equipped with two types of general purpose I/Os—the high-speed I/Os (HSIO) and the high-voltage I/Os (HVIO). Both HSIO and HVIO enable important support for edge applications in Intel Agilex 5 FPGAs and SoCs.

Table 14. I/O Standards Support and Performance

I/O Type	I/Os Per Bank	I/O Standard	Specification	Notes
HSIO	96[16]	LVCMOS	1.0 V, 1.05 V, 1.1 V, and 1.2 V single-ended	—
		TDS	• 1.3 V • Up to 1.6 Gbps	Works with the LVDS SERDES Intel FPGA IP
		MIPI D-PHY	• Version 2.5 • Up to 3.5 Gbps[17] (high speed and low power mode)	Supports up to eight data lanes: • 1D+C • 2D+C • 4D+C • 8D+C
		SGMII (TDS)	Up to 1.25 Gbps	If required, add AC coupling
HVIO	20	LVCMOS/ LVTTL	• 1.8 V single-ended • 0.250 Gbps (125 MHz DDR)	RGMII support at 1.8 V
			• 2.5 V/3.3 V single-ended • 0.200 Gbps (100 MHz DDR)	

(16) There are two sub-banks in each HSIO bank. Each sub-bank is powered by its own V_{CCIO}.

(17) Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel.

9. I/O PLLs in Intel Agilex 5 FPGAs and SoCs

The I/O banks of the Intel Agilex 5 FPGAs and SoCs contain I/O PLLs for use in I/O interfacing or fabric clocking.

Table 15. I/O PLLs in Different I/O Bank Types

I/O Bank Type	Bank I/O PLL	Fabric-Feeding I/O PLL
HSIO (96 I/Os)	2	1
HVIO (2×20 I/Os)	—	1

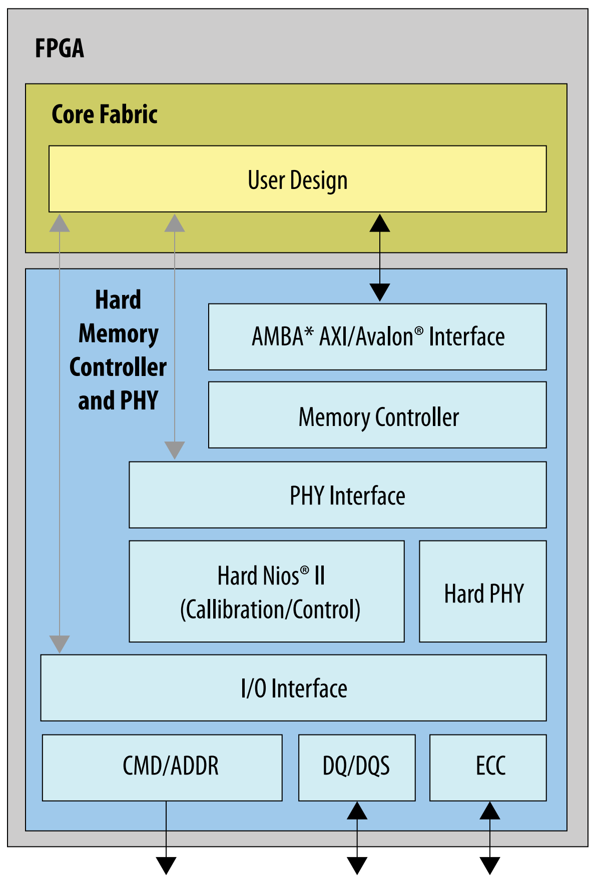
You can use the I/O PLLs for general purpose applications in the core fabric, such as clock network delay compensation and zero-delay clock buffering.

The I/O PLLs are situated adjacent to the hard memory controllers and LVDS serializer/deserializer (SERDES) blocks in the I/O bank. This placement creates a tight coupling of the PLLs with the I/Os that need them. The architecture simplifies designing external memory and high-speed LVDS interfaces, and eases timing closure.

10. External Memory Interface in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs feature a substantial external memory bandwidth. This bandwidth is accompanied by the ease-of-design, lower power, and resource efficiencies of high-performance hard memory controllers. Using the hard or soft memory controller, you can configure external memory interfaces width up to a maximum of 72 bits.

Figure 8. Hard Memory Controller



Each I/O bank contains 96 general purpose I/Os and two high-efficiency hard memory controllers. The hard memory controllers support various memory types, each with different performance capabilities. You can bypass the hard memory controller and implement a soft memory controller in user logic.

Each I/O contains a hard DDR read and write path (PHY) capable of performing key memory interface functions such as:

- Read and write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

Hard microcontrollers aid the timing calibration. Intel customized these hard microcontrollers to control the calibration of multiple memory interfaces. The calibration enables the Intel Agilex 5 device to compensate for process, voltage, and temperature (PVT) variance within the Intel Agilex 5 device or the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

10.1. External Memory Interface Performance

Table 16. D-Series FPGAs External Memory Interface Performance

Interface Protocol	Memory Controller	Interface Performance (Mbps)	Maximum Width (Bits)
DDR4	Hard	3,200	72
DDR5	Hard	4,000	40
LPDDR4/4X	Hard	4,267	32
LPDDR5	Hard	4,267	32

Table 17. E-Series FPGAs External Memory Interface Performance

Interface Protocol	Memory Controller	Interface Performance (Mbps)		Maximum Width (Bits)
		Device Group A	Device Group B	
DDR4	Hard	2,667	2,400	32
DDR5	Hard	3,600	—	40
LPDDR4	Hard	3,733	2,667	32
LPDDR5	Hard	3,733	2,400	32

10.2. Features of the Hard Memory Controller

Table 18. Hard Memory Controller Features

Feature	Description
Protocol	• LPDDR5—two dynamic frequency scaling (DFS) frequencies • DDR4 and DDR5—up to two chip selects and up to two 3D stacks
Interface	• Fully pipelined command, read, and write data interfaces to the controller • Arm AMBA* 4 AXI compliance including AXI ordering rules: — Four priority quality of service (QoS) levels — Programmable address mapping — Exclusive monitors

continued...

Feature	Description
Scheduling	• Software-configurable priority scheduling on individual SDRAM bursts • Advanced bank look-ahead features for high memory throughput • Configurable for one of these placement orders: — Out-of-order placement for writes — In-order placement for writes from the same port — In-order placement for writes from the same AXI master • Configurable for in-order scheduling for reads and writes • Support read or write grouping
Timing	Fully programmable timing parameter support for all JEDEC*-specified timing parameters
Refresh	• All bank refresh or per bank refresh (if supported by memory) • Refresh management for DDR5
ECC	• Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters • Hardened ECC support including configurations for various ECC types with programmable single-bit and double-bit error reporting and automatic correction: — In-line ECC, out-of-band ECC, link ECC, end-to-end (user) ECC, or no ECC — Supports standard single bit error correction and double bit error detection — Support for ECC passthrough for fabric ECC with 8 bits of ECC per 64 bits of data — Supports scrubbing
Power states	Low power DRAM states including active power down, precharge power down, and self-refresh power down states for DRAM: • Under register control; or • Based on idle times
Training	Initial and periodic ZQ calibration (LPDDR4, LPDDR5, DDR5)
Verification	• Performance monitoring statistics • Memory test for DDR memories through register control

11. Hard Processor System in Intel Agilex 5 SoCs

The Intel Agilex 5 SoCs hard processor system (HPS) consists of multicore Arm processors, including a dual-core Arm Cortex-A76 and a dual-core Arm Cortex-A55 processors. Additionally, the HPS adds a system memory management unit that enables system-wide hardware virtualization.

With the HPS architecture improvements, the Intel Agilex 5 SoCs fulfill the requirements of current and future embedded markets, including:

- Wireless and wireline communications
- Datacenter acceleration
- Various industrial applications

Figure 9. Intel Agilex 5 SoCs HPS Block Diagram

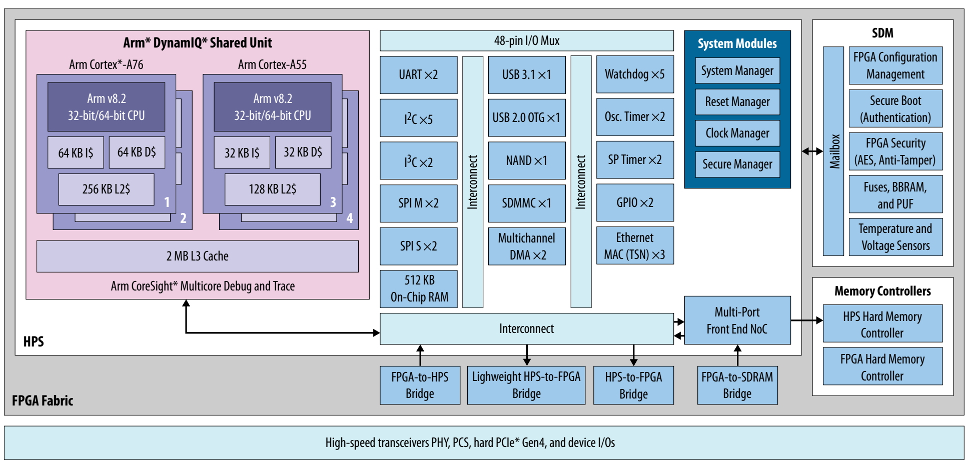


Table 19. Summary of Intel Agilex 5 SoCs Key Features

Feature	Description
Processor units	• Multicore of dual-core Arm Cortex-A76 MPCore and dual-core Arm Cortex-A55 MPCore processor units — CPU frequency: • Dual-core Arm Cortex-A76—up to 1.8 GHz • Dual-core Arm Cortex-A55—up to 1.5 GHz — Arm v8.2-A architecture • Run 64-bit and 32-bit Arm instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Arm Jazelle* runtime compilation target (RCT) execution architecture with 8-bit Java* bytecodes • Superscalar, variable-length, out-of-order pipeline with dynamic branch prediction

continued...

Feature		Description
		• Improved Arm Neon media processing engine • Single-precision and double-precision floating-point unit • Arm CoreSight debug and trace technology
System memory management unit		• Enables a unified memory model • Extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache coherency unit		Propagates changes in shared data stored in cache throughout the system to provide I/O coherency for co-processing elements
Cache memory	Common	Shared 2 MB L3 cache
	Dual-core Arm Cortex-A76	• 64 KB L1 I-cache and 64 KB L1 D-cache with ECC per core • 256 KB unified L2 data and instructions cache per core
	Dual-core Arm Cortex-A55	• 32 KB L1 I-cache and 32 KB L1 D-cache with ECC per core • 128 KB unified L2 data and instructions cache per core
On-chip memory		512 KB on-chip RAM
External SDRAM and flash memory Interfaces for HPS	Hard memory controller	• Supports DDR4, DDR5, LPDDR4, and LPDDR5 • 40-bit (32-bit + 8-bit ECC) • ECC support including calculation, error correction, write-back correction, and error counters • Software-configurable priority scheduling on individual SDRAM bursts • Fully programmable timing parameter support for all JEDEC-specified timing parameters • Multi-port front end (MPFE) interface to the hard memory controller, supporting AMBA 4 AXI QoS for interface to the FPGA fabric
	NAND flash controller	• Integrated descriptor-based controller with DMA • Programmable hardware ECC support • Support for 8-bit and 16-bit flash devices • Compatible with the ONFI 1.x and 2.x specifications • Compatible with Toggle 1.x and 2.x specifications
	SD/SDIO/eMMC controller	• Integrated descriptor-based DMA controller • Supports CE-ATA digital commands • Supports SD devices up to version 6.1 • Supports SDIO devices up to version 4.1 • Supports SD/eMMC devices up to version 5.1 • Supports SD SDR12, SDR25, SDR50, SDR104, and DDR50 • Supports eMMC legacy, high-speed SDR, high-speed DDR, HS200, and HS400 • Does not support UHS-II and UHS-III interfaces
	DMA controller	• Two controllers with four channels each • Supports up to 48 peripheral handshake interfaces

continued...

Feature		Description
Communication interface controllers	Ethernet MAC	• Three Ethernet MACs supporting 10 Mbps, 100 Mbps, 1 Gbps, and 2.5 Gbps with integrated DMA and TSN support • Ethernet standards with TSN endpoint functionality compliant to: — IEEE 1588-2008 advanced timestamps: Precision Time Protocol (PTP), 2-steps, PTP offload and timestamping — IEEE 802.1AS: Timing and synchronization — IEEE 802.1Qav: Time-sensitive streams forwarding and queuing — IEEE 802.1Qbv: Time-scheduled traffic enhancements — IEEE 802.1Qbu: Frame pre-emption — IEEE 802.3br: Interspersing express traffic • Ethernet interfaces: — Supports RGMII operating mode at 10 Mbps, 100 Mbps, and 1 Gbps data rates through HPS I/O — Supports RGMII operating modes at 10 Mbps, 100 Mbps, and 1 Gbps data rates through FPGA HVIO with GMII–to–RGMII soft adapter in FPGA logic — Supports SGMII operating mode at 1 Gbps (1000BASE-X) or 10 Mbps, 100 Mbps, and 1 Gbps (SGMII) data rates with SGMII PCS soft IP through TDS I/O — Supports SGMII+ operating mode at 10 Mbps, 100 Mbps, 1 Gbps, and 2.5 Gbps data rates with SGMII+ PCS soft IP and serial transceiver interface through FPGA I/O
	USB 2.0 OTG	• One USB OTG controller • Dual-role device (device and host functions) — High-speed (480 Mbps) — Full-speed (12 Mbps) — Low-speed (1.5 Mbps) — Supports USB 1.1 (full-speed and low-speed) • Integrated descriptor-based scatter-gather DMA • Support for external ULPI PHY • Up to 16 bidirectional endpoints, including control endpoint • Up to 16 host channels • Supports generic root hub • Configurable to USB OTG 1.3 and USB OTG 2.0 modes
	USB 3.1 Gen1	• Supports both device and host controller modes — Both USB 3.1 and USB 2.0 interfaces must be configured as device or host; mixing modes is not supported • Supports up to 5 Gbps if configured for USB 3.1 Gen1 and interfaced with the transceiver • Supports up to 480 Mbps if configured for USB 2.0 and interfaced with the HPS I/O
	I^2C	• Five I^2C controllers, three can be used by the Ethernet MAC for MIO to external PHY • Support 100 Kbps and 400 Kbps modes • Support 7-bit and 10-bit addressing modes • Support master and slave operating modes
	I^3C	• Two I^3C controllers • — One configured as the primary master — One configured as the secondary master • Supports FM, FM+, and SDR data rates up to 12.5 Mbps
	UART	• Two UART 16550-compatible controllers • Programmable baud rate up to 115.2 kilobaud
	SPI	• Four SPI (two masters, two slaves) • Supports full duplex and half duplex

continued...

Feature		Description
Timers		• Four general-purpose timers • Five watchdog timers
I/O		• 48 HPS direct I/Os allow HPS peripherals to connect directly to the I/Os • Up to two FPGA fabric I/O banks assignable to the HPS for HPS DDR access
Interconnect to logic core	HPS–to–FPGA bridge	• Allows HPS bus masters to access bus slaves in FPGA fabric • Configurable 32-, 64-, or 128-bit AMBA AXI data interface allows high-bandwidth HPS master transactions to FPGA fabric • Supports up to 256 gigabytes (GB) of address space
	Lightweight HPS–to–FPGA bridge	• Lightweight 32-bit AMBA AXI interface suitable for low bandwidth register access from HPS to soft peripherals in the FPGA fabric • Supports up to 512 MB of address space
	FPGA–to–HPS bridge	• 256 bits FPGA–to–HPS interface targeting the HPS peripherals and shared SDRAM • Shared SDRAM accessible using non-coherent[18] or hardware-supported I/O coherent transactions
	FPGA–to–SDRAM bridge	• 64, 128, or 256 bits FPGA–to–SDRAM interface targeting the DDR I/O • Supports only non-coherent[18] transactions

(18) For non-coherent transactions, ensure that the HPS and FPGA soft logic do not interfere in the SDRAM space of each other.

12. Transceivers in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs are equipped with NRZ transceivers optimized for a wide variety of applications, ranging from 1 Gbps to 28.1 Gbps NRZ.

The monolithic GTS transceivers in Intel Agilex 5 FPGAs and SoCs enable low latencies for edge or mid-range FPGA applications. For long reach backplane-driving applications, the devices use advanced adaptive equalization circuits to equalize system loss.

All Intel Agilex 5 FPGA GTS transceiver channels are equipped with these blocks:

- Dedicated PMA—provides primary interfacing capabilities to physical channels.
- Hardened PCS—supports 64b/66b encoding and decoding functions, data scrambling, block alignment, and gearboxing functions.
- FEC—Firecode FEC for 10/25 GbE BASE-KR/CR applications and Reed Solomon FEC.

A single PMA–PCS channel with independent clock domains forms each GTS transceiver channel. Using a highly configurable clock distribution network, you can configure various bonded and non-bonded data rate within each GTS transceiver bank.

Figure 10. D-Series FPGAs GTS Transceiver Block Diagrams

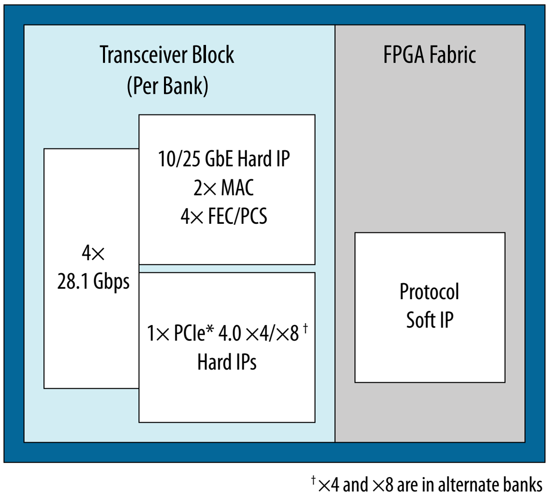


Figure 11. E-Series FPGAs GTS Transceiver Block Diagrams

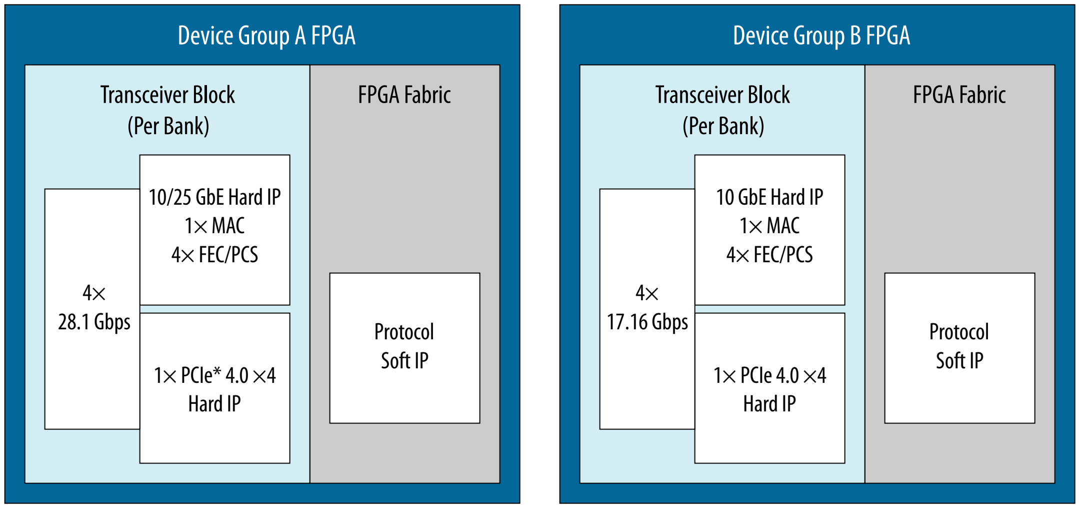


Table 20. Capabilities of FPGA GTS Transceivers in Intel Agilex 5 FPGAs and SoCs

Capability	Maximum Specification		
	D-Series FPGA	E-Series FPGA	
		Device Group A	Device Group B
Maximum speed	28.1 Gbps NRZ (1–28.1 Gbps continuous)	28.1 Gbps NRZ (1–28.1 Gbps continuous)	17.16 Gbps NRZ (1–17.16 Gbps continuous)
FEC	10/25 GbE FEC direct mode (IEEE 802.3 Clause 74 Firecode FEC and Clause 91 RS-FEC hard IPs)	10/25 GbE FEC direct mode (IEEE 802.3 Clause 74 Firecode FEC and Clause 91 RS-FEC hard IPs)	10 GbE FEC direct mode (IEEE 802.3 Clause 74 Firecode FEC hard IP)
PCS	10/25 GbE PCS direct mode[19] (64b/66b hard IP)	10/25 GbE PCS direct mode[19] (64b/66b hard IP)	10 GbE PCS direct mode[19] (64b/66b hard IP)
PCIe	• PCIe 4.0 ×8 controller hard IP • PCIe 4.0 ×4 controller hard IP	PCIe 4.0 ×4 controller hard IP	Up to PCIe 4.0 ×4 controller hard IP
Transmitter / Receiver	Independent transmitter and receiver to support combining simplex protocols		
PMA	PMA direct mode (bypass Ethernet and PCIe hard IPs)		

12.1. PMA Features in Intel Agilex 5 FPGA GTS Transceivers

The transmitter, receiver, and high speed clocking resources form the PMA channels. The transmit features deliver exceptional signal integrity at data rates up to 28.1 Gbps NRZ. Additionally, each PMA features advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

(19) The PCS direct mode is supported on GbE and other protocols.

Table 21. GTS Transceiver PMA Features in Intel Agilex 5 FPGAs and SoCs

Feature	Capability
Data rates	Up to 28.1 Gbps
Optical module support	SFP+ optical module support
Cable driving support	SFP+ Direct Attach
Transmit pre-emphasis	One post-tap and two pre-taps for NRZ
Dynamic reconfiguration	Independent control of each GTS transceiver channel Avalon® memory-mapped interface for transceiver flexibility
Multiple PCS–PMA and PCS to FPGA fabric interface widths	• Flexible deserialization width, encoding, and reduced latency • GTS transceiver (PMA with optional FEC or PCS) to FPGA fabric interface—from 8 bits up to 66 bits options

12.2. PCS Features in Intel Agilex 5 FPGA GTS Transceivers

The PMA channels in the Intel Agilex 5 FPGAs and SoCs interface with the core logic through the configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. The GTS transceiver (PMA with optional FEC or PCS) to FPGA fabric interface support from 8 bits up to 66 bits options. This feature allows you to implement a wide range of applications.

The PCS hard IP supports various standard and proprietary protocols across a wide range of data rates and encoding schemes.

12.3. GTS Transceiver PLL in Intel Agilex 5 FPGAs and SoCs

There are two types of PLL in the Intel Agilex 5 FPGA GTS transceiver.

Table 22. Types of Intel Agilex 5 FPGA GTS Transceiver PLL

PLL Type	Description
TX PLL	• Four TX PLL per bank or one TX PLL per GTS transceiver channel • LC tank-based PLL with precise fractional synthesis and ultra-low jitter • Supports transceiver interfaces • Dedicated for GTS transceiver usage
System PLL	• One System PLL per bank • Supports only integer mode with precise frequency synthesis • Supports transceiver-to-fabric interfaces • If you do not use the System PLL for the GTS transceivers, you can repurpose this PLL for core fabric usage

13. MIPI Protocols Support in Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGAs and SoCs support native MIPI IP D-PHY. The devices support MIPI D-PHY v2.5 at up to 3.5 Gbps(20) per lane. The Intel Agilex 5 FPGAs support MIPI D-PHY high-speed and low-power signaling modes without requiring external components.

Features of the MIPI IP D-PHY:

- Enables unidirectional multi-lane configurations—1, 2, 4, or 8 lanes
- Supports low-power and high-speed signaling up to 3.5 Gbps(20) per lane

The MIPI IP D-PHY implements MIPI transmit and receive interfaces for Intel Agilex 5 FPGAs in accordance to the following protocols:

- Camera Serial Interface (CSI-2) version 3.0 with underlying D-PHY standard
- Display Serial Interface (DSI-2) version 2.0 with underlying D-PHY standard

Table 23. MIPI CSI-2 and DSI-2 Performance in Intel Agilex 5 FPGAs and SoCs

Protocol	D-Series FPGA	E-Series FPGA	
		Device Group A	Device Group B
CSI-2	• CSI-2 version 3, up to eight lanes • D-PHY v2.5 at up to 3.5 Gbps(20)	• CSI-2 version 3, up to eight lanes • D-PHY v2.5 at up to 3.5 Gbps(20)	• CSI-2 version 3, up to eight lanes • D-PHY v2.5 at up to 2.5 Gbps(21)
DSI-2	• DSI-2 version 2, up to four lanes • D-PHY v2.5 at up to 3.5 Gbps	• DSI-2 version 2, up to four lanes • D-PHY v2.5 at up to 3.5 Gbps(20)	• DSI-2 version 2, up to four lanes • D-PHY v2.5 at up to 2.5 Gbps(21)

(20) Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel.

(21) Up to 2.5 Gbps for standard reference and long reference channels.

Figure 12. MIPI Receiver Block Diagram

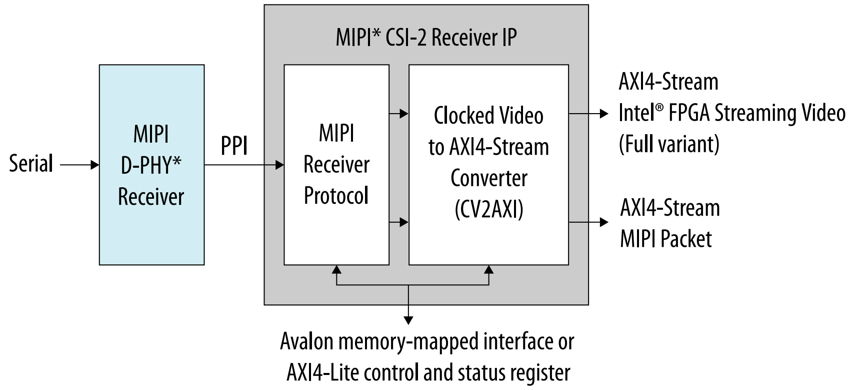
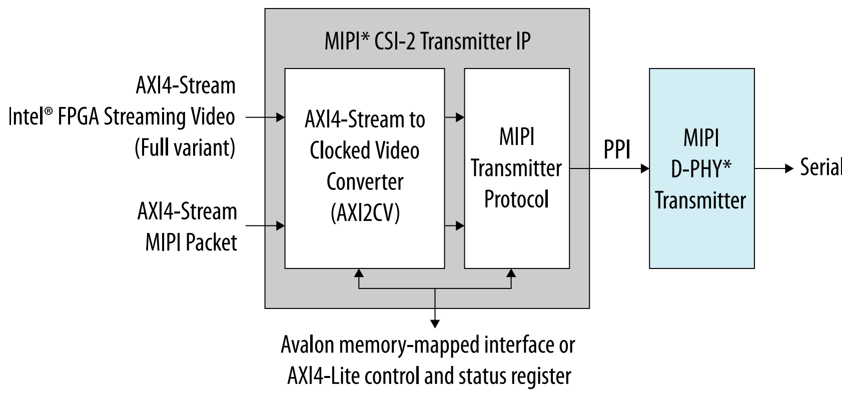


Figure 13. MIPI Transmitter Block Diagram

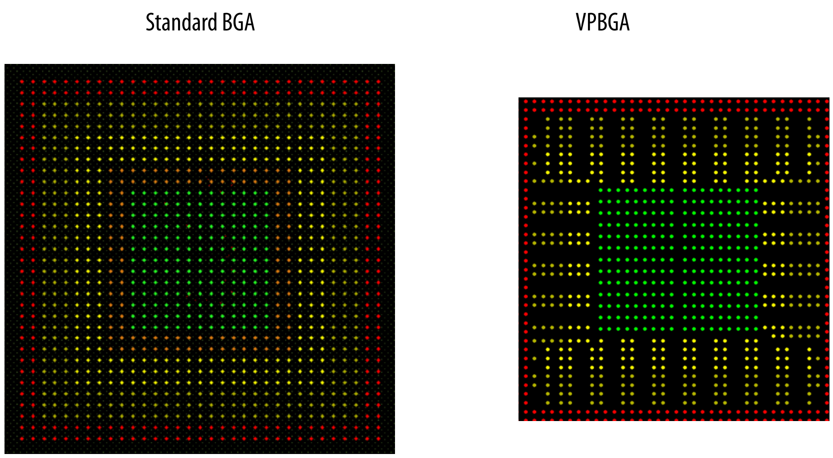


14. Variable Pitch BGA (VPBGA) Package Design of Intel Agilex 5 FPGAs and SoCs

Most of the Intel Agilex 5 FPGAs and SoCs packages use the VPBGA package design. The E-Series FPGAs also offer 0.5 mm ball pitch package with a standard ball grid for small form-factor with more I/O counts.

Compared to the standard ball grid array (BGA) packages, the VPBGA package has a variable ball pitch size with a minimum size of 0.65 mm[22].

Figure 14. Comparison Between Standard BGA and VPBGA

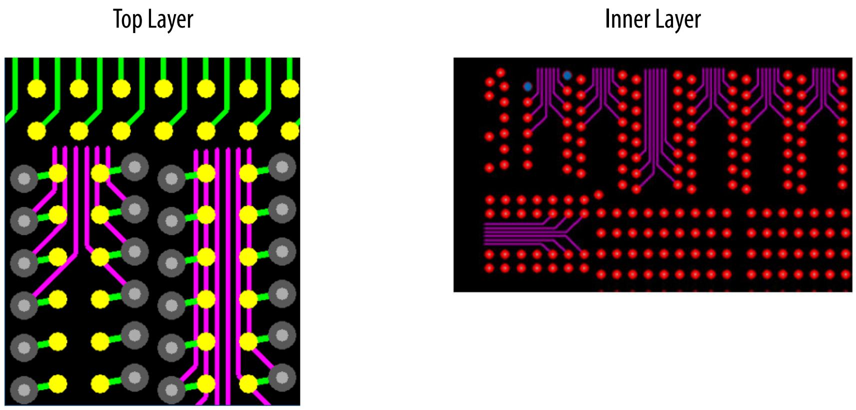


The variable ball pitch helps reduce the package form factor. Despite the smaller package size, the VPBGA packages can provide the same I/O pin count and compatible electrical performance compared to the standard BGA packages.

As shown in the following figure, the variable ball grid pattern eases trace routability, reducing the design complexity, number of PCB layers, and board thickness and size—ultimately, reducing board cost and development time.

(22) 0.65 mm is the minimum ball pitch and is not meant for signal trace routing. The VPBGA design meets the 0.8 mm design rules and the use of standard plated through hole (PTH) via.

Figure 15. Example of PCB Trace Routing for Variable Pitch BGA (VPBGA) Package



15. Configuration via Protocol Using PCIe for Intel Agilex 5 FPGAs and SoCs

Configuration via protocol (CvP) using PCIe allows you to configure the Intel Agilex 5 FPGAs and SoCs across the PCIe bus. This capability simplifies board layout and increases system integration.

The embedded PCIe hard IP operates in autonomous mode before the FPGA is configured. Using this hard IP, you can power up and activate the PCIe bus within the 100 ms time allowed by the PCIe specification.

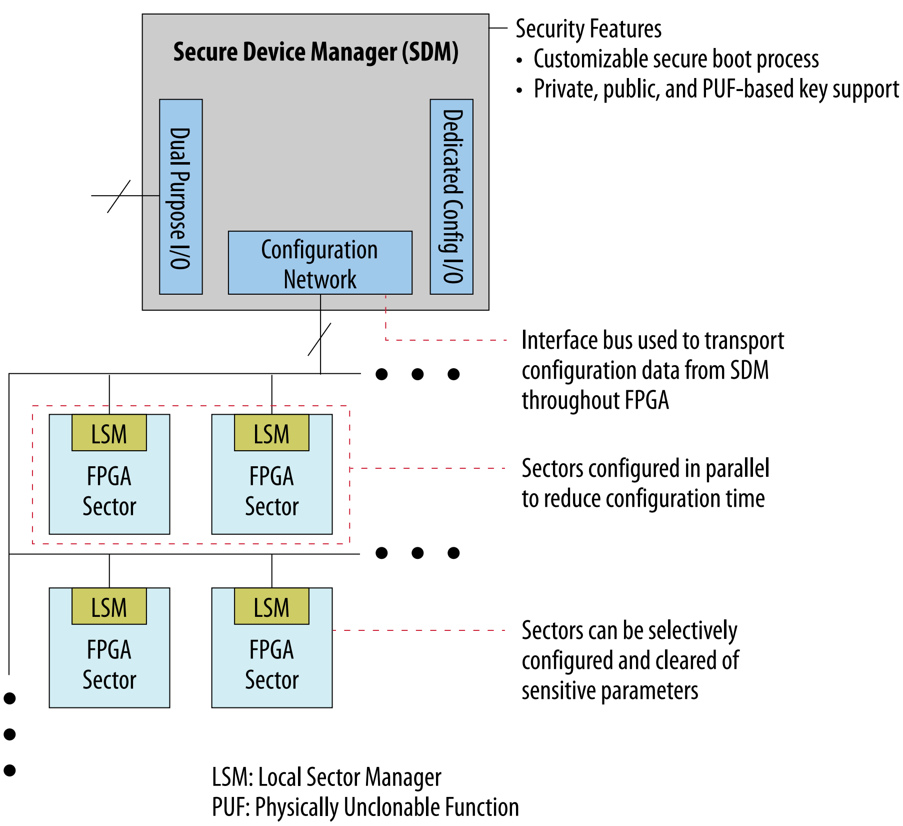
The Intel Agilex 5 FPGAs and SoCs also support partial reconfiguration across the PCIe bus. This capability reduces system downtime by keeping the PCIe link active during device reconfiguration.

16. Device Configuration and the SDM in Intel Agilex 5 FPGAs and SoCs

All Intel Agilex 5 FPGAs and SoCs contain an SDM. The SDM is a triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. Additionally, the SDM in the Intel Agilex 5 FPGAs and SoCs enables system certification to FIPS140-3 layer 2 compliance.

The SDM bootstraps the HPS in Intel Agilex 5 SoCs. This bootstrapping ensures that the HPS boots using the same security features available to the FPGA.

Figure 16. SDM Block Diagram



During configuration, the Intel Agilex 5 FPGA or SoC divides into logical sectors. A local sector manager (LSM) manages each logical sector. The SDM passes configuration data to each LSMs across the on-chip configuration network.

Advantages of the sector-based approach:

- Enables independent configuration of the sectors—one at a time or in parallel
- Achieves simplified sector configuration and reconfiguration
- Reduces overall configuration time caused by inherent parallelism.

The Intel Agilex 5 FPGAs and SoCs use the same sector-based approach to respond to SEUs and security attacks.

Although the sectors provide a logical separation for device configuration and reconfiguration, the sectors overlay the normal rows and columns of FPGA logic and routing:

- No impact to the Intel Quartus Prime software place and route
- No impact to the timing of logic signals that cross the sector boundaries

The SDM enables robust, secure, and fully-authenticated device configuration. Additionally, the SDM allows you to customize the configuration scheme, enhancing device security.

Advantages of the SDM-based device configuration approach:

- Provides a dedicated secure configuration manager
- Reduces device configuration time because sectors are configured in parallel
- Enables an updatable configuration process
- Supports partial reconfiguration
- Allows remote system update
- Supports zeroization of whole device or individual sectors

Table 24. Supported Configuration Schemes for Intel Agilex 5 FPGAs

Configuration Scheme	Data Width	Maximum Data Rate
Active Serial (AS) normal and fast modes	4 bits	4 bits × 166 MHz = 664 Mbps
Avalon streaming interface ×16 (23)	16 bits	16 bits × 125 MHz = 2 Gbps
Avalon streaming interface ×8	8 bits	8 bits × 125 MHz = 1 Gbps
JTAG	1 bit	1 bit × 30 MHz = 30 Mbps
Configuration via Protocol (CvP)	×1, ×2, ×4 and ×8 lanes	The maximum data rate depends on the PCIe generation and number of lanes. Typically, the data rate of the internal configuration data path of the device, instead of the width of the PCIe link, limits the configuration data width.

(23) Not supported in E-Series A5E 005B and A5E 007B devices.

17. Partial and Dynamic Configuration of Intel Agilex 5 FPGAs and SoCs

Intel built the partial reconfiguration process on top of the proven incremental compile design flow in the Intel Quartus Prime design software. With partial reconfiguration, you can reconfigure parts of the FPGA while other sections continue to run. In systems with critical uptime requirement, you can update or adjust functions without disrupting service provision.

Apart from lowering power usage and cost, partial configuration effectively increases the logic density. Instead of placing all functions in the FPGA from the start, you can store functions that do not have to operate simultaneously in external memory. You can load these function into the FPGA when needed. Using this technique, you can run multiple applications on a single FPGA and reduce the requirements for FPGA size, board space, and power.

With dynamic reconfiguration, Intel Agilex 5 FPGAs and SoCs can dynamically change data rates, protocols, and analog settings of a transceiver channel without affecting data transfer on adjacent transceiver channels. This capability is ideal for applications that require on-the-fly multi-protocol or multi-rate support.

You can dynamically reconfigure both the PMA and PCS blocks within the transceiver. You can also use dynamic reconfiguration together with partial reconfiguration to partially reconfigure the FPGA core and transceivers simultaneously.

18. Device Security for Intel Agilex 5 FPGAs and SoCs

Intel Agilex 5 FPGAs and SoCs are built with robust security features and managed by the SDM. The devices prioritize the operations of the SDM over fabric and other microprocessor tasks.

The dedicated SDM manages and supports the following critical security features:

- Manages FPGA configuration process and all security features
- Performs authenticated FPGA configuration and HPS boot
- Supports FPGA bitstream encryption, secure key provisioning, and PUF key storage
- Supports platform attestation using the SPDM protocol
- Manages runtime sensors and supports active tamper detection and responses
- Provides access to hardened cryptographic engines as a service

In addition to the preceding list, the following table summarizes the three pillars of security with the advanced security features that Intel Agilex 5 FPGAs and SoCs support.

Table 25. Intel Agilex 5 FPGAs and SoCs Advanced Security Features

Pillar of Security	Device Security Features
Confidentiality, integrity, and availability	• Encryption • Authentication • Attestation • Secure boot • User access to cryptographic functions • Secure debug • Vendor authorized boot
Key protection	• Side channel mitigation • Physical anti-tamper detection and response
Secure manufacturing	• Black key provisioning • Secure returned merchandise authorization (RMA)

19. SEU Error Detection and Correction in Intel Agilex 5 FPGAs and SoCs

Intel Agilex 5 devices feature a robust SEU error detection and correction circuitry that protects the configuration RAM (CRAM) programming bits and M20K user memories.

To protect the CRAM, a parity checker circuit with integrated ECC runs continuously to automatically correct single-bit or double-bit errors and detect higher order multi-bit errors. The optimized physical layout of the CRAM array makes most multi-bit upsets appear as independent single-bit or double-bit errors. Therefore, the CRAM ECC circuitry can automatically correct these errors.

The user memories also has integrated ECC circuitry and are also layout-optimized for error detection and correction.

To provide a complete SEU mitigation solution, a soft IP and the Intel Quartus Prime software support the SEU error detection and correction hardware. The following components make up the complete solution:

- Hard error detection and correction for CRAM and M20K user memory blocks
- Optimized memory cells physical layout to minimize the probability of an SEU
- Sensitivity processing soft IP that reports if a CRAM upset affects a used or unused bit
- Fault injection soft IP with Intel Quartus Prime software support to change CRAM bits state for testing
- Hierarchy tagging feature in the Intel Quartus Prime software
- Triple modular redundancy (TMR) for the SDM and critical on-chip state machines

Intel Agilex 5 FPGAs and SoCs also support the following SEU mitigation features:

- Fast SEU detection notification through an IP that connects the LSM pin to the fabric. This notification allows the fabric soft logic to detect reported SEU events faster. You can then retrieve further SEU details through the SDM mailbox.
- External scrubbing for SEU errors that are not automatically correctable. You can create scrubbing bitstream—up to one sector granularity—to scrub the SEU-corrupted configuration bits while keeping the remaining parts of the device intact.
- Single-bit ECC injection, ECC error detection, and reporting on memory in the configuration system. You can test the ECC detection logic by issuing ECC injection commands and querying the ECC status from the SDM.

Furthermore, Intel Agilex 5 FPGAs and SoCs are built on the FinFET-based Intel 7 technology. FinFET transistors are less susceptible to SEUs compared to conventional planar transistors.

20. Power Management for Intel Agilex 5 FPGAs and SoCs

The Intel Agilex 5 FPGA product family offers standard power devices that support SmartVID and fixed core voltage devices with limited core speed options.

The Intel Agilex 5 FPGAs and SoCs achieve significant total power reduction:

- D-Series—up to 42% compared to Intel Stratix 10 FPGAs
- E-Series—up to 50% compared to Cyclone V FPGAs

To achieve the total power reduction, the Intel Agilex 5 FPGAs and SoCs capitalizes on:

- Advanced Intel 7 technology
- Second generation Intel Hyperflex core architecture
- SmartVID or fixed core voltage
- Other power reduction techniques such as power island and power gating

Table 26. Intel Agilex 5 FPGAs and SoCs Power Options

Device Type	Series	Description
SmartVID	• D-Series • E-Series Device Group A	• The devices operate at the optimum core voltage that meets the VID power limit and required device performance for various FPGA applications. • A factory-programmed code allows a PMBus voltage regulator to operate at the optimum core voltage to meet the device VID power limit and performance specifications. Therefore, you must mandatorily drive the V_{CC} and V_{CCP} core voltage supplies of the SmartVID device with a dedicated PMBus voltage regulator.
Fixed voltage	E-Series Device Group B	• The devices support 0.75 V, 0.78 V, and 0.8 V. • Using a fixed low core voltage,the devices further reduce the total power consumption. • These fixed voltage devices have lower static power than the SmartVID standard power devices while maintaining device performance.

The power island and power gating feature powers down unused resources in Intel Agilex 5 devices to reduce static power consumption. During configuration, the Intel Quartus Prime software automatically powers down specific unused resources such as the DSP or M20K blocks.

Furthermore, Intel Agilex 5 devices feature industry-leading low power transceivers and include a number of hard IP blocks. The hard IP blocks not only reduce logic resources utilization but also deliver substantial power savings compared to soft implementations. The hard IP blocks generally consume up to 50% less power than equivalent soft logic implementations.

21. Intel Software and Tools for Intel Agilex 5 FPGAs and SoCs

The Intel Quartus Prime Pro Edition design suite supports the Intel Agilex 5 FPGAs and SoCs with a new compiler and the Hyper-Aware design flow.

Together with the Intel oneAPI toolkit, software developers can develop acceleration solutions using Intel Agilex 5 FPGAs and SoCs. The Intel oneAPI toolkit provides a unified, single-sourced, software-friendly, and heterogeneous programming environment for a diverse set of computing engines. The toolkit includes a comprehensive and unified portfolio of developer tools you can use to map software to hardware and accelerate your code.

To improve the efficiency and quality of your designs, Intel also provides the following tools for the Intel Agilex 5 FPGAs and SoCs:

- Transceiver toolkit
- Platform Designer IP integration tool
- Intel DSP Builder for Intel FPGAs advanced blockset
- Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA)

22. Revision History for the Intel Agilex 5 FPGAs and SoCs Device Overview

Document Version	Changes
2024.01.12	• Added 1.0 V LVCMOS support for the HSIO. • Added notes that the minimum ball pitch of 0.65 nm is not meant for signal trace routing. • Updated the fabric-feeding I/O PLL count for the following devices: — A5D 051 and A5D 064—from 13 to 15 — A5E 043A and A5E 043B—from 11 to 13 • Added a figure that shows the available ordering part numbers. • Removed support for ACE5-Lite cache stashing for the FPGA–to–HPS bridge.
2023.09.18	• Updated references to "Balls Anywhere" to "Variable Pitch BGA (VPBGA)". • Updated the package options and vertical migrations for E-Series FPGAs to remove information about conditional migration path.
2023.05.15	• Updated the package options and vertical migrations: — Added package B18A. — Updated pin counts for packages B23B, B23A, and B32A. — Added devices to package B23A of the E-Series FPGA Device Group A. • Updated the supported DDR4 maximum width for E-Series FPGAs • Updated E-Series FPGA Device Group B to support up to PCIe 4.0. • Assigned "GTS" naming to the transceivers. • Updated information about the HPS L2 cache. • Updated the E-Series HPS processors speeds: — Dual core ARM® Cortex-A76—from up to 1.6 GHz to up to: • Device Group A—1.8 GHz • Device Group B—1.4 GHz — Dual core ARM Cortex-A55—from up to 1.33 GHz to up to: • Device Group A—1.5 GHz • Device Group B—1.25 GHz • Updated the HPS block diagram. • Removed ONFI 3.x and 4.x from HPS NAND flash controller. • Updated HPS Ethernet MAC information: — Updated the TSN endpoint functionality compliance. — Removed MII, RMII, and GMII support. — Updated RGMII support.
2023.01.10	Initial release.