Overview

The ATM3201/ATM3221/ATM3231 are part of a family of extreme low-power Bluetooth® 5 system-on-a-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5.0 compliant radio with ARM® Cortex® M0 application processor, 128 KB Random Access Memory (RAM), 256 KB Read Only Memory (ROM), 4 KB One-Time-Programmable (OTP) memory, and state-of-the-art power management.

Support for low duty cycle operation allows systems to run for significantly longer time periods without battery replacement. In addition, this series of SoCs from Atmosic supports operation from various energy harvesting sources, including RF, Photovoltaic, TEG (Thermoelectric generator), and motion. Innovative wake-up mechanisms are supported in order to provide options for further power consumption reduction.

ATM32x1 devices are available in three different packages to meet various I/O and form factor requirements.

Applications

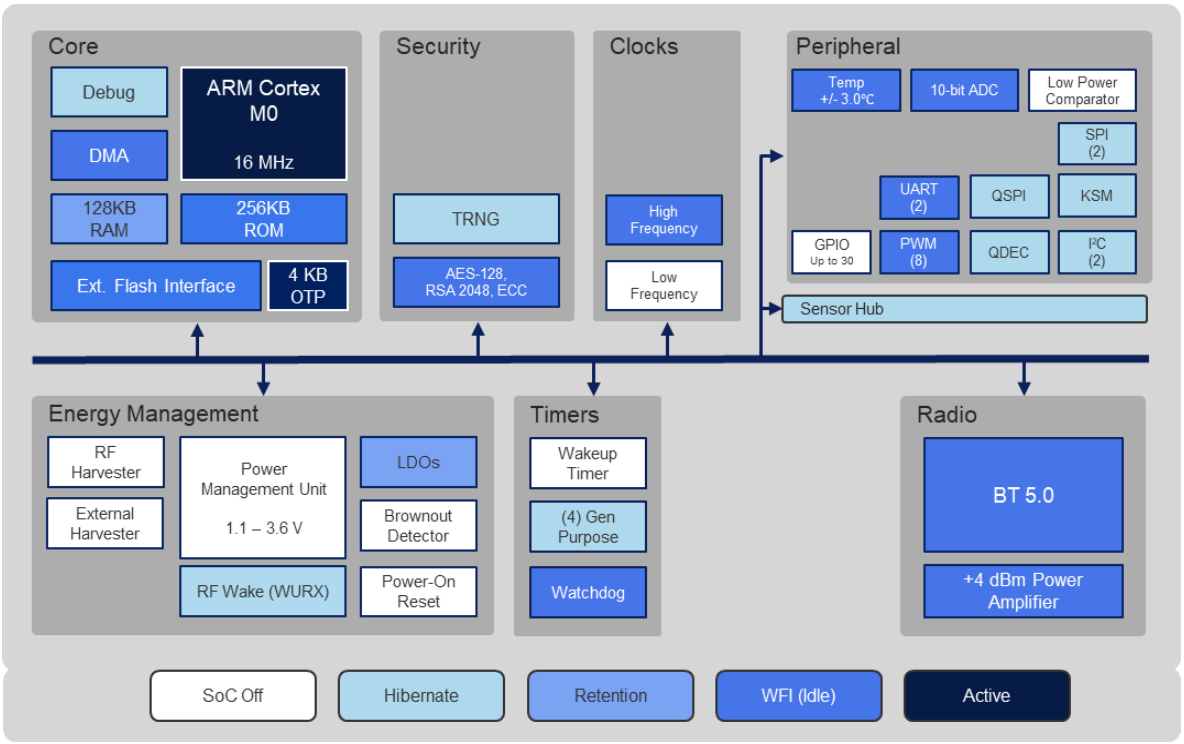
Industrial and Enterprise
- Beacons and Sensors
- Asset Trackers
- Environmental Monitors

Healthcare
- Asset Tracking
- Patient Monitoring

Home
- Home Automation
- Remote Control
- Human Interface Devices (HID)

Personal
- Wearables

Auto
- Key fobs and Accessorie



Features

- On-chip RF Energy Harvesting with dedicated antenna input
- Supports Photovoltaic, Thermal, Motion and other energy harvesting technologies
- Compliant with Bluetooth 5.0 standard
- Supports Bluetooth 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
- Fully integrated RF front-end
- SoC typical power consumption with 3 V battery including PMU
  - **Active Rx @ -95 dBm: 1.0 mA**
  - **Active Tx @ 0 dBm: 2.5 mA**
  - **Retention @ 32 KB RAM: 2 µA**
  - **Hibernate: 0.7 µA**
  - **SoC Off with Harvesting Enabled: 500 nA**
- CPU: 16 MHz ARM Cortex M0 processor, programmable interrupt router
- Memory: 256 KB ROM, 128 KB RAM, and 4 KB OTP
- Retention RAM configuration: 16 KB to 128 KB in 16 KB step sizes
- RF Wakeup Receiver
- Interfaces: I2C, SPI, UART, PWM, GPIO
- Quad SPI with Execute in Place (XIP)
- 10-bit application ADC
- Digital microphone input (PDM)
- 32.768 kHz/16 MHz crystal oscillator
- SWD for interactive debugging
- AES 128 hardware
- True random number generator (TRNG)
- Sensor Hub
- Keyboard matrix controller (KSM)
- Quadrature decoder for mouse input (QDEC)
- 1.1 V to 3.3 V battery input voltage with integrated Power Management Unit (PMU)
- Package:
  - ATM3201 (40-pin 5x5 mm QFN) supports up to 16 GPIOs
  - ATM3221 (64-pin 6x6 mm DR-QFN) supports up to 30 GPIOs
  - ATM3231 (56-pin 7x7 mm QFN) supports up to 29 GPIOs.

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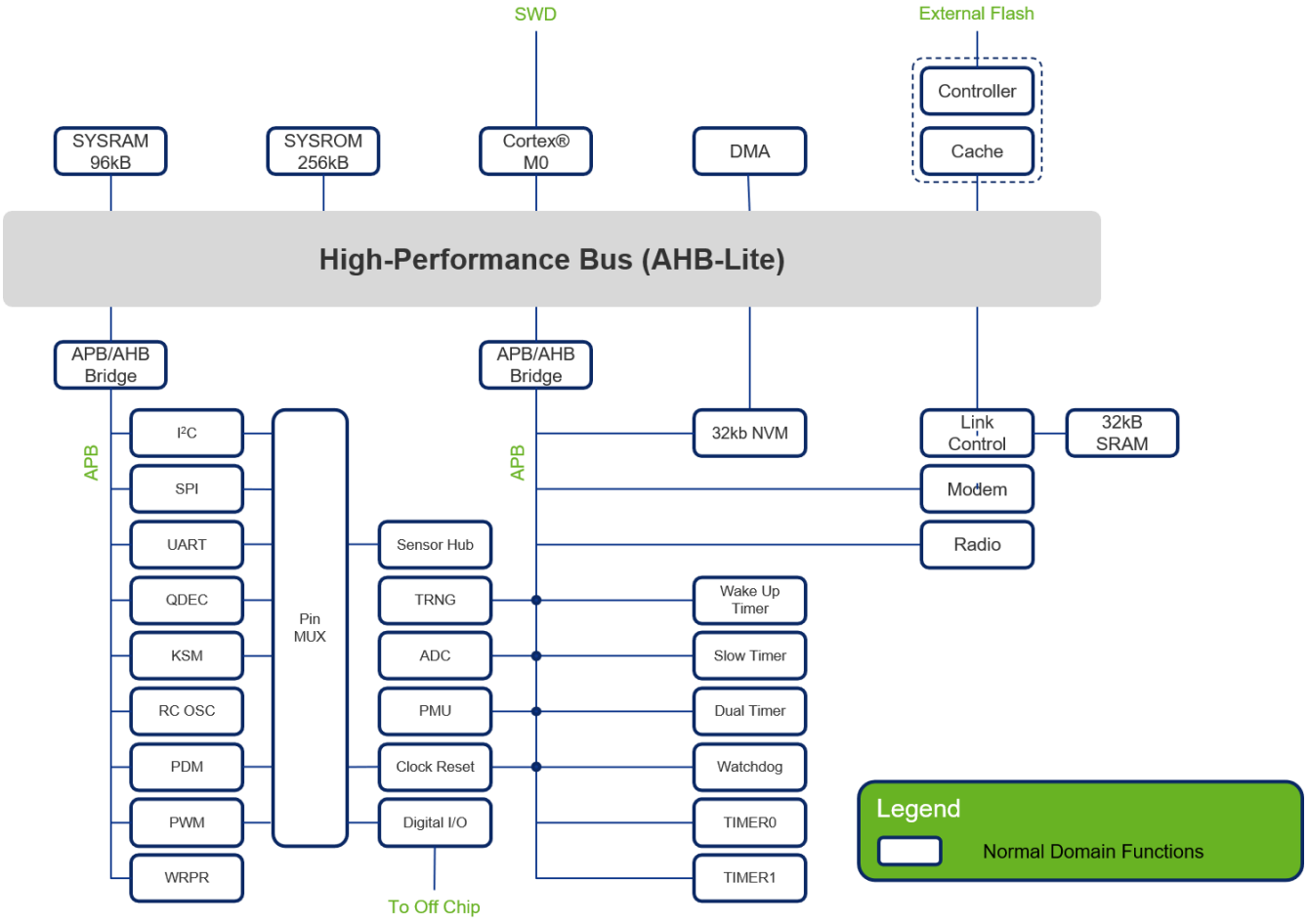


1.1 CPU & Memory

The ATM3 contains a 16 MHz 32-bit ARM® Cortex®-M0 processor that is optimized for low-power operation. The processor is a little endian, 32-bit RISC processor which implements the ARMv6-M architecture specification. It supports most Thumb-1 instructions and some Thumb-2 instructions. It features four breakpoints, a serial access debug port, 32 interrupts, a single cycle multiplier, full wake-on-interrupt support, and two watch points.

To reduce latency, software can use the Direct Memory Access (DMA) core for memory to memory copying and for initializing blocks of memory to a constant. When it is in use, the DMA core masters the Advanced Microcontroller Bus Architecture (AMBA) High-performance Bus (AHB) and has higher precedence than the Cortex®-M0.

The ATM3 includes the following memory components:

- ROM: 256 KB of ROM containing the Bluetooth LE 5 protocol stack up to GATT/GAP layer, a beacon application, and the boot code
- SRAM: 128 KB of SRAM containing both system RAM and data RAM organized as eight 16 KB macros. Two of the macros are reserved for the Bluetooth 5 link controller. The power state of each macro in each low power state can be independently controlled
- NVM: 4 KB of One-Time-Programmable memory (OTP) to store configuration, calibration data and user data
- FLASH: A quad Serial Peripheral Interface (SPI) master port to interface with an external flash chip if needed (up to 16 MB)

The quad SPI master port is equipped with a cache in the read direction to reduce the effective latency of flash accesses. Performance operating out of flash is comparable to that of operating out of RAM. When executing out of RAM and at 16 MHz, the ATM3 has a CoreMark 1.0 score of 29.5. When executing out of external flash, with the quad SPI interface boosted to 32 MHz, the quad SPI cache enabled, and the remainder of the SoC operating at 16 MHz, the ATM3 has a CoreMark 1.0 score of 25.7. Debug access through pins TMC, P0, P1, and P2 can be used to access the Cortex®-M0's serial wire debug port. The on-chip system memory is organized as follows.

Table 1.1 -1 System Memory Map

Start	Stop	Block
0x0000 0000	0x0003 FFFF	ROM
0x1000 0000	0x10FF FFFF	FLASH
0x2000 0000	0x2001 7FFF	SRAM
0x3000 0000	0x3000 FFFF	LC
0x4000 0000	0x4000 FFFF	APB0_Peripherals
0x4001 0000	0x4001 1FFF	GPIO
0x4001 F000	0x4001 FFFF	SYSCTL
0x5000 0000	0x5000 FFFF	APB1_Peripherals
0x6000 0000	0x6000 0FFF	NVM
0x7000 0000	0x7000 0FFF	DMA
0x8000 0000	0x8000 0FFF	PDM

1.1.1 Clocks

There are three primary clock domains on the ATM3:

- low power clock: 32.768 kHz crystal or an internal RC oscillator (RCOSC)
- medium power clock: 16 MHz crystal or an internal RC oscillator (RCOSC)
- high power clock: used by quad SPI for external flash

1.1.2 Reset

The PMU releases the chip-wide reset once the power supplies have stabilized. There is no explicit reset pin on the ATM3 but the user can use PWD for an equivalent purpose. Many of the internal modules can additionally be reset through a software register write.

1.1.3 Power Modes

The SoC supports five primary power states which are Active, Retention, Hibernation, SoC Off and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating.

1. Active: All regions of the SoC are powered on. Active power can be optimized by utilizing clock gating registers and/or by putting the Cortex-M0 into Wait for Interrupt (WFI).
    - CPU Idle: When the CPU function is not required, it can be placed into WFI state to conserve power.
    - Bluetooth LE Deep Sleep: Bluetooth subsystem is powered down while the remainder of the ATM3 is powered up. This state is useful when data needs to be processed but does not need to be transmitted over RF.
2. Retention: All or some of the 128 kB SRAM, in increments of 16 kB, can be retained. All register/flip-flop states are retained. Digital I/Os will hold the state they were at when the transition into either Hibernate or Retain started. Wake can be from a timer expiring, activity detected on GPIOs, activity detected on the keyboard, activity detected on the mouse, the sensor hub reading measurements crossing a threshold, and the detection of a connection over the SWD interface. All selections about how to wake need to be programmed before the transition into the low power state is triggered. The SRAM supply voltage can be lowered to further reduce leakage power consumption.
3. Hibernation: Powers down system memory. Retains only a minimal amount of flip-flop state. Retains I/O state. Wake up setting must be programmed before transitioning into this state.
4. SoC Off: all digital domains including the top level digital domain are powered down, but the PMU remains on in an ultra low-power state with limited functionality. The system must do a complete, cold start reboot when returning from this state to an active state. Wake mechanisms limited to (a) special 40-bit timer, (b) external digital input on P10, (c) ultra-low power analog comparator with input on either P11 or P12
5. Powerdown[1] (PWD pin asserted): All power domains including the PMU are completely shut off. No supplies are internally generated or maintained. This state is only valid with an external IO supply.

1.2 Security

The ATM3 has a true random number generator (TRNG) which generates a single 32 bit random number per invocation. Arbitrarily long random numbers can be achieved by repeatedly invoking this random number generator. The outputs of TRNG can be used to generate public and private keys which in turn can be used to generate the link layer symmetrical key.

[1] Minimum PWD assertion time is 2 seconds. Do not enter Powerdown mode unless the device will be in this state for at least 2 seconds.

The ATM3 also has an AES-128 hardware accelerator. This core is directly accessible by software and it is also used by the hardware to encrypt and decrypt packets when needed during Bluetooth LE operation.

If necessary a fuse within the OTP can be set to disable all slave interfaces. This would prevent keys being read out by a third party but it would also disable the SWD interface which in turn blocks future debug. Setting this disabling fuse should be used with caution. Alternatively, writes to the OTP can be permanently blocked. This mechanism would prevent the alteration of public keys but would not block the SWD interface.

1.3 Power Management

The power management unit provides the core and I/O power supplies to the ATM3 SoC. Harvested energy can extend the battery life or enable operation without a battery for some low duty-cycle applications. PMU generates the three power supply outputs: DVDD1P, AVDD1P, VDDIOP, and a fourth auxiliary supply VAUX used internally by the PMU. The following connections must be made on the board:

- DVDD1P to DVDD1
- AVDD1P to VDD1A

Table 1.3 -1 PMU External Pins

PIN	Description
VBAT	Battery input. Battery voltages from 1.1 V to 3.3 V can be used. Must be connected to a battery, external supply, or ground (battery-free applications).
VSTORE	Connection to a large storage capacitor (typical value 220 µF). Must be grounded when the harvester is not used.
HARV_OUT	Connection to a storage capacitor of typical value 10 µF. Must be grounded when the harvester is not used.
LEXT1, LEXT2	Terminals between which the switching regulator inductor is connected.
DVDD1P, AVDD1P VDDIOP	DVDD1P and AVDD1P are PMU generated digital and analog core supply outputs. VDDIOP is a PMU generated 1.8 V IO supply output.
VAUX	Auxiliary supply output of typical value 3.2 V, used internally by the PMU.
DVDD1, VDD1A	Power supply input for digital and analog core circuits.
VDDIO, VDDIOA	Power supply input for digital and analog IO circuits.

The PMU provides multiple brownout interrupts to enable more reliable operation, especially when using energy harvesting.

1.3.1 PMU configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

(a) One external power supply or battery with external IO supply:

For applications that cannot support fixed 1.8 V IO supply

- Connect VBAT to VDDIO/VDDIOA
- Connect VAUX to VDDIOP
- Disable IO supply generation

(b) One external power supply or battery with internally generated IO supply:

For applications that can use a fixed 1.8 V IO supply for better power consumption or VBAT <= 1.8 V

- Connect VDDIOP to VDDIO/VDDIOA

(c) Energy harvesting with no battery and internally generated IO supply:

- Connect VBAT to ground
- Connect VDDIOP to VDDIO/VDDIOA

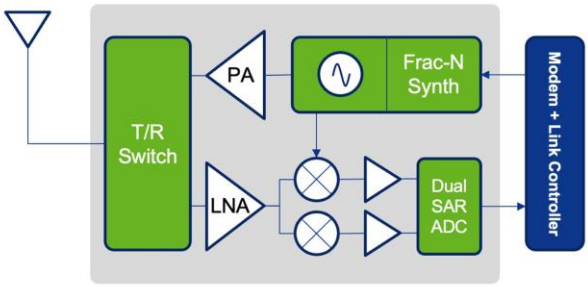
1.4 Sensor Hub

The sensor hub is a hardware module that, when suitably programmed, can read data from external sensors and write to an external flash device on the quad SPI interface. This function can be performed with all other power domains, including the CPU power domain, powered down. Additionally, the sensor hub can trigger a chip wide wake up if any of the read data crosses preprogrammed thresholds.

1.5 Bluetooth LE Radio

The block diagram of the low-power radio is shown in Figure 1.5-1. The radio supports Bluetooth 5.0 including 1 Mbps basic PHY, 2 Mbps high-speed PHY, 500 kbps and 125 kbps PHY. The basic 1 Mbps PHY is compatible with Bluetooth 4.0, while the 2 Mbps rate provides 2X speed and the long range rates provide up to 4X range. The transmit path uses digital direct frequency modulation of a fractional-N synthesizer to create a constant amplitude GFSK signal that is amplified by a power amplifier to provide the desired RF output level. On the receive path, an incoming RF signal is first amplified by an LNA before downconversion to baseband and digitized by two successive-approximation analog-to-digital converters. The digitized signal is sent to the Modem for further digital processing. The radio architecture is optimized for burst data transmission using Frequency-Hopping Spread Spectrum (FHSS) with 40 channels with 2 MHz spacing (3 advertising channels/37 data channels). Only a single RF Input/Output pin is needed, thereby simplifying board-level design.

Figure 1.5-1 Bluetooth LE Radio Block Diagram



1.5.1 Link Controller

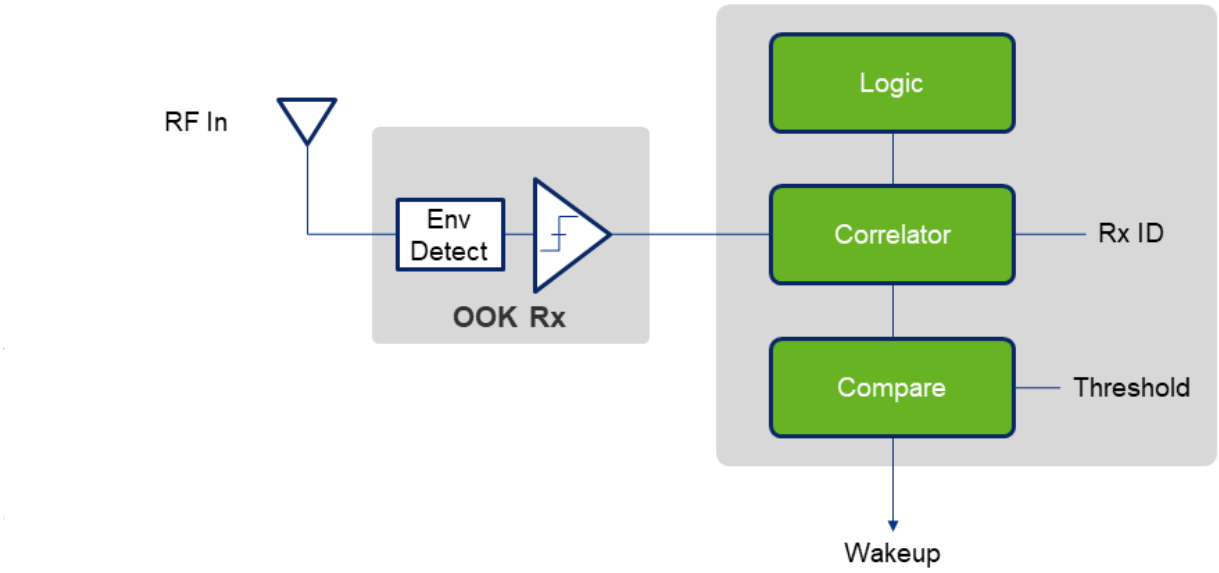
The Bluetooth 5 link controller (LC) and host stack provides an interface between the microcontroller (MCU), modem (MDM) and exchange memory (EM), allowing the MCU to access through the AHB bus to the control registers and exchange memory. During transmission, software writes the packet payload and control structures into the exchange memory. The link controller serializes the data into a bit stream to the modem. During receive, the operation is reversed. Received data from the modem is processed and stored in the exchange memory to be read by software. The design runs on an 8 MHz clock and is synchronous to MDM (16 MHz) and AHB bus (16 MHz) and exchange memory (16 MHz).

1.5.2 Modem

The modem (MDM), along with the radio, link controller and software stack, forms a highly efficient Bluetooth 5 solution. Transmission and reception at rates of 2 Mbps, 1 Mbps, 500 kbps and 125 kbps are supported. During receive operation, the modem and radio are enabled prior to expected packet reception as determined by the link controller. Incoming packets are detected, tracked, processed, and then forwarded to the link controller. The modem and radio receiver are turned off by the link controller at the end of a completed packet. Channel information is provided directly from the link controller to the radio without involvement of the modem. There is minimal involvement of the modem in the transmit process. The link controller provides the symbol bit stream, which is then shaped consistent with the GFSK requirements to provide a frequency deviation for the radio. Channel information and target transmit power are provided directly from the link controller to the radio.

1.6 Wakeup Receiver

Figure 1.6-1 Wakeup Receiver Block Diagram



The use of a wakeup receiver allows a system to be in sleep mode while waiting for incoming RF activities. In this SoC, the wakeup receiver is designed to decode an incoming RF paging or wakeup signal with very low power consumption. This dedicated low-power wakeup receiver continuously monitors the incoming RF signal for a predefined paging signal. This continuous Rx mode is based on an OOK radio, which has ultra-low power consumption. The wakeup receiver is intended for short range and short latency applications. Latency of the wakeup receiver is typically in the order of 20 ms to 1 s, depending on the length of the Rx ID code used to identify the target device.

1.7 OTP Access

The OTP is accessible through two separate cores. One resides on the Advanced Peripheral Bus (APB) and provides indirect access for byte reads and bit writes. The other resides on the AHB bus and provides memory mapped addresses for byte, half word, and word reads.

1.8 Timers and Interrupts

1.8.1 Wakeup Timer

Wakeup timer is a 40-bit timer based on the low power 32 kHz clock. When this timer is enabled during SoC Off mode, it will determine the SoC off duration.

1.8.2 General Purpose Timers

There are four general purpose timer cores: Timer0, Timer1, Dual Timer, and Slow Timer. The value of the timers are readable by the CPU. All timers are clocked by the medium power clock except for the Slow Timer which uses the low power clock. All these timers stop when the system enters a low power mode. The state of the timer is maintained during Retention mode but is reset during hibernate mode.

- Timer0, if enabled, will decrement from a 32 bit reload value to 0 triggering a maskable interrupt as it transitions from 1 to 0. The reload value is loaded as the next timer value when the timer reaches 0.
- Timer1 is identical to Timer0.
- Dual Timer contains two timers and each timer is independent of the other but sharing a single interrupt output. Each timer counts down and can run in one-shot, periodic, or free running mode. The timers are configurable to be either 16 bit or 32 bit. Additionally there is a rescale in front of each timer that can reduce the incoming clock by 1x (no change), 16x, or 256x.
- Slow Timer is a 40 bit count down timer with three programmable thresholds. The interrupt is optionally asserted when the counter counts from one above the threshold to the threshold. It is recommended that the timer be read twice and the value used only if the values from both reads are the same. If the values are not the same then the read should happen a third time. The timer is updating every 16000000/32768 cycles or approximately 488 cycles of the 16 MHz medium power clock.

1.8.3 Interrupts

There is one non-maskable interrupt and it is the watchdog interrupt. There are 32 possible maskable interrupts of which 16 are connected to the GPIO interrupts and 16 are the programmable combination of 48 possible interrupt sources. Each of these 16 configurable interrupts has its own combining function.

1.9 Pin Multiplexing

The ATM3231 7x7 mm package SoC supports 33 programmable I/O pins, P0, - P26, P28 - P33. The ATM3221 6x6 mm package SoC supports 34 programmable I/O pins, P0 - P33. And the ATM3201 5x5 mm package SoC supports 17 programmable pins P0 - P2, P9 - P11, P13, P17, P19 - P20, P22 - P25, P30, P32 - P33. These programmable I/O pins may be connected to multiple functional signals. In addition, each of these I/O pins can be configured to be input only, output only, input/output, with or without pull-up.

1.10 Peripherals and I/O

The following peripherals are supported by the SoC.

- **GPIO**
  There are up to 29 GPIOs available on the ATM3231 7x7 mm package, up to 30 GPIOs available on the ATM3221 6x6 mm package, and up to 16 GPIOs on the ATM3201 5x5 mm package. In addition to providing general purpose read and write access, the GPIOs can also be used to generate interrupts and to wake the ATM3 from low power states.

- **I2C**
  There are two identical I2C masters. Software preloads the transaction and then initiates the hardware controller. Software can either poll for completion or respond to the completion interrupt. I2C clock speed is programmable and ranges from 3.9 kHz to 4 MHz.

- **Serial Peripheral Interface (SPI)**
  There are two general purpose 1-bit SPI masters. Software can preload the transaction, initiate it, and then either poll for completion or respond to the completion interrupt. Opcode, transaction type, data, and number of bytes are all software programmable. The hardware will serialize and sample incoming data as required by the protocol. The SPI port clock frequency is programmable and ranges from 7.8 kHz to 8 MHz.

- **Quad serial peripheral interface (QSPI)** supports external flash up to 32 MHz
  There is one quad SPI master port and it is intended to be connected to an external flash (if needed). Internally there are three cores that can act as master for the interface:
  (a) 1-bit core identical to the SPI core described previously. It provides read and write support to the external flash via indirect addressing.
  (b) Software specified protocol / content. The hardware's role is limited to serial shift in or out. Read and write access via indirect addressing is provided by this core.
  (c) Direct memory mapping of the entire external flash contents. It essentially acts as an AHB bridge to the external flash. The hardware handles all protocols. Additionally this core contains a cache in the read direction to reduce latency.

- **UART**
  There are two UART cores with flow control present on the ATM3. UART0 should be used for HCI type applications and UART1 primarily for debug messaging (without flow control).

- **PDM Digital microphone**
  PDM (Pulse Density Modulation) provides microphone support using two pins and supports three clock speeds (500 kHz, 1 MHz, and 2 MHz).
  The PDM-to-PCM conversion block takes as input a 1-bit PDM output from a digital microphone and outputs a 16-bit PCM signal at 16 kHz sample rate. The clock frequency to the PDM microphone can be selected to be 500 kHz, 1 MHz or 2 MHz. The 1-bit PDM signal is filtered through a 3rd order sinc decimation filter to filter out ADC quantization noise. This is followed by a 1st order IIR filter (that can be bypassed) which attenuates any residual DC content. The corner frequency of the IIR filter is programmable. The gain control block has a programmable gain from -30 dB to 30 dB in steps of 0.5 dB. The output bit rate is 16 bit x 16 kHz = 256 kbps.
  The output from the PDM core is captured in a FIFO which supports a ping-pong type drain mechanism.

- **PWM**
  The PWM has eight independent pulse width modulation output channels. Each channel has frequency and duty cycle options. Additionally, all channels can be started at exactly the same time if synchronization is required. The frequency ranges from 250 kHz to 8 MHz and the duty cycle is tunable in 1/64th steps.

- **Quadrature decoder for mouse inputs (QDEC)**
  The QDEC is a 3-axis (x,y,z) quadrature decoder. Each axis is independent and requires 2 input pins. QDEC continuously updates the internal integrators and their values can be read by software.

- **Keyboard matrix controller (KSM)**
  The KSM is a keyboard scanner which supports up to 8 rows by 20 columns or 20 rows by 8 columns. Key pressed and key released events can optionally require that the key be pressed or be released across multiple consecutive scans. Up to 12 simultaneous key events can be tracked.
  A portion of the KSM can continue to scan during low power states. The key pressed or key released event can

also optionally wake the ATM3 from a low power state. Key events are not lost when the ATM3 is in a low power state. Key events are packetized and written into a FIFO via the hardware for later reading by the software.

- **Analog Comparator**
  A 16-level analog comparator provides an ultra-low power approach to sense an analog input signal from sensors.

- **Application ADC**
  10-bit Application ADC with 1 differential inputs or 3 single-ended inputs. The ADC input can be one of the input pins, internal signals such as temperature or voltage (supply, battery). The selected input signal is digitized by 10-bit ADC at 2 MSamples/s.

2 Electrical Specification

All parameters are based on 3 V supply at 25 °C unless otherwise specified.

Table 2-1 Maximum Electrical Ratings

Maximum Ratings					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VBAT	Battery voltage[2]	-0.2		3.6	V
VDDIO	I/O supply	-0.2		3.6	V
VIO	I/O pin (VDDIO > 3.4 V) I/O pin (VDDIO <= 3.4 V)	-0.2 -0.2		3.6 VDDIO+0.2	V
VRF	RF I/O pin			10	dBm
ESD_{HBM}	ESD HBM (Class 2)			2000[3]	V
ESD_{CDM}	ESD CDM			500	V
T_{STORE}	Storage Temperature	-40		125	°C

Table 2-2 Recommended Operating Conditions

Recommended Operating Conditions					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VDDIO	I/O supply	1.7	1.8	3.3	V
VBAT	Battery supply	1.1[4]		3.3	V
VPP25	OTP Programming Voltage[5]	2.3	2.5	2.7	V
VIO	I/O pin	-0.2		VDDIO+0.2	V
	Crystal Osc - 16.000 MHz	-20		20	ppm
	Crystal Osc - 32.768 kHz	-500		500	ppm
TA	Operating (Ambient) Temperature	-40	25	85	°C

2 VBAT minimum slew rate is 0.3 V/ms

3 Pins TMC and PWD are 1250 V

4 VBAT minimum supply after boot is 1.0 V

5 VPP25 is physically connected to VDDIO. Set VDDIO to within VPP25 range when programming the OTP.

Table 2-3 Radio Transceiver Characteristics

Radio Transceiver Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Frequency		2.402		2.480	GHz
Rx sensitivity	37-byte packets, clean Tx				
	125 kbps		-101		dBm
	500 kbps		-98.5		dBm
	1 Mbps		-95		dBm
	2 Mbps		-93		dBm
	255-byte packets, dirty Tx				
	125 kbps		-100		dBm
	500 kbps		-96.5		dBm
	1 Mbps		-94		dBm
	2 Mbps		-91		dBm
Tx output power	4, 2, 0, -2, -4, -6, -10, -20	-20		4	dBm
Tx power accuracy			+/- 1.5		dB
Tx spectral mask	2 MHz offset	-20			dBm
@ 1M sym/s	> 3 MHz offset	-30			dBm
Rx	Co-channel interference	21			dB
Carrier-to-Interferer	Adjacent 1 MHz interference	15			dB
(LE 1M PHY)	Adjacent 2 MHz interference	-17			dB
	Adjacent 3 MHz interference	-27			dB
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		+/- 2		dB

Table 2-4 Wakeup Receiver Characteristics

Wakeup Receiver Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Sensitivity[6]	915 MHz and 2440 MHz, 14-byte packets at 1 ms interval for 40 ms		-44		dBm

Table 2-5 PMU Characteristics

PMU Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
AVDD1P Output Voltage			1.0		V
DVDD1P Output Voltage			1.0		V
VDDIOP Output Voltage			1.8		V
VAUX Output Voltage			3.2		V

Table 2-6 GPIO Characteristics

GPIO Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input VIH		VDDIO-0.5		VDDIO	V
Input VIL		-0.2		0.2	V
Output VOH	2 mA Load		VDDIO-0.2		V
Output VOL	2 mA Load		0.2		V
Drive Strength - High Drive (P4-P7, P14-P20, P22-P24)	VDDIO = 3.3 V VDDIO = 1.7 V		16 10		mA mA
Drive Strength - Standard Drive (P0-P3, P8-P13, P21, P25-P33)	VDDIO = 3.3 V VDDIO = 1.7 V		8 5		mA mA
Pull-up Resistance	VDDIO = 3.3 V VDDIO = 1.7 V		45 100		kΩ kΩ

6 >= 90% wakeup success rate

Table 2-7 Application ADC Characteristics

Application ADC Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Resolution			10		bits
Sampling Rate	Without averaging		2		MHz
Temperature measurement accuracy			+/- 5		°C
Voltage measurement gain error			+/- 1		%
Voltage measurement offset error			+/- 2		LSB

Table 2-8 Power Consumption

Power Consumption VBAT current at 3 V with internally generated IO supply					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Active RX	Sensitivity at -95 dBm		1		mA
Active TX @ 4 dBm	Output power at 4 dBm		4		mA
Active TX @ 0 dBm	Output power at 0 dBm		2.5		mA
Active TX @ -10 dBm	Output power at -10 dBm		1.4		mA
CPU Active	Executing CoreMark from RAM at 16 MHz		0.4		mA
CPU Idle + Bluetooth LE Deep Sleep			0.2		mA
Powerdown	PWD pin asserted		75		nA
Retention (32 KB RAM)			2		µA
Hibernation			0.7		µA
Hibernation with Wakeup Receiver			0.85		µA
SoC Off with Harvesting Enabled			500		nA

Table 2-9 Energy Harvesting

Symbol	Parameter	Min	Typ	Max	Unit
HARV_OUT	Cold Start Voltage	1.65		3.3	V
	Steady State Regulated Voltage	1.0		3.3	V
	Input Power	30[7]		9000[8]	µW
VSTORE	Voltage			3.3	V
HARV1_IN	RF Input Level (operation)	-15		9	dBm
	RF Input Level (Cold Start) @ 915 MHz		-9.5		dBm
	Frequency Range	400		2500	MHz

[7] Battery free configurations only.

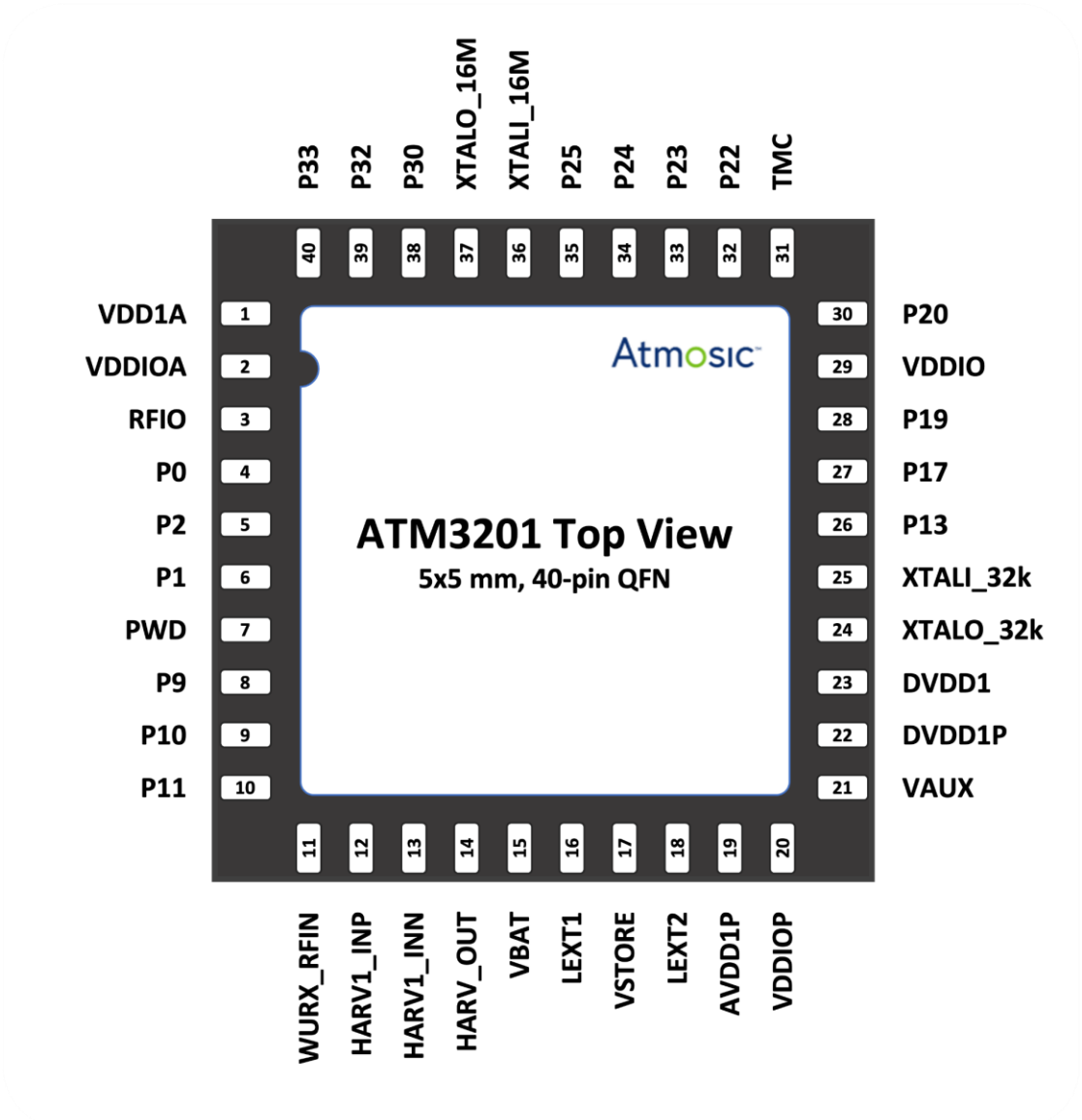
[8] Power limit only at 3.3V.

3 Pinout Description

3.1 ATM3201 Pinout

The ATM3201 is packaged in a 40-pin 5x5 mm Quad Flat Package No Leads (QFN). The pin assignment is shown in Table 4.1-2 . All pins are on the bottom side of the package.

Figure 3.1-1 ATM3201 40-Pin 5x5 mm QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
GND	Ground

Table 3.1-1 ATM3201 40-pin 5x5 mm QFN Pin Description

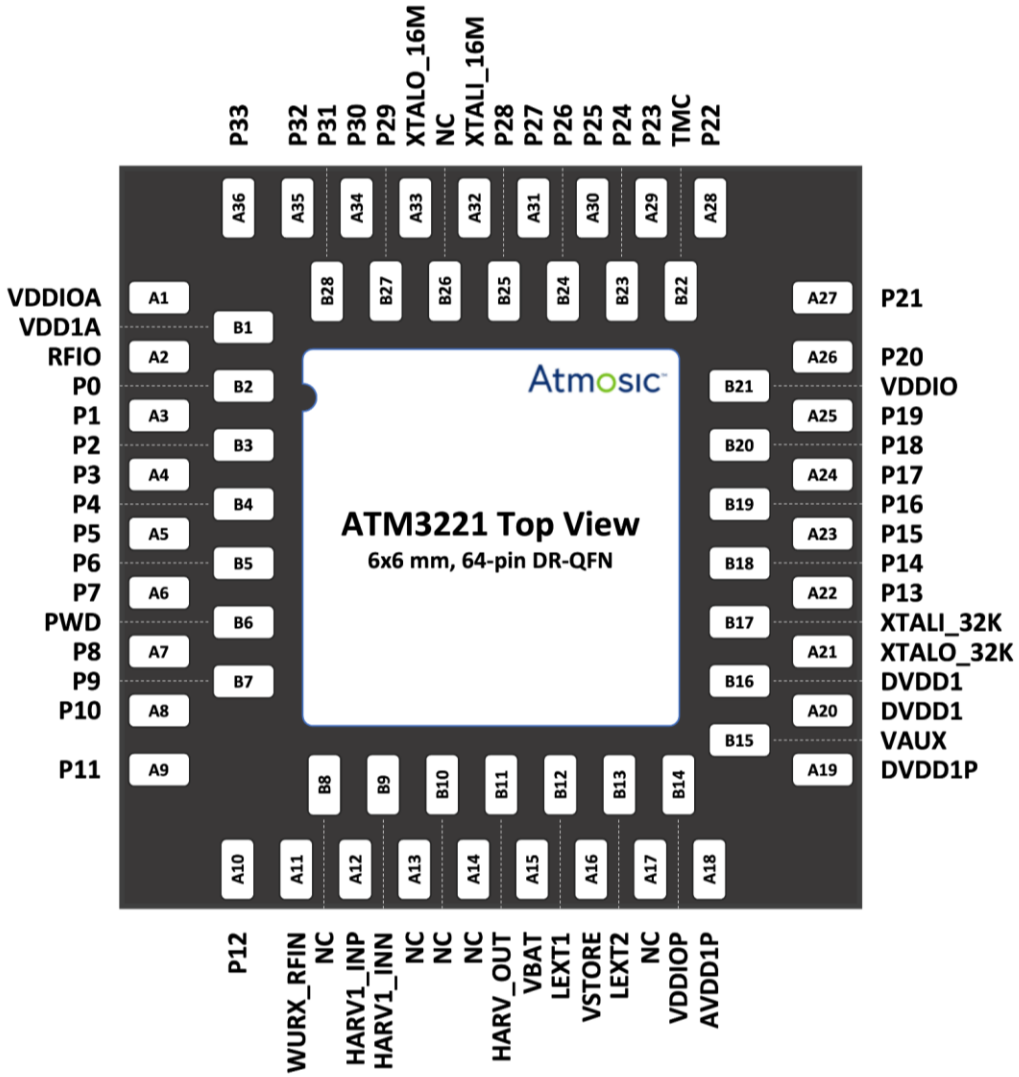
ATM3201 Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	VDD1A	PWR	Analog and RF core power supply
2	VDDIOA	PWR	Analog and RF I/O power supply
3	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
4	P0	I/O	Programmable Digital I/O (standard drive)
5	P2	I/O	Programmable Digital I/O (standard drive)
6	P1	I/O	Programmable Digital I/O (standard drive)
7	PWD	I/O	Power Down Input (Active High)
8	P9	I/O	Programmable Digital or Analog I/O (standard drive)
9	P10	I/O	Programmable Digital or Analog I/O (standard drive)
10	P11	I/O	Programmable Digital or ANalog I/O (standard drive)
11	WURX_RFIN	RF	Wakeup receiver RF input
12	HARV1_INP	RF	Differential RF Harvester Input (positive)
13	HARV1_INN	RF	Differential RF Harvester Input (negative)
14	HARV_OUT	A	Output of RF Harvester; can be used as input from other harvesting modalities to supply energy to the ATM chip
15	VBAT	PWR	Battery connection
16	LEXT1	A	Switcher Inductor
17	VSTORE	PWR	Storage node for Switching regulator
18	LEXT2	A	Switcher Inductor
19	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
20	VDDIOP	PWR	1.8 V I/O power supply generated by switcher, connect to VAUX if unused
21	VAUX	PWR	Reserved for switching regulator internal use
22	DVDD1P	PWR	1 V Digital core power supply generated by switcher
23	DVDD1	PWR	1 V Digital core power supply

24	XTALO_32k	A	32.768 kHz crystal oscillator output
25	XTALI_32k	A	32.768 kHz crystal oscillator input
26	P13	I/O	Programmable Digital I/O (standard drive)
27	P17	I/O	Programmable Digital I/O (high drive)
28	P19	I/O	Programmable Digital I/O (high drive)
29	VDDIO	PWR	Digital I/O Power Supply
30	P20	I/O	Programmable Digital I/O (high drive)
31	TMC	I/O	Test Mode Control
32	P22	I/O	Programmable Digital I/O (high drive)
33	P23	I/O	Programmable Digital I/O (high drive)
34	P24	I/O	Programmable Digital I/O (high drive)
35	P25	I/O	Programmable Digital I/O (standard drive)
36	XTALI_16M	A	16 MHz crystal oscillator input
37	XTALO_16M	A	16 MHz crystal oscillator output
38	P30	I/O	Programmable Digital I/O (standard drive)
39	P32	I/O	Programmable Digital I/O (standard drive)
40	P33	I/O	Programmable Digital I/O (standard drive)
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.2 ATM3221 Pinout

The ATM3221 is packaged in a 64-pin 6x6 mm Dual Row Quad Flat Package No Leads (DR-QFN). The pin assignment is shown Table 4.2-1. All pins are on the bottom side of the package.

Figure 3.2-1 ATM3221 64-Pin 6x6 mm DR-QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input or Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

NOTE: Highlighted in gray are signals not supported by the ATM3201 (P3, P5, P7, P8, P4, P6, P12, P15, P21, P14, P16, P18, P27, P26, P28, P29, P31).

Table 3.2-1 ATM3221 64-pin 6x6 mm DR-QFN Pin Description

ATM3221 Pin Description			
Pin Number	**Name**	**Type**	**Description**
A1	VDDIOA	PWR	Analog and RF I/O power supply
A2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
A3	P1	I/O	Programmable Digital I/O (standard drive)
A4	P3	I/O	Programmable Digital I/O (standard drive)
A5	P5	I/O	Programmable Digital I/O (high drive)
A6	P7	I/O	Programmable Digital I/O (high drive)
A7	P8	I/O	Programmable Digital I/O (standard drive)
A8	P10	I/O	Programmable Digital or Analog I/O (standard drive)
A9	P11	I/O	Programmable Digital or Analog I/O (standard drive)
B1	VDD1A	PWR	Analog and RF core power supply
B2	P0	I/O	Programmable Digital I/O (standard drive)
B3	P2	I/O	Programmable Digital I/O (standard drive)
B4	P4	I/O	Programmable Digital I/O (high drive)
B5	P6	I/O	Programmable Digital I/O (high drive)
B6	PWD	I/O	Power Down Input (Active High)
B7	P9	I/O	Programmable Digital or Analog I/O (standard drive)
A10	P12	I/O	Programmable Digital or Analog I/O (standard drive)
A11	WURX_RFIN	RF	Wakeup Rx RF Input
A12	HARV1_INP	RF	Differential RF Harvester1 Input (positive)
A13	NC	NC	No connection, must be open
A14	NC	NC	No connection, must be open
A15	VBAT	PWR	Battery supply

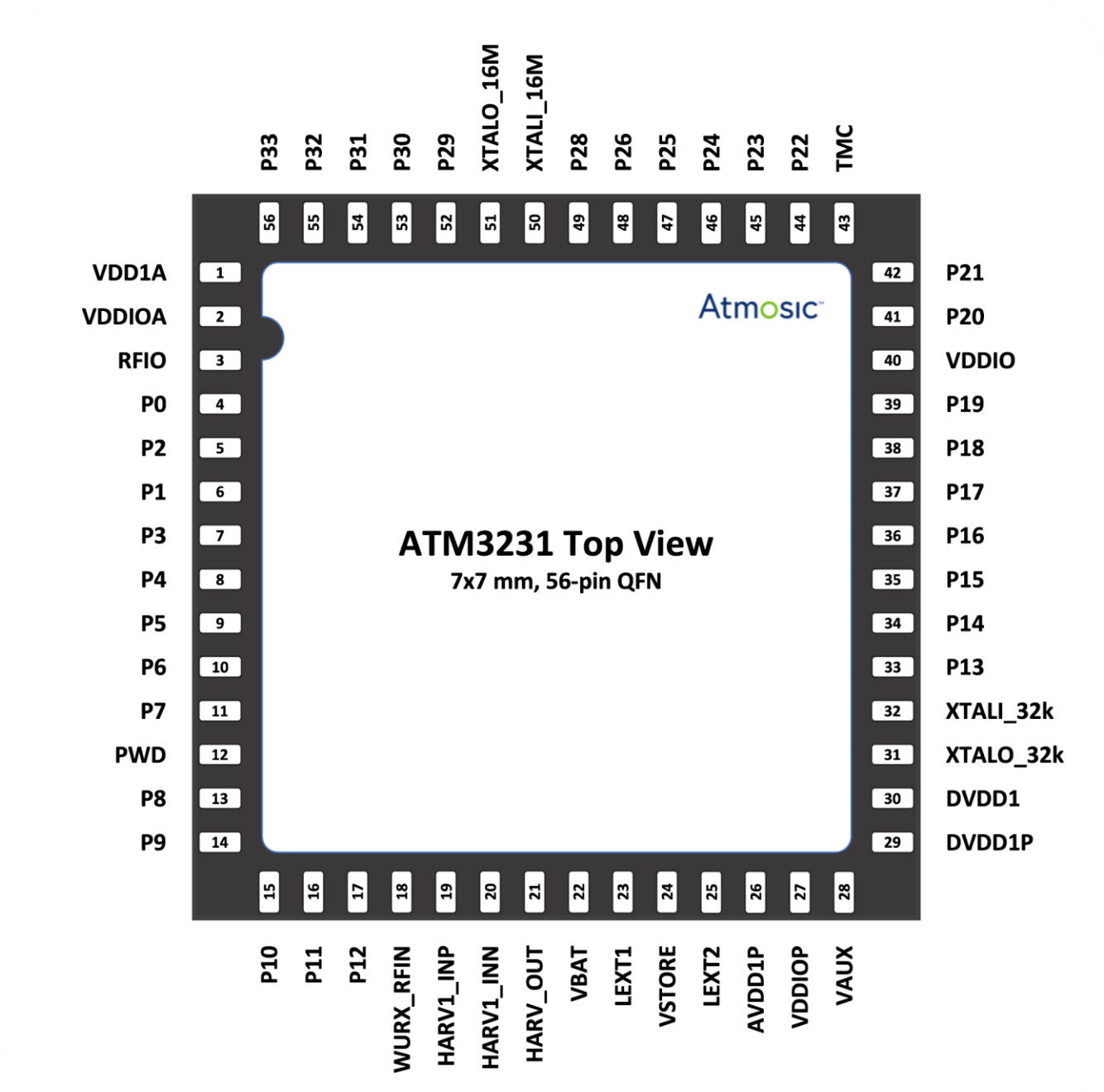
A16	VSTORE	PWR	Storage node for Switching regulator
A17	NC	NC	No connection, must be open
A18	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
B8	NC	NC	No connection, must be open
B9	HARV1_INN	RF	Differential RF Harvester1 Input (negative)
B10	NC	NC	No connection, must be open
B11	HARV_OUT	A	Output of RF Harvester; can be used as input from other harvesting modalities to supply energy to the ATM chip
B12	LEXT1	A	Switcher Inductor
B13	LEXT2	A	Switcher Inductor
B14	VDDIOP	PWR	1.8 V I/O power supply generated by switcher, connect to VAUX if unused
A19	DVDD1P	PWR	1 V Digital core power supply generated by switcher
A20	DVDD1	PWR	1 V Digital core power supply
A21	XTALO_32k	A	32.768 kHz crystal oscillator output
A22	P13	I/O	Programmable Digital I/O (standard drive)
A23	P15	I/O	Programmable Digital I/O (high drive)
A24	P17	I/O	Programmable Digital I/O (high drive)
A25	P19	I/O	Programmable Digital I/O (high drive)
A26	P20	I/O	Programmable Digital I/O (high drive)
A27	P21	I/O	Programmable Digital I/O (standard drive)
B15	VAUX	PWR	Reserved for switching regulator internal use
B16	DVDD1	PWR	1 V Digital core power supply
B17	XTALI_32k	A	32.768 kHz crystal oscillator input
B18	P14	I/O	Programmable Digital I/O (high drive)
B19	P16	I/O	Programmable Digital I/O (high drive)
B20	P18	I/O	Programmable Digital I/O (high drive)
B21	VDDIO	PWR	Digital I/O supply
A28	P22	I/O	Programmable Digital I/O (high drive)
A29	P23	I/O	Programmable Digital I/O (high drive)
A30	P25	I/O	Programmable Digital I/O (standard drive)
A31	P27	I/O	Programmable Digital I/O (standard drive)
A32	XTALI_16M	A	16 MHz crystal oscillator input
A33	XTALO_16M	A	16 MHz crystal oscillator output
A34	P30	I/O	Programmable Digital I/O (standard drive)
A35	P32	I/O	Programmable Digital I/O (standard drive)
A36	P33	I/O	Programmable Digital I/O (standard drive)
B22	TMC	I/O	Test Mode Control
B23	P24	I/O	Programmable Digital I/O (high drive)
B24	P26	I/O	Programmable Digital I/O

B25	P28	I/O	Programmable Digital I/O
B26	NC	NC	No connection, must be open
B27	P29	I/O	Programmable Digital I/O
B28	P31	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 64-pin DR-QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.3 ATM3231 Pinout

The ATM3231 is packaged in a 56-pin 7x7 mm Quad Flat Package No Leads (QFN). The pin assignment is shown in Table 4.3-1 . All pins are on the bottom side of the package.

Figure 3.3-1 ATM3231 56-Pin 7x7 mm QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
GND	Ground

Table 3.3-1 ATM3231 56-pin 7x7 mm QFN Pin Description

ATM3231 Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	VDD1A	PWR	Analog and RF core power supply
2	VDDIOA	PWR	Analog and RF I/O power supply
3	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
4	P0	I/O	Programmable Digital I/O (standard drive)
5	P2	I/O	Programmable Digital I/O (standard drive)
6	P1	I/O	Programmable Digital I/O (standard drive)
7	P3	I/O	Programmable Digital I/O (standard drive)
8	P4	I/O	Programmable Digital I/O (high drive)
9	P5	I/O	Programmable Digital I/O (high drive)
10	P6	I/O	Programmable Digital I/O (high drive)
11	P7	I/O	Programmable Digital I/O (high drive)
12	PWD	I/O	Power Down Input (Active High)
13	P8	I/O	Programmable Digital I/O (standard drive)
14	P9	I/O	Programmable Digital or Analog I/O (standard drive)
15	P10	I/O	Programmable Digital or Analog I/O (standard drive)
16	P11	I/O	Programmable Digital or Analog I/O (standard drive)
17	P12	I/O	Programmable Digital or Analog I/O (standard drive)
18	WURX_RFIN	RF	Wakeup receiver RF input
19	HARV1_INP	RF	Differential RF Harvester Input (positive)
20	HARV1_INN	RF	Differential RF Harvester Input (negative)
21	HARV_OUT	A	Output of RF Harvester; can be used as input from other harvesting modalities to supply energy to the ATM chip
22	VBAT	PWR	Battery connection
23	LEXT1	A	Switcher Inductor

24	VSTORE	PWR	Storage node for Switching regulator
25	LEXT2	A	Switcher Inductor
26	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
27	VDDIOP	PWR	1.8 V I/O power supply generated by switcher, connect to VAUX if unused
28	VAUX	PWR	Reserved for switching regulator internal use
29	DVDD1P	PWR	1 V Digital core power supply generated by switcher
30	DVDD1	PWR	1 V Digital core power supply
31	XTALO_32k	A	32.768 kHz crystal oscillator output
32	XTALI_32k	A	32.768 kHz crystal oscillator input
33	P13	I/O	Programmable Digital I/O (standard drive)
34	P14	I/O	Programmable Digital I/O (high drive)
35	P15	I/O	Programmable Digital I/O (high drive)
36	P16	I/O	Programmable Digital I/O (high drive)
37	P17	I/O	Programmable Digital I/O (high drive)
38	P18	I/O	Programmable Digital I/O (high drive)
39	P19	I/O	Programmable Digital I/O (high drive)
40	VDDIO	PWR	Digital I/O Power Supply
41	P20	I/O	Programmable Digital I/O (high drive)
42	P21	I/O	Programmable Digital I/O (standard drive)
43	TMC	I/O	Test Mode Control
44	P22	I/O	Programmable Digital I/O (high drive)
45	P23	I/O	Programmable Digital I/O (high drive)
46	P24	I/O	Programmable Digital I/O (high drive)
47	P25	I/O	Programmable Digital I/O (standard drive)
48	P26	I/O	Programmable Digital I/O (standard drive)
49	P28	I/O	Programmable Digital I/O (standard drive)
50	XTALI_16M	A	16 MHz crystal oscillator input
51	XTALO_16M	A	16 MHz crystal oscillator output
52	P29	I/O	Programmable Digital I/O (standard drive)
53	P30	I/O	Programmable Digital I/O (standard drive)
54	P31	I/O	Programmable Digital I/O (standard drive)
55	P32	I/O	Programmable Digital I/O (standard drive)
56	P33	I/O	Programmable Digital I/O (standard drive)
EPAD	VSS	GND	Ground supply for all circuits. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

4 Mechanical Drawing

4.1 ATM3201

Figure 4.1-1 ATM3201 40-Pin 5x5 mm QFN Mechanical Drawing

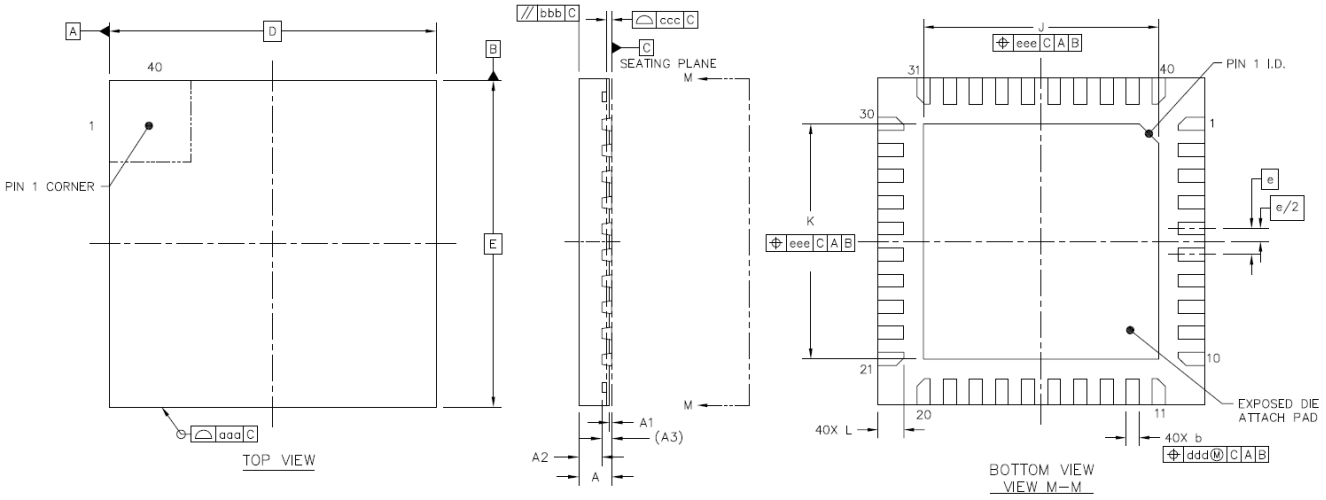


Table 4.1-1 ATM3201 40-Pin 5x5 mm QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.45	0.5	0.55
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	---	0.35	---
L/F Thickness		A3		0.152 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		5 BSC	
	Y	E		5 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	3.5	3.6	3.7
	Y	K	3.5	3.6	3.7
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads and die attached pad.

4.2 ATM3221

Figure 4.2-1 ATM3221 64-Pin 6x6 mm DR-QFN Mechanical Drawing

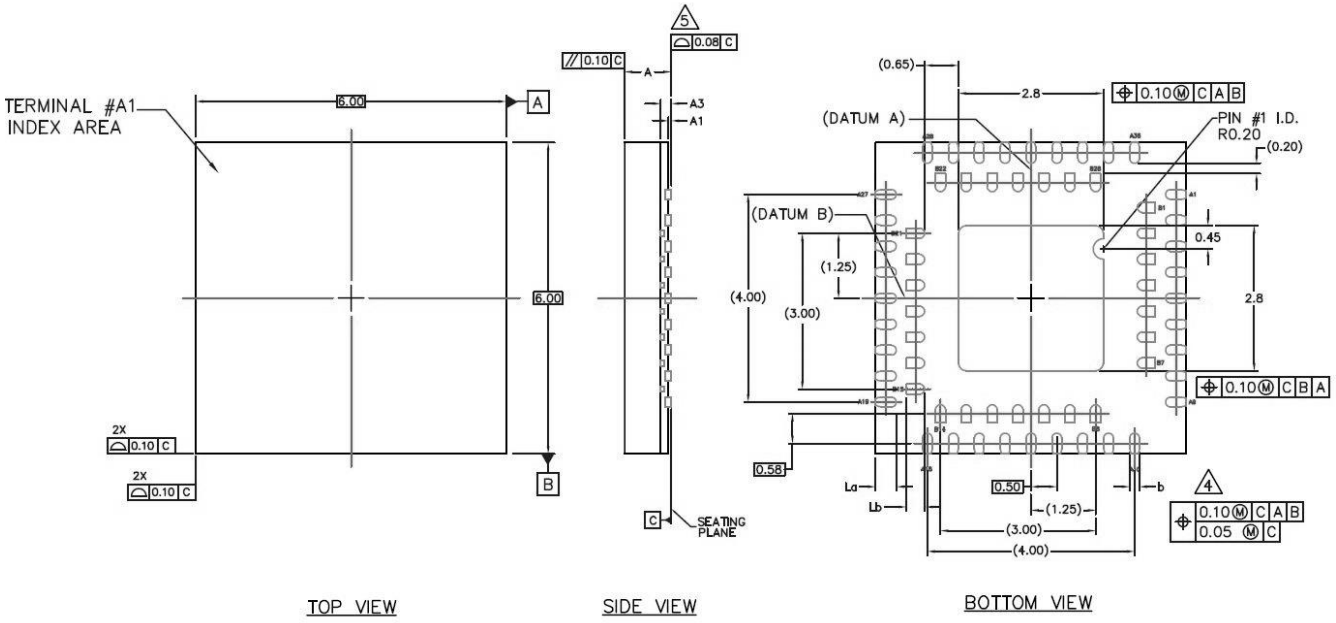


Table 4.2-1 ATM3221 64-Pin 6x6 mm DR-QFN Dimensions

Symbol	Min	Nom	Max	Note
A	0.50	0.55	0.60	---
A1	0.00	0.02	0.05	5
A3		0.152 REF		---
N	---	64	---	3
Na	---	36	---	3
Nb	---	28	---	3
La	0.30	0.40	0.50	---
Lb	0.30	0.35	0.40	4
b	0.15	0.20	0.25	4

Notes:

1. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
2. All dimensions are in millimeters, 0 is in degrees.
3. N is the total number of terminals.
   Na is the number of terminals in outer land.
   Nb is the number of terminals in inner land.
4. Dimension b applies to plated terminal and is measured between 0.10 and 0.20 mm from terminal tip.
5. Unilateral coplanarity zone applies to the exposed pad as well as the terminals.

4.3 ATM3231

Figure 4.3-1 ATM3231 56-Pin 7x7 mm QFN Mechanical Drawing

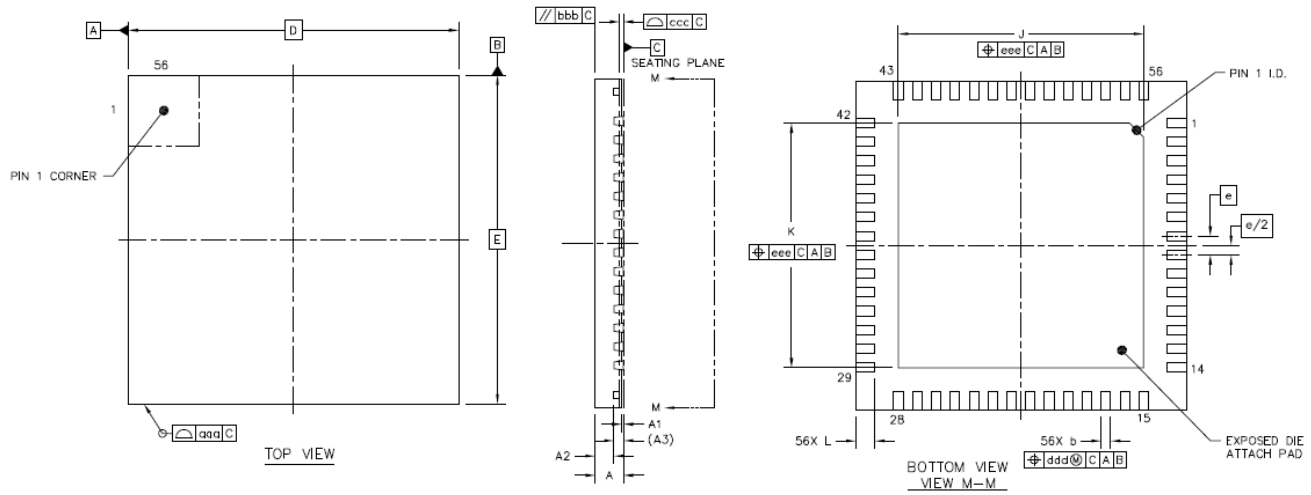


Table 4.3-1 ATM3231 56-Pin 7x7 mm QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.55	0.60	0.65
Stand Off		A1	0	---	0.05
Mold Thickness		A2	0.35	0.40	0.45
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		7 BSC	
	Y	E		7 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	5.1	5.2	5.3
	Y	K	5.1	5.2	5.3
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads and die attached pad.

5 Part Ordering

Table 5-1 Part Ordering Numbers

Part Number	Product Line	Description
ATM3201SR	Wireless MCU	5x5 mm 40-Pin QFN M3 series Bluetooth 5.0 SoC with RF energy harvesting Tape and Reel, 7” Small Reel
ATM3221SR	Wireless MCU	6x6 mm 64-Pin DR-QFN M3 series Bluetooth 5.0 SoC with RF energy harvesting Tape and Reel, 7” Small Reel
ATM3231TR	Wireless MCU	7x7 mm 56-Pin QFN M3 series Bluetooth 5.0 SoC with RF energy harvesting Tape and Reel, 13” Standard Reel

Revision History

Date	Version	Description
September 6, 2022	1.22	Update Figure 4.3-1 ATM3231 56-Pin 7x7 mm QFN Mechanical Drawing.
September 3, 2022	1.21	Updated Part Ordering Numbers.
July 14, 2022	1.20	Updated Part Ordering Numbers.
April 20, 2022	1.12	Updated Application ADC Characteristics, changed format of ATM3201 40-Pin 5x5 mm QFN Pinout (Top View), ATM3221 64-Pin 6x6 mm DR-QFN Pinout (Top View), ATM3231 56-Pin 7x7 mm QFN Pinout (Top View) pinout diagrams, corrected typos.
April 1, 2022	1.11	Changed format, corrected typos.
December 8, 2021	1.10	Added support of ATM3231, 56-pin 7x7 mm package. Updated GPIO Characteristics, Energy Harvesting, ATM3201 Pin Description, ATM3221 Pin Description, Part Ordering sections. Changed format.
April 17, 2021	1.00	Updated Electrical Specification, Part Ordering sections.
December 2, 2020	0.99	Corrected typos.
July 23, 2020	0.98	Updated CPU & Memory under SRAM, Added Wakeup Receiver Characteristics, updated Maximum Electrical Ratings, Energy Harvesting and various sections.
April 13, 2020	0.97	Corrected typos, updated Power Modes section, Power Consumption.
March 6, 2020	0.96	Updated Features, Block Diagram, PMU, Wakeup Receiver, ATM3201 Pin Description, ATM3221 Pin Description, Radio Transceiver Characteristics, added Energy Harvesting.
December 10, 2019	0.95	Updated Figure 5.1-1 and 5.2-1, added Table 5.1-1 and 5.2-1 under Mechanical Drawing section.
November 7, 2019	0.94	Added SoC Off typical power consumption under Features; updated Table 3-1, Table 3-2, and Table 3-6 under Electrical Specification; updated Table 6-1 under Part Ordering.
October 11, 2019	0.93	Updated Features, Power Modes, Power Management, Wakeup Receiver, Electrical Specification sections, minor formatting updates.
June 28, 2019	0.92	Updated section 2.11, 2.12 GPIO, UART; pins A14, A15, B16 and descriptions; Figure 4.2.
June 10, 2019	0.91	Typos corrected.

June 7, 2019	0.9	Initial version created.

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