Lead-free Green

Description

The APR348 is a secondary-side MOSFET driver for synchronous rectification, which can effectively reduce the secondary-side rectifier power dissipation and provide a high-performance solution.

The APR348 can support continuous or discontinuous conduction mode (CCM and DCM) and quasi-resonant flyback operation based on a MOSFET operating on-time control technology. This technology provides very fast turn-on and turn-off delay to reduce power loss and keep safe operation without adding any external components or circuitry. The APR348 can configure into high-side or low-side application to fit various design needs, and it can also provide high-performance solutions up to 20V output voltage application. APR348 detects load conditions and determines safe pulse generation at light loads. The APR348 power supply can be charged by VDET or VCC, depending on PLR voltage from VCC pin, and can provide a wide output operation voltage to 20V.
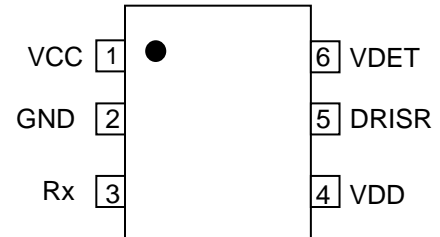
The APR348 is available in SOT26 (Type CJ) package.

Pin Assignments

(Top View)

VCC	1		6	VDET
GND	2		5	DRISR
Rx	3		4	VDD

SOT26 (Type CJ)

Features

- Synchronous Rectification Controller
- Suited for High-Side and Low-Side Flyback Converters in CCM/DCM/QR Operation
- Fast Turn-On and Turn-Off Delay
- Internal UVLO Protection
- Light Load Mode
- Eliminate Resonant Ring Interference
- Fewest External Components
- Moisture Sensitivity: MSL Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per M2003 JESD22-B102, Method 208 ⓔ3
- Weight: 0.016 grams (Approximate)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

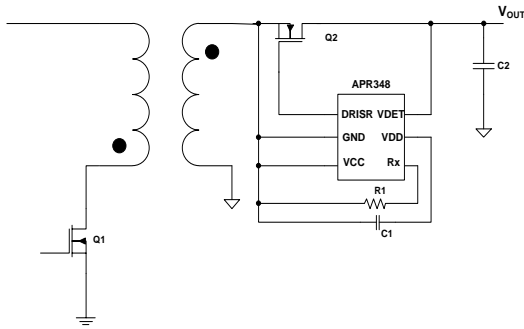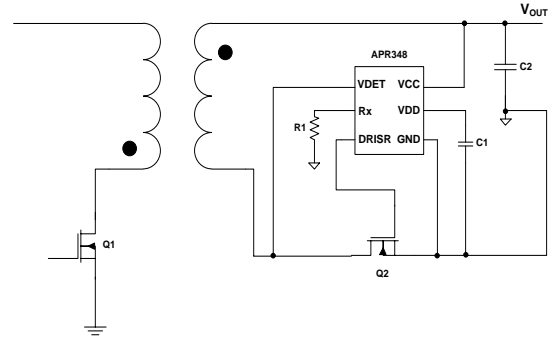## Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

High-Side Application

Low-Side Application

Pin Descriptions

Pin Number	Pin Name	Function
1	VCC	Internal Linear Regulator Input
2	GND	Ground, also used as FET source sense reference for VDET
3	Rx	Programming for Turn-On Signal by Sensing V_{DS} Slew Rate
4	VDD	Linear Regulator Output. It provides bias voltage for the internal logic circuit and the MOSFET driver. Connect this pin to a capacitor.
5	DRISR	Synchronous Rectification MOSFET Gate Drive
6	VDET	Synchronous Rectification MOSFET Drain Voltage Sense Input

Functional Block Diagram

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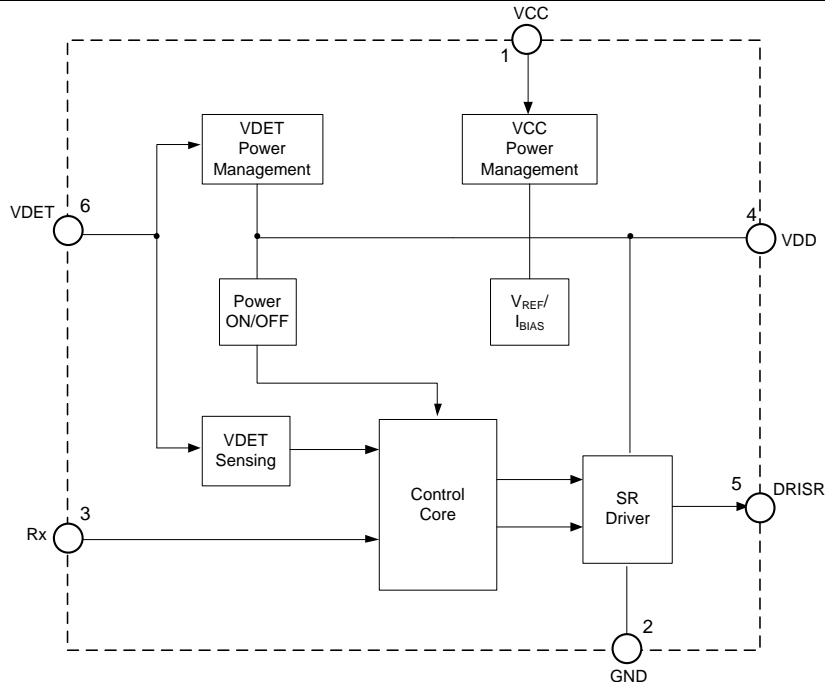
Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 28	V
V_{DET}	Voltage at VDET Pin	-0.7 to 150	V
V_{DRISR}	Voltage at DRISR Pin	-0.3 to 7	V
V_{SLOPE}	Voltage at Rx Pin	-0.3 to 7	V
P_D	Power Dissipation at T_A = +25°C	0.6	W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	197	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	76	°C/W
ESD	Human Body Model (Except VDET Pin) (Note 6)	6,000	V
	Charge Device Model	1500	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
   5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 cooling area.
   6. VDET pin are ESD sensitive. (HBM: V_{DET} = 2000V).

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	0	22	V
T_A	Ambient Temperature	-40	+85	°C

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Electrical Characteristics (@V_{CC} = 5V, T_A = -40°C <T_A<+85°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$V_{LDO\_DISABLE}$	V_{CC} LDO Disable Threshold at VCC Falling	—	4.25	4.55	4.85	V
$V_{LDO\_ENSABLE}$	V_{CC} LDO Enable Threshold at VCC Rising	—	4.35	4.65	4.95	V
V_{LDO_HYS}	LDO Operating Hysteresis at VCC Pin	—	—	100	—	mV
Supply Linear Regulator (VDD Pin)						
V_{DD}	Internal Power Supply	V_{CC} = 12V, V_{DET} = 12V	5	5.5	6	V
		V_{CC} = 3V, V_{DET} = 12V	5.3	5.9	6.5	V
$I_{STARTUP}$	V_{DD} Startup Current	V_{CC} = 0, V_{DET} = V_{DD} = V_{DD_ST} - 0.1V	—	125	160	µA
V_{DD_ST}	V_{DD} Startup Voltage	—	3.55	3.75	3.95	V
V_{DD_UVLO}	V_{DD} UVLO Voltage	—	3.30	3.50	3.70	V
$V_{UVLO\ HYSTERESIS}$	UVLO Hysteresis	—	—	0.25	—	V
I_{Q_VDD}	Quiescent Current	V_{DD} = 5.5V, V_{CC} = 0	—	170	220	µA
Synchronous Rectification MOSFET Sense (VDET Pin)						
V_{THON}	Gate Turn-On Threshold	Voltage at VDET Pin	-130	-90	-60	mV
V_{FWD}	Gate Regulation Voltage	Voltage at VDET Pin	-55	-45	-35	mV
V_{THOFF}	Gate Turn-Off Threshold	Voltage at VDET Pin	—	-7	0	mV
Slope Rate Programming (Rx Pin)						
t_{SLOPE}	Turn-On Slope Rate Detection Timer	Rx = 300kΩ, V_{DS} from 2V Falling Down	70	110	150	ns
Gate Driver (DRISR Pin)						
$V_{DRISR(High)}$	Synchronous Rectification Drive Voltage High	—	V_{DD} - 0.1	—	—	V
$V_{DSRISR(Low)}$	Synchronous Rectification Drive Voltage Low	I_{G_LOAD} = 100mA, V_{DD} = 5V	—	70	140	mV
t_{DON}	Turn-On Delay Time	C_{LOAD} = 2.2nF	—	30	60	ns
t_{DOFF}	Turn-Off Propagation Delay Time	C_{LOAD} = 2.2nF	—	25	45	ns
t_{ON_MIN}	Minimum On-Time	—	0.8	1.2	1.6	µs
I_{SOURCE}	Maximum Source Current (Note 7)	—	—	0.6	—	A
I_{SINK}	Maximum Sink Current (Note 7)	—	—	3.5	—	A
Rg	Pull-Down Impendent	I_{G_LOAD} = 100mA, V_{DD} = 5V	—	0.7	1.4	Ω

Note: 7. These parameters are guaranteed by design and characterization.

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Synchronous Rectification Principle Description

Synchronous Rectification MOSFET Turn-On

The APR348 determines the synchronous rectification MOSFET turn-on time by monitoring the MOSFET drain-to-source voltage. When the drain voltage is lower than the turn-on threshold voltage (2V), the IC begins to prepare turn-on. Because of the parasitic parameter, the voltage on the MOSFET drain pin has moderate voltage ringing, which may impact the SR controller VDET voltage sense and bring about a turn-on/off fault. To avoid this fault situation happening, the APR348 has several judge criteria to determinate whether synchronous rectification MOSFET turns on properly including:

a) A programmable V_{DET} slew rate detection to determine turn-on time
b) A minimum on-time (t_{ONMIN}) blanking period that keeps the power MOSFET on for a minimum amount of time

Figure 1 shows the turn-on blanking time t_{ONMIN}, which prevents the MOSFET drain-to-source voltage from ringing effect. When the controlled MOSFET gate turns on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator, which keeps the controlled MOSFET on for at least the minimum on-time. During the minimum on-time, the turn-off threshold is blanked unless the V_{DS} ringing voltage goes over 2V during this period.
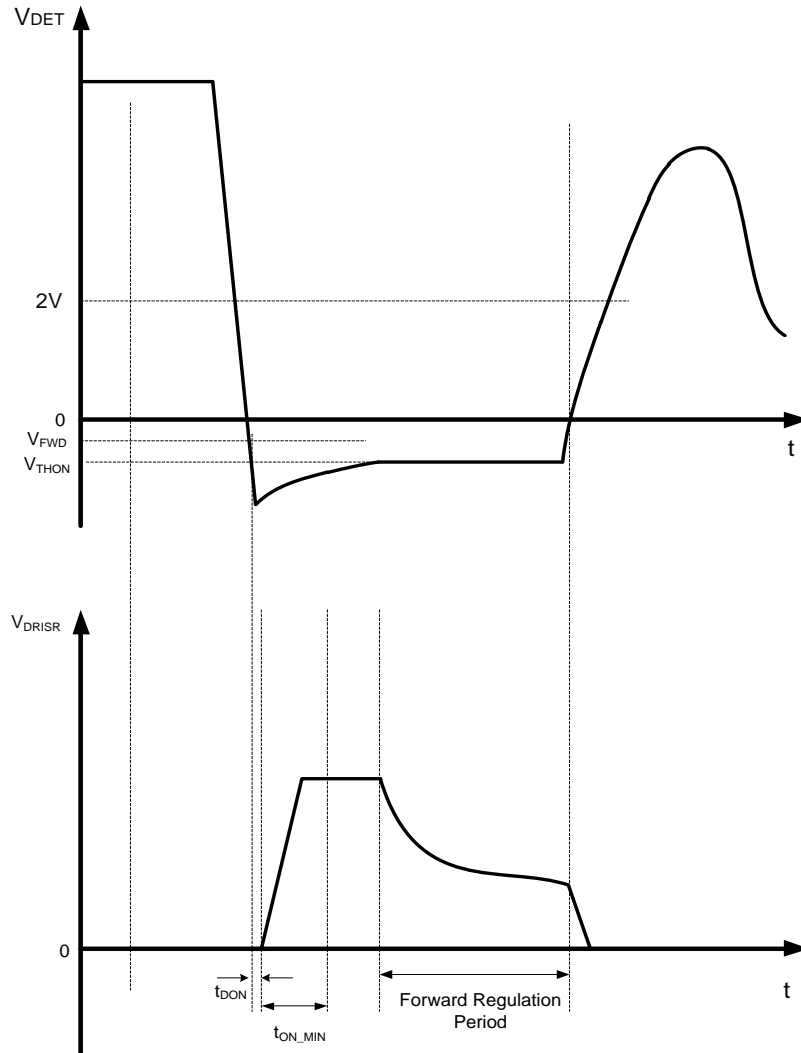
Figure 1. APR348 Switch Period

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Synchronous Rectification Principle Description (continued)

The Value and Meaning of Rx Resistance

On DCM operation after the secondary rectifier stops conduction, the primary MOSFET drain-to-source generates a ringing waveform, which results from the resonant of primary inductance and equivalent switch-device output capacitance. This ringing waveform most likely leads to the synchronous rectifier fault conduction. Therefore, along with an internal fixed volt-sec setting, the APR348 can also use a drain-to-source voltage slew rate detection to determine whether synchronous rectification MOSFET can turn on. The APR348 senses the voltage of VDET pin. The device generates a programmable t_{SLOPE} by usage of the Rx pin resistor and an internal sink current. This time calculation starts from V_{DET} = 2V, V_{DET} is compared with V_{THON} within the t_{SLOPE} time. If V_{DET} < V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). Slew-rate time, t_{SLOPE}, can be programmed with the following equation. The Rx is the resistance connected on the Rx pin.

$$t_{SLOPE} = \frac{110ns}{300K\Omega} \times \text{Rx}$$

If the Rx pin floats, an internal timer is used to set a fixed t_{SLOPE} 120ns for slew rate calculation.

Synchronous Rectification Forward Regulation and Turn-Off Stage

Once the synchronous rectification gate outputs high levels and the synchronous rectification MOSFET turns on, the secondary-side current goes through synchronous rectification MOSFET. The voltage drop on synchronous rectification MOSFET is found by $R_{DS(ON)}$ **x** secondary-side current. After minimum turn-on time t_{ONMIN}, the IC continuously monitors V_{DS} by the VDET pin and generates a pull-down current from the MOSFET gate until V_{DET} > -45mV. The MOSFET drain-to-source voltage would remain at around -45mV with the secondary-side current decreasing. Real MOSFET gate voltage depends on the MOSFET characteristics and drain current. When the primary MOSFET turns on, the secondary V_{DS} would rise up. Once V_{DET} rises to trigger the turn-off threshold, the gate signal will be pulled down to GND. The synchronous rectification MOSFET gate voltage drops quickly from a low voltage to zero after a very short turn-off delay.

Light Load Mode (LL Mode)

The APR348 provides light-load mode at light or no load when the system goes into burst or no-load mode with interval-time pulse for low standby loss. The IC internal has two timers to record 640µs and 2.5ms. When the interval-time is between 640µs and 10ms, the gate drive outputs with skipping the first two cycles. When the interval time is over 2.5ms, gate drive outputs with skipping the first eight cycles.

VDD Regulator and UVLO Protection

The VDD is an internal linear regulator output. The capacitor at VDD pin is charged from V_{DET} or V_{CC} side. When the synchronous rectification MOSFET and the IC are connected in low side, the V_{DD} is supplied by both VDET pin and VCC pin. When synchronous rectification MOSFET and IC are connected in high side, the V_{DD} is supplied only via V_{DET}. A large capacitance at VDD pin is proposed for system design. The APR348 also has the UVLO protection. When V_{DD} drops below V_{DD_UVLO}, the IC will stop working.

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Ordering Information

APR348 X - X

Product Name

Package
W6 : SOT26 (Type CJ)

Packing
7 : 7" Tape & Reel
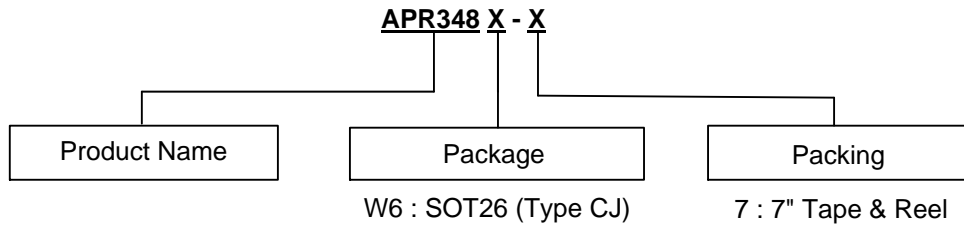
Package	Temperature Range	Part Number	Identification Code	7" Tape and Reel	
				Quantity	Part Number Suffix
SOT26 (Type CJ)	-40°C to +85°C	APR348W6-7	DY	3000/Tape and Reel	-7

Marking Information

SOT26 (Type CJ)

(Top View)

```
6   5   4
   XX Y W X
1   2   3
```
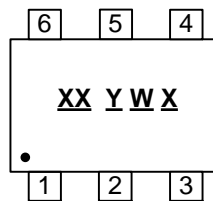
XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
     a~z : 27~52 week; z represents
     52 and 53 week
X : Internal Code

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.
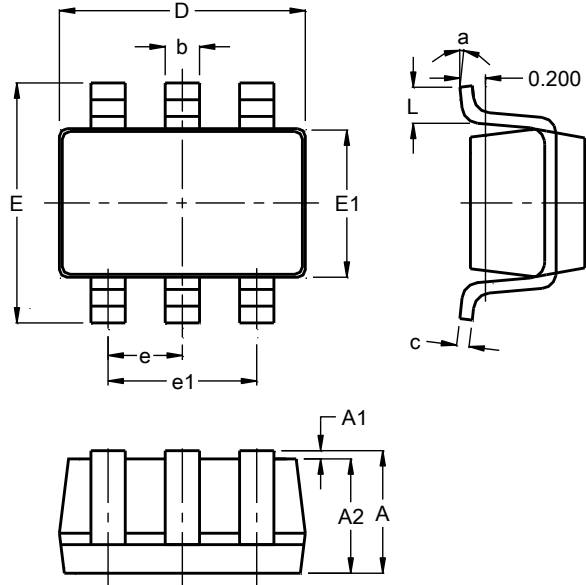
SOT26 (Type CJ)

SOT26 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	1.050	1.250	--
A1	0.00	0.10	--
A2	1.050	1.150	--
b	0.300	0.500	--
c	0.100	0.200	--
D	2.820	3.020	--
E	2.650	2.950	--
E1	1.500	1.700	--
e	0.950BSC		
e1	1.800	2.000	--
L	0.300	0.600	--
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (Type CJ)
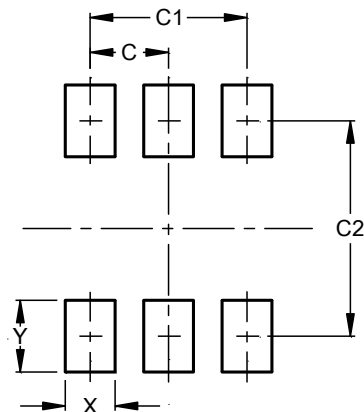
Dimensions	Value (in mm)
C	0.95
C1	1.90
C2	2.40
X	0.60
Y	1.00

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