API2155X EVB1 User Guide
Isolated Gate Drivers

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1 Introduction

The API2155X is an isolated dual-channel gate driver family with up to 4A/6A peak source/sink driving capabilities. According to different working circumstances, the API2155X family has 5V, 8V, and 12V VDD UVLO options for driving GaN, MOSFET, and IGBT/SIC. The API2155X operates with a maximum supply voltage of 30V while the input-side works in 3V to 5.5V. It has a configuration of two low-side drivers, two high-side drivers, or a half-bridge driver as the dead time between INA and INB and can be programmed with the resistor.

The API2155X family provides 5700Vrms reinforced isolation in the SO-16W and SO-14W packages, and 3000Vrms basic isolation in the SO-16 package. All models achieve a minimum of 125V/ns common-mode transient immunity (CMTI). The API2155X in the SO-14W package offers a 3.3mm minimum of channel-to-channel spacing for the secondary-side, which gives better functional isolation.

2 Features

- Isolated dual channel driver
- Input side supply voltage: 2.8V to 5.5V
- Up to 4A peak source and 6A peak sink output
- Common-mode transient immunity (CMTI) greater than 125 V/ns
- Up to 30V VDD output drive supply
- 5-V ,8-V, 12V VDD UVLO options
- Switching parameters:
  - 33ns typical propagation delay
  - 5ns maximum delay matching
  - 6ns maximum pulse-width distortion
  - 10μs maximum VDD power-up delay
- Isolation barrier life >40 Years
- Resistor-programmable dead time
- Safety-related certifications:
  - 8000-VPK (SO-14W/16W)/4242-VPK (SO-16) isolation per DIN V VDE V 0884-11:2017-01
  - 5700-VRMS (SO-14W/16W)/3000-VRMS (SO-16) isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2011
- Packaged in SO-16, SO-16W, and SO-14W (3.3mm Ch-Ch spacing)
- Operation temperature range -40 to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
  For automotive applications requiring specific change control, (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949:2016 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

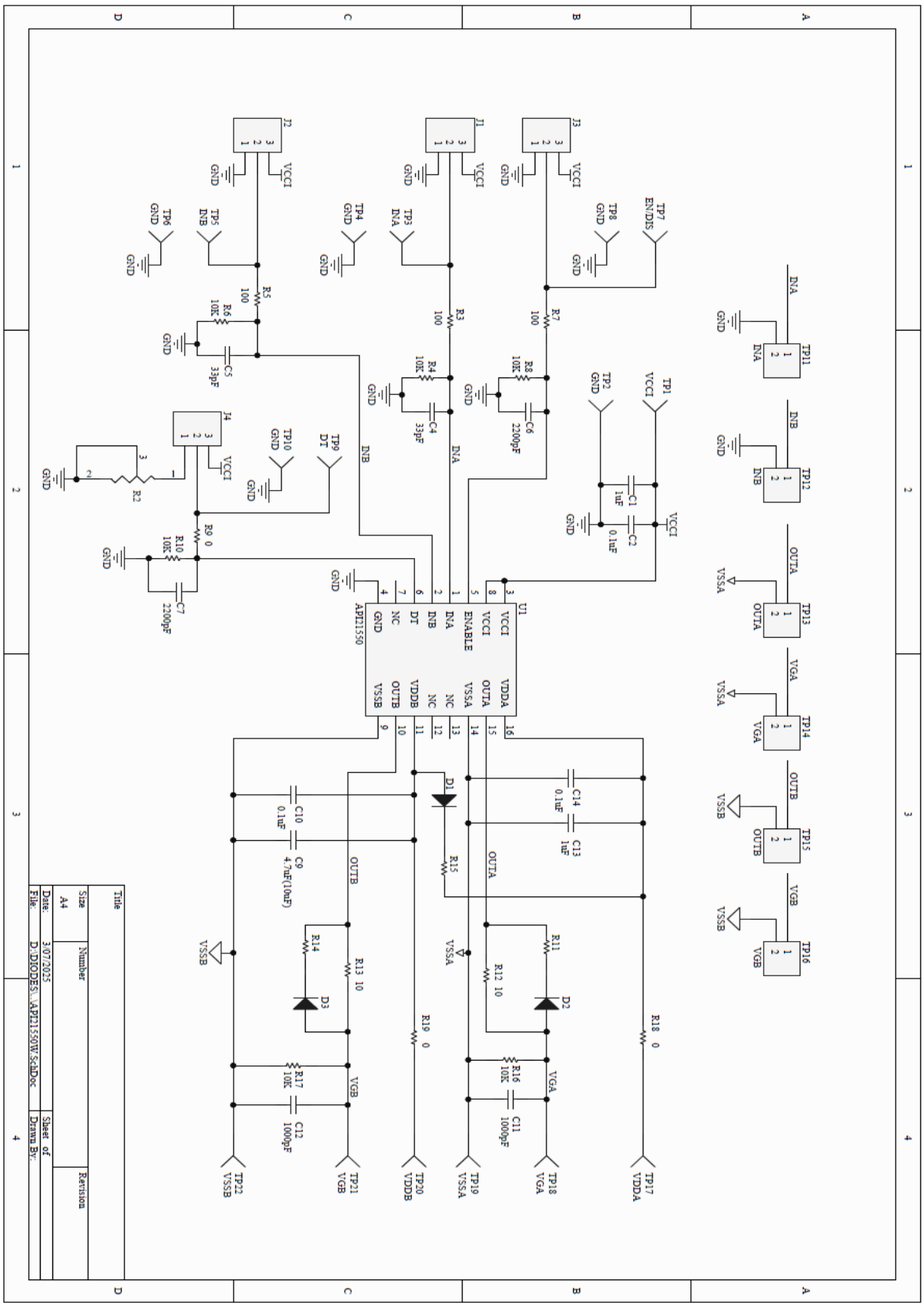
3 Description

The API2155X evaluation modules are crafted for the evaluation of SO-14W/SO-16W package dual-channel gate driver family. This family features 5700 Vrms isolation and a 4A source and 6A sink peak current, which is specifically designed to drive Si MOSFETs, IGBTs, and widebandgap (WBG) devices like SiC and GaN transistors.

The API2155X evaluation board (EVB) is equipped with three independent screw terminal blocks, dedicated to VCCI, VDDA, and VDDB respectively. For all crucial input signals like PWM INPUTs (INA, INB), dead time (DT) programming, and the enable/disable function (EN/DIS), there are 3-position headers with jumpers. This setup enables designers to effortlessly evaluate diverse protection functions. Additionally, a wide range of testing points are provided, which can support the probing of most of the key features of the API2155X.

Notably, the PCB layout has been meticulously optimized. In each gate driver loop and power supply loop, the loop area is minimized, and bypassing capacitors are incorporated. Moreover, the layout can support high-voltage testing between the primary and secondary sides, with a 3mm PCB board cutout. Significantly, the creepage distance between the two output channels has been maximized by using a bootstrap diode in the footprint of SMA. This greatly facilitates high-voltage, half-bridge testing for a broad spectrum of power converter topologies. For detailed device information, please refer to the data sheets of the API2155X, as well as Diodes Incorporated's (Diodes') isolated gate driver solutions.

4 Evaluation Board Schematic



5 Evaluation Board Layout

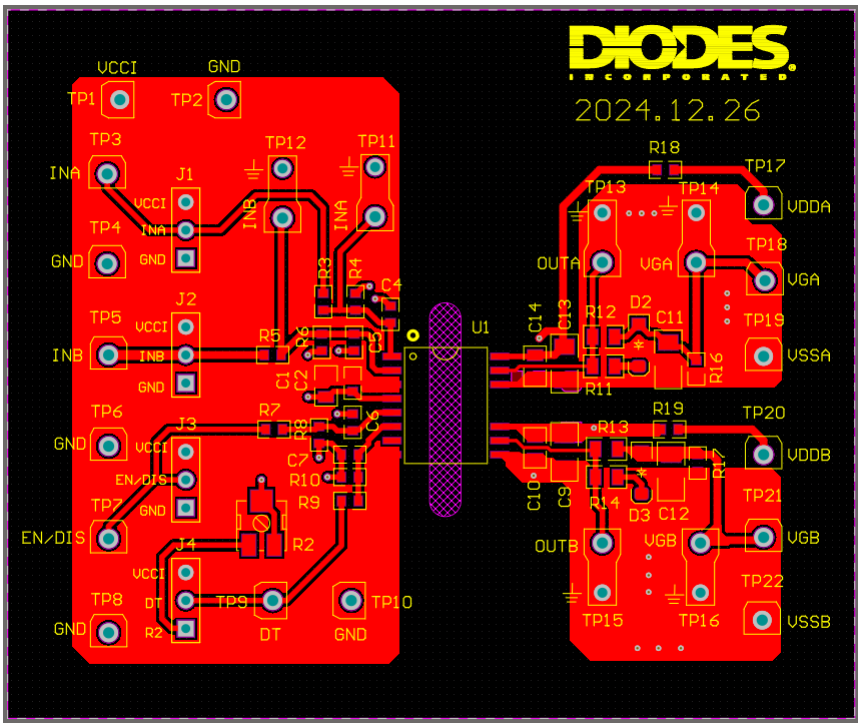


Figure 1: PCB Layout Top View

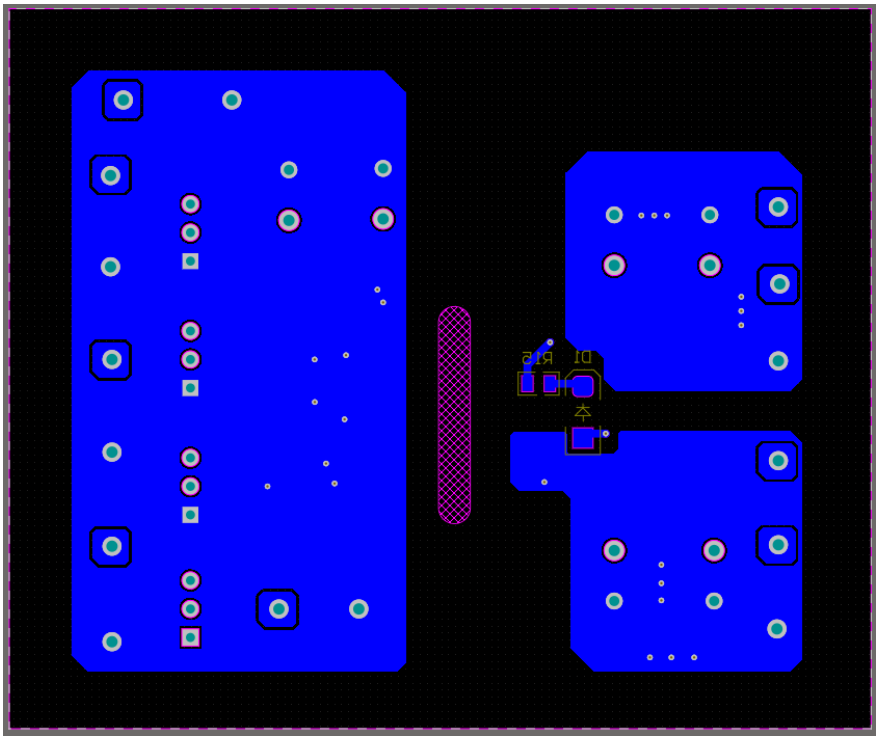


Figure 2: PCB Layout Bottom View

6 Bill-of-Materials (BOM) List

Quantity	Designator	Description	Footprint	Manufacturer
1	C1	CAP, CERM, 1uF, 25V, +/-10%, X7R	0805	STD
2	C10, C14	CAP, CERM, 0.1uF, 50V, +/-10%, X7R	0805	STD
1	C2	CAP, CERM, 0.1uF, 50V, +/-10%, X7R	0603	STD
2	C4, C5,	CAP, CERM, 33pF, 25V, +/-10%, X7R	0603	STD
2	C6, C7	CAP, CERM, 2.2nF, 25V, +/-10%, X7R	0603	STD
1	C9	CAP, CERM, 4.7uF, 50V, +/-10%, X7R	1206	STD
1	C13	CAP, CERM, 1uF, 50V, +/-10%, X7R	1206	STD
2	C11, C12	CAP, CERM, 1nF, 50V, +/-10%, X7R	1206	STD
1	D1	DIODE, Ultrafast, 600V, 1A, ES1J	SMA	Not Populated
2	D2, D3	DIODE, Schottky, 30V, 1A, ACE-Q101	SOD-123	Not Populated
4	J1, J2, J3, J4	Header, 2.54mm, 3X1, tin	TH	STD
1	R2	Trimmer,100K, 0.25w, 3314j-1-104E	SMD	Not Populated
3	R3, R5, R7	RES, 100, 1%, 0.1W	0603	STD
6	R4, R6, R8, R10, R16, R17	RES, 10K, 1%, 0.1W	0603	STD
3	R9, R18, R19	RES, 0, 1%, 0.1W	0603	STD
3	R11, R14, R15	RES, 3.9, 1%, 0.125W	0805	Not Populated
2	R12, R13	RES, 10, 1%, 0.5W	0805	STD
16	TP1~10, TP17~22	Socket	Probe	STD
6	TP11~16	Test Point	Probe	Not Populated
1	U1	API2155X	SO-16W	STD

7 Board Interface—Jumpers Setting

Pins	Description
J1	Jumper not installed, INA signal provided by external signal and this pin is default low if left open. Jumper on J1-INA and J1-GND set INA low. Jumper on J1-INA and J1-VCCI set INA high.
J2	Jumper not installed, INB signal provided by external signal and this pin is default low if left open. Jumper on J1-INB and J1-GND set INB low. Jumper on J1-INB and J1-VCCI set INB high.
J3	Jumper not installed, the devices are enabled by external signal when left open on enable/disable pin. Jumper on J3-EN/DIS and J3-GND set low. Jumper on J3-EN/DIS and J3-VCCI set high.
J4	Jumper on J4-DT and J4-VCCI, interlock with 10-ns dead time. Jumper on J4-DT and J4-R2 (trimmer potentiometer) set the dead time by DT (ns) = 10 × R2 (kΩ) when R2 is 500Ω≤R2≤100kΩ. If DT pin floating, RDT>100kΩ, DT pin connect to GND or RDT<500Ω, dead time always is around 10ns.
TP1	Primary VCC input
TP2/TP4/TP6/TP8/TP10	Primary Ground input
TP3	INA signal input
TP5	INB signal input
TP7	EN/DIS signal input
TP9	Dead-time programing
TP17	VDDA secondary side supply
TP18	VGA driver output
TP19	VSSA secondary side ground
TP20	VDDB secondary side supply
TP21	VGB driver output
TP22	VSSB secondary side ground

8 Electrical Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCI	Input Power Supply Voltage	3	-	5.5	V
VDDA, VDDB	Output power supply for API21550A	6.5	-	25	V
	Output power supply for API21550B	9.2	-	25	V
	Output power supply for API21550C	14.5	-	25	V
FS	Switching frequency	0	-	5	MHz
TJ	Operating junction temperature range	-40	-	125	°C

9 Test Equipment

Power Supplies

Three DC power supplies with voltage/current above 25 V/1 A (for instance, GW Instek PSM3004).

Signal Generators

One two-channel signal generator over 25MHz (for instance, RIGOL DG5352)

Digital Multi Meter

Two digital multi meters above 4 1/2 digit multi meters (for instance, Agilent 34401A)

Oscilloscope

One oscilloscope with bandwidth 500MHz or above 500MHz (for instance, LECROY 66MXs-B)

10 Bench Setup

The bench setup diagram includes power supplies, a signal generator, an oscilloscope, and digital multi meters. The equipment are connected as follows. To achieve more accurate test data, it is recommended that the oscilloscope bandwidth is 500MHz or higher.

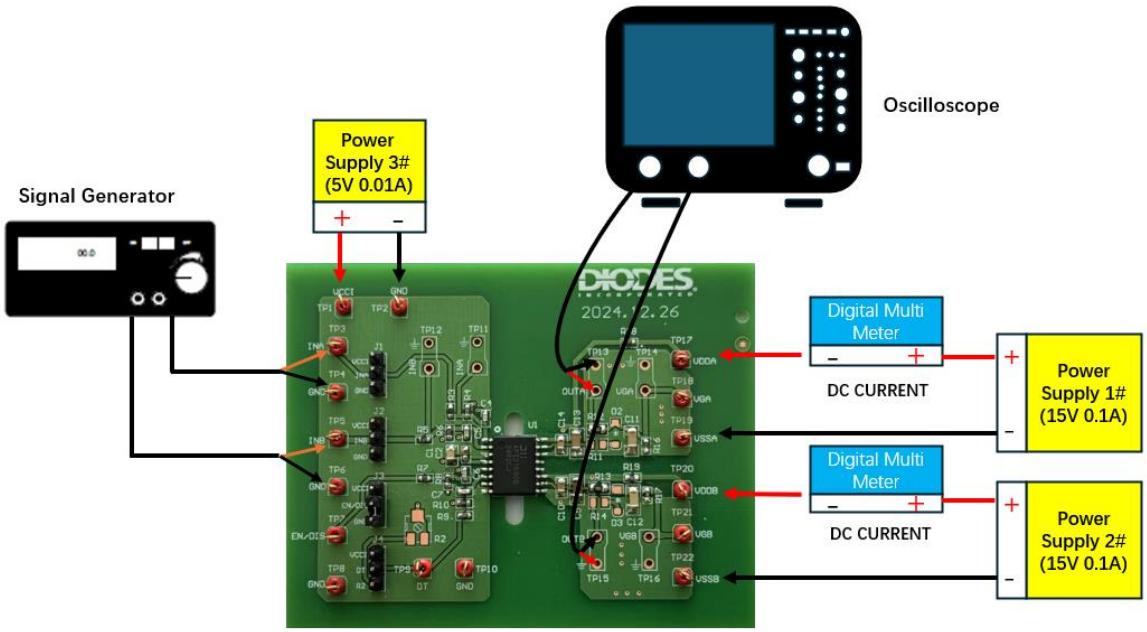


Figure 3: Bench Setup Diagram and Configuration

11 Power-Up and Power-Down Sequence

Power Up

All equipment is connected as shown in the above figure and have been configured; power-up sequence is as follows:

1. Enable power supply #3.
2. Enable power supply #1 and #2. If the DC current range on the two digital multi-meters is from 1mA to 3mA , the setup is OK.
3. Enable the signal generator, then the OUTA and OUTB will output.

Power Down

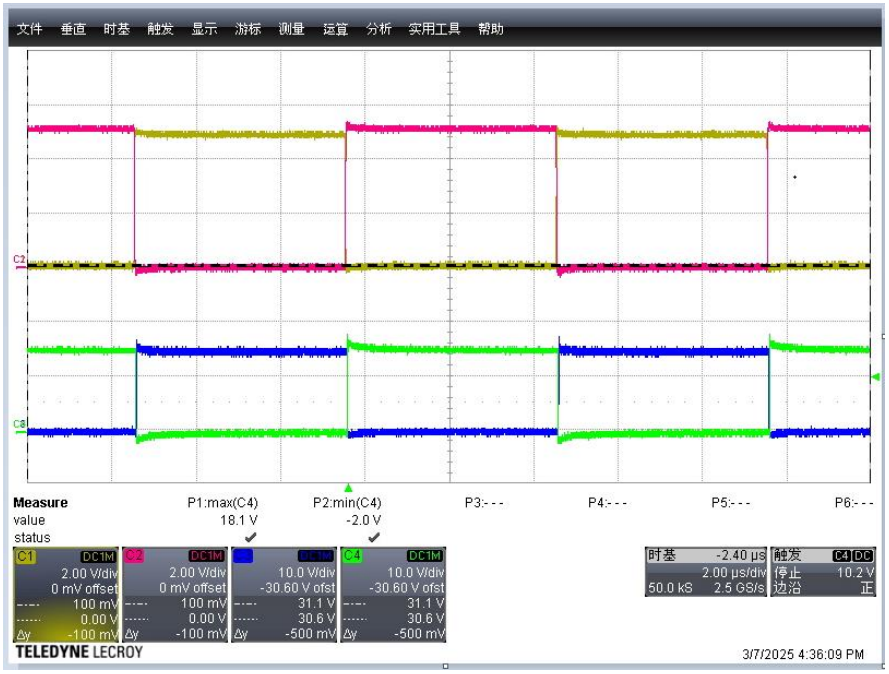
1. Disable signal generator.
2. Disable power supply #1 and #2.
3. Disable power supply #3.
4. Disconnect wires and probes.

12 Test Waveforms

The test condition of the following waveforms is CL=0pF with different RDT.

Channel 1 is INA. Channel 2 is INB. Channel 3 is OUTA. Channel 4 is OUTB.

DT Pin Floating



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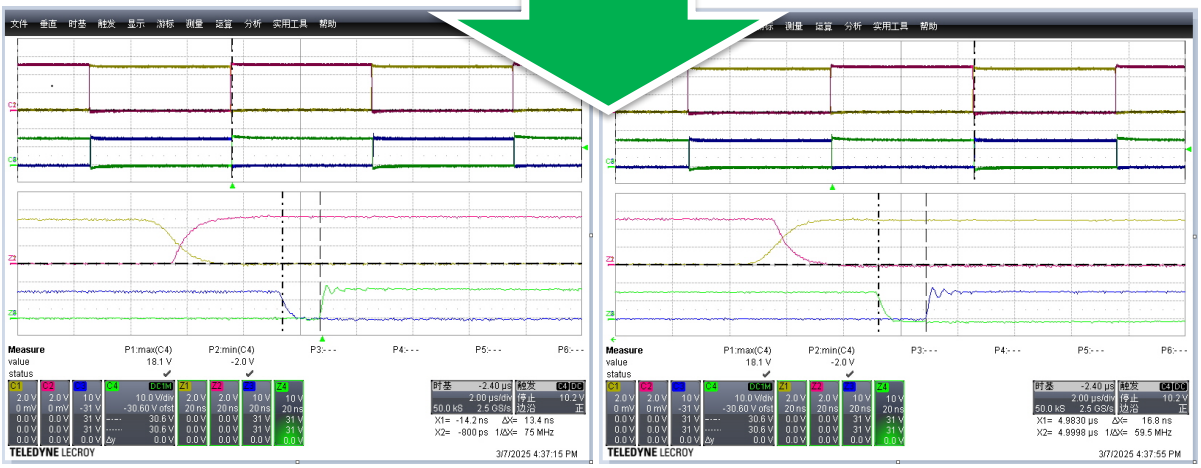
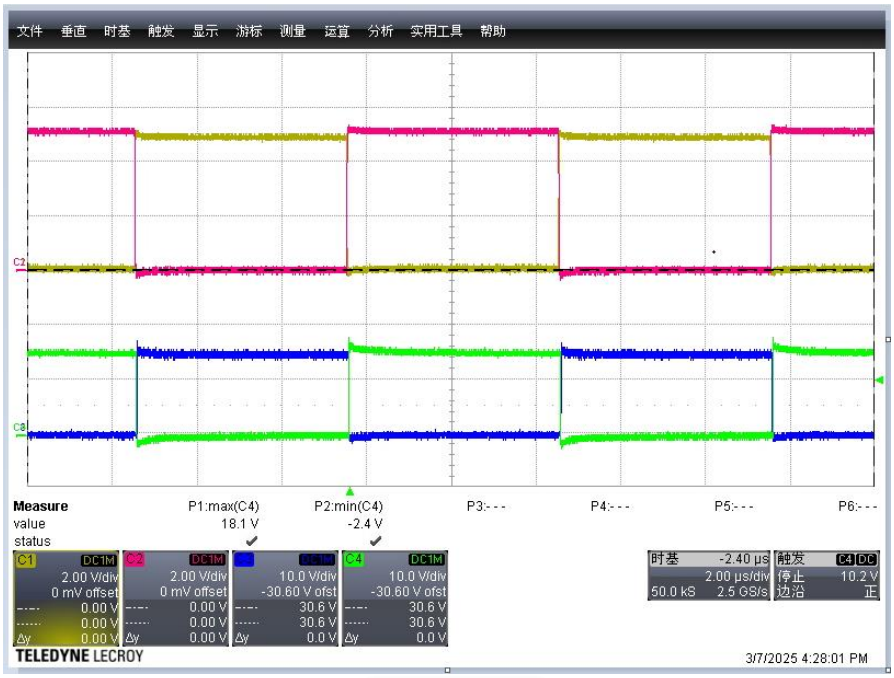


VCCI connect to DT pin



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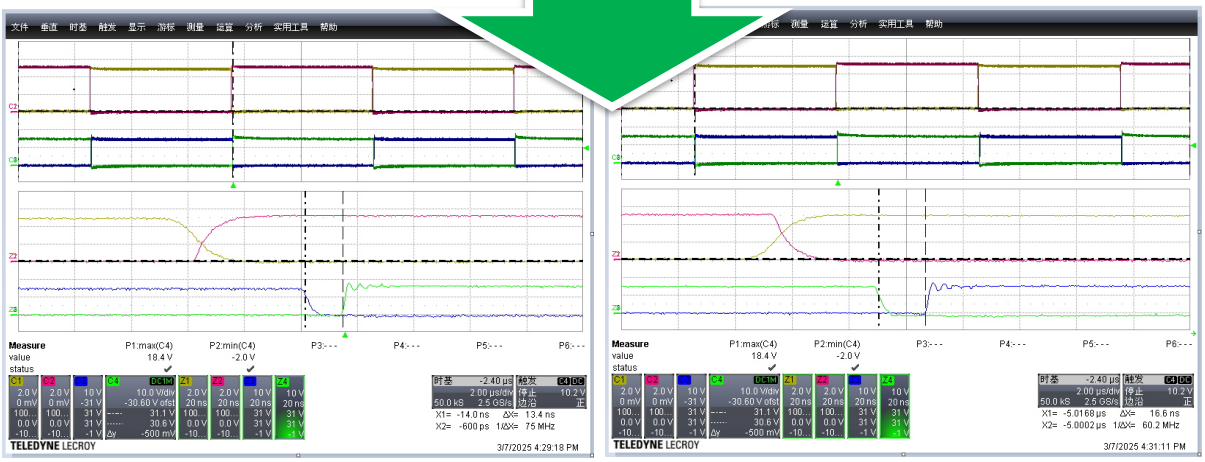
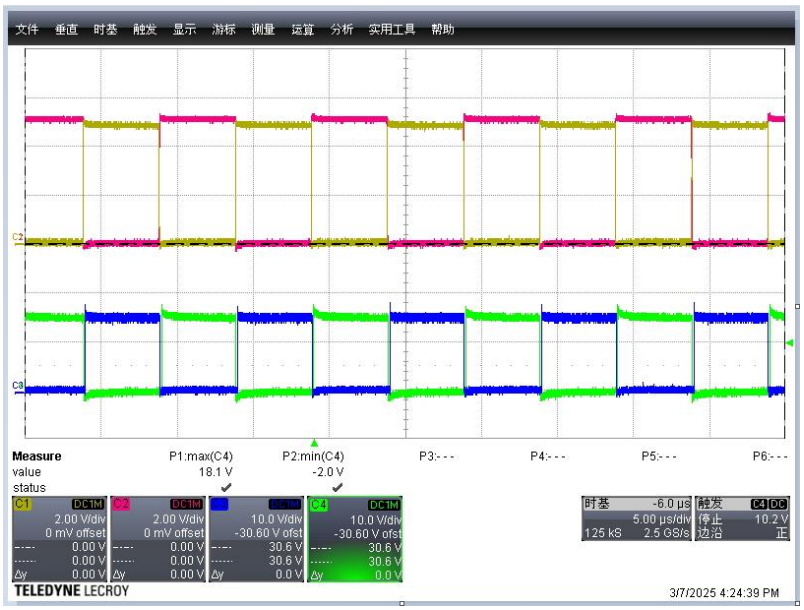


10k Resistor Connect to DT Pin



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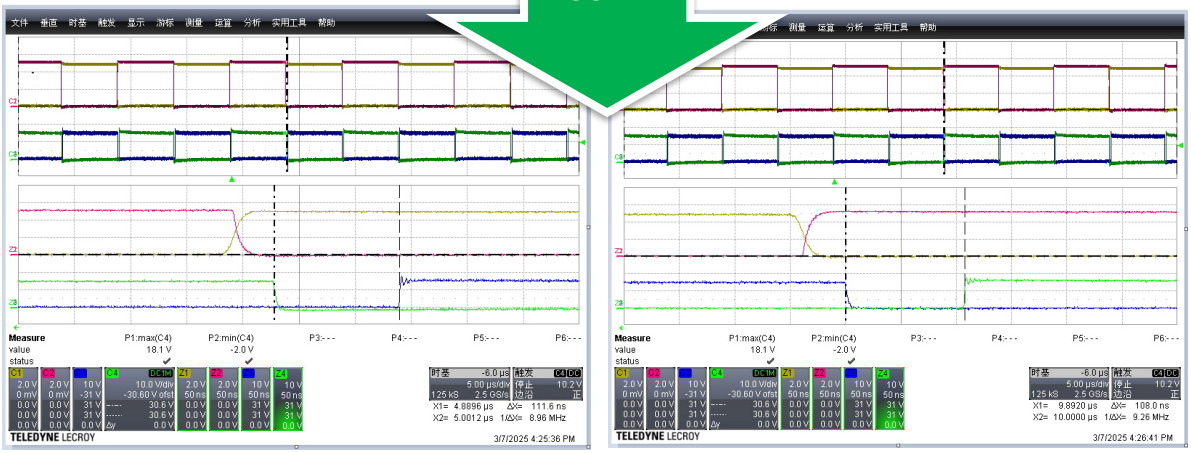

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