Description

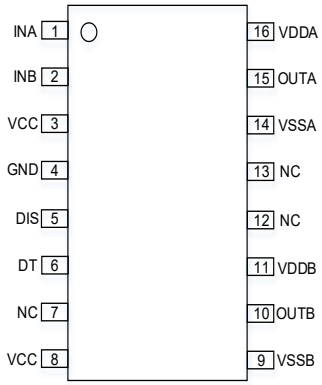
The API21550Q is an isolated high-side/low-side gate driver family with up to 4A/6A peak source/sink driving capability. According to different working circumstances, the API21550Q has 5V, 8V, 12V VDD UVLO options for driving GaN, MOSFET, and IGBT/SIC. The API21550Q operates with a maximum supply voltage of 25V for VDD while the input side works in 3V to 5.5V.

The API21550Q is designed to transfer input signal to output drive signal with short propagation delay and minimum pulse-width distortion. It also provides shoot-through protection with programmable dead time, and the external disable function improves the flexibility for application. An integrated 14ns deglitch filter effectively makes the driver immune from noise interference.

The API21550Q provides 5700V_{RMS} reinforce isolation in SO-16W (Type CJ) package. All models can achieve a minimum of 125-V/ns common-mode transient immunity (CMTI).

Pin Assignments

SO-16W (Type CJ)



Top View

Features

- Isolated H/L Half-Bridge Gate Driver
- Input Side Supply Voltage VCC: 3V to 5.5V
- Up to 4A Peak Source and 6A Peak Sink Current Output
- Common-Mode Transient Immunity (CMTI) Greater than 125V/ns
- Up to 25V VDD Output Drive Supply
- 5V, 8V, 12V VDD UVLO Options
- Switching Parameters:
  - 40ns Typical Propagation Delay
  - 8ns Maximum Delay Matching
  - 7ns Maximum Pulse-Width Distortion
  - 10μs Maximum VDD Power-up Delay
- Isolation Barrier Life > 40 Years
- Shoot-Through Protection and Resistor-Programmable Dead Time
- 14ns Integrated Deglitch Filter
- Active Pulldown Feature
- Safety-Related Certifications:
  - 8000-V_{PK} SO-16W (Type CJ) per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5700-V_{RMS} SO-16W (Type CJ) for 1 Minute per UL 1577
  - CQC Certification per GB4943.1
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1
  - Device HBM ESD 4kV
  - Device CDM ESD 1.5kV
- Packaged in SO-16W (Type CJ)
- Operation Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The API21550Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- HEV and EV on-board chargers
- Motor drives in automotive
- Inverter control in HEV and EV
- Isolated DC-to-DC converters in automotive

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

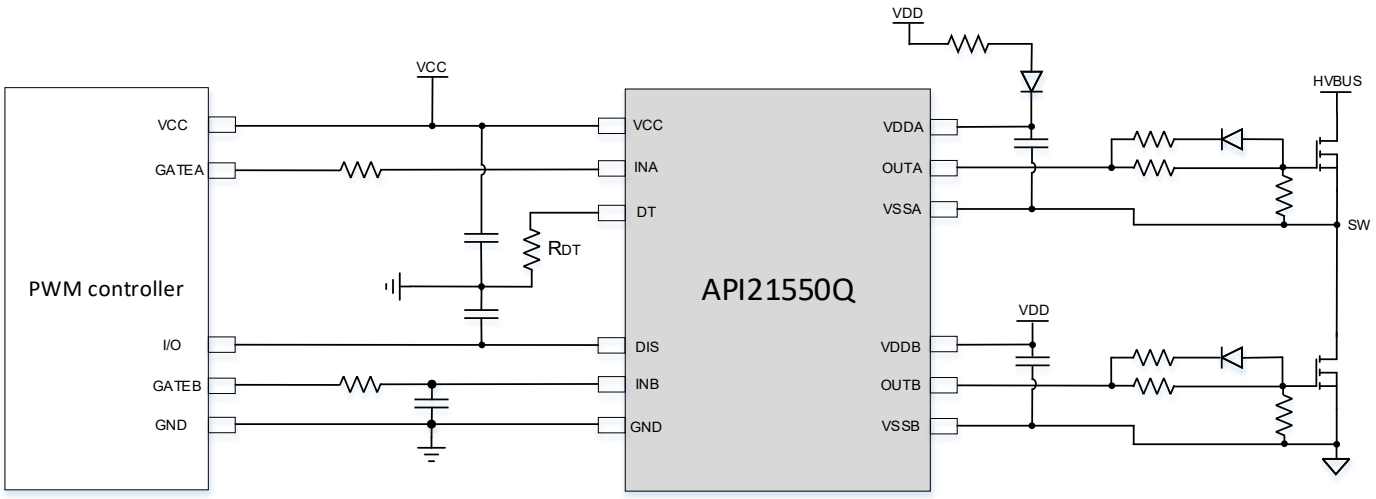


Figure 1. Typical Application Circuit of API21550Q

Pin Descriptions

Pin Name	Pin Number	Function
	SO-16W (Type CJ)	
INA	1	TTL/CMOS compatible input signal for channel A with internal pulldown to GND. It is recommended to connect this pin to GND if not used.
INB	2	TTL/CMOS compatible input signal for channel B with internal pulldown to GND. It is recommended to connect this pin to GND if not used.
VCC	3, 8	Input supply voltage. It is recommended to place a capacitor from VCC to GND as close as possible.
GND	4	Input ground
DIS	5	Disables the driver outputs if pulled to high, enables driver outputs if pulled to low or left open. It is recommended to connect this pin to GND if not used.
DT	6	Programmable dead time control. Connect a resistor (R_{DT}) between DT and GND to setup dead time: t_{DT} (ns) = 10 x R_{DT} (kΩ). R_{DT} is recommended between 1kΩ and 100kΩ.
VSSB	9	Ground for output channel B
OUTB	10	Output of driver B
VDDB	11	Output supply voltage for channel B
NC	7, 12, 13	Not connected
VSSA	14	Ground for output channel A
OUTA	15	Output of driver A
VDDA	16	Output supply voltage for channel A

Functional Block Diagram

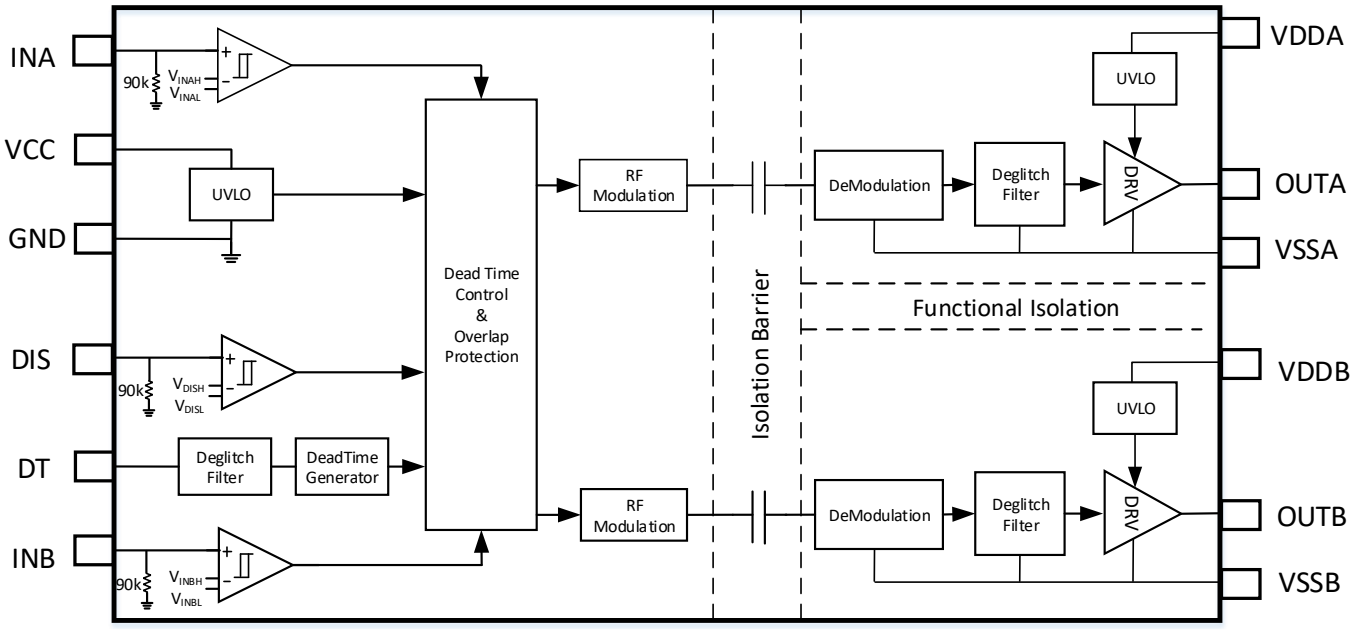


Figure 2. Functional Block Diagram of API21550Q

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{VCC}	Input Power-Supply Voltage	-0.3 to 6	V
V_{VDDA}, V_{VDDB}	Output Power-Supply Voltage	-0.3 to 30	V
V_{INA}, V_{INB}, V_{DT}, V_{DIS}	Input Signal Voltage	-0.3 to V_{Vcc} +0.3	V
	Input Signal Voltage, Transient for 200ns	-2 to V_{Vcc} +0.3	
V_{OUTA}, V_{OUTB}	Output Signal Voltage	-0.3 to $V_{VDDA/B}$ +0.3	V
	Output Signal Voltage, Transient for 200ns	-2 to $V_{VDDA/B}$ +0.3	
V_{VSSA}, V_{VSSB}	Channel to Channel Isolation Voltage SO-16W (Type CJ)	1500	V
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
ESD	Human Body Model	±4000	V
ESD	Charged Device Model	±1500	V

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Power-Supply Voltage	3	5.5	V
V_{VDDA}, V_{VDDB}	Output Power-Supply Voltage (API21550AQ)	6.5	25	V
	Output Power-Supply Voltage (API21550BQ)	9.2	25	V
	Output Power-Supply Voltage (API21550CQ)	14.5	25	V
T_A	Ambient Temperature	-40	+125	°C

Package Thermal Information

Symbol	Parameter	SO-16W (Type CJ)	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance	65.8	°C/W
$R_{\theta JC(top)}$	Junction to Case Thermal Resistance	28.1	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	23.2	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	7.35	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	31.3	°C/W

Power Ratings

Symbol	Parameter	Test Condition	Max	Unit
P_D	Maximum Power Dissipation (Both Sides)	VCCI = 5V, VDDA/VDDB = 20V, INA/B = 3.3V, 460kHz 50% duty cycle square wave, C_L = 2.2nF, T_J = +150℃, T_A = +25℃	950	mW
P_{DI}	Maximum Power Dissipation by Transmitter Side		50	mW
P_{DA}, P_{DB}	Maximum Power Dissipation by Each Driver Side		450	mW

Insulation Specifications

Symbol	Parameter	Condition	SO-16W (Type CJ)	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance Through the Insulation	Minimum internal gap (internal clearance)	26	µm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
—	Material Group	According to IEC 60664-1	I	—

Insulation Specifications (continued)

Symbol	Parameter	Condition	SO-16W (Type CJ)	Unit
DIN EN IEC 60747-17 (VDE 0884-17) (Note 5)				
V_{IORM}	Maximum Repetitive Peak Isolation Voltage	AC voltage	2121	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	8000	V_{PK}
V_{IMP}	Maximum Impulse Voltage	Tested in air, 1.2/50-μs waveform per IEC 62368-1	8000	—
V_{IOSM}	Maximum Surge Isolation Voltage	$V_{IOSM} \geq 1.6 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-μs waveform, per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent Charge	Method a, After I/O safety test subgroup 2/3. Vini = V_{IOTM}, tini = 60s; Vpd(m) = 1.2 x V_{IORM}, tm = 10s	< 5	pC
		Method a, After environmental tests subgroup 1. Vini = V_{IOTM}, tini = 60s; Vpd(m) = 1.6 x V_{IORM}, tm = 10s	< 5	pC
		Method b1; At routine test (100% production) and preconditioning (type test) Vini = 1.2 × V_{IOTM}; tini = 1s; Vpd(m) = 1.875 x V_{IORM}, tm = 1s	< 5	pC
C_{IO}	Barrier Capacitance, Input to Output	V_{IO} = 0.4 sin (2πft), f = 1MHz	1.2	pF
R_{IO}	Isolation Resistance, Input to Output	V_{IO} = 500V at T_A = +25°C	> 10^{12}	Ω
		V_{IO} = 500V at +100°C ≤ T_A ≤ +125°C	> 10^{11}	
		V_{IO} = 500V at T_S = +150°C	> 10^{9}	
—	Pollution Degree	—	2	—
—	Climatic Category	—	40/125/21	—
UL 1577				
V_{ISO}	Withstand Isolation Voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5700	V_{RMS}

Note: 5. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Safety-Related Certifications

Packages	VDE	UL	CQC
	DIN EN IEC 60747-17 (VDE 0884-17)	UL 1577	GB 4943.1
SO-16W (Type CJ)	Reinforced insulation at V_{IORM} = 2121V_{PEAK} V_{IOSM} = 10400V_{PEAK} V_{IOTM} = 8000V_{PEAK}	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced insulation
—	Certificate planned	E550819	Certificate planned

Safety- Limiting Values

Symbol	Parameter	Condition	Side	SO-16W (Type CJ)	Unit
I_S	Safety Output Supply Current	T_J = +150°C, T_A = +25°C $V_{VDDA/B}$ = 15V, T_A = +25°C	DRIVER A/ DRIVER B	61	mA
P_S	Safety Output Supply Power	T_J = +150°C, T_A = +25°C	INPUT	50	mW
			DRIVER A/ DRIVER B	925	
			Total	1900	
T_S	Safety Temperature	—	—	+150	°C

Electrical Characteristics

(V_{CC} = 3.3V, 0.1μF capacitance from VCC to GND, V_{VDDA} = V_{VDDB} = 12V for API21550A/BQ, V_{VDDA} = V_{VDDB} = 15V for API21550CQ, 1μF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin connected to VCC except DT test, DIS short to GND, T_A = -40°C to +125°C, C_L = 0, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
I_{VCCQ}	VCC Quiescent Current	V_{INA} = V_{INB} = 0, V_{CC} = 5V	—	1.5	2.5	mA
I_{VDDAQ}, I_{VDDBQ}	VDDA and VDDB Quiescent Current	V_{INA} = 0, V_{INB} = 0	—	1.4	3.7	mA
I_{VCC}	VCC Operating Current	V_{INA}/V_{INB} swing between 0 and V_{CC} with f = 500kHz, 50% duty cycle	—	2.7	4.6	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB Operating Current	V_{INA}/V_{INB} swing between 0 and V_{CC} with f = 500kHz, 50% duty cycle, C_L = 100pF	—	3	5	mA
VCC SUPPLY UNDERVOLTAGE THRESHOLD						
V_{VCC_ON}	VCC UVLO Rising Threshold	—	2.55	2.7	2.85	V
V_{VCC_OFF}	VCC UVLO Falling Threshold	—	2.35	2.5	2.65	V
V_{VCC_HYS}	VCC UVLO Threshold Hysteresis	—	—	0.2	—	V
t_{VCCF}	VCC UVLO Deglitch Filter	(Note 6)	—	1.7	—	μs
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLD AND DELAY						
V_{VDD_ON}	VDD UVLO Rising Threshold	API21550AQ	5.7	6.0	6.3	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		5.4	5.7	6.0	
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis			0.3		
V_{VDD_ON}	VDD UVLO Rising Threshold	API21550BQ	7.7	8.5	8.9	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		7.2	7.9	8.4	
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis			0.6		
V_{VDD_ON}	VDD UVLO Rising Threshold	API21550CQ	11.3	12.2	13.4	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		10.3	11.1	12.0	
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis			1.1		
t_{VDDF}	VDDx UVLO Deglitch Filter	(Note 6)	—	0.3	—	μs
INA, INB AND DISABLE						
V_{INAH}, V_{INBH}, V_{DISH}	Input High Threshold Voltage	—	1.6	1.8	2	V
V_{INAL}, V_{INBL}, V_{DISL}	Input Low Threshold Voltage	—	0.8	1	1.2	V
V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	Input Threshold Hysteresis	—	—	0.8	—	V
$R_{INA/B}$, R_{DIS}	INA/INB/DIS Pin Pulldown Resistance	—	50	90	185	kΩ
OUTPUT						
I_{OA+}, I_{OB+}	Peak Output Source Current	(Note 6)	—	-4	—	A
I_{OA-}, I_{OB-}	Peak Output Sink Current		—	6	—	A
R_{OH}	Pullup Resistance	I_{OX} = -10mA	—	4	10	Ω
R_{OL}	Pulldown Resistance	I_{OX} = 10mA	—	0.55	1.1	
V_{OUTPD}	Output Active Pulldown on OUTX	I_{OUT} = 200mA, VDDx floating and unpowered.	—	1.6	2	V
DEAD TIME AND OVERLAP PROGRAMMING						
DT	Dead Time Programming for 1kΩ ≤ R_{DT} ≤ 100kΩ DT (ns) = 10 × R_{DT} (kΩ)	DT pin connected to GND (Note 6)	—	10	—	ns
		DT pin connected to VCC (Note 6)	—	8	—	
		R_{DT} = 10kΩ	80	100	120	
		R_{DT} = 20kΩ	160	200	240	
		R_{DT} = 50kΩ	400	500	600	
$\lvert DT_{AB}-DT_{BA}\rvert$	Dead Time Matching	R_{DT} = 10kΩ	—	0	10	ns
		R_{DT} = 20kΩ	—	0	20	
		R_{DT} = 50kΩ	—	0	65	

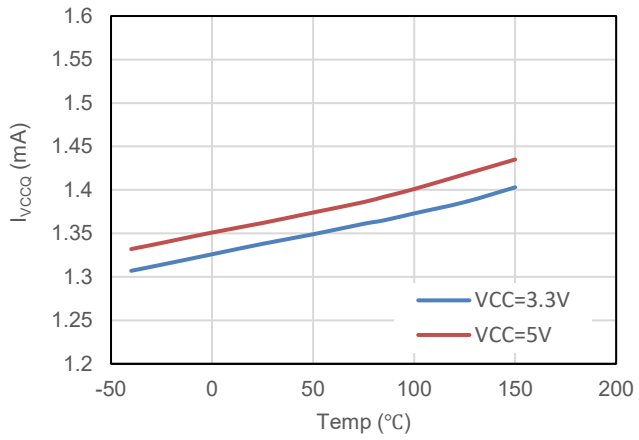
Note: 6. Guaranteed by design.

Switching Characteristics (V_{CC} = 3.3V, 0.1µF capacitance from VCC to GND, V_{VDDA} = V_{VDDB} = 12V for API21550A/BQ, V_{VDDA} = V_{VDDB} = 15V for API21550CQ, 1µF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin connected to VCC except DT test, DIS short to GND, T_A = -40°C to +125°C, C_L = 0, unless otherwise noted.)

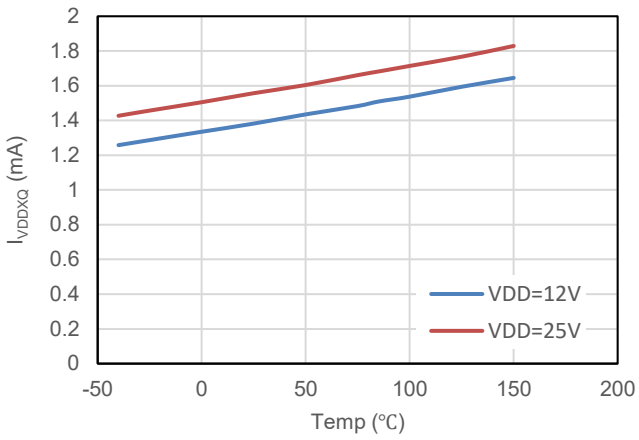
Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{RISE}	Output Rise Time	C_L = 1.8nF, V_{VDDX} = 12V, 20% to 80% (API21550A/BQ)	—	5	16	ns
		C_L = 1.8nF, V_{VDDX} = 15V, 20% to 80% (API21550CQ)	—	5	16	
t_{FALL}	Output Fall Time	C_L = 1.8nF, V_{VDDX} = 12V, 10% to 90% (API21550A/BQ)	—	6	12	ns
		C_L = 1.8nF, V_{VDDX} = 15V, 10% to 90% (API21550CQ)	—	6	12	
t_{PDLH}	Propagation Delay (Low to High)	C_L = 1.8nF, input pulse width = 100ns, 500kHz, measured with input V_{INXH} to output 10%	—	40	60	ns
t_{PDHL}	Propagation Delay (High to Low)	C_L = 1.8nF, input pulse width = 100ns, 500kHz, measured with input V_{INXL} to output 90%	—	40	60	ns
$t_{PD\_DIS\_LH}$	DIS Response Delay (Low to High)	C_L = 1.8nF, input pulse width = 100ns, 500kHz, measured with input V_{DISH} to output 90%	—	45	70	ns
$t_{PD\_DIS\_HL}$	DIS Response Delay (High to Low)	C_L = 1.8nF, input pulse width = 100ns, 500kHz, measured with Input V_{DISL} to output 10%	—	45	70	ns
t_{PWmin}	Minimum Input Pulse Width That Passes to Output	Measured with input V_{INXH} to V_{INXL}	—	10	30	ns
t_{PWD}	Pulse-Width Distortion	C_L = 1.8nF, input pulse width = 100ns, 500kHz, $\lvert t_{PDLHA} - t_{PDHLA} \rvert$, $\lvert t_{PDLHB} - t_{PDHLB} \rvert$	0	—	7	ns
$t_{VCC\ to\ OUT}$	VCC Power-up Delay Time	C_L = 1.8nF	—	50	100	µs
$t_{VDD\ to\ OUT}$	VDDX Power-up Delay Time	C_L = 1.8nF	—	10	20	µs
$\lvert CM_H \rvert$	High-Level Common Mode Transient Immunity	V_{CM} = 1500V (Note 6)	125	—	—	V/ns
$\lvert CM_L \rvert$	Low-Level Common Mode Transient Immunity		125	—	—	V/ns

Note: 6. Guaranteed by design.

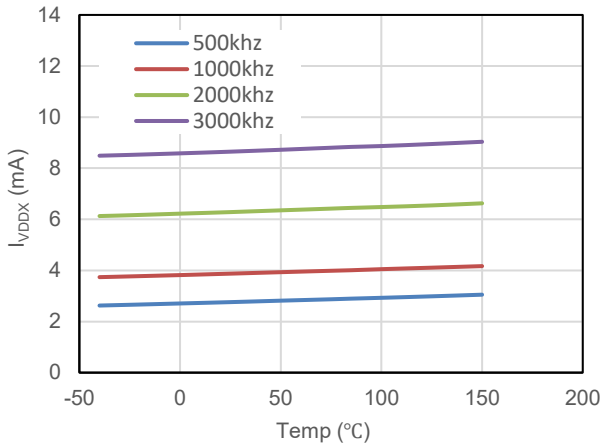
Typical Characteristics



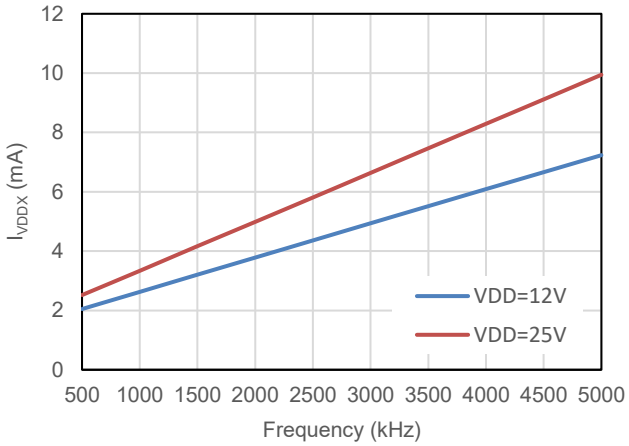
VCC Quiescent Current vs. Temperature



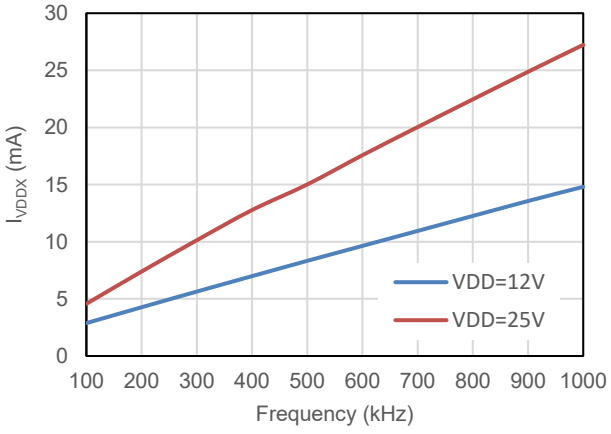
VDD Quiescent Current vs. Temperature



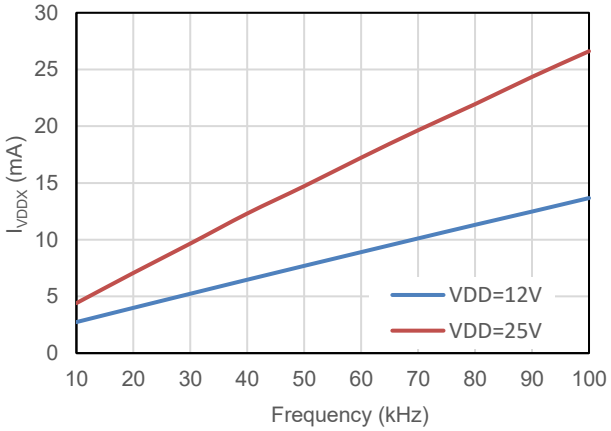
VDD Operating Current with Different Switching Frequency vs. Temperature



VDD Operating Current vs. Switching Frequency (C_L = 0)

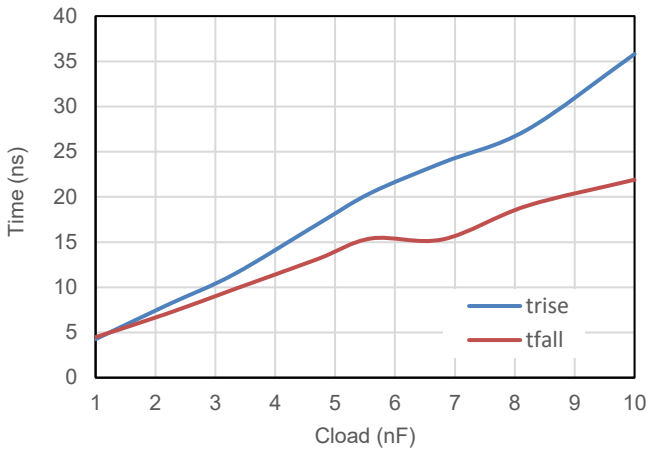


VDD Operating Current vs. Switching Frequency (C_L = 1nF)

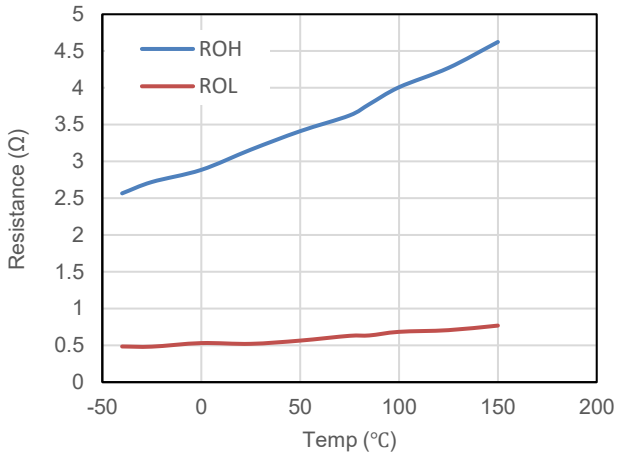


VDD Operating Current vs. Switching Frequency (C_L = 10nF)

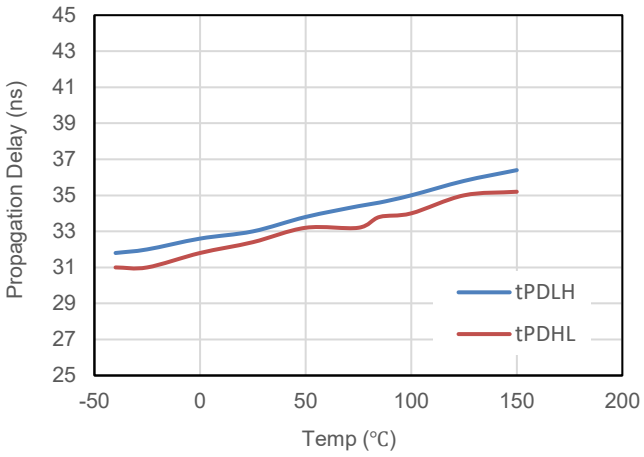
Typical Characteristics (continued)



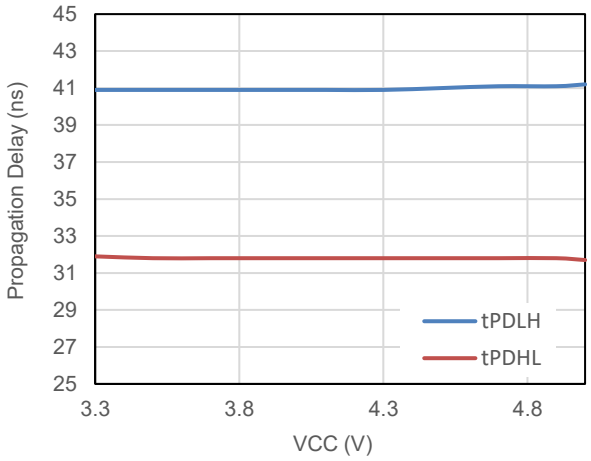
Rising/Falling Time vs. Cload



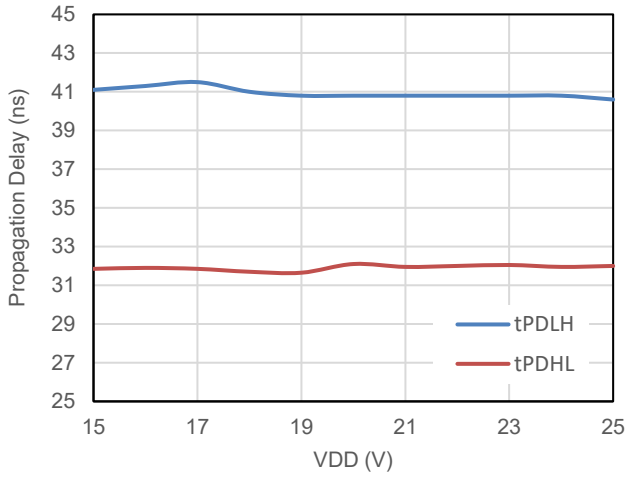
Output Resistance vs. Temperature



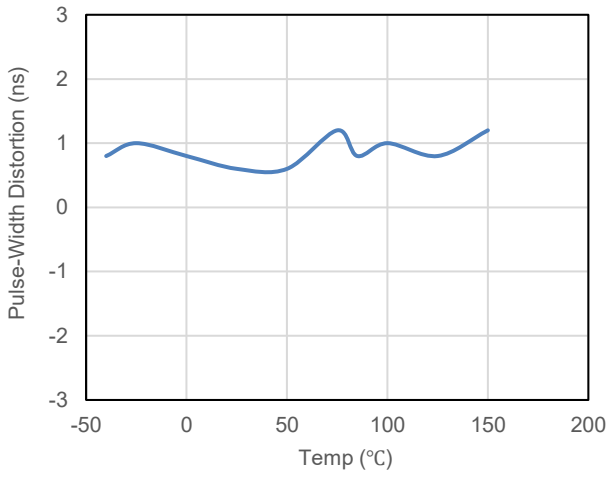
Propagation Delay Time vs Temperature



Propagation Delay Time vs. VCC Voltage

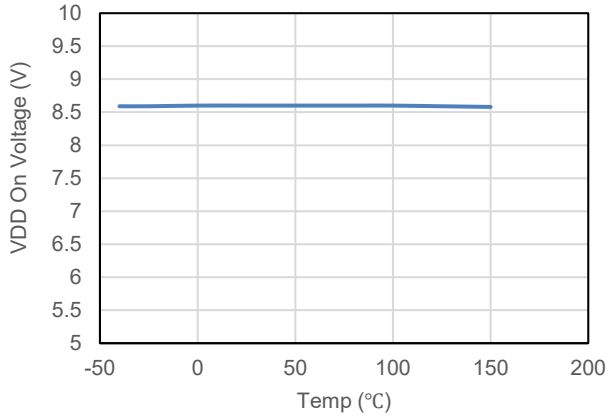


Propagation Delay Time vs. VDD Voltage

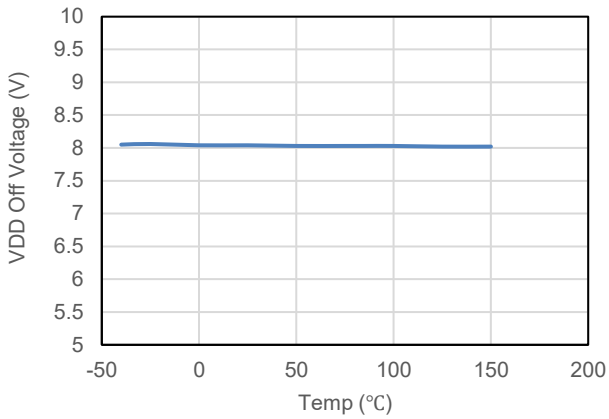


Pulse-Width Distortion Time vs. Temperature

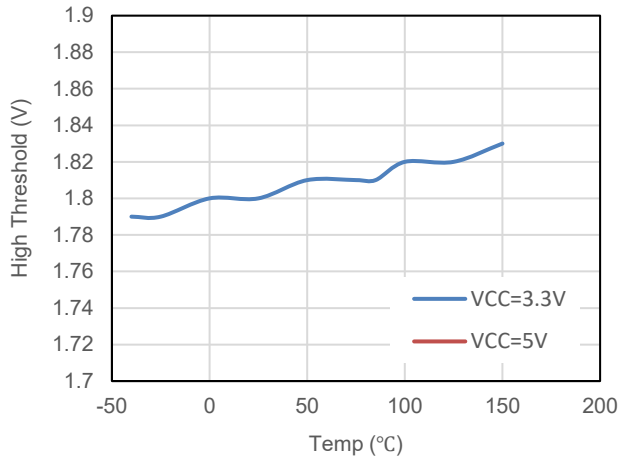
Typical Characteristics (continued)



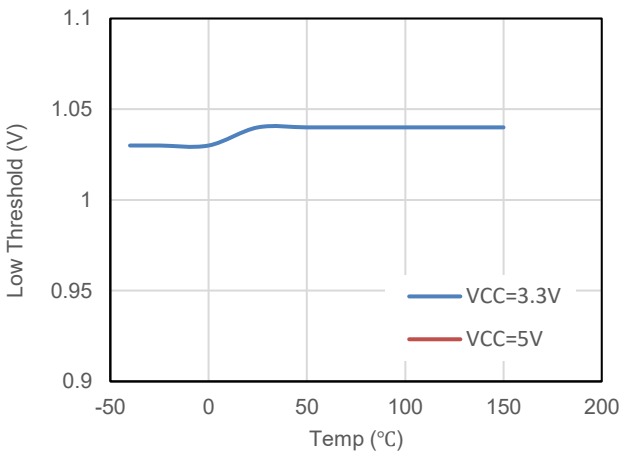
VDD On Voltage vs. Temperature



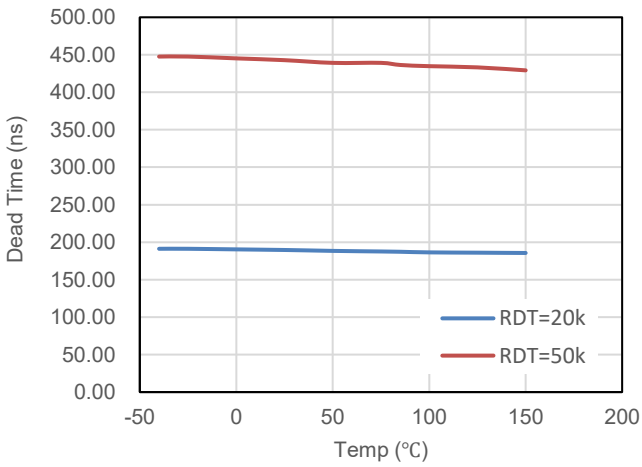
VDD Off Voltage vs. Temperature



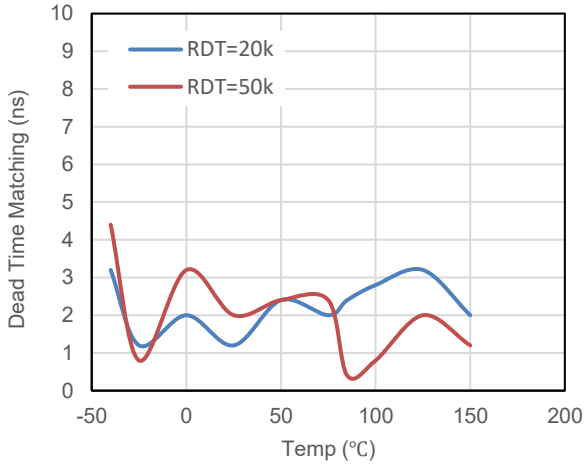
IN/DIS High Threshold vs. Temperature



IN/DIS Low Threshold vs. Temperature

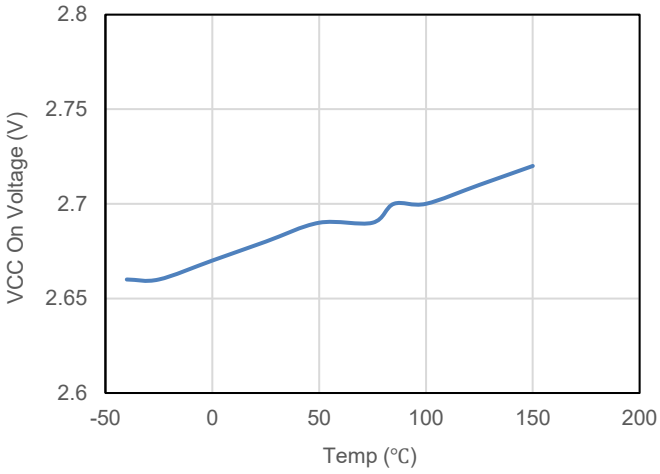


Dead Time vs. Temperature

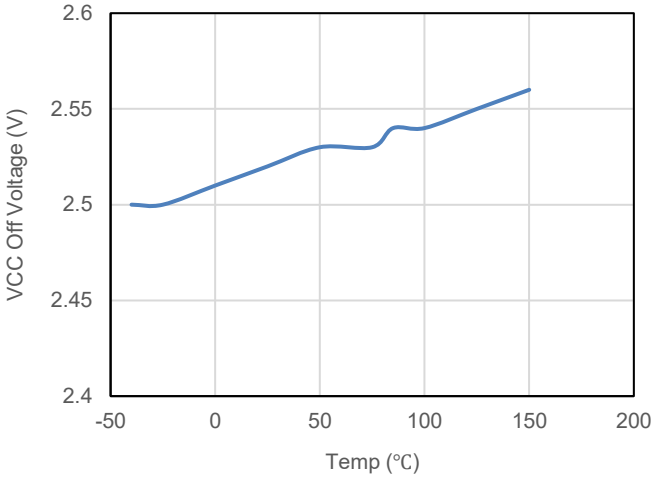


Dead Time Matching vs. Temperature

Typical Characteristics (continued)



VCC On Voltage vs. Temperature



VCC Off Voltage vs. Temperature

Parameter Measurement

1. Minimum Pulses

A minimum pulse t_{PWmin} is introduced to filter small input pulses caused by ground bounce or switching noise. An input pulse time duration shorter than t_{PWmin} (typically 10ns) on INA or INB will not cause an output state change on OUTA or OUTB. Figures 3 and 4 below show the detailed operation scheme.

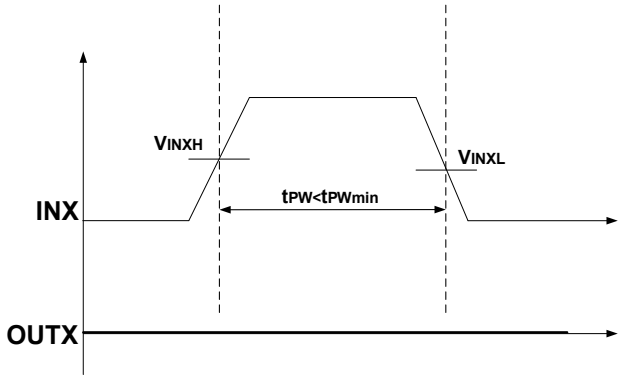


Figure 3. t_{PWmin} control at OUTX is low

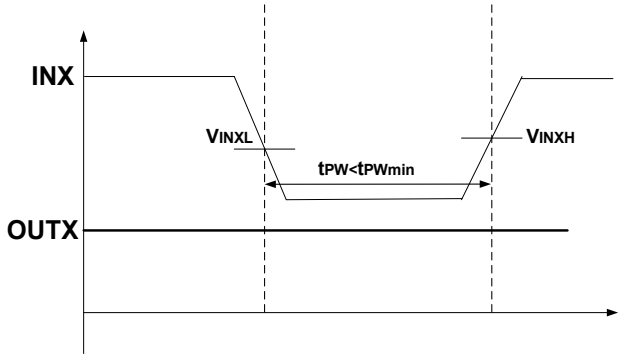


Figure 4. t_{PWmin} control at OUTX is high

2. Propagation Delay and Pulse-Width Distortion

- t_{PDLHA} – propagation delay from low to high of OUTA compared with INA
- t_{PDHLA} – propagation delay from high to low of OUTA compared with INA
- t_{PDLHB} – propagation delay from low to high of OUTB compared with INB
- t_{PDHLB} – propagation delay from high to low of OUTB compared with INB
- t_{PWD} – pulse-width distortion defined as $|t_{PDLHA} - t_{PDHLA}|$ for channel A and $|t_{PDLHB} - t_{PDHLB}|$ for channel B. The measure criteria can be referred to Figure 5.

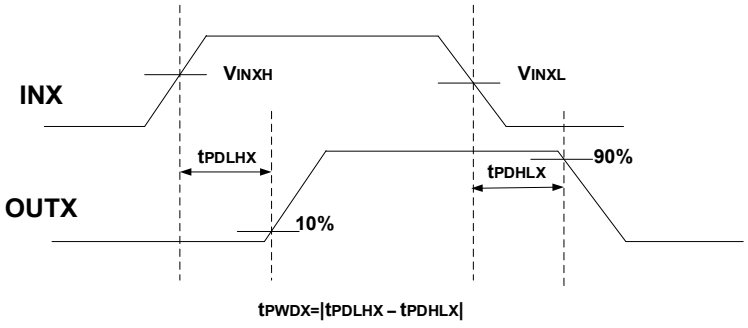


Figure 5. Delay Matching and Pulse-Width Distortion

3. Rising and Falling Time

The method of measuring rising and falling time is shown as Figure 6. Note that rising time and falling time have different measure criteria.

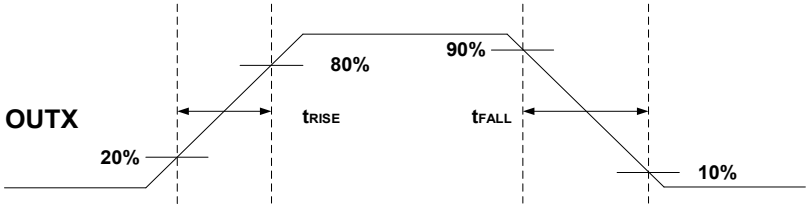


Figure 6. Rising and Falling Time

Parameter Measurement (continued)

4. Input and Disable Operation Timing Diagram

Figure 7 shows the response time when the function of Disable is activated.

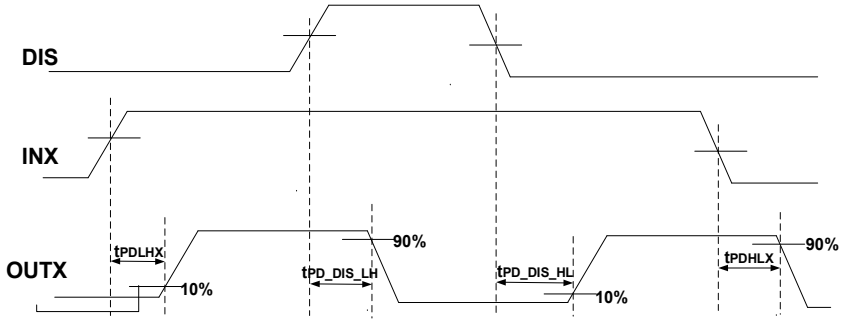


Figure 7. Disable Response Time

5. Dead Time Setting

An appropriate dead time can be set by placing a resistor (R_{DT}) between DT and GND, the dead time control timing is shown in Figure 8.

Notes: 7. If dead time function was set with t_{DT}, while the dead time between INA and INB is shorter than t_{DT}, the dead time of OUTA and OUTB will follow t_{DT}.
8. If dead time function was set with t_{DT}, while the dead time between INA and INB is longer than t_{DT}, the dead time of OUTA and OUTB will follow dead time between INA and INB.

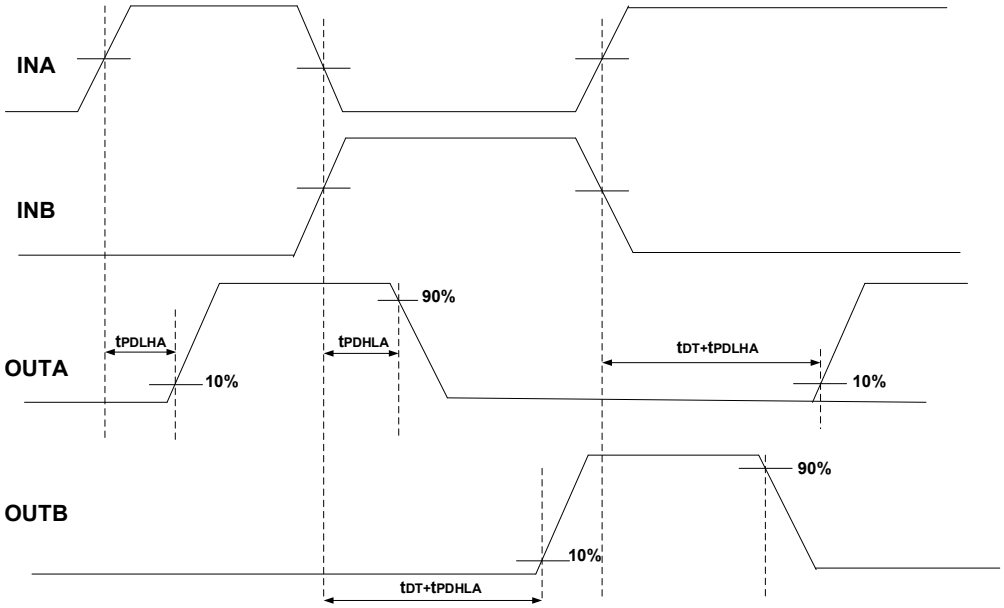


Figure 8. Dead Time Determined by R_{DT}

Parameter Measurement (continued)

6. Power-up Sequence

Before the gate driver starts to transfer signal, both V_{VCC} and V_{VDD} need time to cross from low to high (larger than threshold) and finally achieve stable voltage, during this time interval, the output was disabled after a delay called $t_{VCC\ to\ OUT}$ (for VCC UVLO) and $t_{VDD\ to\ OUT}$ (for VDD UVLO). The following Figures 9 and 10 show the power-up UVLO delay timing diagram for VCC and VDD.

If control signal was already established before VCC/VDD have crossed above their respective ON thresholds, the output will not respond until $t_{VCC\ to\ OUT}$ after VCC crossed V_{VCC_ON} and $t_{VDD\ to\ OUT}$ after VDDX crossed V_{VDD_ON}.

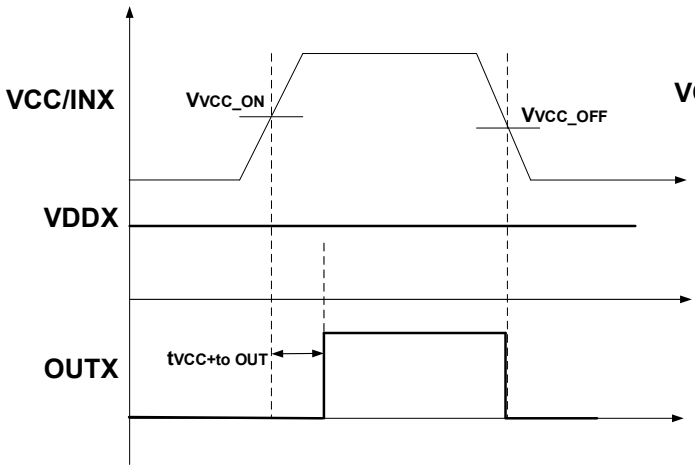


Figure 9. V_{CC} Power-up Sequence

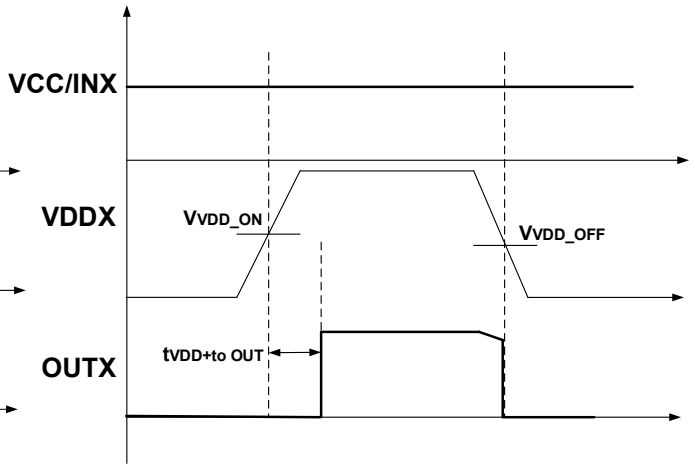


Figure 10. V_{DD} Power-up Sequence

7. CMTI Testing

A simple CMTI testing circuit is shown in Figure 11.

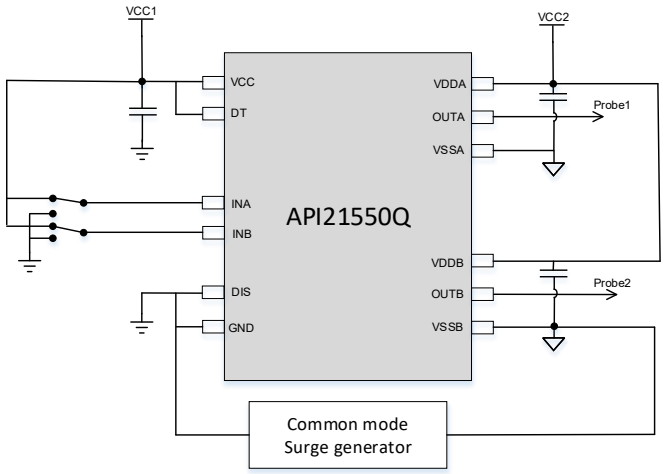


Figure 11. Common-Mode Transient Immunity Test Circuit

Feature & Operation Description

Overview

API21550Q can transfer signals from primary controllers and provide sufficient current to drive various types of transistors in the secondary. API21550AQ usually drives GaN with 5V UVLO, API21550BQ usually drives Si-MOSFET or SiC-MOSFET with 8V UVLO, API21550CQ usually drives SiC-MOSFET or IGBT with 12V UVLO.

VCC/VDD UVLO, programmable dead time, and disable functions are integrated in API21550Q and such features make the application more reliable and flexible. The fine-tuned spectrum spread helps to reduce the emission energy and improve the EMI performance.

1. Undervoltage Lockout (VCC/VDDA/VDDB UVLO)

To deal with unstable power supply in the application system, API21550Q integrates undervoltage lockout (UVLO) protection for both input and output power supply voltage respectively. API21550Q monitors VCC, VDDA/VDDB in real time. When VCC exceeds V_{VCC_ON}, the transmitter part will work normally and be ready to transfer signal to receiver part; at the same time, whenever VCC is lower than V_{VCC_OFF}, the VCC UVLO protection will be activated, and no signal will be transferred to receiver part. VDDA/VDDB has the same UVLO function, when VDDA/VDDB is higher than V_{VDD_ON}, the receiver part can transfer INA/INB signal to OUTA/OUTB and drive the transistors normally, but if VDDA/VDDB falls below V_{VDD_OFF}, the corresponding UVLO function will be activated and the OUTA/OUTB will be pulled low regardless of the status of INA/INB.

API21550Q provides three VDDA/VDDB UVLO option versions for different applications.

2. On-Off-Keying (OOK)

There is a semi-conductor-based isolation barrier between transmitter part and receiver part, namely the isolation capacitor to transfer input signal INA/INB to output signal OUTA/OUTB. API21550Q develops an on-off-keying architecture to module and de-module the signal. Figure 12 shows the basic architecture and the signal. As Figure 12 shows, the input signal is modulated by an RF signal produced by an embedded oscillator. The modulation is implemented in transmitter part, and this modulated RF frequency signal is transferred through the isolation capacitor. With the help of bandpass filter and envelop detector block, the RF signal will be de-modulated to output signal, and the output signal will then be sent to driver block to get the driver capability. As Figure 13 illustrated, with fine designed API21550Q OOK architecture, the input signal could be restored as output signal with nearly no distortion and much small propagation delay.

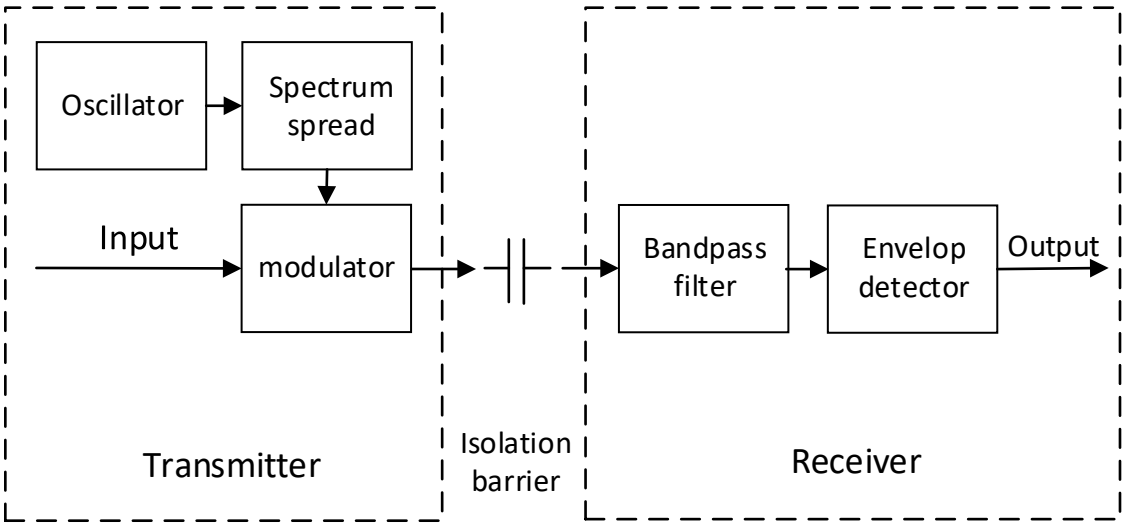


Figure 12. OOK Operation Block

Feature & Operation Description (continued)

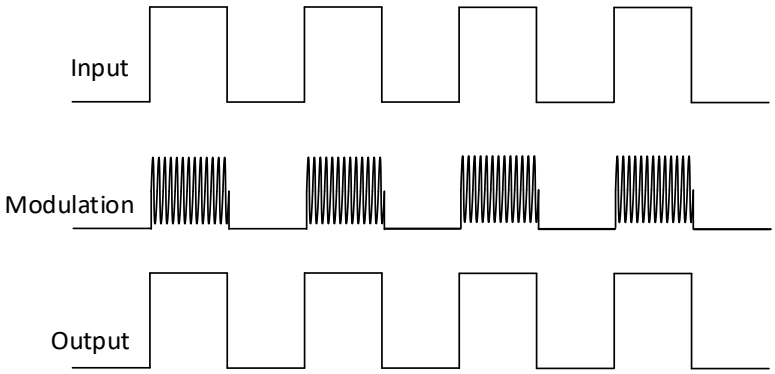


Figure 13. OOK Signal Transfer

3. Spectrum Spread

Along with the use of ultra-high frequency carrier for modulation, the electromagnetic interference (EMI) increases. API21550Q introduces a spectrum spread technique to realize frequency modulation. This spectrum spread technique effectively spreads the emission energy and the EMI performance is improved.

As shown in Figure 14, the oscillation frequency is modulated by another triangular signal, the final oscillation signal varies between fmax and fmin with a certain pattern.

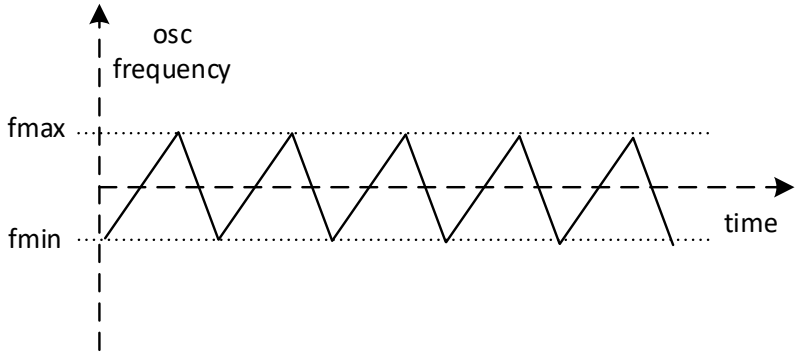


Figure 14. Spectrum Spread Patten

4. Input Stage (INA/INB/DIS Pin)

The input pins, containing INA, INB, and DIS, are compatible with both TTL and CMOS logic level, providing great convenience for different applications. If the input voltage is higher than the high threshold voltage, typically 1.8V, the input logic is recognized as high, while the input voltage is lower than low threshold voltage, typically 1V, the input logic is recognized as low, and the sufficient hysteresis is good for noise immunity. There is a pulldown resistor for each input pin, so if these pins are left open, they are actually logic low, but it is still recommended to connect the input pin to ground externally if the logic low is preferred.

INA/INB is input signal to transfer, while DIS is a disable pin, whenever a logic high is received on DIS pin, the output of API21550Q (OUTA/OUTB) would be set to low at once.

5. Output Stage (OUTA/OUTB Pin)

API21550Q is used as a H/L gate driver, OUTA is configured as the high-side driver while OUTB is the low-side driver. The driver voltage is a rail-to-rail output, and the high output is equal to VDDA/VDDB. As the high-side driver, an external bootstrap circuit is needed to provide sufficient drive voltage for OUTA. Both OUTA and OUTB adopt push-pull structure to achieve good drive ability, the peak source current is up to 6A while the peak sink current is 4A, and the large source and sink current would be helpful to turn on and off the transistors rapidly.

In VDDA/VDDB UVLO condition, to avoid falsely high output on OUTA/OUTB and protect the external transistors, an active pulldown feature is embedded in API21550Q. With this feature, OUTA/OUTB will always be pulled low even when the output stage is in UVLO condition.

Feature & Operation Description (continued)

6. Dead Time Control (DT Pin)

For different transistor types, the switching characteristics are usually different as well. An appropriate dead time between high-side and low-side switch is most important to effectively prevent shoot through. API21550Q introduces a programmable dead time control logic to meet the various requirements. Designers could set a desired dead time between OUTA and OUTB through a resistor R_{DT} connected between DT pin and ground.

- R_{DT} is between 1kΩ and 100kΩ
  $t_{DT}(ns) = 10 * R_{DT}(\text{k}\Omega)$
  As the formula shows, the dead time t_{DT} (ns) is proportional to R_{DT} (kΩ) within some specific R_{DT} range, and this R_{DT} range is recommended.
- DT pin is floating, connected to ground or VCC.
  Under such conditions, the dead time will be set to a small value internally, approximately 8ns. But it is still recommended to set the dead time through the R_{DT} to improve reliability.

The dead time control logic can only be active when the OUTA/OUTB transits from low to high, as is illustrated in Figure 15 and Figure 16. Figure 15 shows the typical control logic. The dead time of OUTA starts from the falling edge of INB and OUTB starts from INA. If the dead time of INA and INB is larger than the set value, the output signal will synchronize with the input signal perfectly, just as ② in Figure 16 shows. In the abnormal condition where INA and INB are overlapped as ① in Figure 16 shows, AP21550 will simultaneously pull OUTA and OUTB down at once to eliminate the shoot through risk and thus protect the whole system.

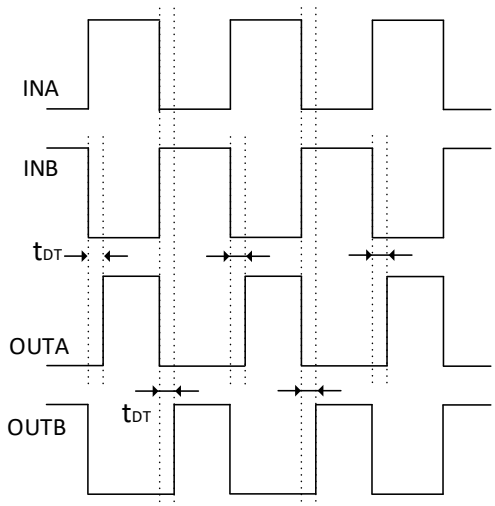


Figure 15. Typical Dead Time

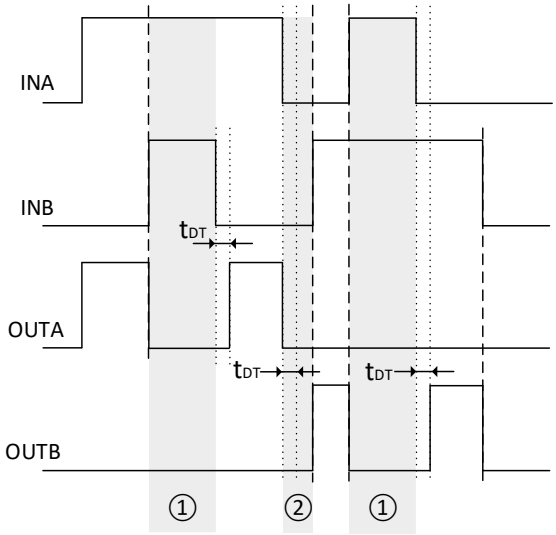


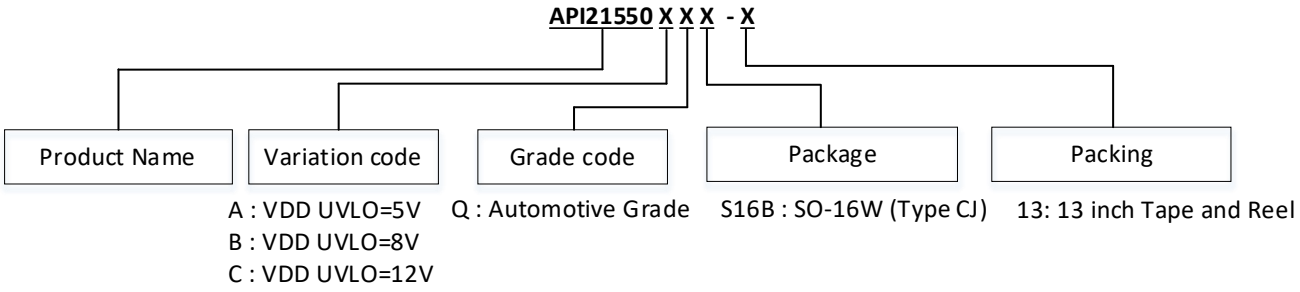
Figure 16. Dead Time with Overlap Input

7. Input and Output Logic Table (Note 9)

INA	INB	DIS	VCC	VDDA	VDDB	OUTA	OUTB
L	L	L	H	H	H	L	L
L	H	L	H	H	H	L	H
H	L	L	H	H	H	H	L
H	H	L	H	H	H	L	L
O	O	L	H	H	H	L	L
X	X	H	X	X	X	L	L
X	X	X	L	X	X	L	L
X	L	L	H	L	X	L	L
L	X	L	H	X	L	L	L

Note: 9. H = Logic High; L = Logic Low; O = Left Open; X = Irrelevant.

Ordering Information (Note 10)



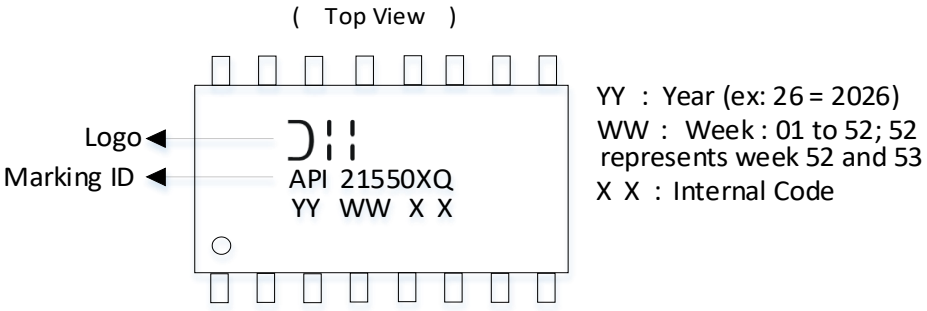
Orderable Part Number	Marking ID	Package	Packing	
			Qty.	Carrier
API21550AQS16B-13	API21550AQ	SO-16W (Type CJ)	1000	Tape and Reel
API21550BQS16B-13	API21550BQ	SO-16W (Type CJ)	1000	Tape and Reel
API21550CQS16B-13*	API21550CQ	SO-16W (Type CJ)	1000	Tape and Reel

* Future Part Number

Note: 10. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

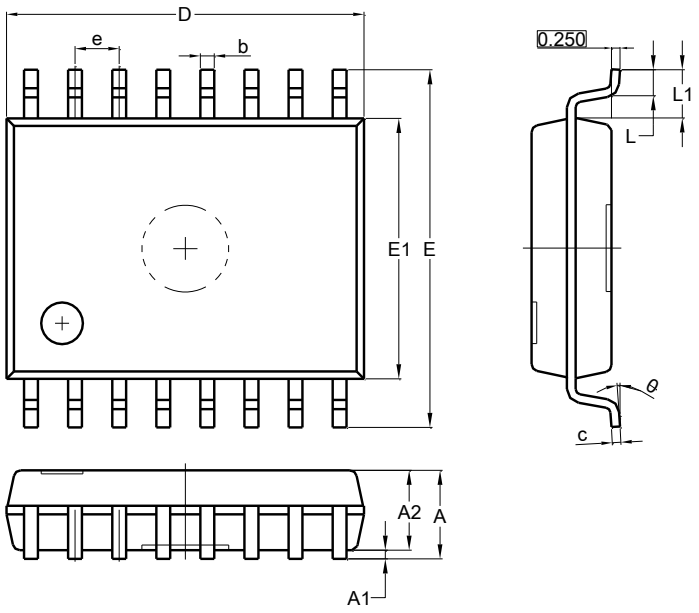
SO-16W (Type CJ)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-16W (Type CJ)

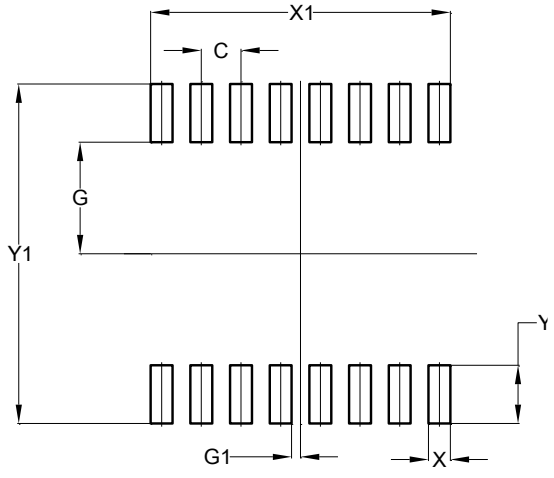


SO-16W (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	--	2.650	--
A1	0.100	0.300	--
A2	2.250	2.350	--
b	0.350	0.430	--
c	0.240	0.290	--
D	10.200	10.400	--
E	10.100	10.500	--
E1	7.400	7.600	--
e	1.270 BSC		
L	0.550	0.850	--
L1	1.400 REF		
θ	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-16W (Type CJ)



Dimensions	Value (in mm)
C	1.270
G	3.550
G1	0.285
X	0.700
X1	9.590
Y	1.800
Y1	10.800

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight:
  - SO-16W (Type CJ): 307m grams (Approximate)

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