AUTOMOTIVE, 2.3V TO 5.5V INPUT, 1A LOW IQ SYNCHRONOUS BUCK CONVERTER

Description

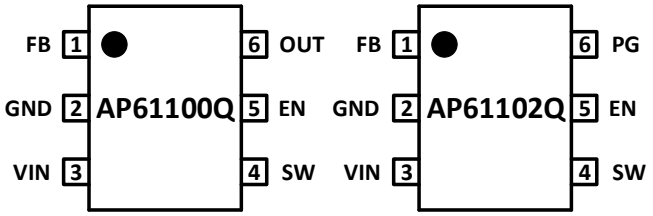
The AP61100Q/AP61102Q is an automotive-compliant, 1A, synchronous buck converter with a wide input voltage range of 2.3V to 5.5V. The device fully integrates a 110mΩ high-side power MOSFET and an 80mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP61100Q/AP61102Q device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

The device is available in a SOT563 package.

Pin Assignments

(Top View)



SOT563

Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C5
- VIN: 2.3V to 5.5V
- Output Voltage (VOUT): 0.6V to 3.6V
- 1A Continuous Output Current
- 0.6V ± 2% Reference Voltage
- 15μA Low Quiescent Current (Pulse Frequency Modulation)
- 2.2MHz Switching Frequency (VIN = 5V, VOUT = 1.8V)
- Up to 89% Efficiency at 5mA Light Load
- Programmable Operation Mode Through EN
  - Pulse Frequency Modulation
  - Pulse Width Modulation Regardless of Output Load
- Power-Good Indicator
  - AP61102Q
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - VIN Overvoltage Protection (OVP)
  - Peak Current Limit
  - Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP61100Q and AP61102Q are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- 5V Automotive Distributed Power Bus Supplies
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Advanced Driver Assistance Systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

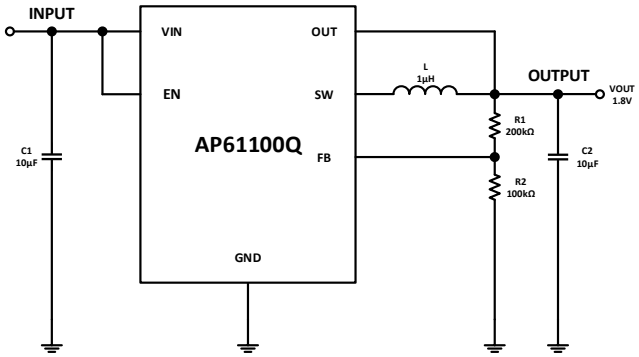


Figure 1. Typical AP61100Q Application Circuit

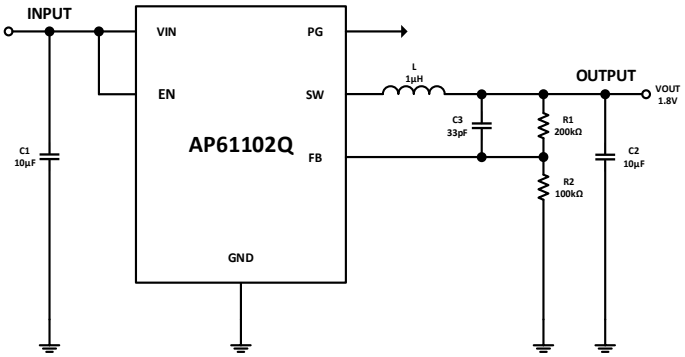


Figure 2. Typical AP61102Q Application Circuit

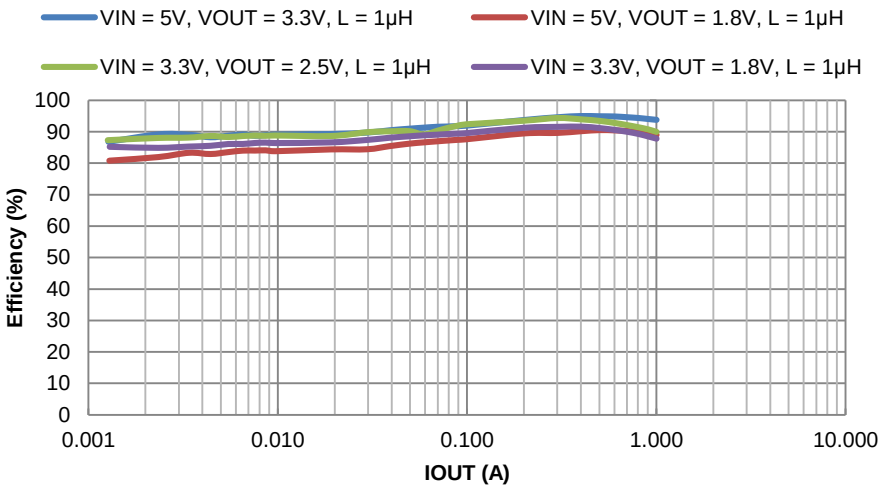


Figure 3. PFM Efficiency vs. Output Current

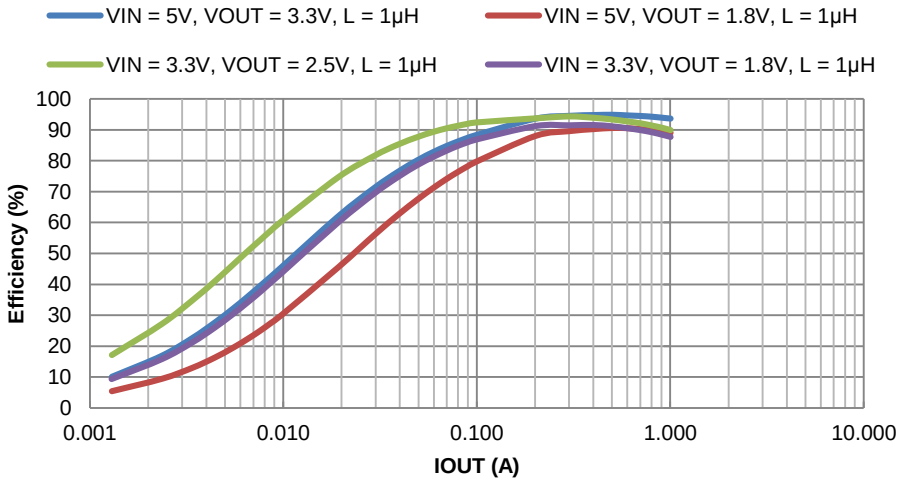


Figure 4. PWM Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
FB	1	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
GND	2	Power Ground.
VIN	3	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 2.3V to 5.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
SW	4	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
EN	5	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. EN is used to program the Operation Mode (PFM or PWM). See **Enable** section for more details.
OUT (AP61100Q)	6	Output Voltage Power Rail. Connect OUT to the output load.
PG (AP61102Q)		Power-Good. Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start.

Functional Block Diagram

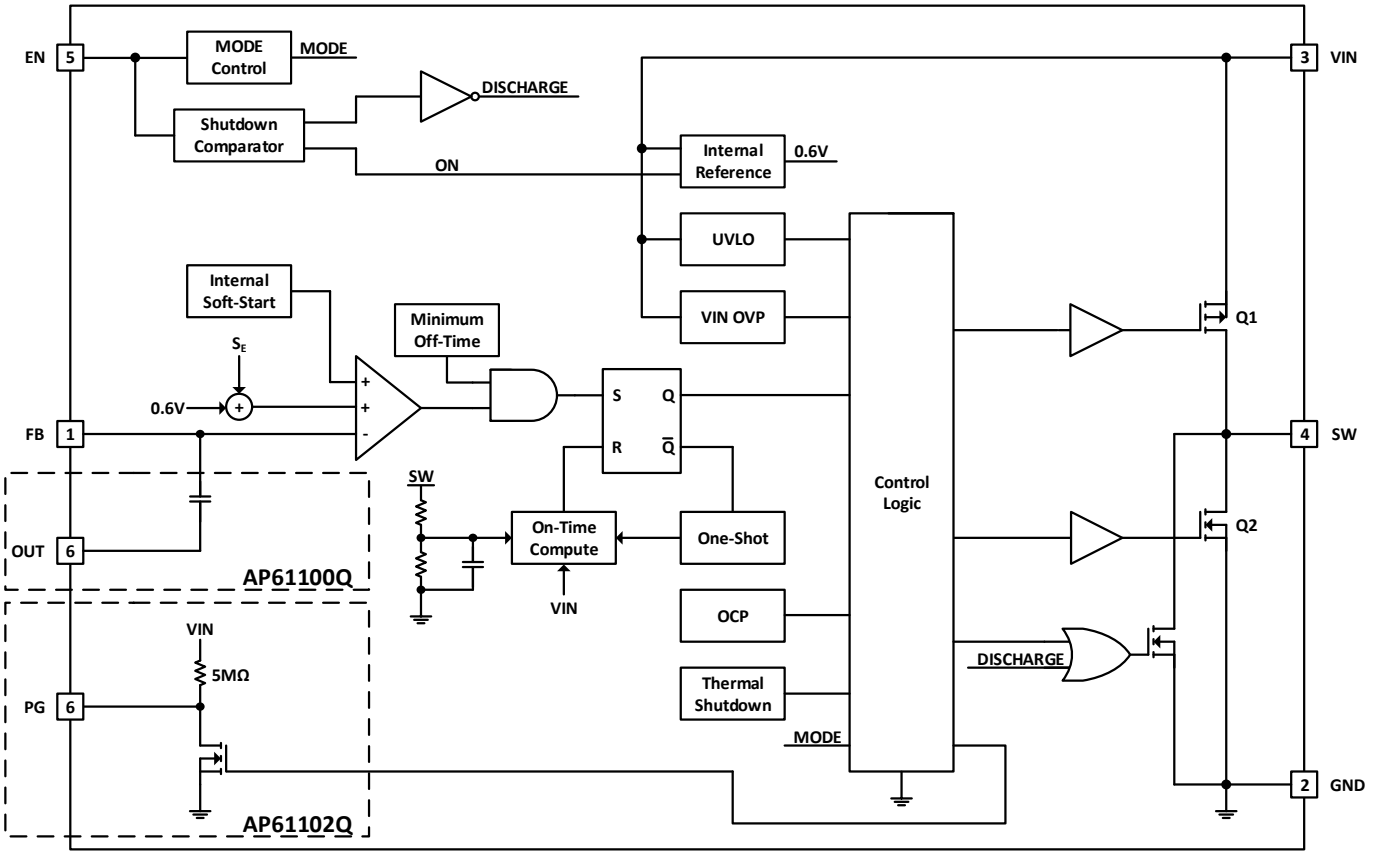


Figure 5. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +6.5 (DC)	V
		-0.3 to +7.0 (400ms)	
V_{FB}	Feedback Pin Voltage	-0.3 to VIN + 0.3	V
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{EN}	Enable Pin Voltage	-0.3 to VIN + 0.3	V
VOUT (AP61100Q)	Output Pin Voltage	-0.3 to +6.0 (DC)	V
V_{PG} (AP61102Q)	Power-Good Pin Voltage	-0.3 to +6.0 (DC)	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±6000	V
CDM	Charged Device Model	±1500	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SOT563	141	°C/W
θ_{JC}	Junction to Case	SOT563	33	°C/W

Note: 6. Test condition for SOT563: Device mounted on FR-4 substrate, two-layer PCB, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	2.3	5.5	V
VOUT	Output Voltage	0.6	3.6	V
T_A	Operating Ambient Temperature	-40	+125	°C
T_J	Operating Junction Temperature	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_J = +25°C, VIN = 5V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +150°C, and input voltage range, 2.3V to 5.5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	0.1	—	μA
I_Q	Quiescent Supply Current	PFM, V_{FB} = 0.65V	—	15	—	μA
		PWM, V_{FB} = 0.65V	—	620	—	μA
POR	VIN Power-on Reset Rising Threshold	—	—	2.00	2.25	V
UVLO	VIN Undervoltage Lockout Falling Threshold	—	—	1.84	—	V
OVP_{VIN}	VIN Overvoltage Rising Threshold	—	—	6.3	—	V
OVP_{VIN_HYS}	VIN Overvoltage Hysteresis	—	—	300	—	mV
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	110	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	80	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	From Source to Drain	1.7	2.5	—	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	From Source to Drain	—	1.9	—	A
f_{SW}	Oscillator Frequency	VOUT = 1.8V, CCM	—	2.2	—	MHz
t_{ON_MIN}	Minimum On-Time	—	—	70	—	ns
t_{OFF_MIN}	Minimum Off-Time	—	—	70	—	ns
V_{FB}	Feedback Voltage	CCM	0.588	0.600	0.612	V
V_{EN_H}	EN Logic High Threshold	—	—	0.91	—	V
V_{EN_L}	EN Logic Low Threshold	—	—	0.83	—	V
t_{SS}	Soft-Start Time	—	—	0.5	—	ms
PG_{UV_FALL}	Undervoltage Falling Threshold	AP61102Q, Percent of Output Regulation, Fault	—	90	—	%
PG_{UV_RISE}	Undervoltage Rising Threshold	AP61102Q, Percent of Output Regulation, Good	—	95	—	%
PG_{OV_RISE}	Overvoltage Rising Threshold	AP61102Q, Percent of Output Regulation, Fault	—	110	—	%
PG_{OV_FALL}	Overvoltage Falling Threshold	AP61102Q, Percent of Output Regulation, Good	—	105	—	%
t_{PG_RD}	Power-Good Rise Delay Time	AP61102Q	—	55	—	μs
V_{PG_OL}	Power-Good Output Logic Low	AP61102Q, I_{PG} = -1mA	—	—	0.4	V
R_{PG}	Power-Good Pull-Up Resistor	AP61102Q	—	5	—	MΩ
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	+30	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP61100Q/AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, unless otherwise specified.)

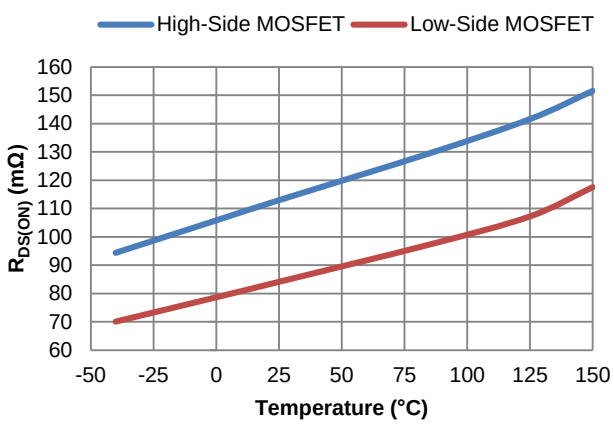


Figure 6. Power MOSFET $R_{DS(ON)}$ vs. Temperature

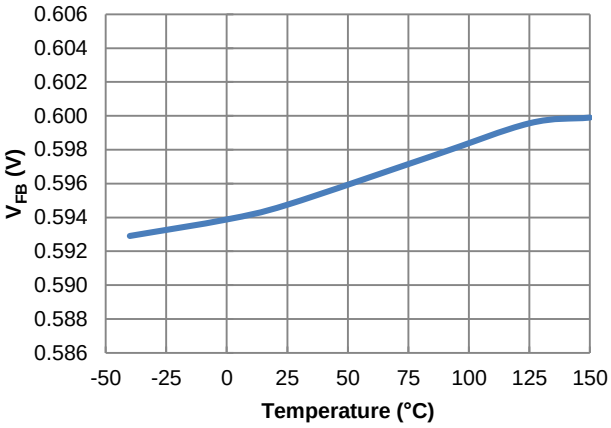


Figure 7. V_{FB} vs. Temperature

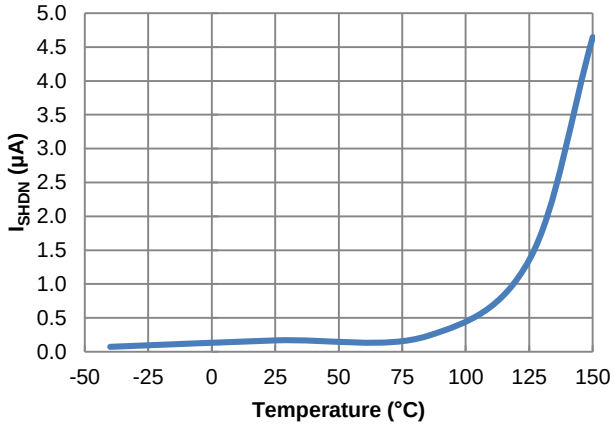


Figure 8. I_{SHDN} vs. Temperature

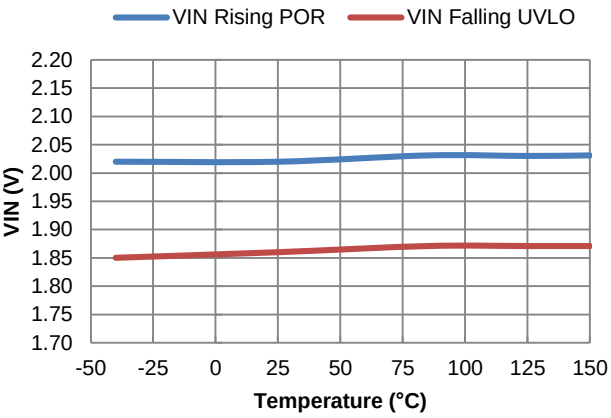


Figure 9. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (AP61100Q/AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, PFM, unless otherwise specified.)

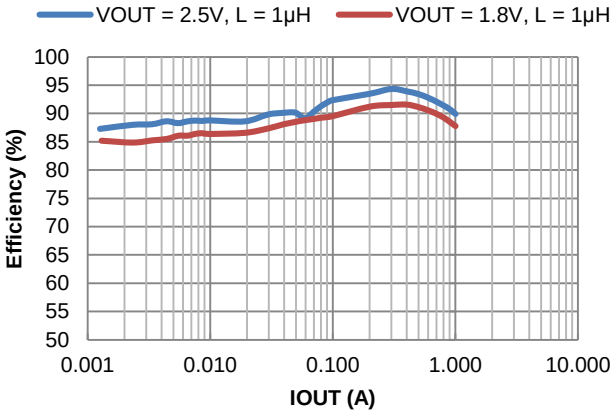


Figure 10. Efficiency vs. Output Current, VIN = 3.3V

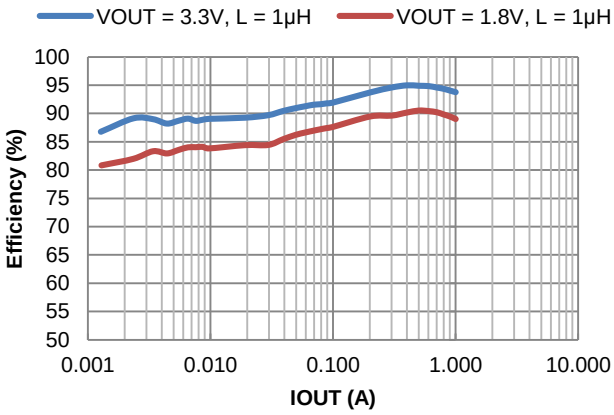


Figure 11. Efficiency vs. Output Current, VIN = 5V

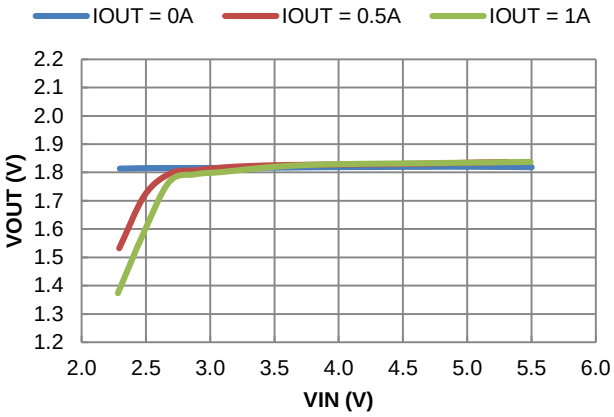


Figure 12. Line Regulation

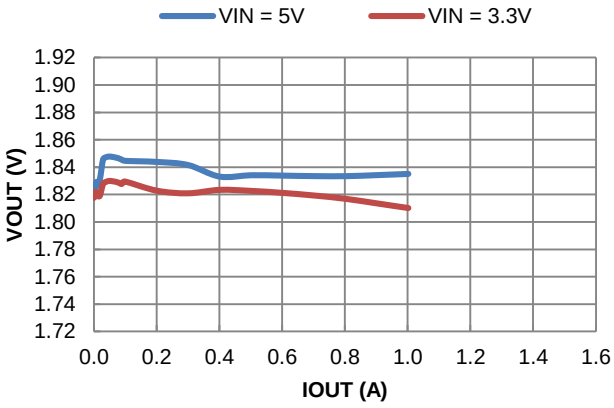


Figure 13. Load Regulation

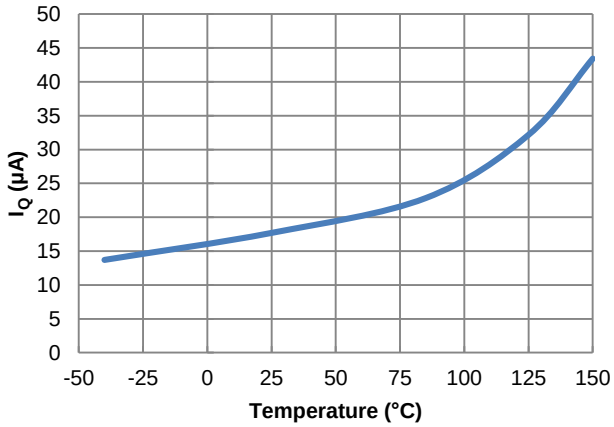


Figure 14. I_Q vs. Temperature

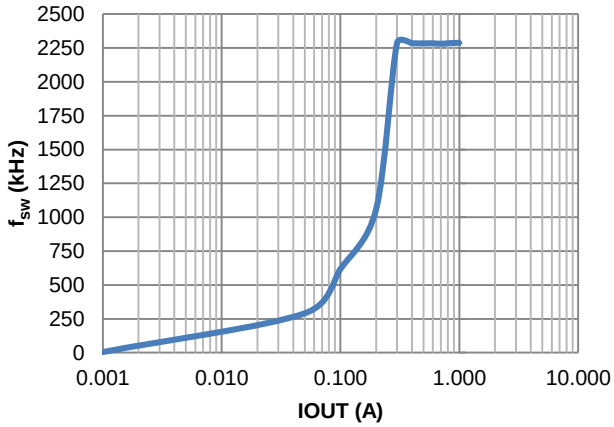


Figure 15. f_{sw} vs. Load

Typical Performance Characteristics (AP61100Q/AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, PFM, unless otherwise specified.) (continued)

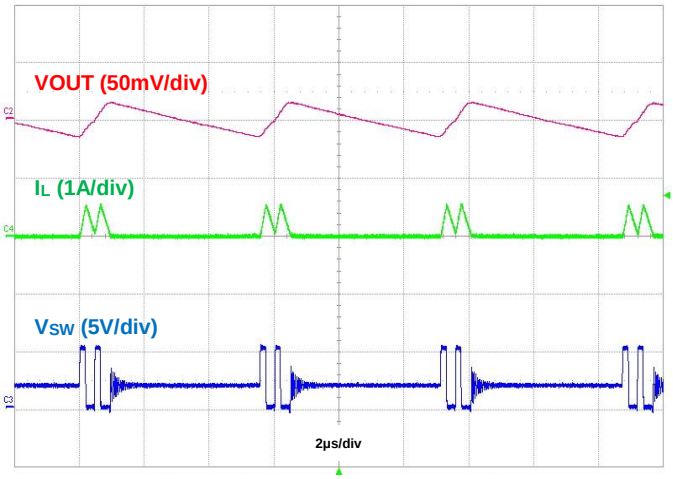


Figure 16. Output Voltage Ripple, IOUT = 50mA

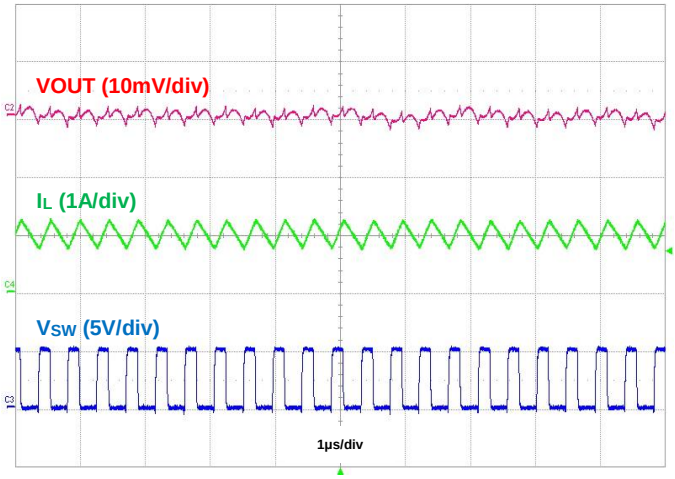


Figure 17. Output Voltage Ripple, IOUT = 1A

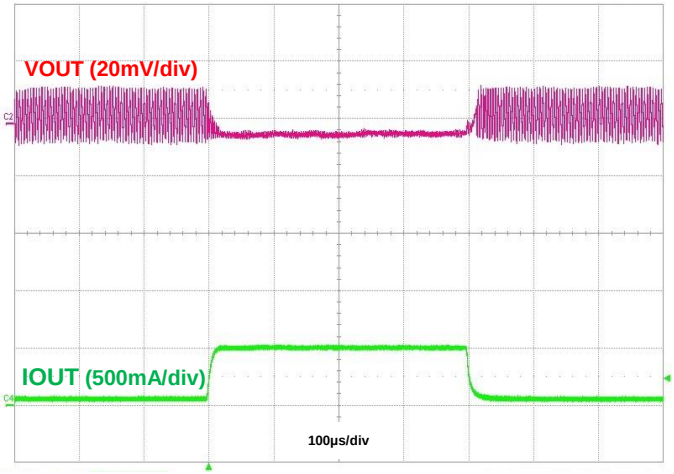


Figure 18. Load Transient, IOUT = 50mA to 500mA to 50mA

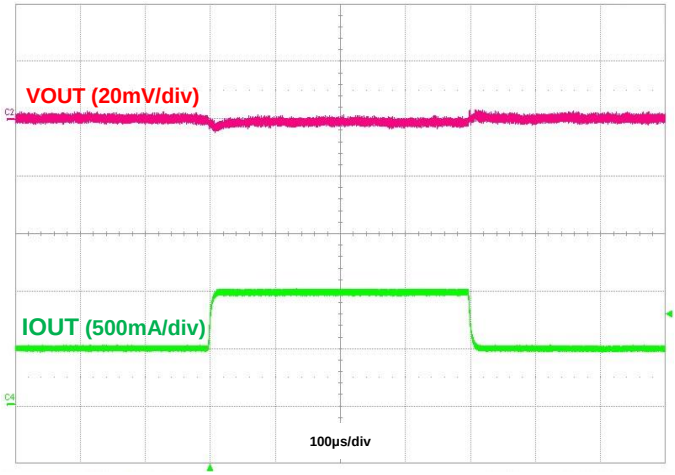


Figure 19. Load Transient, IOUT = 500mA to 1A to 500mA

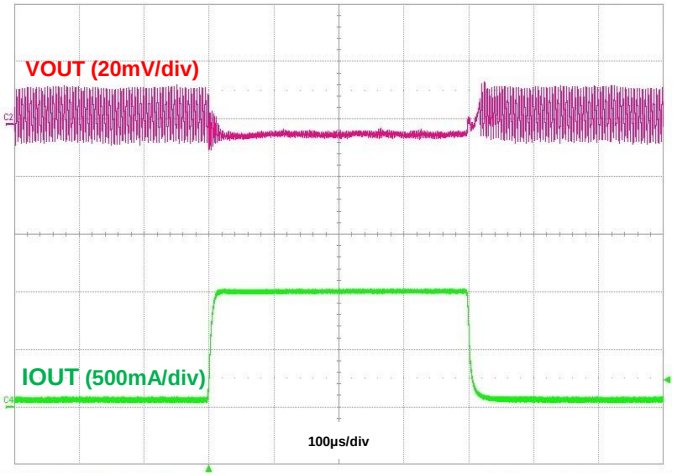


Figure 20. Load Transient, IOUT = 50mA to 1A to 50mA

Typical Performance Characteristics (AP61100Q/AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, PWM, unless otherwise specified.)

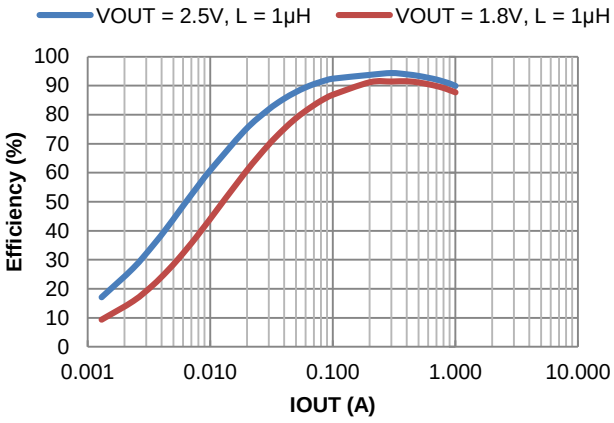


Figure 21. Efficiency vs. Output Current, VIN = 3.3V

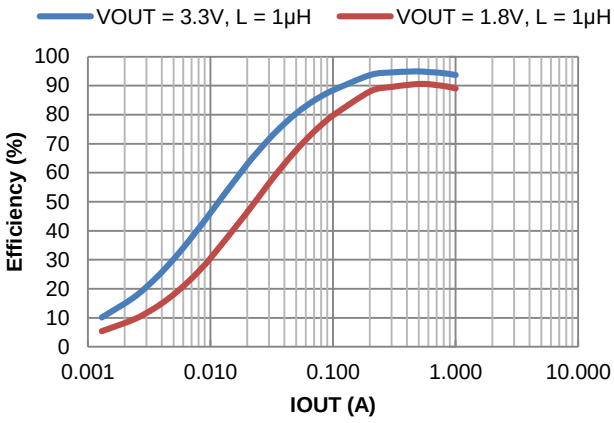


Figure 22. Efficiency vs. Output Current, VIN = 5V

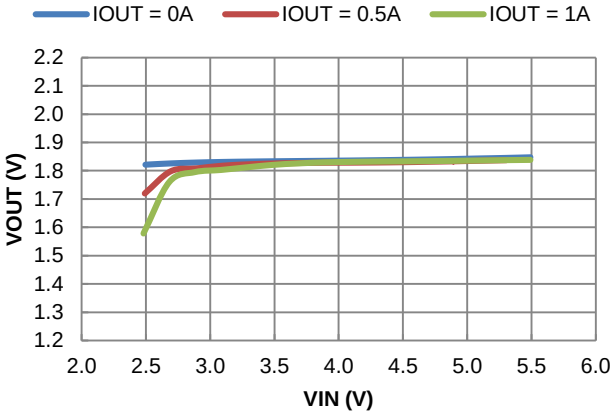


Figure 23. Line Regulation

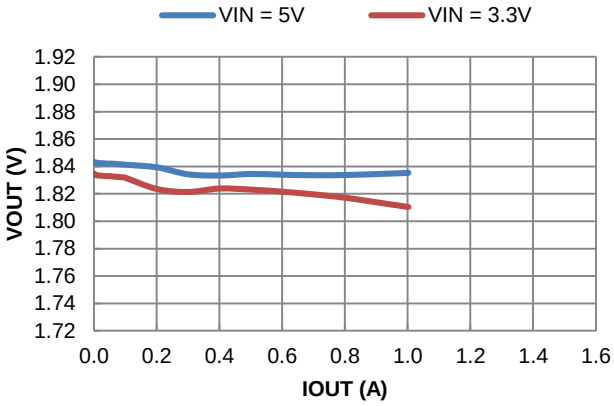


Figure 24. Load Regulation

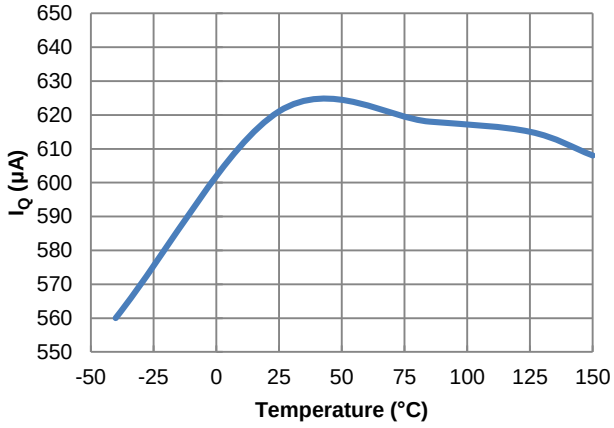


Figure 25. I_Q vs. Temperature

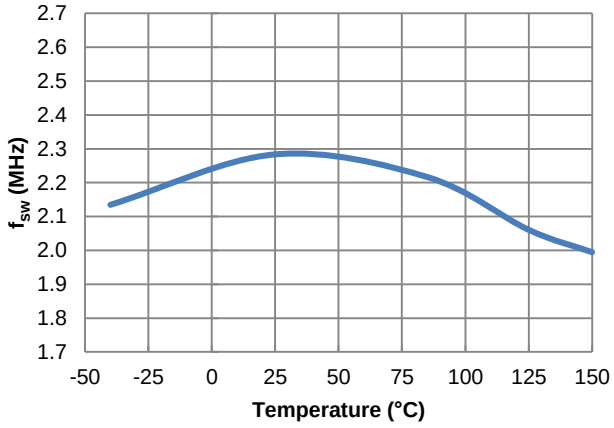


Figure 26. f_{sw} vs. Temperature, IOUT = 0A

Typical Performance Characteristics (AP61100Q/AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, PWM, unless otherwise specified.) (continued)

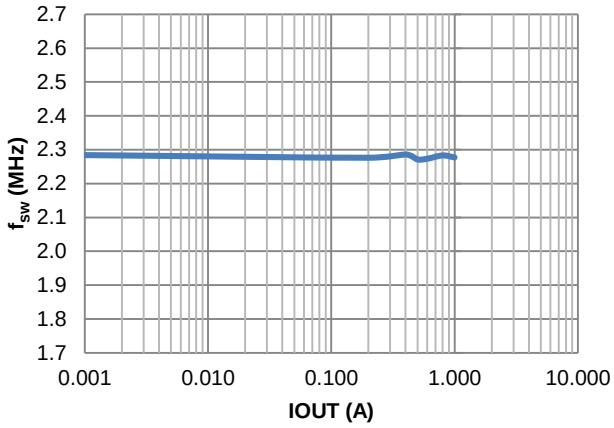


Figure 27. f_{sw} vs. Load

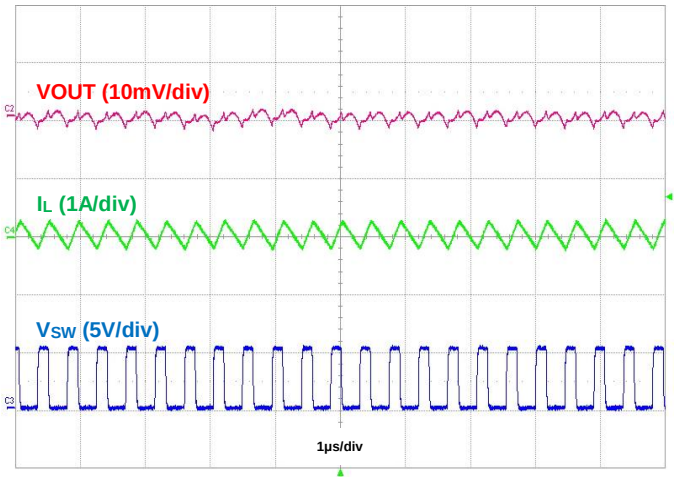


Figure 28. Output Voltage Ripple, IOUT = 50mA

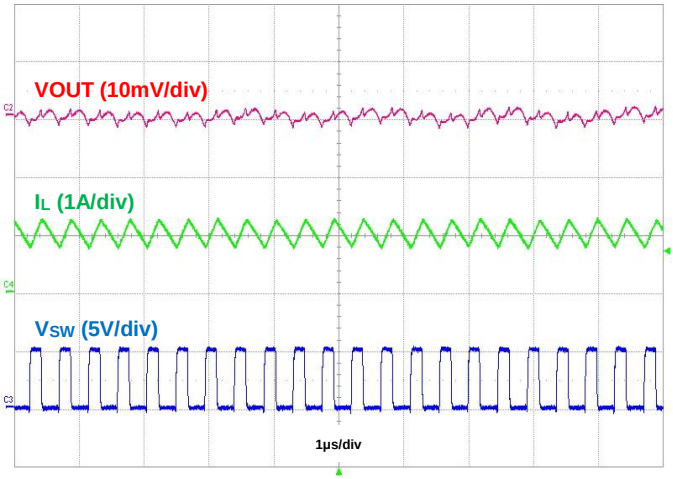


Figure 29. Output Voltage Ripple, IOUT = 1A

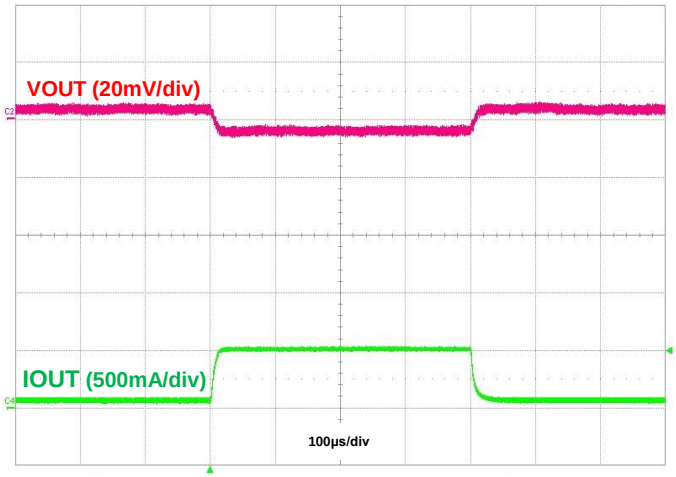


Figure 30. Load Transient, IOUT = 50mA to 500mA to 50mA

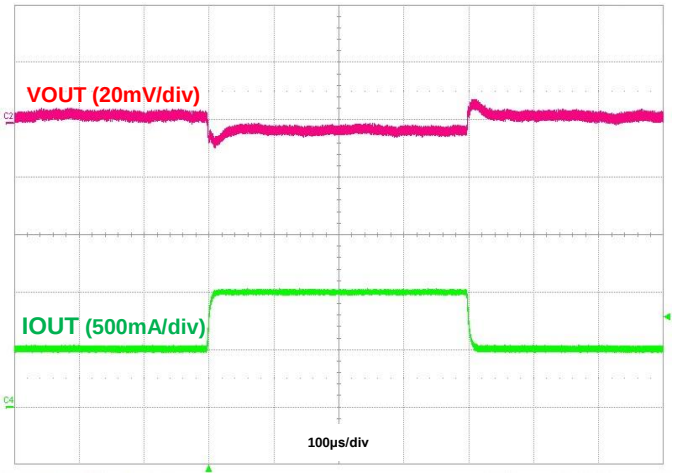


Figure 31. Load Transient, IOUT = 500mA to 1A to 500mA

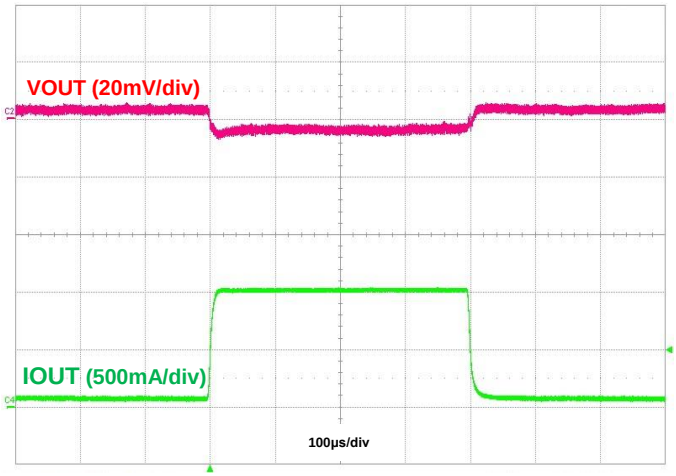


Figure 32. Load Transient, IOUT = 50mA to 1A to 50mA

Typical Performance Characteristics (AP61100Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, unless otherwise specified.)

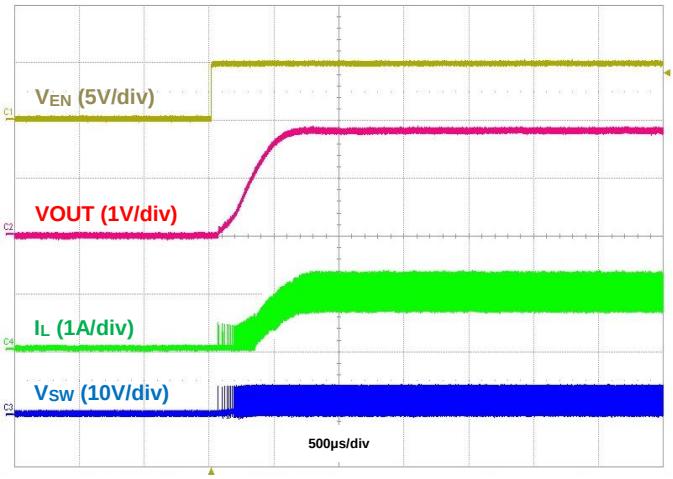


Figure 33. Startup Using EN, IOUT = 1A

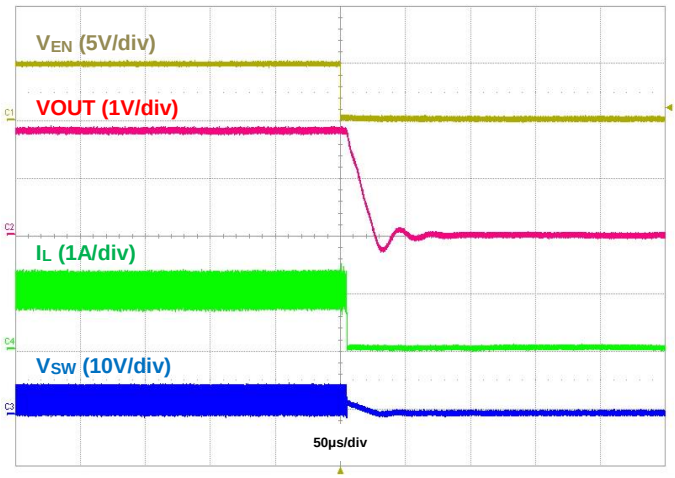


Figure 34. Shutdown Using EN, IOUT = 1A

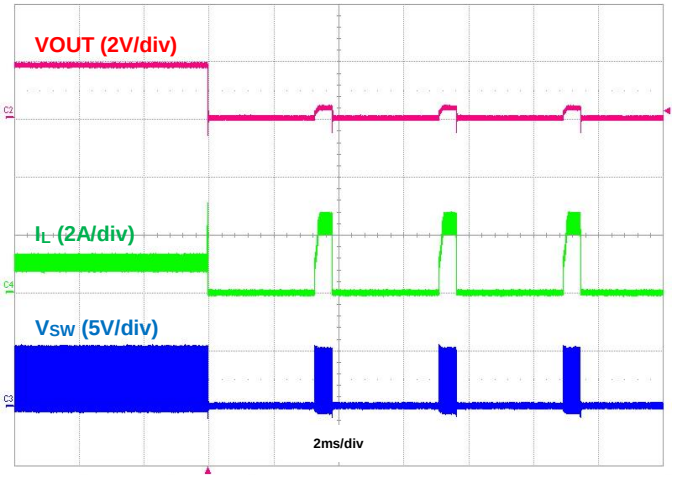


Figure 35. Output Short Protection, IOUT = 1A

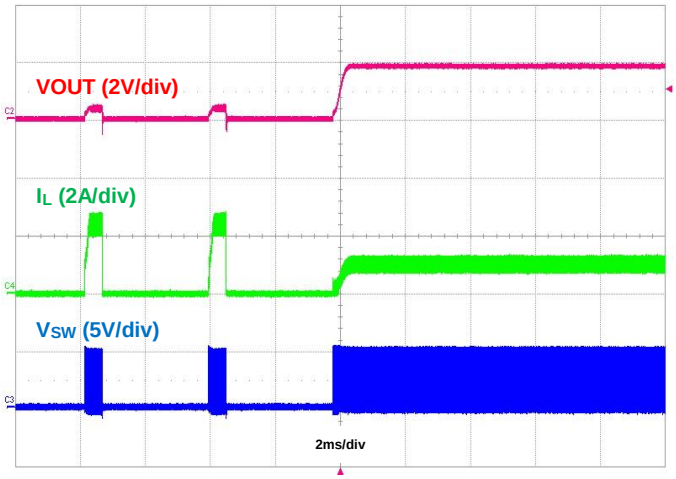


Figure 36. Output Short Recovery, IOUT = 1A

Typical Performance Characteristics (AP61102Q @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, unless otherwise specified.)

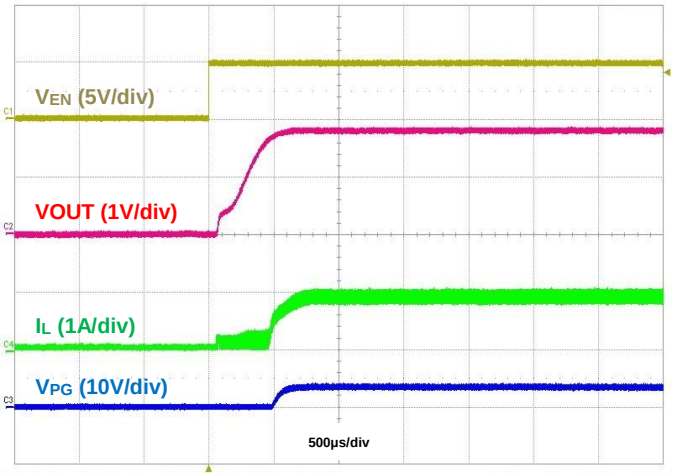


Figure 37. Startup Using EN, IOUT = 1A

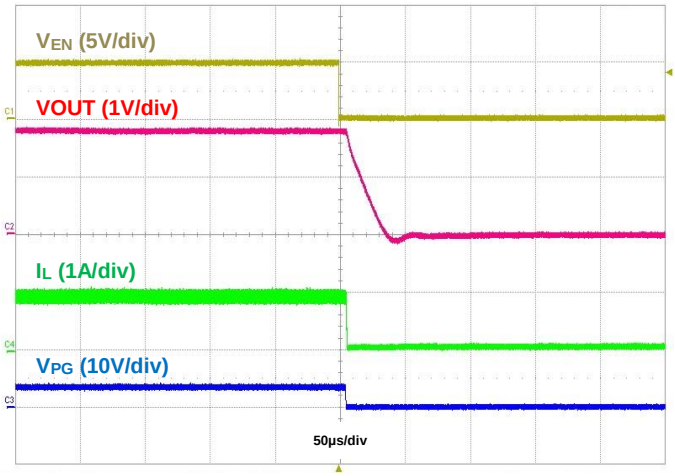


Figure 38. Shutdown Using EN, IOUT = 1A

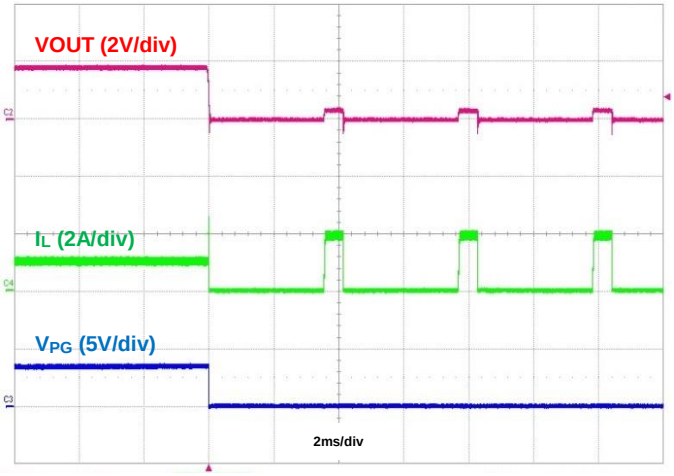


Figure 39. Output Short Protection, IOUT = 1A

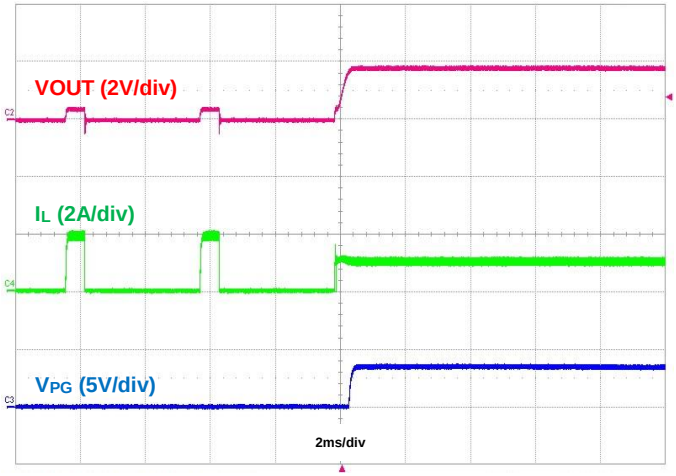


Figure 40. Output Short Recovery, IOUT = 1A

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP61100Q/AP61102Q device is a 2.3V-to-5.5V input, 1A output, fully integrated synchronous buck converter. Refer to the block diagram in Figure 5. The device employs constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the low-side power MOSFET, Q2, turns on. Once the output voltage drops below the output regulation, Q2 turns off. The one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$\mathbf{t_{ON} = \frac{VOUT}{VIN \cdot f_{sw}}} \qquad \textbf{Eq. 1}$$

Where:

- VIN is the input voltage
- VOUT is the output voltage
- f_{sw} is the switching frequency

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. The minimum off-time is 70ns typical.

2 Pulse Frequency Modulation (PFM) Operation

The AP61100Q/AP61102Q can be programmed to enter PFM operation at light load conditions for high efficiency. During light load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, so too does the inductor current. The inductor current, I_L, eventually reaches 0A, marking the boundary between Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.6V, the next cycle begins, and Q1 turns on. Because the AP61100Q/AP61102Q can work in PFM during light load conditions, it can achieve power efficiency of up to 89% at a 5mA load condition.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy load conditions can be calculated using the following equation:

$$\mathbf{I_{LOAD} = \left(\frac{VIN - VOUT}{2L}\right) \cdot t_{ON}} \qquad \textbf{Eq. 2}$$

Where:

- L is the inductor value

The quiescent current of AP61100Q/AP61102Q is 15μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 0.1μA. When applying a voltage greater than the EN logic high threshold (typical 0.91V, rising), the AP61100Q/AP61102Q enables all functions and the device initiates the soft-start phase. The AP61100Q/AP61102Q has a built-in 0.5ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 0.83V, falling), the internal SS voltage discharges to ground and device operation disables.

The device operates in PFM when a logic high voltage is applied to the EN pin greater than VIN – 200mV. The device operates in PWM regardless of output load when a logic high voltage is applied to the EN pin less than VIN – 200mV.

Application Information (continued)

4 Power-Good (PG) Indicator (AP61102Q)

The PG pin of AP61102Q is an open-drain output that is actively held low during the soft-start period until the output voltage reaches 95% of its target value. When the output voltage is outside of its regulation by ±10%, PG pulls low until the output returns within 5% of its set value. The PG rising edge transition is delayed by 55µs. The PG pin is connected to VIN through an internal 5MΩ pull-up resistor.

5 Undervoltage Lockout (UVLO) and Input Overvoltage Protection (OVP)

Undervoltage lockout is implemented to protect the IC from insufficient input voltages. The AP61100Q/AP61102Q disables if the input voltage falls below 1.84V. In this UVLO event, both the high-side and low-side power MOSFETs turn off and the 1kΩ active discharge enables to discharge the output voltage to ground.

Similarly, input overvoltage protection is implemented to protect the IC from excess input voltages. The AP61100Q/AP61102Q disables if the input voltage rises above 6.3V. In this OVP event, both the high-side and low-side power MOSFETs turn off and the 1kΩ active discharge enables to discharge the output voltage to ground.

6 Overcurrent Protection (OCP)

The AP61100Q/AP61102Q has cycle-by-cycle valley current limit protection by sensing the current through the internal low-side power MOSFET, Q2. While Q2 is on, the internal sensing circuitry monitors its conduction current. The overcurrent limit has a corresponding voltage limit, V_{LIMIT}. When the voltage between GND and SW is lower than V_{LIMIT} due to excessive current through Q2, the OCP triggers, and the controller turns off Q2. During this time, both Q1 and Q2 remain off. A new switching cycle begins only when the voltage between GND and SW rises above V_{LIMIT}. If Q2 consistently hits the valley current limit for 0.6ms, the buck converter enters hiccup mode and shuts down. After 3.4ms of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

The AP61100Q/AP61102Q also has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1, through a similar mechanism as the cycle-by-cycle valley current limit protection.

Because the $R_{DS(ON)}$ values of the power MOSFETs increase with temperature, V_{LIMIT} has a temperature coefficient of 0.4%/°C to compensate for the temperature dependency of $R_{DS(ON)}$.

7 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP61100Q/AP61102Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+130°C typical), the device initiates a normal power-up cycle with soft-start.

Application Information (continued)

8 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA}) \quad \text{Eq. 3}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 4}$$

Where:

- T_A is the ambient temperature of the environment

For the SOT563 package, the θ_{JA} is 141°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 41 shows a typical derating curve versus ambient temperature.

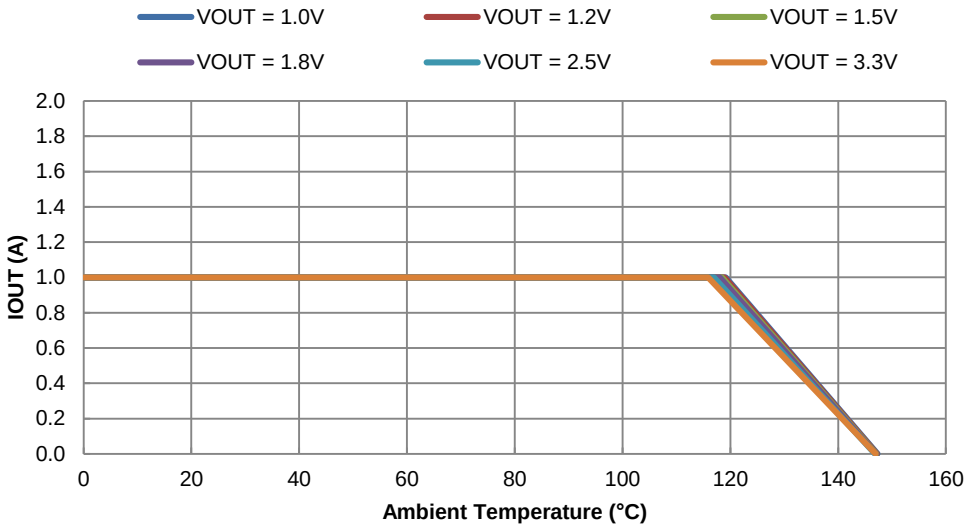


Figure 41. Output Current Derating Curve vs. Ambient Temperature, VIN = 5V

Application Information (continued)

9 Setting the Output Voltage

The AP61100Q/AP61102Q has adjustable output voltages starting from 0.6V using an external resistive divider. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R2 can be determined by the following equation:

$$\mathbf{R2} = \frac{\mathbf{0.6 \cdot R1}}{\mathbf{VOUT - 0.6V}} \quad \textbf{Eq. 5}$$

Table 1 shows a list of recommended component selections for common AP61100Q/AP61102Q output voltages referencing Figure 1 and Figure 2.

Table 1. Recommended Component Selections

AP61100Q/AP61102Q							
Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C1 (μF)	C2 (μF)	C3 (pF)	
						AP61100Q	AP61102Q
1.0	200.0	301.0	1.0	10	10	OPEN	33
1.2	200.0	200.0	1.0	10	10	OPEN	33
1.5	200.0	133.0	1.0	10	10	OPEN	33
1.8	200.0	100.0	1.0	10	10	OPEN	33
2.5	200.0	63.2	1.0	10	10	OPEN	33
3.3	200.0	44.2	1.0	10	10	OPEN	33

10 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L} = \frac{\mathbf{VOUT \cdot (VIN - VOUT)}}{\mathbf{VIN \cdot \Delta I_L \cdot f_{sw}}} \quad \textbf{Eq. 6}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP61100Q/AP61102Q, choose ΔI_L to be 30% to 50% of the maximum load current of 1A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}}} = \mathbf{I_{LOAD}} + \frac{\mathbf{\Delta I_L}}{\mathbf{2}} \quad \textbf{Eq. 7}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 1.0μH to 1.5μH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 50mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (continued)

11 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with a RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 10µF or greater is sufficient for most applications.

12 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 8}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 10µF to 22µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 9}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

Layout

PCB Layout

1. The AP61100Q/AP61102Q works at 1A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 42 and Figure 43 for more details.

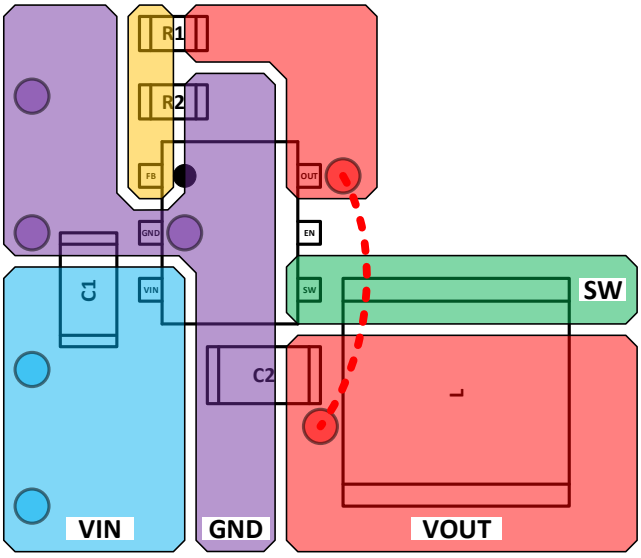


Figure 42. Recommended AP61100Q PCB Layout

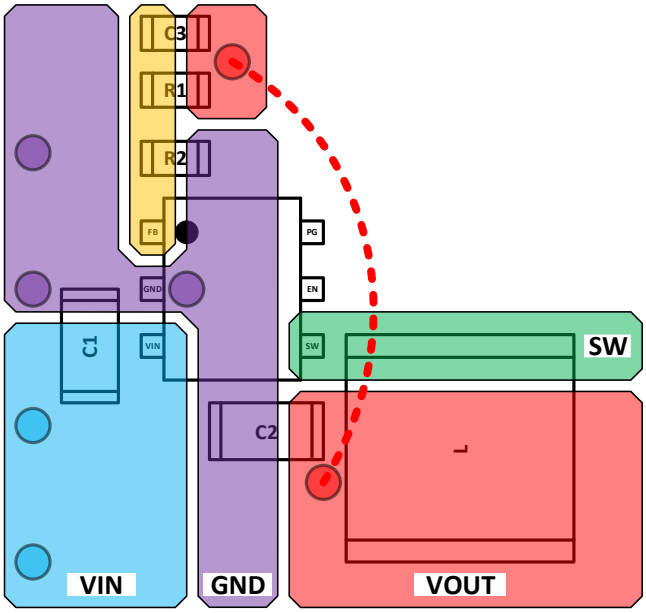
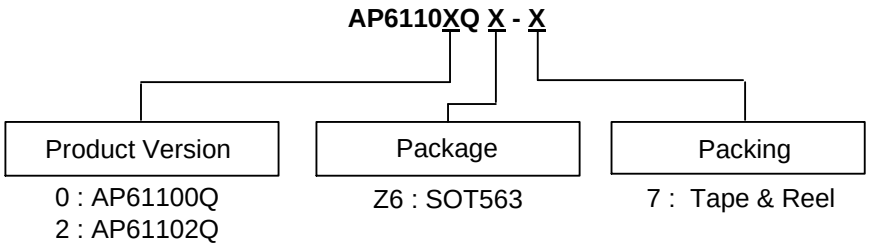


Figure 43. Recommended AP61102Q PCB Layout

Ordering Information

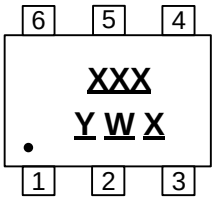


Part Number	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP61100QZ6-7	Z6	3000	-7
AP61102QZ6-7 (Future Part)	Z6	3000	-7

Marking Information

SOT563

(Top View)



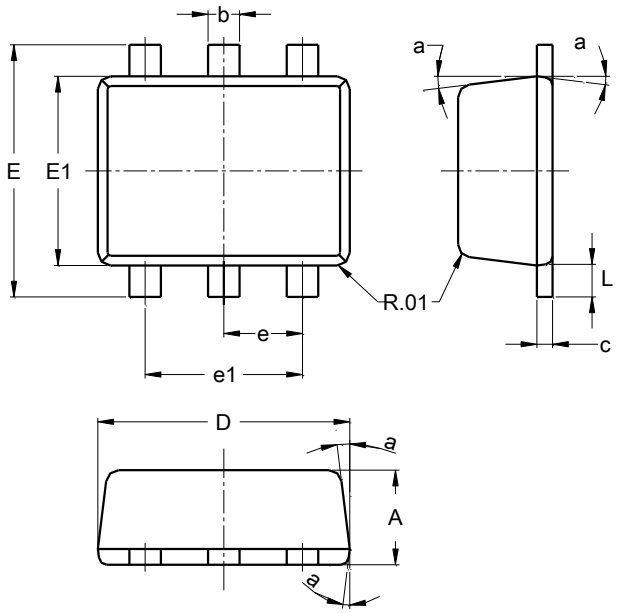
XXX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP61100QZ6-7	SOT563	HJQ
AP61102QZ6-7 (Future Part)	SOT563	HKQ

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563

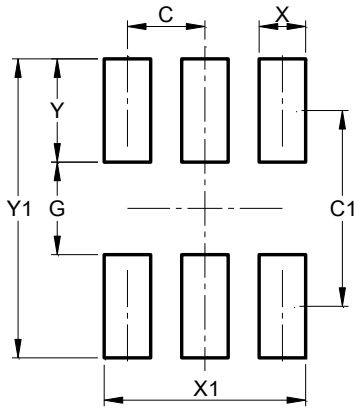


SOT563			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.60	0.60
b	0.15	0.30	0.20
c	0.10	0.18	0.11
D	1.50	1.70	1.60
E	1.55	1.70	1.60
E1	1.10	1.25	1.20
e	—	—	0.50
e1	0.90	1.10	1.00
L	0.10	0.30	0.20
a	8°	9°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563



Dimensions	Value (in mm)
C	0.500
C1	1.270
G	0.600
X	0.300
X1	1.300
Y	0.670
Y1	1.940

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.003 grams (Approximate)

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