AN4451

SAMA5D2 Hardware Design Considerations

Scope

This document facilitates the bring-up of any hardware design featuring a SAMA5D2 MPU by providing a short checklist for the hardware designer.

Abbreviations

- SDRAM – Synchronous Dynamic Random Access Memory
- DDR – Double Data Rate
- LP – Low Power
- PCB – Printed Circuit Board

Reference Documents

All the documents listed below are available on www.microchip.com.

Type	Name
Data sheet	SAMA5D2 Series
Data sheet	SAMA5D29
Errata	SAMA5D2 Device Silicon Errata and Data Sheet Clarification
Errata	SAMA5D29 Device Silicon Errata and Data Sheet Clarification
Board design files	ATSAMA5D2C-XULT board design files

Table of Contents

1. Design Checklists

1.1 Schematic Checklist

- Is the MPU supplied with the correct voltage levels?
- Does the power management IC provide enough current for the system?
- Are the correct power supply power-up and power-down sequences implemented?
- Are the decoupling capacitors adequate?
- Is the MPU configured correctly?
- Is the DDR controller configured correctly?

1.2 Layout Checklist

- Does the board feature an uninterrupted GND plane?
- Is a proper layer stack-up defined?
- Are the decoupling capacitors placed as close as possible to the IC pins?
- Are high-speed signal lengths matched and routed over continuous planes (USB, SDCARD, DDR, etc.)?

2. Schematic Checklist Description and Examples

This section describes each item in the schematic checklist and provides implementation examples.

2.1 Provide Adequate Voltage and Sufficient Current

2.1.1 Requirements

Refer to table “SAMA5D2 Power Supplies”, in section “Power Considerations” of the SAMA5D2 data sheet, for the power supplies needed to power the MPU.

2.1.2 Implementation Example

The MCP16502 and MCP16501 PMICs are designed especially for SAMA5D2 applications, as they can output all the power supply domains required by the MPU.

Figure 2-1. Application Schematic Example with MCP16502AA

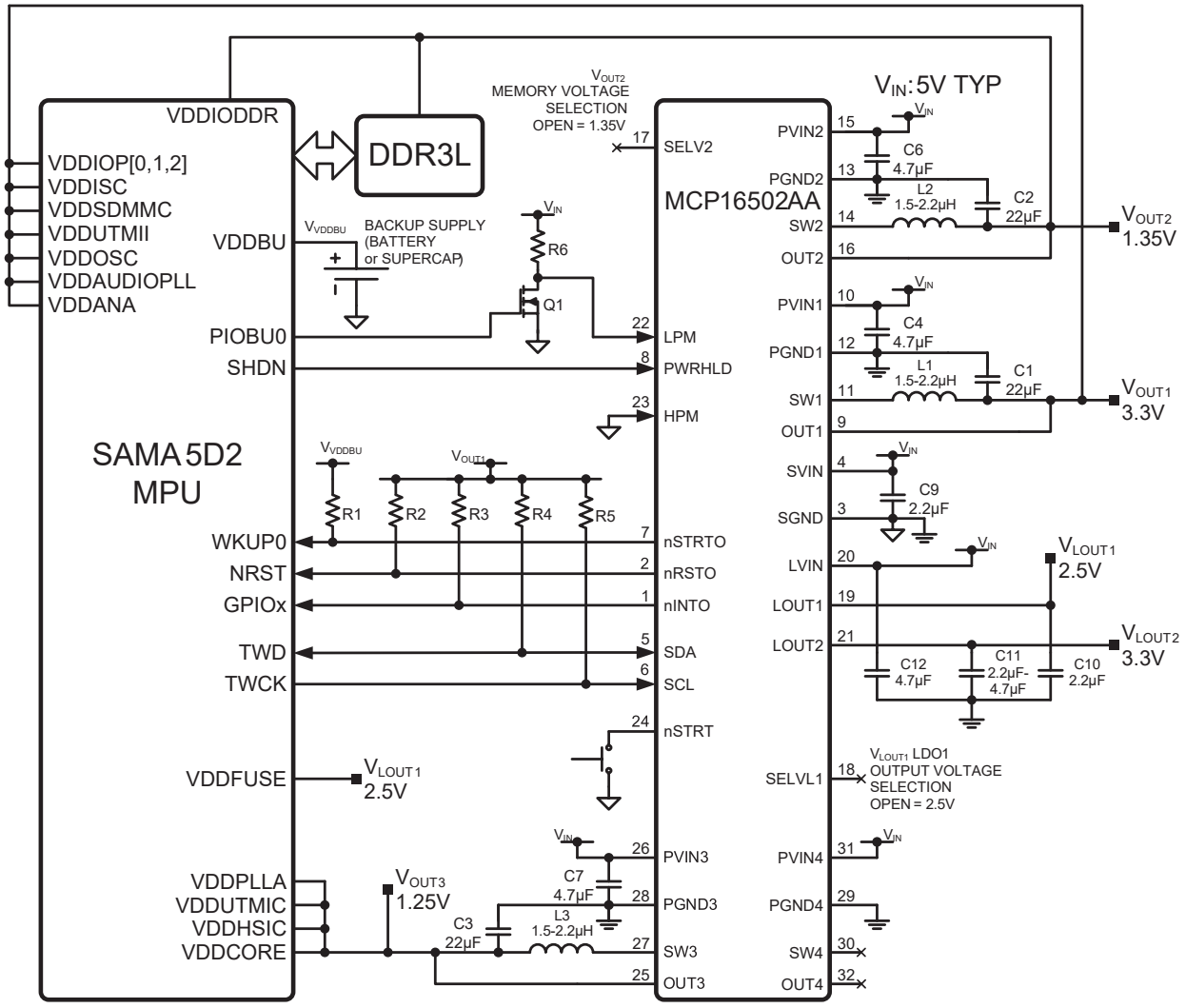
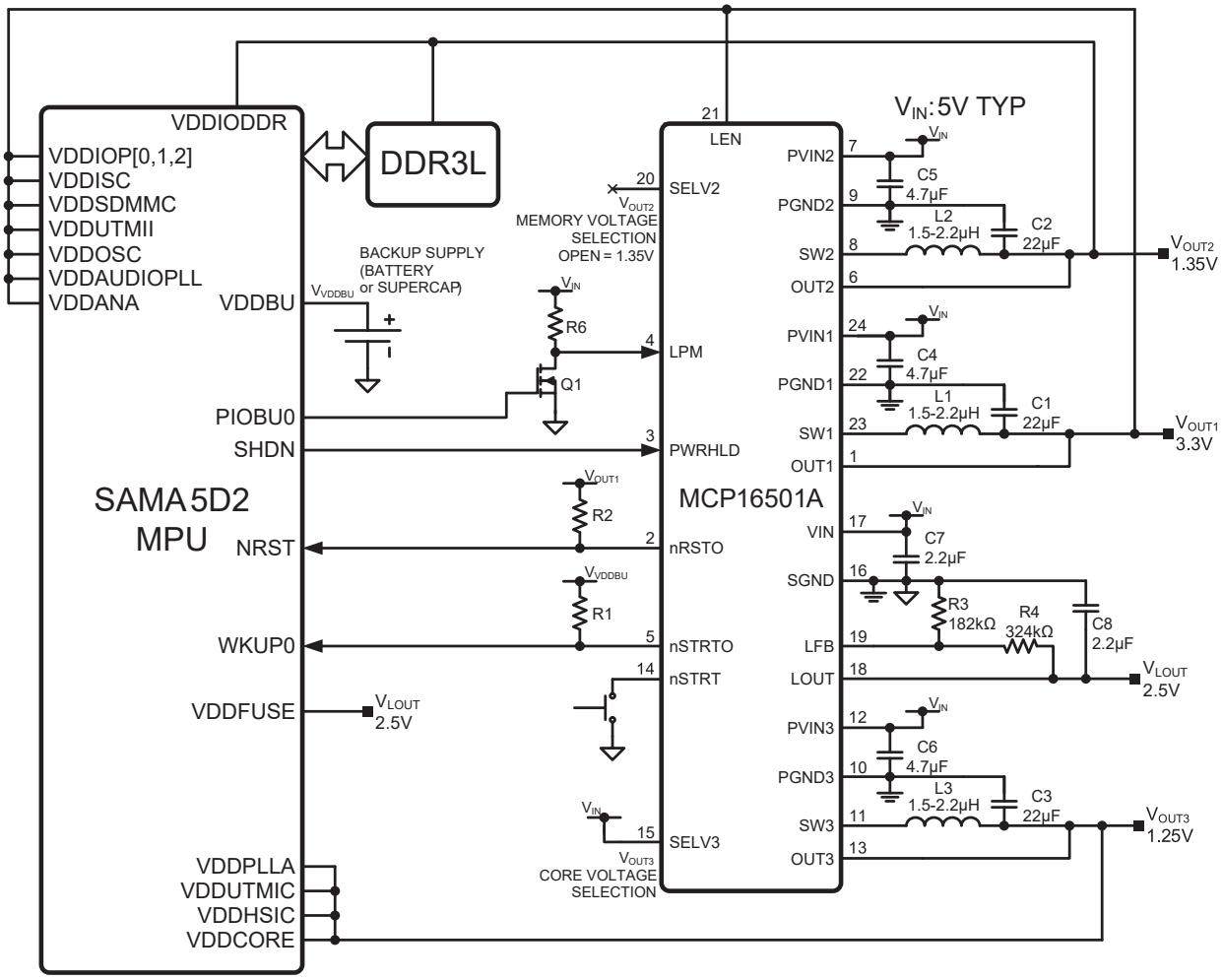


Figure 2-2. Application Schematic Example with MCP16501A



2.2 Ensure Correct Power-Up and Power-Down Sequences

2.2.1 Requirements

Refer to figures “Recommended Power-up Sequence” and “Recommended Power-down Sequence” in the section “Power Considerations” of the SAMA5D2 data sheet for the applicable power supply sequencing.

The table “Power-up Timing Specification” establishes that:

- Power groups 1 and 2 can be established at the same time or Group 2 before Group 1,
- There should not be a delay of more than 1 ms between the establishment of any power supply from Group 1,
- There should be at least 1 ms delay between the VDDBU establishment and VDDFUSE turn-on
- NRST signal should be held low for at least 1 ms after the last established supply.

The table “Power-down Timing Specification” establishes that:

- NRST should be held low before or at the same time with the first supply turn-off,
- VDDFUSE should drop below 1V before or at the same time with the first supply turn-off.

All these power-up and power-down requirements are already implemented in the MCP16502/1 PMIC solutions.

2.3 Ensure that the Power Supply Pins have Adequate Decoupling Capacitors

2.3.1 Requirements

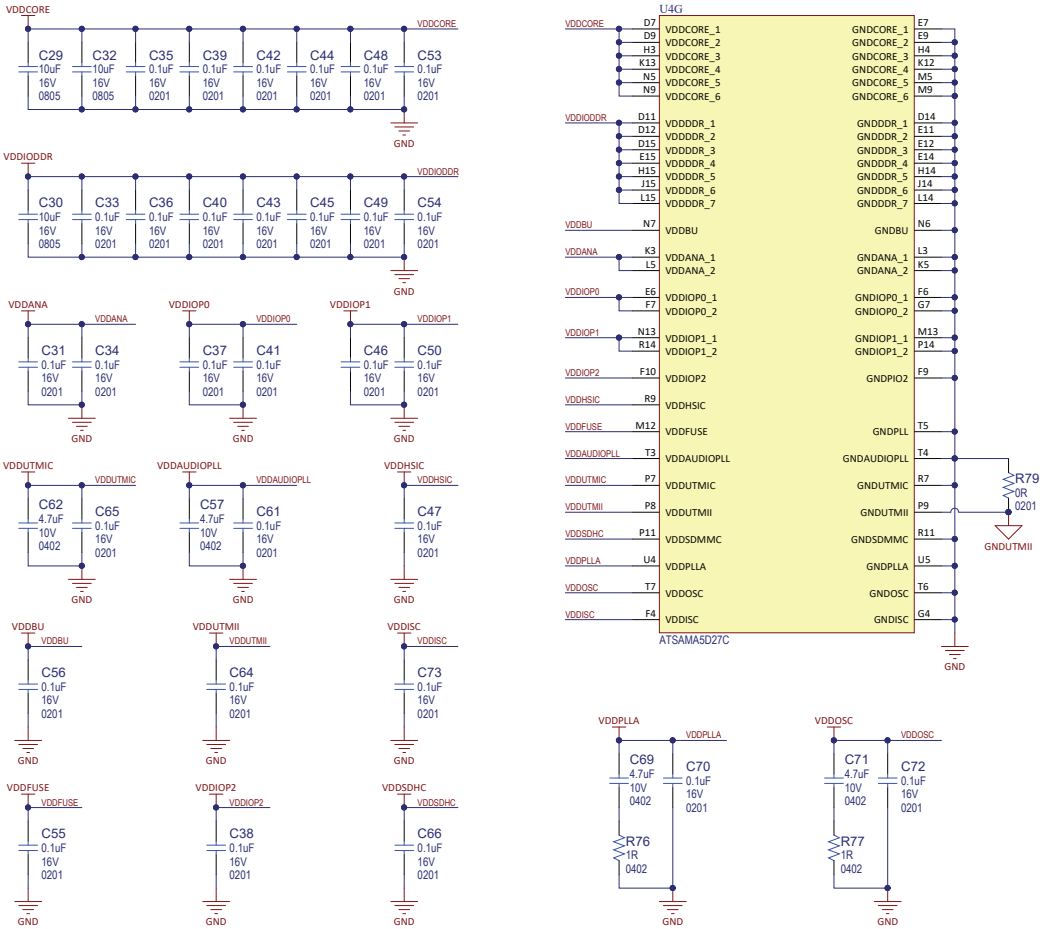
Low-impedance decoupling/filtering of the device power supply inputs must be provided. A 100 nF ceramic X7R (or X5R) capacitor placed very close to each power supply input is a minimum requirement. A 10 µF ceramic X7R (or X5R) ceramic capacitor should also be placed on the VDDCORE and VDDIODDR power rails, close to the MPU.

In the SAMA5D2-XULT, we have opted for 100 nF 0402, X7R rated at 16V and 10 µF 0805, X5R rated at 16V multilayer ceramic capacitors with good results. Smaller sized capacitors provide better decoupling due to reduced inductance.

2.3.2 Implementation Example

It is recommended to separate the power inputs of the internal oscillators and PLL circuits (VDDOSC, VDDAUDIOPLL and VDDPLLA) using a series 10 µH inductors on each input. Other peripheral power inputs (VDDIOP0, VDDIOP1, VDDISC etc.) may use series 180Ω ferrite beads instead when necessary, but the preferred choice is to connect those belonging to the same voltage in a single, solid, unsplit power plane..

Figure 2-3. Processor Power Supplies



2.4 Check MPU Configuration

2.4.1 Requirements

- A 5.62 kΩ resistor is connected to the VBG pin for USB external tuning and an adequate voltage divider is placed on USB VBUS to transform the 5V into the PIO voltage.
  Refer to “Typical Connection” in sections “USB High Speed Device Port (UDPHS)” and “USB Host High Speed Port (UHPHS)” of the SAMA5D2 data sheet.
- The TST pin is grounded.
- If the design does not need JTAG boundary scan, tie the JTAGSEL pin to GND or leave it floating.
- The SDCAL calibration cell input should be connected to ground with a 20 kΩ resistor for 1.8V SDMMC memories or a 16.9 kΩ resistor for 3.3V memories. If the memory device operates in both 1.8V and 3.3V modes, then use a 20 kΩ resistor.
- A 32.768 kHz crystal is placed between XIN32 and XOUT32.
  Refer to section “32.768 kHz Crystal Oscillator Characteristics” in the “Electrical Characteristics” of the SAMA5D2 data sheet.
- A high-frequency clock source is provided either through a crystal oscillator placed between XIN and XOUT or through an external clock generator.
  Refer to section “Main Oscillator Characteristics” in the “Electrical Characteristics” of the SAMA5D2 data sheet.
- If the clock generator option is chosen, it is recommended to ground XOUT to improve stability.
- Clock sources should be chosen with great care.
  Refer to section “Recommended Crystal Characteristics” in the “Electrical Characteristics” of the SAMA5D2 data sheet.

2.4.2 Implementation Example

Figure 2-4. Main Oscillator Connection

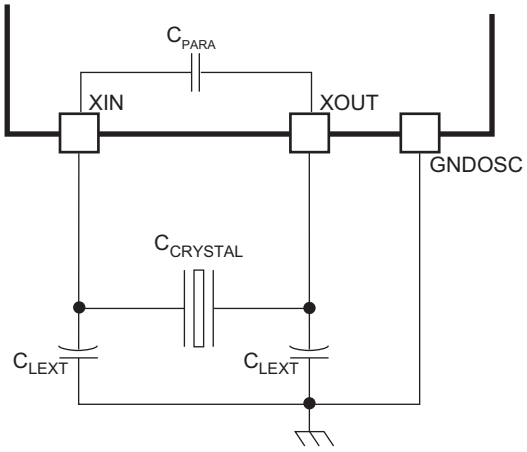
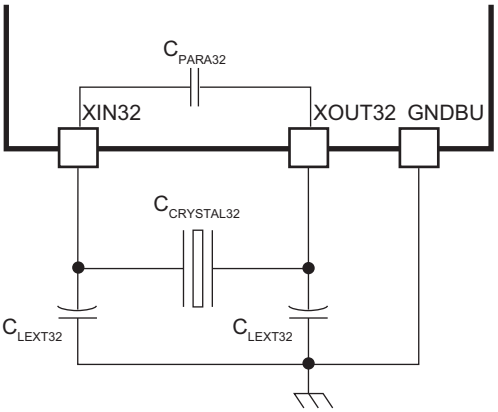
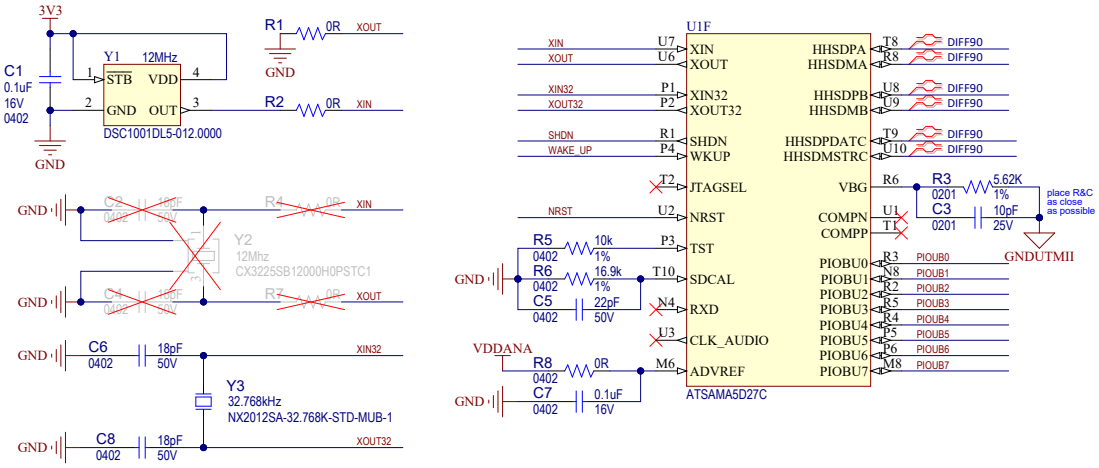


Figure 2-5. 32 kHz Oscillator Connection



In the design schematic below, the SAMA5D2 MPU features the 12MHz DSC1001DL5-012.0000 MEMS oscillator as default main clock source and the NX2012SA-32.768K-STD-MUB-1 crystal loaded with 18 pF capacitors to provide the 32.786 kHz slow clock. Alternatively, by removing R1 and R2 resistors and populating the corresponding parts associated with Y2, then the CX3225SB12000H0PSTC1 12MHz crystal oscillator is used as main clock source.

Figure 2-6. Processor Configuration



2.5 Check the DDR Controller Configuration

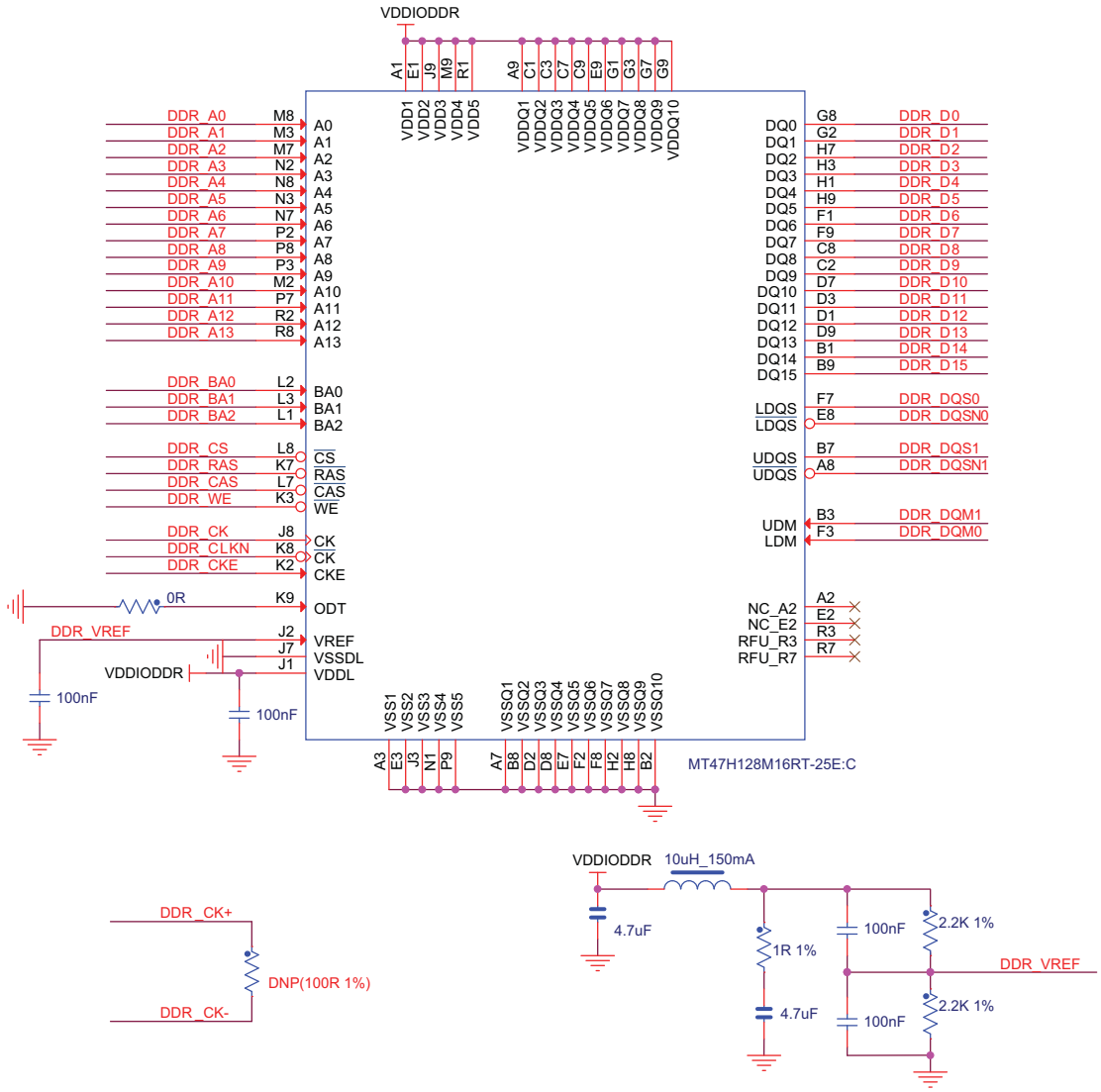
2.5.1 Requirements

- Connect the external memory chosen as required in table “I/O Lines Usage vs. Operating Mode” in the section “External Memories” of the SAMA5D2 data sheet.
- Select the correct value for DDR_CAL depending on the memory used:
  - 21 kΩ for DDR2 and LPDDR1
  - 22 kΩ for DDR3
  - 23 kΩ for DDR3L
  - 24 kΩ for LPDDR2/LPDDR3
- Connect the DDR_VREF pin to VDDIOM/2
- SiP (System-in-Package) versions of the SAMA5D2 MPUs do not have a DDR_CAL pin. They do feature the ZQ pin necessary for the embedded DRAM, which should be connected to ground with a 240Ω resistor.

Refer to “DDR I/O Calibration” in the section “Memories” of the SAMA5D2 data sheet.

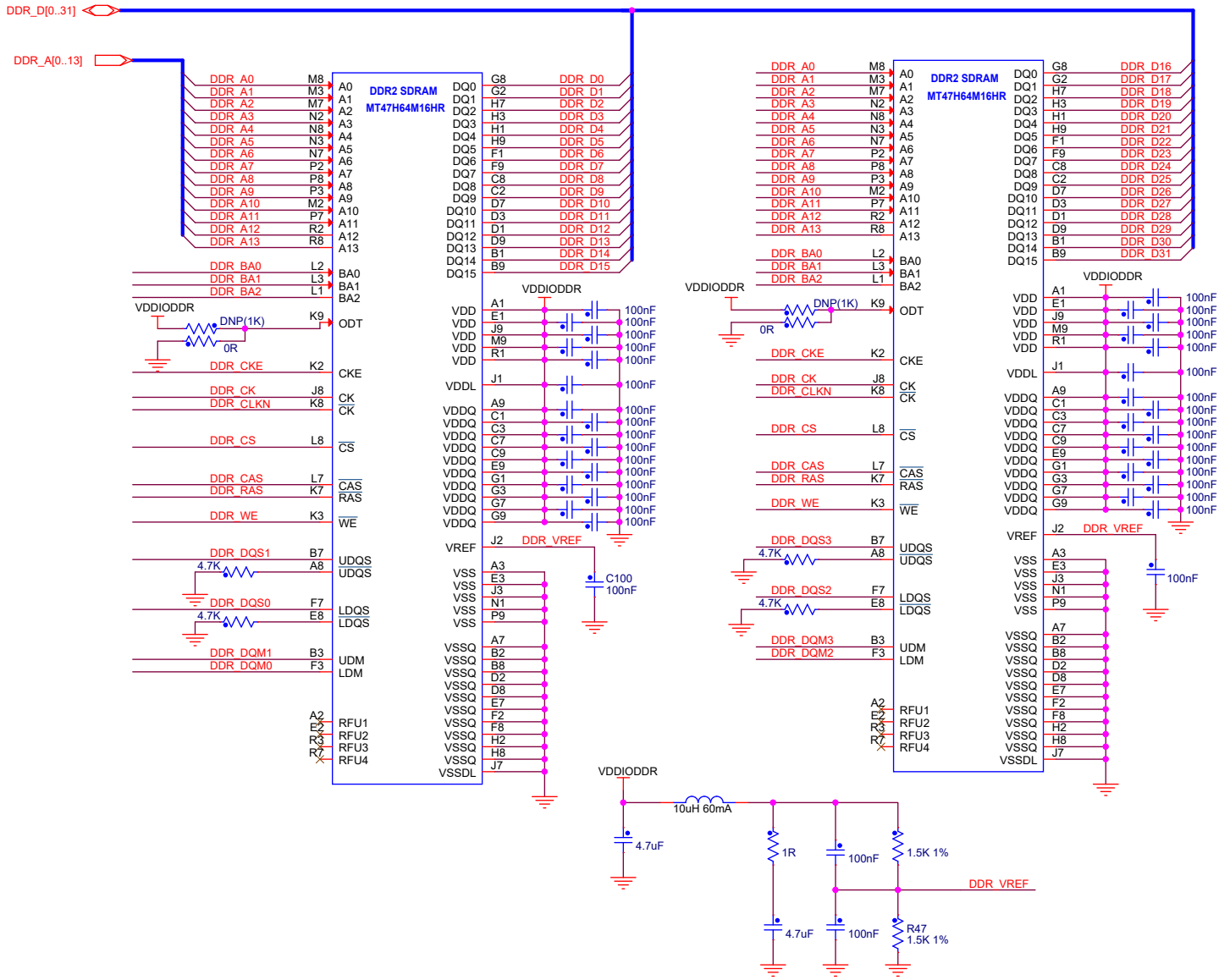
2.5.2 Implementation Example for 16-bit DDR2

Figure 2-7. 16-bit DDR2 Hardware Configuration



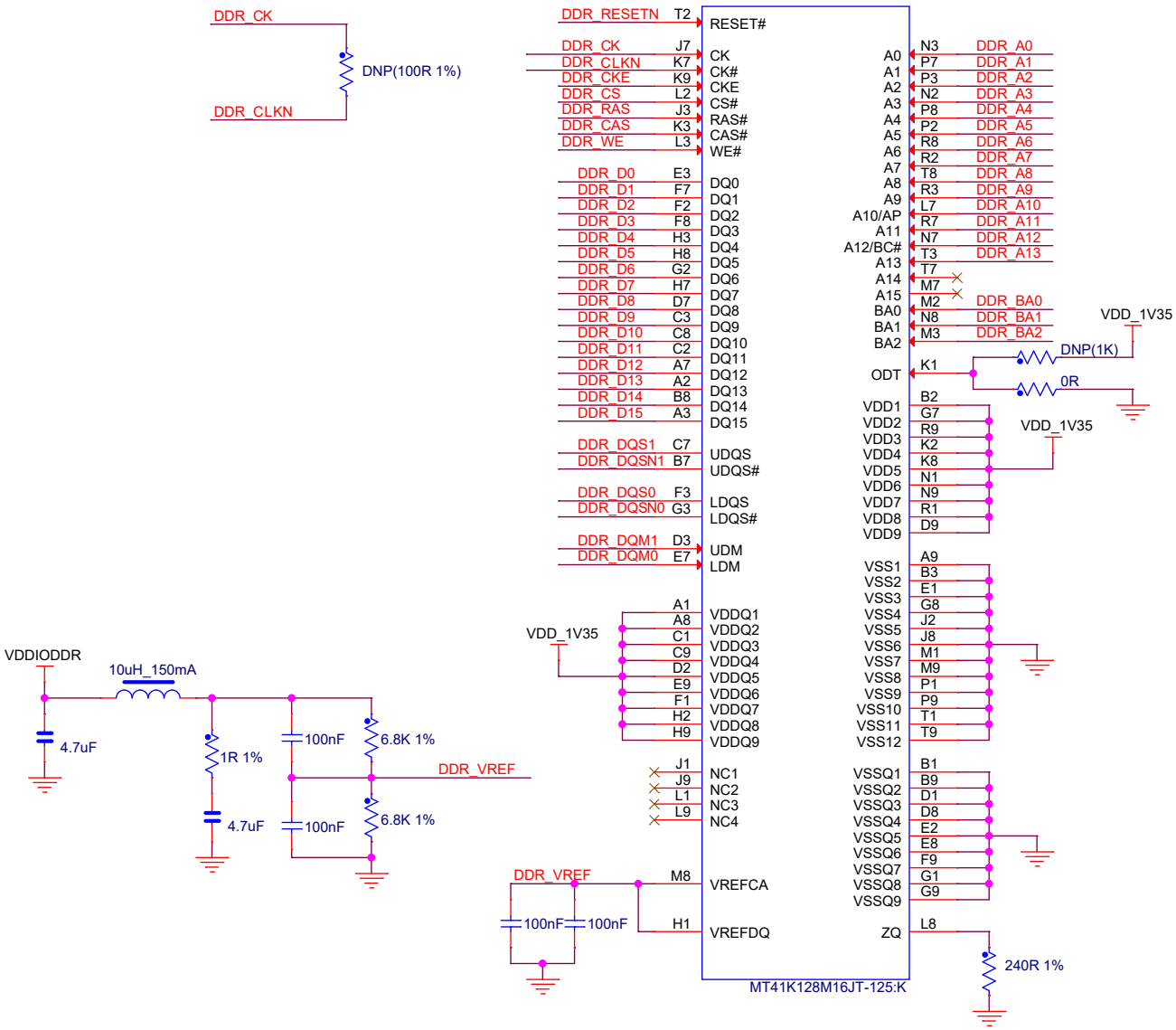
2.5.3 Implementation Example for 2x16-bit DDR2

Figure 2-8. 2x16-bit DDR2 Hardware Configuration



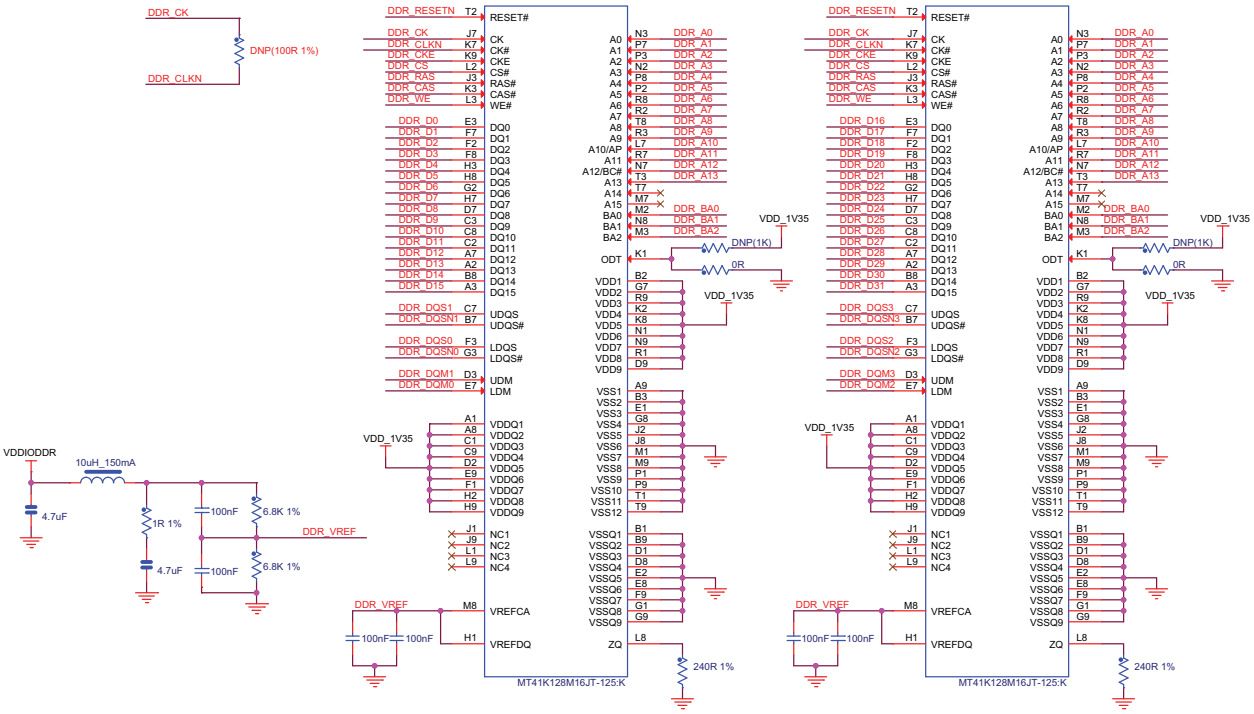
2.5.4 Implementation Example for 16-bit DDR3/DDR3L

Figure 2-9. 16-bit DDR3/DDR3L Hardware Configuration



2.5.5 Implementation Example for 2x16-bit DDR3/DDR3L

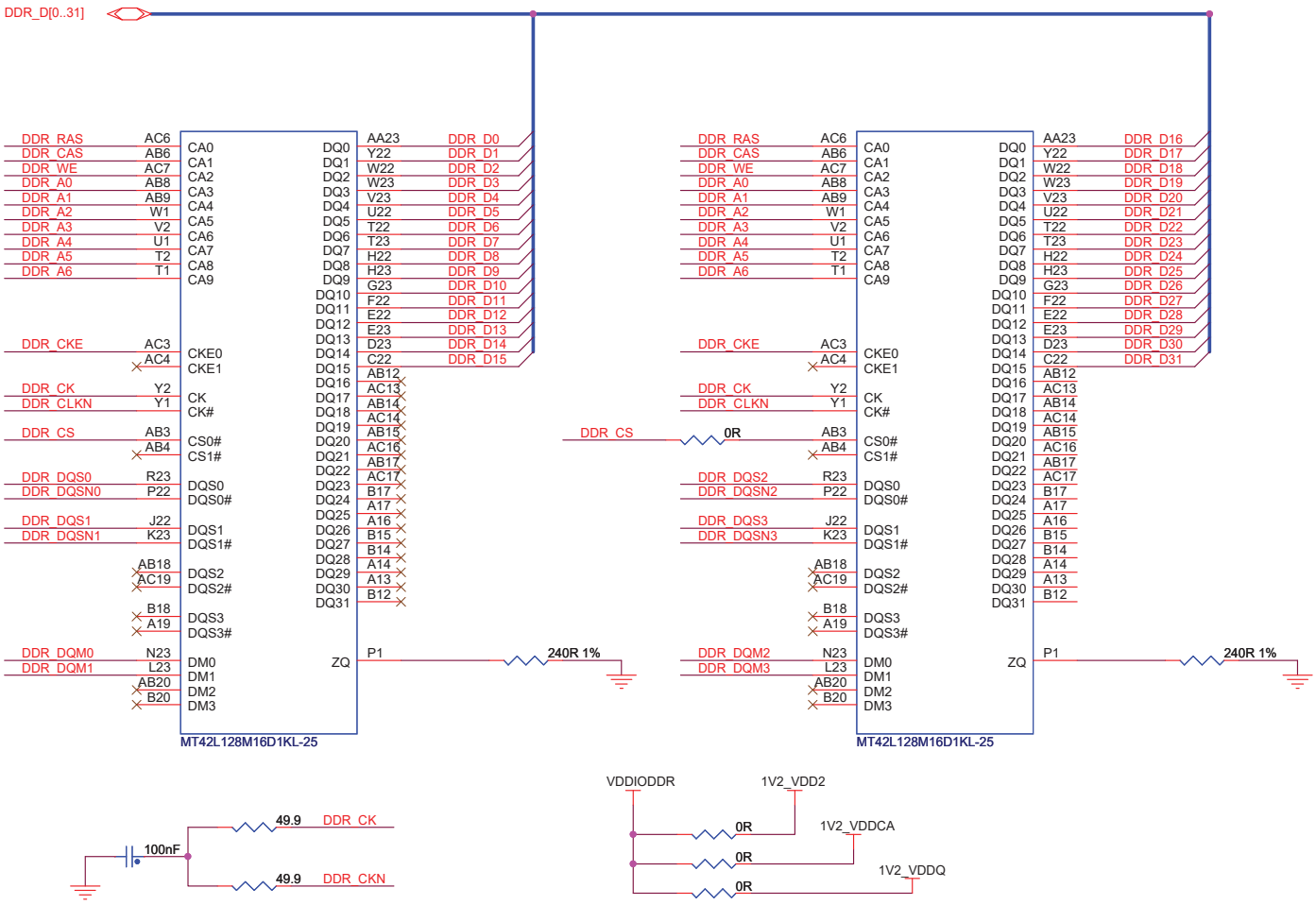
Figure 2-10. 2x16-bit DDR3/DDR3L Hardware Configuration



2.5.6 Implementation Example for 2x16-bit LPDDR2

For the correct signal connection of LPDDR2/LPDDR3 devices, refer to table “CAx LPDDR2 Signal Connection” in the section “External Memories” of the SAMA5D2 data sheet.

Figure 2-11. 2x16-bit LPDDR2 Hardware Configuration



3. Layout Checklist Description and Examples

3.1 Check that the Board has an Uninterrupted GND Plane

3.1.1 Requirements

A PCB with a low-impedance ground plane must be provided. A single unbroken ground plane is a minimum requirement.

3.1.2 Implementation Example

Figure 3-1 depicts a solid/uninterrupted GND plane that stretches all over the board. This is the ideal implementation.

Figure 3-2 shows several cut-outs assigned to a different power supply. This arrangement is to be avoided by all means, as it is a proven source of EMI, therefore prone to failing the EMC compliance tests.

Figure 3-1. Correct GND Plane

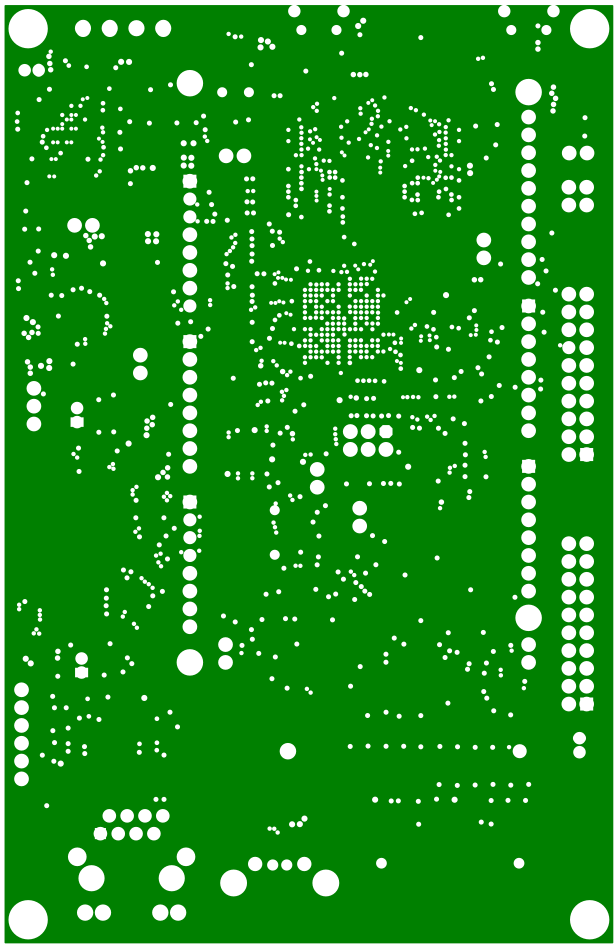
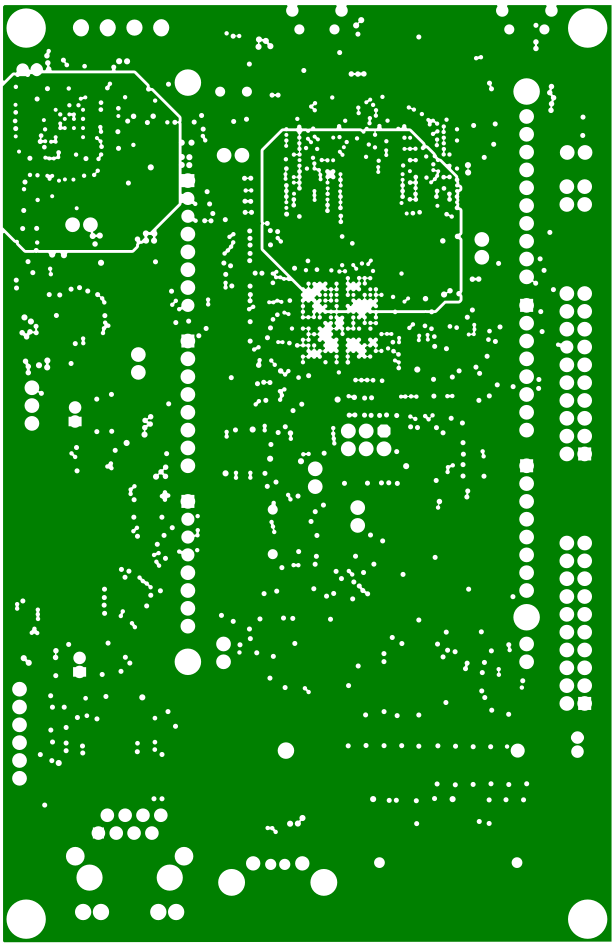


Figure 3-2. Incorrect GND Plane



3.2 Define a Layer Stack-Up so that Line Impedances are matched to Driver Impedances

3.2.1 Requirements

Match the PCB line impedances to their corresponding driver impedances to reduce line reflections:

- Single-ended lines should have 50Ω ±10% single-ended impedance.
- USB lines should have 90Ω ±15% differential impedance.
- DDR CLOCK and STROBE should have 100Ω ±10% differential impedance.

3.2.2 Implementation Example

The SAMA5D2 is available in multiple packages of different sizes and requirements:

Package Name	Pin Count	Ball Pitch
LFBGA289	289	0.8 mm
TFBGA256	256	0.4 mm
TFBGA196	196	0.75 mm

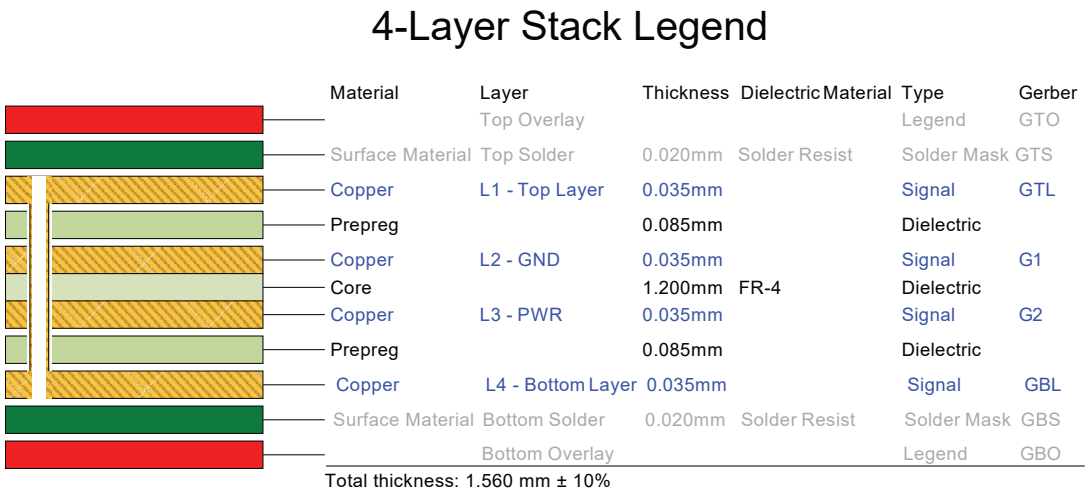
To optimize performance, we recommend using the layer stack-ups, line widths and clearances in the following illustrations.

These stack-ups were selected because they can provide all the required impedances by using minimum 100 µm-wide traces.

The minimum trace width is 100 µm (~4 mil) which is standard for PCB manufacturers. This also ensures that the routing does not take much space on the board.

SAMA5D2 MPUs available in a TFBGA196 package can be implemented on a PCB with a stack-up of minimum four layers.

Figure 3-3. 4-Layer Stack-Up



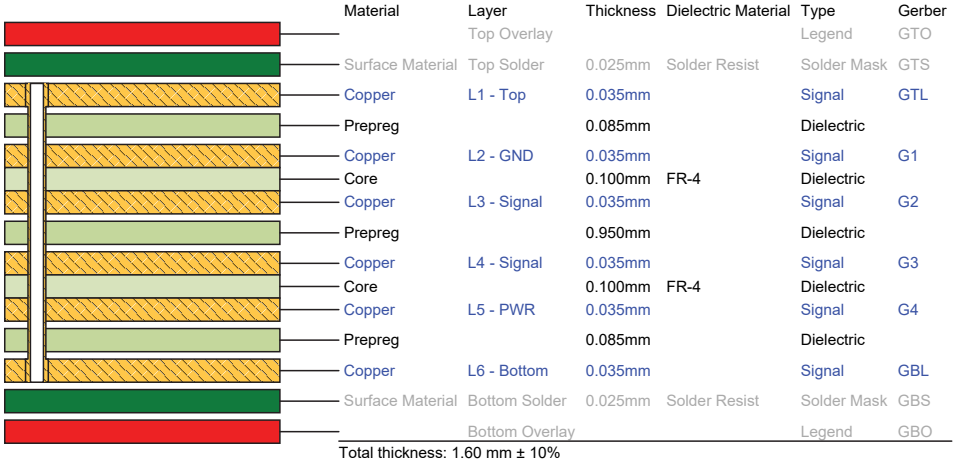
PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L4	L3	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L4	L3	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L4	L3	125	

SAMA5D2 MPUs available in TFBGA289 package can be implemented on a PCB with a stack-up of minimum six layers.

Figure 3-4. 6-Layer Stack-Up

6-Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.025mm	Solder Resist	Solder Mask	GTS
Copper	L1 - Top	0.035mm		Signal	GTL
Prepreg		0.085mm		Dielectric	
Copper	L2 - GND	0.035mm		Signal	G1
Core		0.100mm	FR-4	Dielectric	
Copper	L3 - Signal	0.035mm		Signal	G2
Prepreg		0.950mm		Dielectric	
Copper	L4 - Signal	0.035mm		Signal	G3
Core		0.100mm	FR-4	Dielectric	
Copper	L5 - PWR	0.035mm		Signal	G4
Prepreg		0.085mm		Dielectric	
Copper	L6 - Bottom	0.035mm		Signal	GBL
Surface Material	Bottom Solder	0.025mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

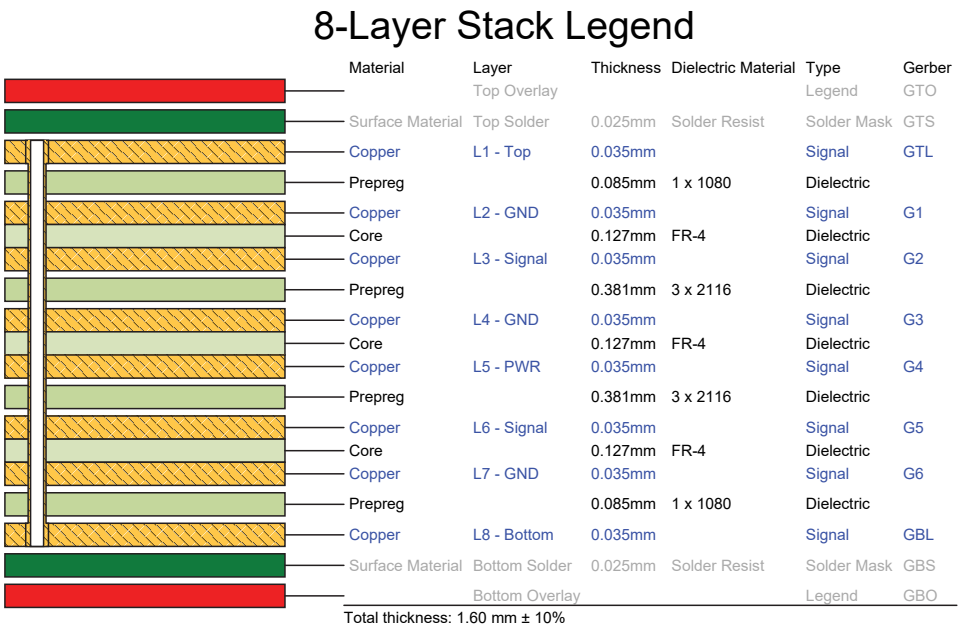
Total thickness: 1.60 mm ± 10%

PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L6	L5	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L6	L5	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L6	L5	125	
SE	50Ω	± 10%	L3	L2	125	
SE	50Ω	± 10%	L4	L5	125	

SAMA5D2 MPUs available in TFBGA256 package can be implemented on a PCB with a stack-up of minimum eight layers.

Figure 3-5. 8-Layer Stack-Up



PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L8	L7	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L8	L7	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L8	L7	125	
SE	50Ω	± 10%	L3	L2;L4	125	
SE	50Ω	± 10%	L6	L5;L7	125	

3.2.3 Additional Tips

Important: Ensure that your PCB manufacturer can produce the specific stack-up.

If the PCB manufacturer does not have the required materials in stock and has to order them specifically, overall production costs may be increased.

Additionally, the manufacturer may recommend a different layer stack-up that can be produced at a lower cost with the materials in stock.

In such cases, a layout can be easily adapted to the recommended stack-up by changing the width of the traces so the required impedances are preserved. With the help of an impedance calculator tool, ensure that the recommendations given in this document are respected (e.g. check that enlarging the traces satisfies the impedance while not infringing the minimal spacing).

Using an impedance calculator eases the design of proper transmission lines. The following example shows the Altium Designer impedance calculator.

After defining the PCB stack-up, you can either use the software to compute the ideal trace width that will yield a specific impedance, or input the trace width so that the tool calculates the resulting impedance.

Figure 3-6. Impedance Calculation

The ATSAMA5D2C-XULT was designed on a six-layer PCB so that the final thickness of the board should be 1.6 mm. Designs which require a different board thickness can be obtained only by modifying the central dielectric height. This does not impact the previously calculated trace impedances.

3.3 Place Decoupling Capacitors as Close as Possible to IC Pins

3.3.1 Requirements

Low-impedance decoupling of the device power supply inputs must be provided. The minimum requirement is that of 100nF ceramic X7R (or X5R) capacitors are placed very close to each power supply input.

3.3.2 Implementation Example

The SAMA5D2 BGA289 is a full 17x17 ball grid array without any depopulated balls. In order to fit 0402 decoupling capacitors on each pin, the capacitor pads land on vias used to connect to power planes, therefore the PCB should be manufactured in respect of this constraint.

Using 0201 decoupling capacitors eliminates the via-in-pad constraint and are the preferred option due to their better performance.

Power is supplied through solid copper polygons placed on the inner layer (power layer). These polygons are formed in such a way that the signals on the bottom layer have their return path through them.

In the ATSAMA5D2C-XULT design files, the power planes are split to allow the user to measure the MPU power consumption, which was a requirement of the evaluation board. However, if this is not a requirement in your design, we highly recommend a single unsplit plane for each power rail.

In the following figure, capacitors are the green rectangles.

Figure 3-7. SAMA5D2 BGA289 Capacitor Placement

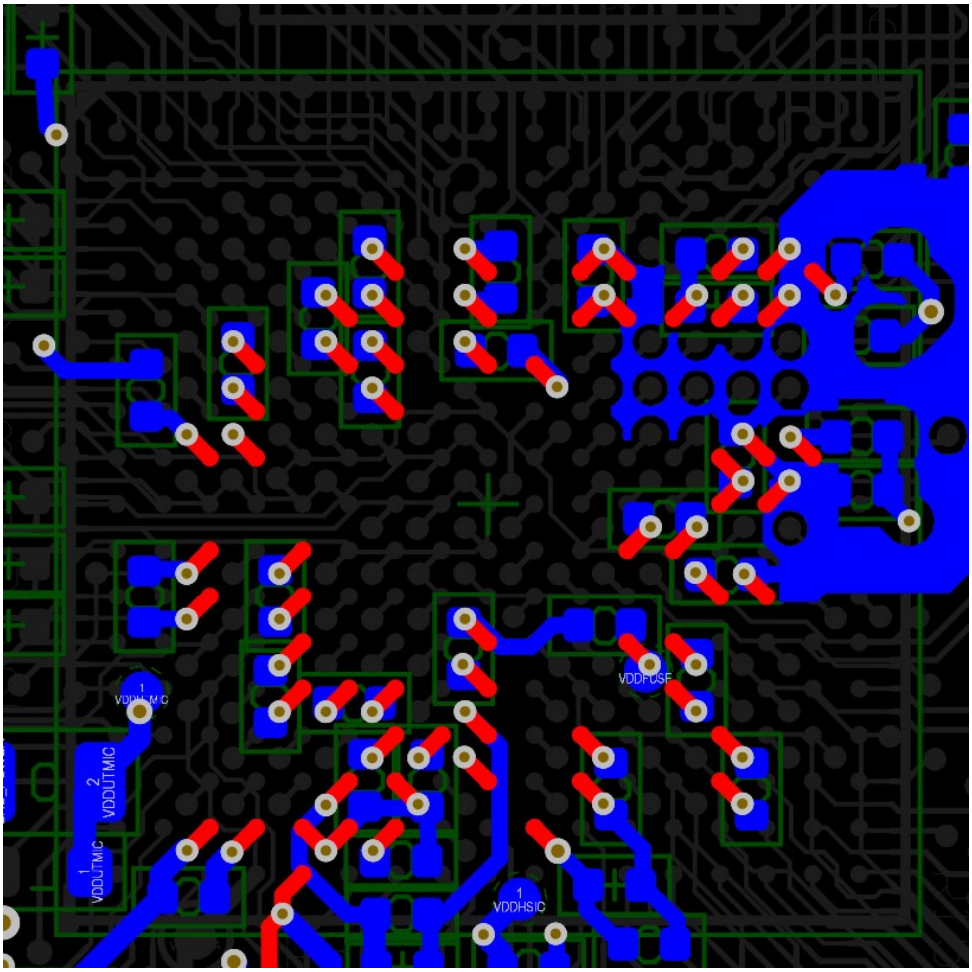
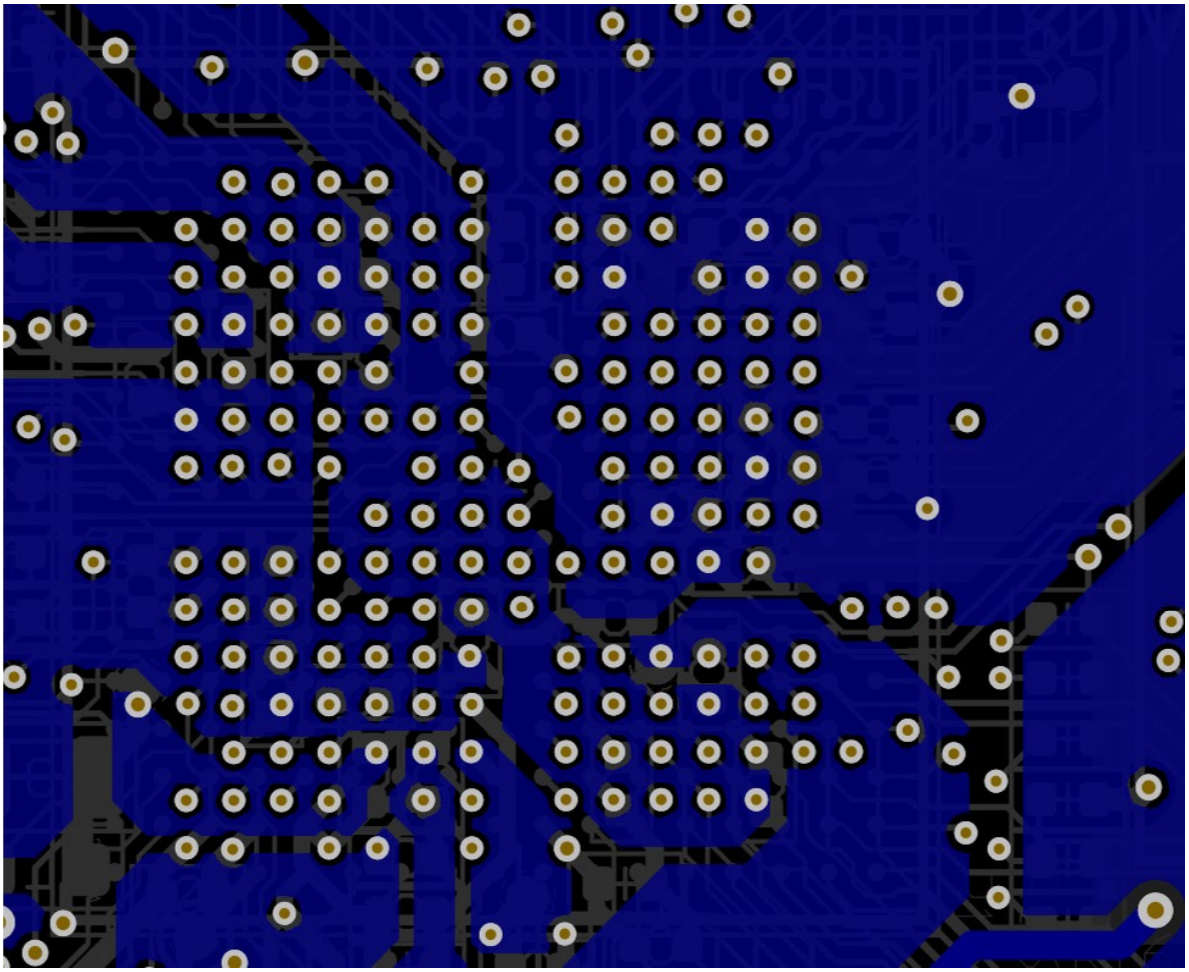


Figure 3-8. SAMA5D2 BGA289 Power Planes



3.4 Length-Match High-Speed Signals

3.4.1 Requirements

High-speed signals must be length-matched and routed over an uninterrupted reference plane (power or ground).

3.4.2 Implementation Example

When routing a 32-bit bus width DRAM interface, it is recommended to use 2x16-bit memory devices. The two devices should be routed using a tree topology, with a midpoint split for the address/command/control signals bus.

For this bus, length matching should be done so that traces connecting the individual memory device to the MPU are matched within a margin.

Traces from each data byte lane should also be matched within its own lane.

It is good practice to route data signals that belong to the same byte lane on the same layer. Figure 3-10 shows the signal routing of data byte lane 0 and 2. For the address/command/control signals bus in Figure 3-9, the routing constraints can be relaxed and routing can be made on any available signal layer.

It is recommended to route the DRAM clock and DQS differential signals on the top and bottom layer, or on the same layer as the rest of the signals from the same group.

Figure 3-9. DDR3L Address and Control

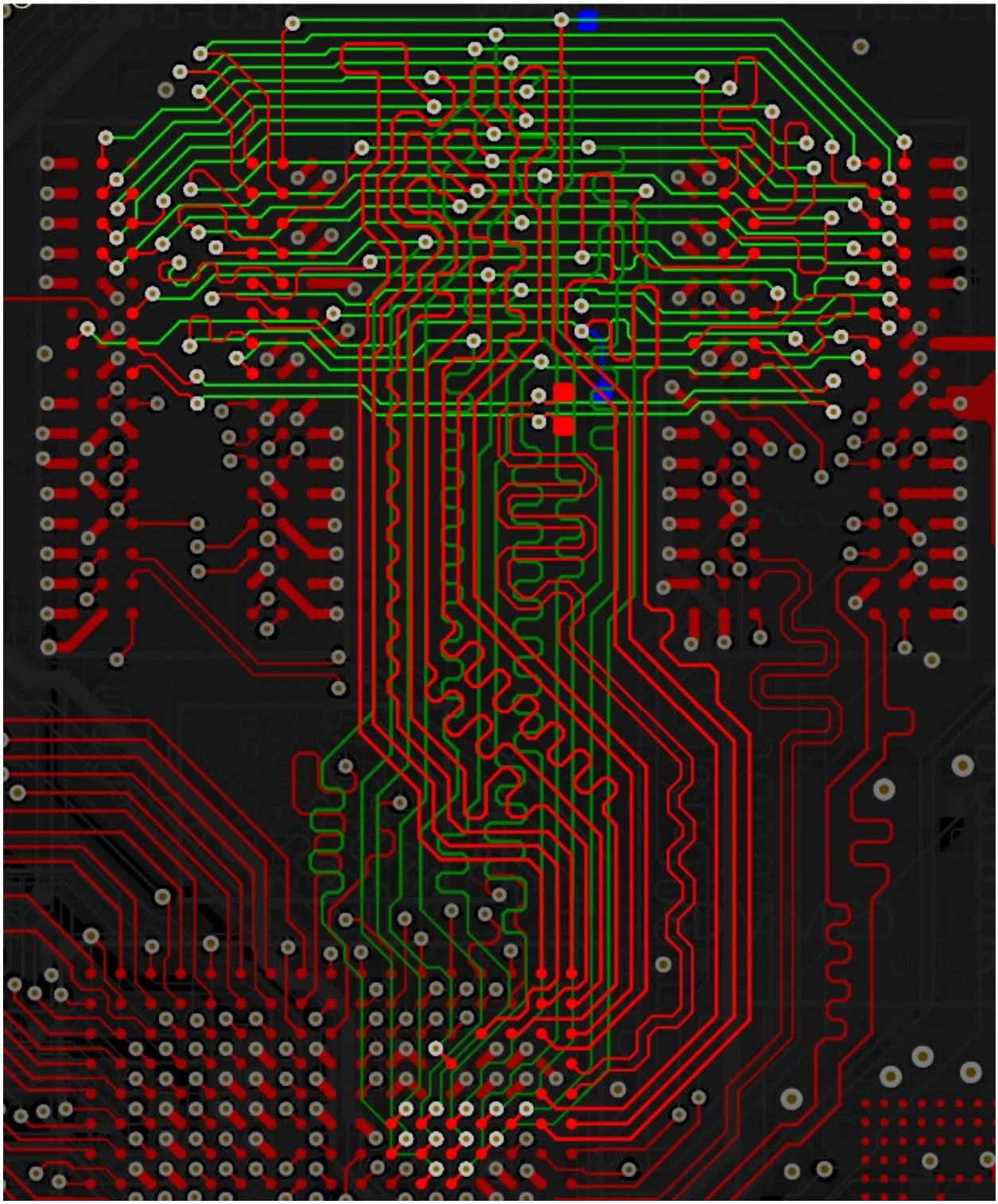
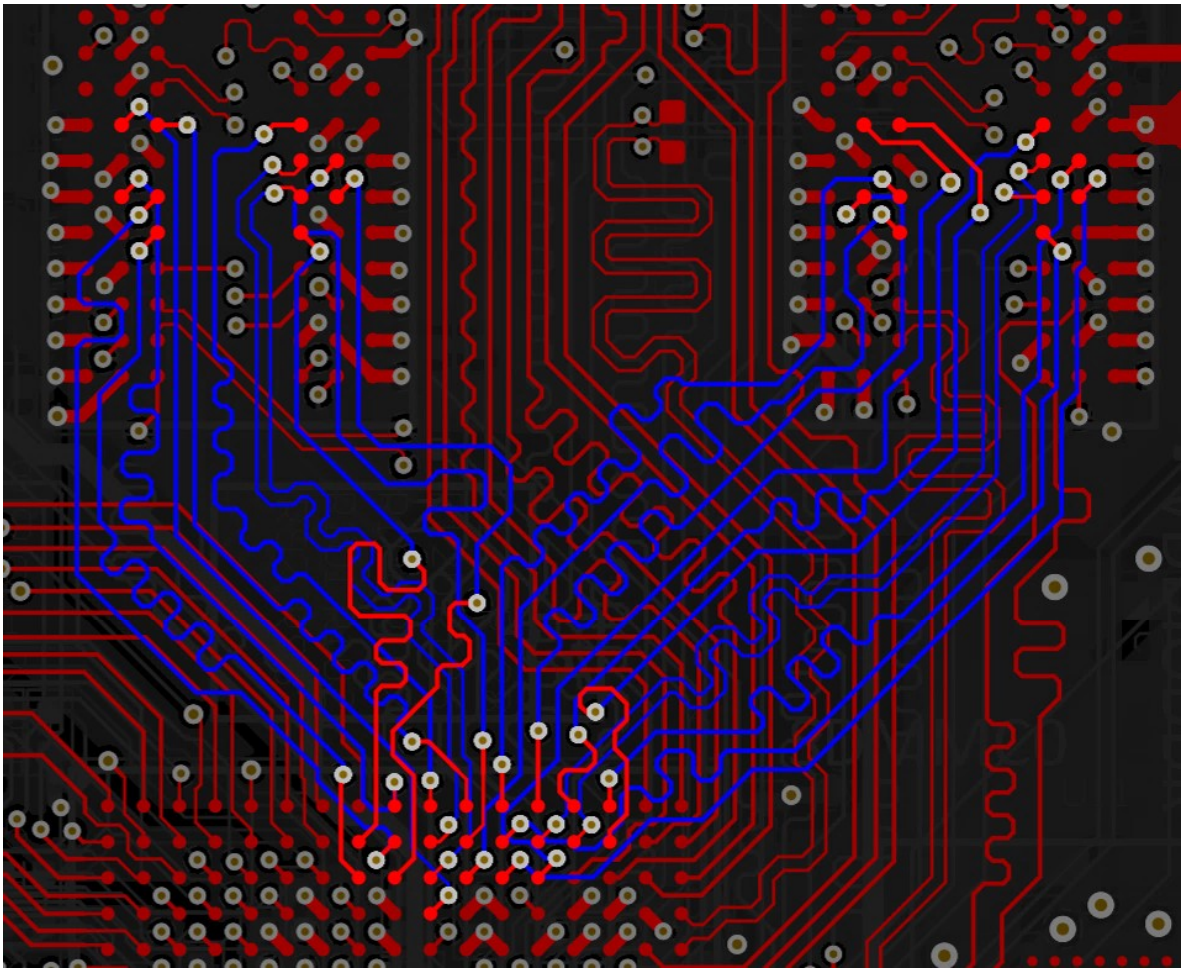


Figure 3-10. DDR3L Data Lanes



4. Revision History

4.1 Rev. A - 03/2022

First issue.

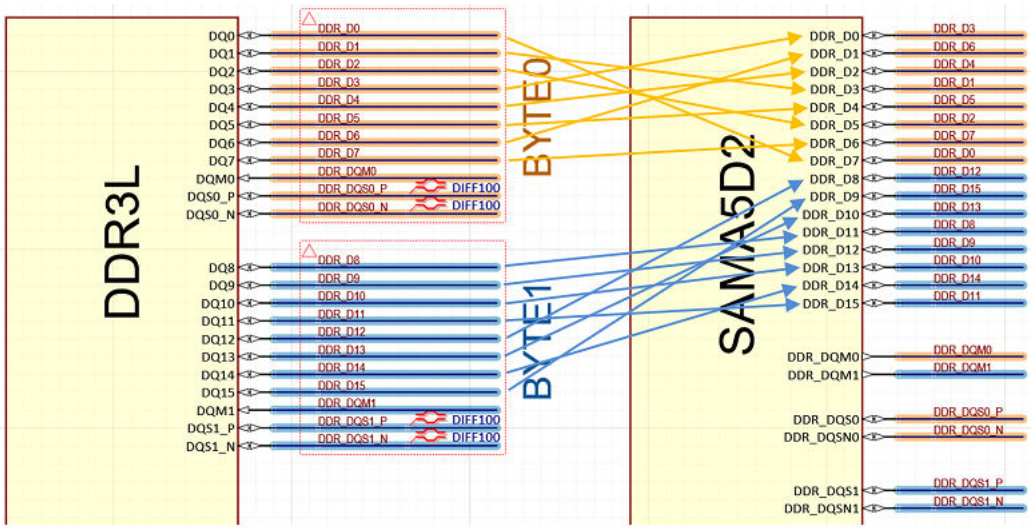
5. Appendix

5.1 Bit and Byte Swapping

DDR3L memories support **bit swapping**, a technique the designer can use to interchange data lines with one another, provided that they correspond to the same byte lane (e.g. any bits inside the D[0..7] lane). This is very useful when trying to optimize a DDR layout routing.

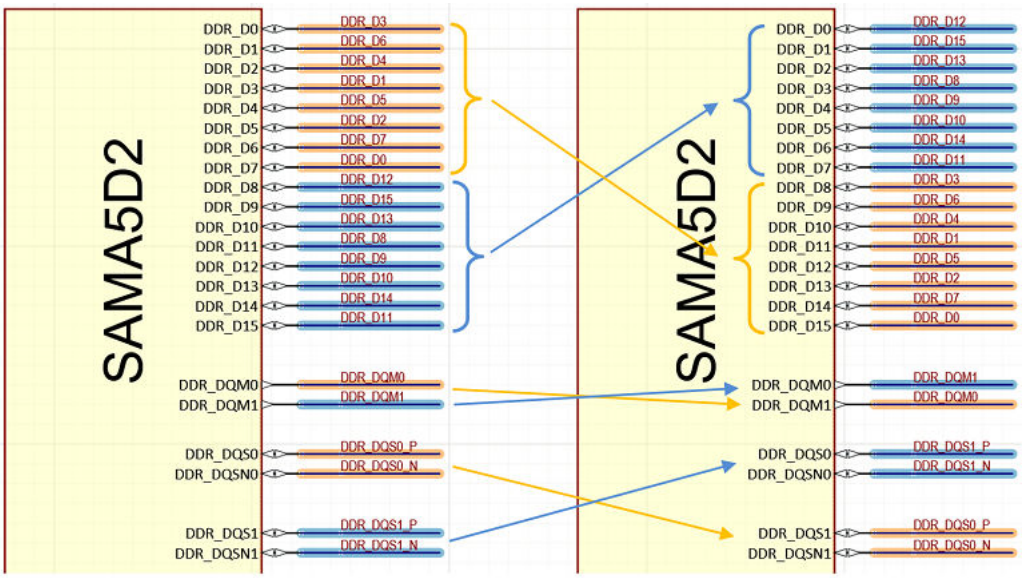
The following figure shows an example of the bit swapping technique which can be implemented in a SAMA5D2 board design.

Figure 5-1. DDR3L Bit Swapping



Byte swapping is another technique that can be used on DDR3L memories. It allows the designer to swap the data lanes with one another, also for the purpose of optimizing the layout. Remember to also swap the DQMx and DQSx signals corresponding to the swapped byte lanes, as illustrated below.

Figure 5-2. DDR3L Byte Swapping



5.2 Good Practices

The following is a list of suggestions for designing with high-speed signals:

- Use controlled impedance PCB traces that match the specified single-ended (50Ω) and differential (100Ω) impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing required to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs, any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- Route CMOS/TTL and differential signals on different layers, which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Use a minimum of 20 mils spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND), avoiding cross splits or openings in those planes.
- For microstrip or stripline transmission lines, keep the spacing between adjacent signal paths at least twice the line width.
- Keep all traces at least five line widths away from the edge of the board.
- Follow the return path of each signal and keep the width of the return path under each signal path at least as wide, and preferably at least three times as wide, as the signal trace.
- To avoid EMIs, avoid routing switching signals across splits or openings in ground planes. Routing around them is preferable even if it results in longer paths.
- Minimize the loop inductance between the power and ground paths.
- Allocate power and ground planes on adjacent layers with as thin a dielectric as possible to create plane capacitance.
- Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
- Supply voltages must be composed of planes only, not traces. Short connections (≈ 8 mils) are commonly used to attach vias to planes. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance (20 mils trace width).

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

Trademarks

ISBN: 978-1-5224-9842-1

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820