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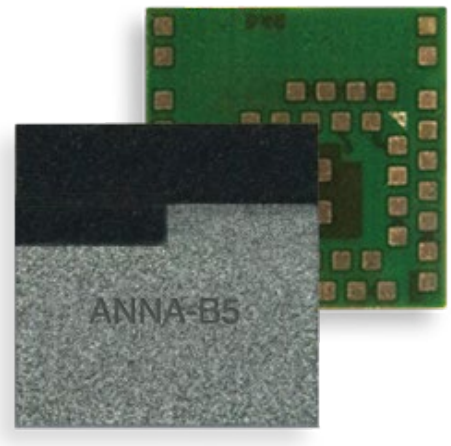
ANNA-B50 series

Stand-alone Bluetooth® LE modules

System integration manual



Abstract

Targeted towards hardware and software engineers, this document describes how to integrate ANNA-B50 series stand-alone Bluetooth® LE module in an application product. It explains the hardware design-in, software, component handling, regulatory compliance, and testing of the modules. It also lists the external antennas approved for use with the module.

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Document information

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Document status descriptions	
Draft	For functional testing. Revised and supplementary data will be published later.
Objective specification	Target values. Revised and supplementary data will be published later.
Advance information	Data based on early testing. Revised and supplementary data will be published later.
Early production information	Data from product verification. Revised and supplementary data may be published later.
Production information	Document contains the final product specification.

This document applies to the following products:

Product name	**Document status**
ANNA-B501	Advance information
ANNA-B505	Advance information

☞ For information about the related hardware, software, and status of listed product types, see also the ANNA-B50 data sheet [2].

Contents

1 Product overview

Based on the Nordic nRF54L15 chipset, the ANNA-B5 series of small stand-alone modules includes an Arm® Cortex®-M33 processor, with floating-point unit (FPU), digital signal processor (DSP) instruction set, and CryptoCell™-312 security architecture. It also features a 128 MHz RISC-V coprocessor with 1.5 MB non-volatile Memory (NVM) and 256 kB RAM. All module variants are qualified against Bluetooth® Core 6.0.

ANNA-B50 modules support multiple peripherals over high-speed SPI, QSPI, TWI, ADC and PWM interfaces, and include a 2.4 GHz radio capable of handling Bluetooth® LE and IEEE 802.15.4 short-range wireless radio with Thread®, Matter™ and Zigbee™, and Nordic proprietary protocols. The modules operate at ambient temperatures of -40 to 85 °C.

ANNA-B50 series modules include an internal power management circuitry that requires only a single supply voltage in the range of 1.7–3.6 V. The wide supply range also enhances the suitability of the modules in battery powered systems.

You can integrate several variants into your product, including ANNA-B501, which has a dedicated pin for connecting an external antenna, or ANNA-B505, which includes an internal chip antenna.

☞ Already globally certified for use with an internal antenna or range of external antennas, the time, cost, and effort required to deploy ANNA-B50 modules into customer applications is significantly reduced.

For detailed product descriptions of all module variants, see the ANNA-B50 data sheet [2].

2 Module integration

ANNA-B50 series modules operate as stand-alone (host-less), Open CPU configurations that allow customer applications to run on the module itself – without any need for a supporting host MCU. The modules support Bluetooth® LE and IEEE 802.15.4 wireless radio with Thread®, Matter™ and Zigbee™. ANNA-B50 series modules support a wide range of IO interfaces, such as GPIO, UART, SPI, I2C, PWM, I2S, NFC, and QDEC to connect external peripherals.

Figure 1 shows a typical integration in which ANNA-B50 is configured as main CPU.

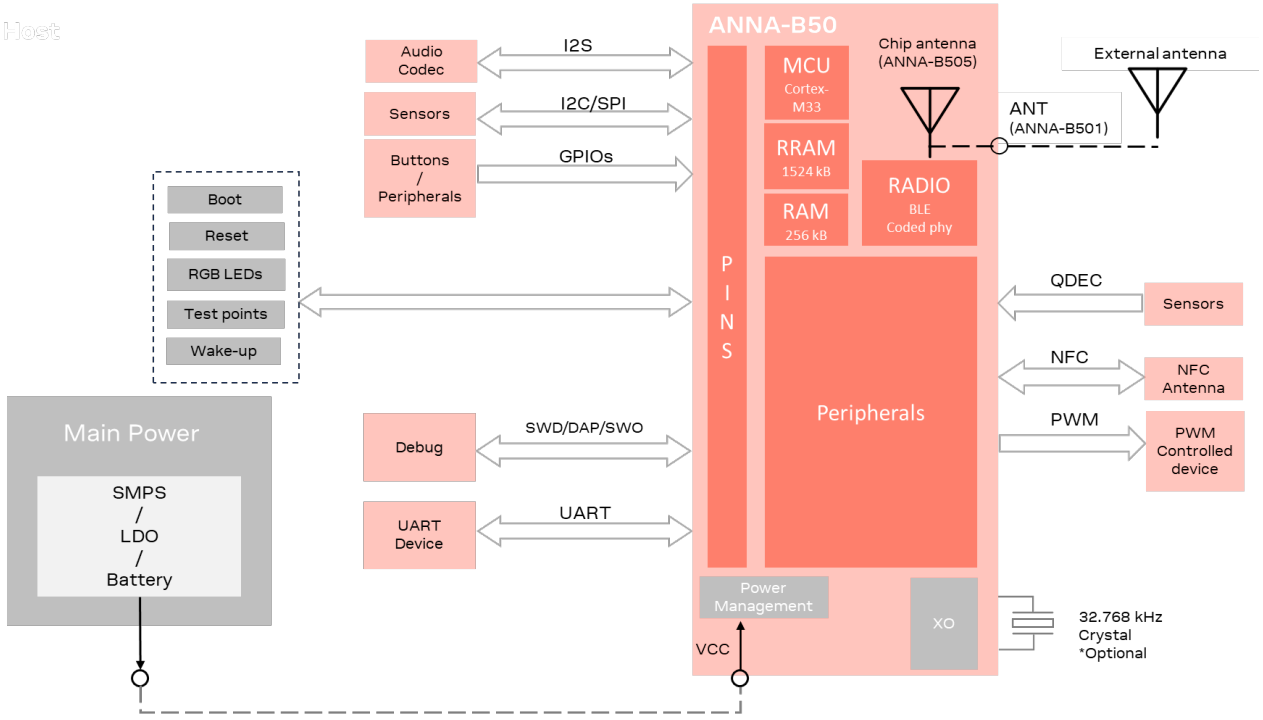

Figure 1: Example of ANNA-B50 integrated as Main CPU

Figure 2 shows how to control ANNA-B50 series modules through a host CPU and interface connections.

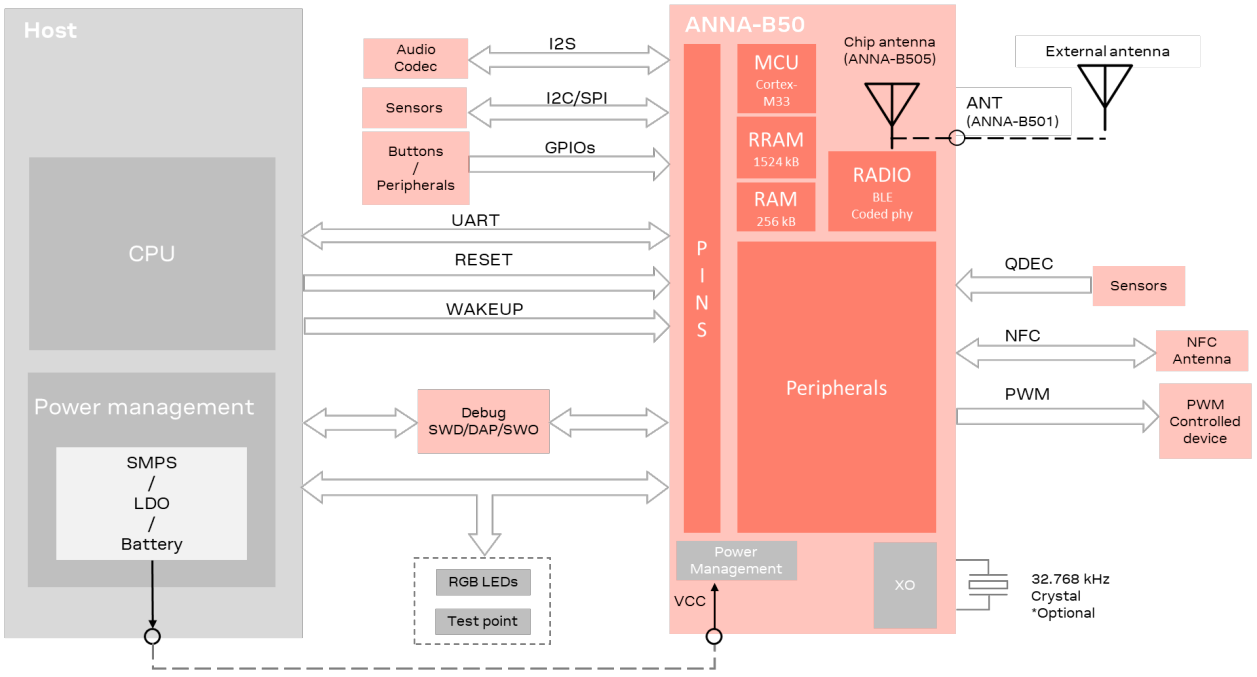

Figure 2: Example of ANNA-B50 integration in a host system with external CPU

Connect ANNA-B50 to a host system via UART to add Bluetooth LE communication capabilities to host application product.

With ANNA-B50, application designs are simplified. Developers can either connect an external antenna via the antenna pin on ANNA-B501 or utilize the internal antenna on ANNA-B505.

2.1 Power supply

The power for ANNA-B50 series modules is applied through the **VCC** pin.

The internal power and clock management system monitors the SoC's components power and clock requests to operate the lowest power consumption mode.

2.1.1 VCC application circuits

Although ANNA-B50 includes a complete power management system and can be sourced from a battery, an external regulator might be required. Then the supplies are taken from either of the following sources:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

An SMPS is the ideal design choice when the available primary supply source is significantly higher than the operating supply voltage of the module. This offers the best power efficiency for the application design and minimizes the amount of current drawn from the main supply source.

⚠ When taking VCC supplies from an SMPS, make sure that the AC ripple voltage is kept as low as possible at the switching frequency. Design layouts should focus on minimizing the impact of any high-frequency ringing.

Use an LDO linear regulator for primary VCC supplies that have a relatively low voltage. As LDO regulators dissipate power linearly related to the step-down voltage, LDOs are not recommended for the step down of high voltages.

DC/DC efficiency should be regarded as a trade-off between the active and idle duty cycles of an application. Although some DC/DC devices achieve high efficiency at light loads, these efficiencies typically degrade as soon as the idle current drops below a few milliamps. This can have a negative impact on the life of the battery.

If decoupling capacitors are needed on the supply rails, it is best practice to position these as close as possible to the ANNA-B50 series module. The power routing of some host system designs makes decoupling capacitance unnecessary.

For electrical specifications, see ANNA-B50 series data sheet [2].

2.2 System functions

2.2.1 Power modes

ANNA-B50 series modules support the following power modes:

- *System ON*
- *System ON low power - Default*
- *System ON IDLE sub-modes*
- *System OFF*

In system on IDLE mode, ANNA-B50 runs in one of the sub modes Constant latency or Low-power mode. Constant latency provides a predictable CPU latency at the cost of increased current consumption. Low-power mode provides lowest possible power consumption.

For a detailed description of each power mode, see also the ANNA-B50 data sheet [2].

2.2.2 Module reset

ANNA-B50 series module is reset / rebooted through the **RESET_N** pin:

- **RESET_N** has an internal pull-up resistor that sets its default state to high. Setting the pin low triggers a “hardware reset” of the module.
- **RESET_N** is preferably driven by either an open-drain or open-collector output or a contact switch.

ANNA-B50 series modules can also be reset using other methods. For more information, see also ANNA-B50 data sheet [2].

2.2.3 Global Real Time Clock (GRTC)

The LFCLK oscillator control, included in the module’s chip, manages the low frequency clock sources and requests.

When peripherals require a low frequency clock, LFCLK, for watchdog timer, or global real-time counter (GRTC). This is provided by the LFCLK control system. The LFCLK is generated from either of the following sources:

- RC oscillator, LFRC, included in the chip
- Crystal oscillator, LFXO, with an external oscillator connected to pin XL1 and XL2.
- Synthesized by the LFSYNT from the high frequency clock, HFCLK.

The LFCLK source is selected by the LFCLK.SRC register. If LFXO is selected, it initially starts with the LFRC and switch to LFXO once the oscillator is stable.

An external crystal provides the lowest sleep current consumption. Although the 32 kHz LFRC consumes slightly more sleep current, it provides a leaner Bill of Materials (BOM).

☞ For RTC pinout information, see also ANNA-B50 data sheet [2].

2.2.3.1 Internal oscillator - 32 kHz LFRC

Using the embedded 32 kHz low-frequency RC oscillator (LFRC) as the module clock provides a more cost-effective Bill of Materials (BoM), lowering costs for end users. However, this choice may result in a slight increase in power consumption.

If you choose to source the module clock from the LFRC, pins 1 and 2, **P1.00/XL1, P1.01/XL2** can be assigned as GPIOs.

2.2.3.2 External crystal

In addition to the embedded 32 kHz low-frequency RC oscillator (LFRC), developers can use an external 32.768 kHz low-frequency crystal oscillator (LFXO) with ANNA-B50 series modules to achieve the lowest overall power consumption. The crystal oscillator requires an external crystal and tuning capacitors to be connected to pin 17 and 18 on ANNA-B50 (P1.00/XL1 and P1.01/XL2). The ANNA-B50 series datasheet provides the specifications for the optional LFXO.

Table 1 describes the specification of the crystal used on EVK-ANNA-B50.

Component	Value	Note
Crystal	32.768 kHz – 20 ppm	Crystal CL=9pF Epson FC-135 NI/SN Termination

Table 1: Specification of the low-frequency crystal used on the EVK-ANNA-B50 evaluation kit

2.3 Antenna integration

ANNA-B50 series modules support either an internal antenna in ANNA-B505 or an external antenna connected through the dedicated antenna pin in ANNA-B501.

2.3.1 Antenna solutions

ANNA-B50 series modules support two antenna solutions:

- ANNA-B501 includes an antenna pin to connect an external antenna to the ANNA-B501 module.
- ANNA-B505 is equipped with an internal chip antenna.

2.3.2 Approved antenna designs

ANNA-B50 series modules come with a pre-certified design that can significantly reduce costs and save time during the certification process. To leverage this benefit, customers must implement an antenna layout that fully complies with the u-blox reference design outlined in Appendix B.
Reference design source files, available from u-blox on request.[1]

Designers integrating a u-blox reference design into an end-product assume sole responsibility for any unintentional emission levels produced by the end product.

For Bluetooth operation, ANNA-B50 series modules have been tested and approved for use with the antennas listed in the pre-approved antennas list.

⚠ To ensure that the compliance and pre-certification of u-blox modules with the various regulatory bodies remains valid, use only the external antennas listed in the Pre-approved antennas list. Reference design source files are available from u-blox on request.

[1] Reference design files are made available only after certification

⚠ If the module is integrated with other antennas, the OEM installer must certify the design with respective regulatory agencies.

2.4 Data interfaces

ANNA-B50 supports five serial interfaces with EasyDMA, including UART, I2C, I2S, and SPI controller/peripheral.

A helpful tool to use when designing for the nRF54L chipset is the nRF54L Pin Planner [30]. Note that this is not an official Nordic tool.

2.4.1 Universal Asynchronous Receiver/Transmitter (UART)

ANNA-B50 series modules include a UART interface for data communication and firmware upgrade. The UART can continue operating while the processor is in low-power mode if an appropriate peripheral clock is available.

The UART supports the following signals:

- Data lines (**RXD** as input, **TXD** as output)
- Hardware flow control lines (**CTS** as input, **RTS** as output)

The UARTs can be used in 4-wire mode with hardware flow control, or in 2-wire mode with **TXD** and **RXD** only.

☞ 2-wire mode is not recommended as it is prone to buffer overruns.

The IO level of the UARTs follows **VCC**.

2.4.2 Serial peripheral interface (SPI)

ANNA-B50 supports a Serial Peripheral Interface (SPI) interface.

Main and *Sub* node operations are possible on the interface.

The SPI interfaces use the following signals:

Signal name	Description
SPI_SCK	Serial clock output, up to 24 MHz
SPI_CS	Chip select
SPI_MISO	MISO serial input data/ Data 1 I/O signal
SPI_MOSI	MOSI serial output data/ Data 0 I/O signal

Table 2: SPI signals in Main mode

2.4.3 Inter-Integrated Circuit (I2C)

ANNA-B50 series modules include a two-wire Interface which is I2C interface compatible.

The I2C interfaces can operate as Controller with multiple *Target* devices on the I2C bus and support standard-mode (100 kbps), fast-mode (400 kbps), and fast-mode plus (1 Mbps) operation.

The interface uses the **SCL** signal to clock instructions and data on the **SDA** signal.

- I2C 2-wire pin configuration:
  - SCL - Clock output in *Controller* device and input in *Target* device
  - SDA - Data input/output pin

The I2C interface requires external pull-up resistors. These shall be connected to the same voltage as the IO voltage of the ANNA-B50. The pull up resistor value you choose depends on the number of

devices connected to the bus, the total capacitive load, and the interface speed selected. With a single device connected, 8– 10 kΩ is recommended. Use a smaller value if more devices are connected.

It is recommended that you verify the interface signal performance to decide optimum resistor value.

2.4.4 Inter-IC Sound interface (I2S)

ANNA-B50 includes an I2S interface with two-channel format and left- and right-aligned formats.

Simultaneous bidirectional audio streaming

- Original I2S and left- or right-aligned formats
- 32-, 24-, 16-, and 8-bit sample widths
- Separate sample and word widths
- Low jitter

2.5 Other Digital interfaces

2.5.1 Near Field Communication (NFC)

ANNA-B50 includes a Near Field Communication Tag (NFCT) that is compliant with listening device NFC-A. The NFCT peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator with 106 kbps data rate.

Connect the NFC antenna to ANNA-B50 pins 22 (NFC1) and 23 (NFC2) and use tuning capacitors to achieve resonance at 13.56 MHz.

The reader and tag are magnetically coupled with each other. The energy transferred depends on the antenna tuning, the size of the antennas, and antenna orientation.

If a specific operating distance is desired these parameters must be considered.

2.5.2 Pulse Width Modulation (PWM)

ANNA-B50 modules support three pulse width modulators with up or up-down counters and four PWM channels that drive assigned GPIOs.

The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

2.5.3 Quadrature Decoder (QDEC)

ANNA-B50 includes two quadrature decoders (QDEC)

Each QDEC is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction.

The QDECs have two inputs, channel 0 (PHASE_A) and channel 1 (PHASE_B), to control incremental and decremental counting in the Timer/PWM Module (TPM). Each QDEC supports two encoding modes: count and direction encoding mode and phase encoding mode. See also Timer/ PWM Module (TPM).

The TPM counter is clocked by channel 0 and channel 1 input signals when the quadrature decoder mode is selected. Therefore, in quadrature decoder mode, channel 0 and channel 1 can only be used in software compare mode. Other TPM channels can only be used in input capture or output compare modes.

2.6 Analog interfaces

ANNA-B50 has up to 32 GPIOs, 8 of which have analog input pins supporting the following functions:

- 8/10/12-bit Analog to Digital Converter (ADC) with up to eight programmable gain channels
- Comparator (COMP)
- 1x Voltage reference (Vref)

☞ For more information about ADC, LPCMP and VREF, see also the ANNA-B50 data sheet [2].

2.7 Debug interfaces

2.7.1 SWD

ANNA-B50 series modules provide a 2-pin, serial-wire, debug interface with a clock (**SWDCLK**) and a single bi-directional data pin (**SWDIO**) for debug and test functionality.

Pin name	SWD		Internal pull-up/pull-down
	Type	Description	
SWDCLK	I	Clock	Pull-down
SWDIO	I/O	Data	Pull-up

Table 3: SWD signals

2.7.2 DAP

ANNA-B50 series modules provide a Debug Access Port (DAP) to debug and trace the core system of the module. On ANNA-B50 series modules, the SWD interface is used as the external connection interface of DAP.

2.7.3 SWO

ANNA-B50 supports a 1-bit Serial Wire Output (SWO) trace port for efficiently accessing core trace information from outside of the module. The SWO port is used to stream-out trace information from various parts of the module, including the Data Watchpoint and Trace (DWT) part, Instrumentation Trace Macrocell (ITM) part, and Breakpoint Unit (BPU) part.

2.8 ANNA migration

The ANNA-B50 module shares similar mechanical outline and footprint as other modules in the ANNA family. When designing for migration, pay special attention to the following:

Power Supply

- The ANNA-B50 power supply is connected to the same **VCC** pin as the generic ANNA family pinout.
- The ANNA-B50 power supply range is 1.7 to 3.6 V which is equal to the generic ANNA family.

Control Signals

- ANNA-B50 uses a power-down signal, **RESET_N**, positioned on the same ANNA family pin position and includes, equal to other ANNA family modules, a generic pull-up resistor.

Flashing and Debug

- The SWDIO/SWDCLK interface is located on generic ANNA family pins.

Internal Antenna

When using ANNA-B50's integrated antenna pay attention to that the layout of the PCB and placement of ANNA-B50 is different from ANNA-B1 and ANNA-B4.

- ANNA-B505 includes a fully integrated antenna.
- ANNA-B505 placement on the application PCB when using the internal antenna is different from ANNA-B1 and ANNA-B4.
- When using ANNA-B505 with internal antenna corresponding land patterns for ANNA-B1 and ANNA-B4 pins 44, 45, 46, and 52 shall be removed from the main PCB layout.

External Antenna

- ANNA-B501 uses the generic ANNA family pin for antenna connection and is fully compliant with ANNA family implementation.

3 Design-in

Follow the design guidelines in this chapter to optimize the integration of ANNA-B50 series modules in the final application board.

3.1 Overview

All application circuits must be properly designed, but several points require special attention during the application design. In an order of importance consider:

- Module antenna connection: **ANT** pin RF transmission lines connecting the **ANT** pin with the related antenna connector or antenna, must be designed with a 50 Ω impedance characteristic. See also RF transmission line design.
- Module supply: **VCC** pin.
  Supply circuits can affect RF performance, so it is important to observe the schematic and layout design for these supplies. See also VCC application circuits. Select appropriate power supply source and bypass capacitors, and then carefully route the power supply nets or planes ANNA-B50 series data sheet [2].
- High-speed interfaces: **UART, SPI, I2C** pins.
  High-speed interfaces are a potential source of radiated noise that can affect the regulatory compliance standards for radiated emissions. It is important to follow the schematic and layout design recommendations described in the General layout guidelines.
- System functions: **RESET_N**, GPIO, and other System input and output pins
  Careful utilization of these pins in the application design is required to guarantee for correct boot up and system operation. Ensure that the voltage level is correctly defined during module boot. It is important to follow the schematic and layout design recommendations described in the General layout guidelines.
- Other pins: **ADC**, **I2S, QDEC,** and NC pins.
  Careful utilization of these pins is required to guarantee proper functionality. It is important to follow the schematic and layout design recommendations described in the General layout guidelines.

3.2 RF Interface

ANNA-B505 feature an **internal chip antenna** and ANNA-B501 an **antenna pin** for connecting an external antenna, offering flexibility in integration across a wide range of application products.

The choice between using the internal or external antenna depends on several factors, including the product housing material, restrictions on module placement on the PCB, and RF performance requirements. Notably, the internal chip antenna is unsuitable for enclosures made of metal or plastic containing metallic flakes, conductive paint, or lacquer. In such cases, using an external antenna is strongly recommended to ensure reliable RF performance.

⚠ According to FCC regulations, the transmission line from the module's antenna pin to the antenna or antenna connector on the host PCB is considered part of the certified antenna design. Integrators must either follow one of the reference designs used in the module's FCC type approval or certify their own design.

3.2.1 Antenna integration

Antenna design should begin early in the product development cycle. Using prototype PCBs and antenna assemblies allows evaluation of key RF parameters such as gain, efficiency, and radiation pattern. Always follow the antenna manufacturer's recommendations for layout, matching circuitry,

and installation. A pi filter is recommended to facilitate impedance matching of the antenna connection if needed.

- To avoid degradation of the antenna characteristics, do not place physically tall or large components closer than 10 mm to the antenna.
- To minimize detuning and signal loss, maintain at least 10 mm clearance between the antenna and the device casing. Materials such as polycarbonate (PC) and acrylonitrile butadiene styrene (ABS) are preferred for enclosures due to their relatively low dielectric constant and loss tangent, which reduce their impact on antenna performance
- Consider the end products use case and assembly to make sure that the antenna is not obstructed by any external item.

Table 4 summarizes the key requirements for the antenna RF interface to ensure radiated performance.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the ANT pin.
Frequency Range	2400 - 2500 MHz	Bluetooth LE.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or S_{11}. As a parameter of the of the standing waves ratio (VSWR) measurement, S_{11} refers to the amount of reflected power. This parameter indicates how well the primary antenna RF connection matches the 50 Ω characteristic impedance of the ANT pin. To maximize the amount of the power transferred to the antenna, the impedance of the antenna termination must match (as much as possible) the 50 Ω nominal impedance of the ANT pin over the entire operating frequency range.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	Radiation efficiency is the ratio of the radiated power against the power delivered to the antenna input; the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain	+3 dBi	Although higher gain antennas can be used, these must be evaluated and/or certified. To comply with regulatory agencies radiation exposure limits, the maximum antenna gain must not exceed the value specified in the data sheet [2]. See also Regulatory compliance.

Table 4: Summary of antenna interface requirements for ANNA-B50

Certification Considerations

The RF certification of the ANNA-B50 module extends to the final product. Antenna performance directly influences both product functionality and regulatory compliance.

3.2.2 ANNA-B505 with Internal Antenna

The embedded chip antenna in ANNA-B505 does not require an external antenna tuning strip. Connect the ANT pin 6 to the ANT_INT pin 5 to use the internal antenna. However, it imposes physical constraints on ANNA placement and PCB layout, regarding ground clearance and GND plane size and PCB placement. The antenna performance is sensitive to nearby conductive materials and depends on the overall mechanical and electromechanical design of the product.

For optimal operating performance, observe the following layout considerations when integrating ANNA-B505 in an application product:

- The module shall be placed in the center of an edge of the host PCB.
- A large ground plane on the host PCB is a prerequisite for good antenna performance. A ground plane extending at least 10 mm on the three non-edge sides of the module is recommended, as shown in Figure 3.

- Include a continuous GND plane underneath the module with a cut out underneath the antenna, as shown in Figure 3.
- Observe the antenna “keep-out” area on all layers, as shown in figures Figure 3 .
- ANNA-B50 has GND pads located close to the antenna, as shown in the upper part of Figure 3. Connect these pads to GND. Detailed dimensions of the footprint, including those related to these GND pads, can be found in the ANNA-B50 series data sheet [2].
- Include plenty of stitching vias from the module ground pads to the GND plane layer. Ensure that the impedance between the module pads and ground reference is minimal.

Figure 3 shows the PCB layout of ANNA-B505 with internal antenna. Observe the GND clearance on the top of ANNA-B505 footprint implemented on all PCB layers, the GND area and stitching vias.

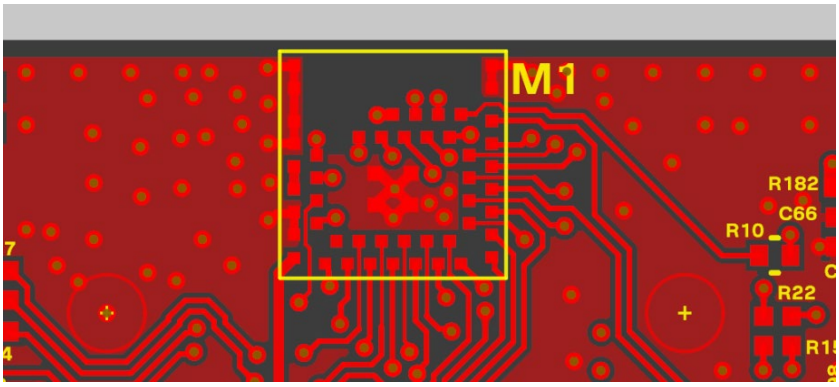

Figure 3: ANNA-B505 layout prepared for internal antenna.

3.2.3 ANNA-B501 with External Antenna

The use of an external antenna offers flexible placement and do not constrain module positioning on the PCB. To maintain antenna performance, connect the antenna with low-loss RF cables and high-quality 50 Ω coaxial connectors. Antennas should be selected based on their radiation characteristics and suitability for the operating frequency bands. The antenna shall be connected to ANNA-B501’s ANT pin.

Common external antenna types used in Bluetooth applications include:

- **Monopole Antennas**: Require a counterpoise, typically the PCB ground plane or cable shield. Performance is highly dependent on ground plane size which preferably shall not be shorter or narrower than a quarter wavelength. For 2.4 GHz, a quarter-wavelength is approximately 1.5 cm on FR4.
- **Dipole Antennas**: Balanced and self-contained, they do not require a counterpoise and are less sensitive to PCB GND and product size.
- **Inverted-F Antennas (IFA)**: Electrically similar to monopoles but folded for compactness. Require a ground plane and are sensitive to layout and nearby components.
- **Ceramic Chip Antennas**: Small surface-mount antennas placed on the application PCB. Require matching networks and careful layout to perform well.
- **Flexible PCB Antennas**: Printed on flexible substrates for integration in constrained spaces, common in wearables. Require RF routing and careful placement.
- **Wire Antennas**: Simple quarter-wave wires soldered or connected to the PCB. Cost-effective and tunable, but sensitive to placement and grounding.

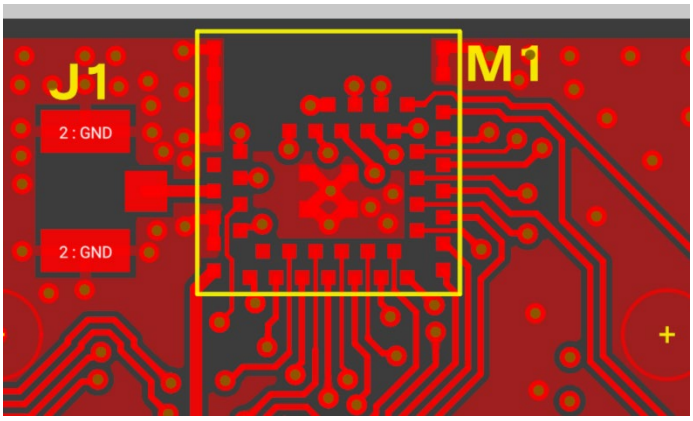

Figure 4: ANNA-B501 layout prepared for u.FL connector in combination with the internal antenna for ANNA-B505.

3.2.4 RF transmission line design

RF transmission lines connecting the **ANT pin** with the related antenna connector or antenna, must be designed with a 50 Ω impedance characteristic.

Figure 5 shows the design options for PCB transmission lines, where:

- **Microstrip**: A conductive trace positioned above a single ground plane, separated by a dielectric substrate. Signal coupling occurs primarily with the ground plane beneath.
- **Coplanar Microstrip**: A microstrip configuration where the trace is flanked by adjacent ground conductors on the same layer, in addition to coupling with the underlying ground plane. All elements are separated by dielectric material.
- **Stripline**: A conductive track embedded between two parallel ground planes, fully enclosed within dielectric material. This structure provides excellent isolation and symmetrical field distribution.

The parameters shown in the cross-sectional area of each trace design include:

- **Width (W)**: Represents the width of the copper trace.
- **Spacing (S)**: Denotes the lateral distance between the top copper trace and the adjacent ground planes on the same layer (used in coplanar configurations).
- **Substrate Thickness (H)**: Indicates the vertical distance between the top copper trace and the reference ground plane located on the bottom layer of the PCB.
- **Copper Thickness (T)**: Refers to the thickness of the copper layer itself. This is often specified as **Base Copper Weight**, a standard parameter in PCB stack-up definitions.

Dielectric constant (ε_r) defines the ratio between the electric permeability of the material against the electric permeability of free space.

☞ The width of a 50 Ω microstrip depends on mainly "ε_r" and "H", which must be calculated for each PCB layer stack-up.

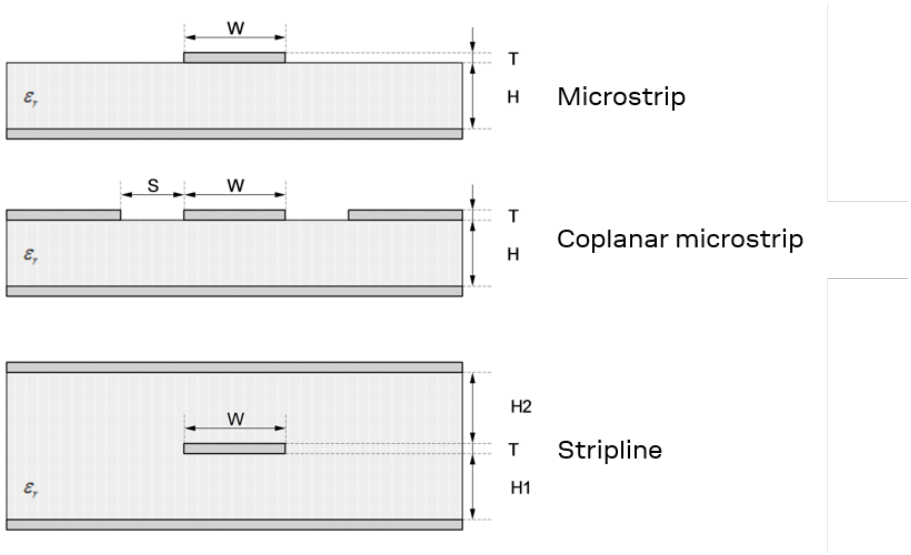

Figure 5: Transmission line trace design

Follow these recommendations to design a 50 Ω transmission line correctly:

- Trace Clearance

Ensure sufficient clearance between RF traces and surrounding conductors or ground areas on the same layer. A minimum clearance of 2× the trace width is recommended. Additionally, RF transmission lines should be guarded by adjacent ground plane areas to minimize coupling and interference.

- Impedance Control

Use layout software tools for initial characteristic impedance estimation.

  - Request final impedance values from the PCB manufacturer, who typically uses specialized simulation tools and production stack-up data.
  - Consider adding an impedance coupon on the panel edge to allow for real-world impedance measurement during fabrication.

- Use of FR-4 in RF Designs

Despite its higher dielectric losses at RF frequencies, FR-4 can be used under certain conditions:

  - Keep RF trace lengths short to minimize dielectric losses.
  - For longer traces (several centimeters), use coaxial connectors and cables to reduce signal degradation.
  - Ensure the stack-up supports thick 50 Ω traces; a minimum trace width of 200 µm is recommended for reliable impedance control.
  - Be aware that FR-4 has poor thickness stability, which can affect impedance consistency. Always consult the PCB manufacturer for tolerance specifications on controlled impedance traces.

- Routing Guidelines

  - Maintain uniform trace width and spacing to ground throughout the RF path.
  - Route RF lines using 45° angles or smooth arcs to minimize reflections and impedance discontinuities.
  - Add ground stitching vias around transmission lines to enhance shielding and reduce EMI.

- Ensure solid via connections between adjacent metal layers and the main ground plane to maintain low impedance return paths.
- Keep RF traces isolated from noise sources such as switching regulators and fast switching digital signals, and away from sensitive analog or high-impedance nodes to prevent crosstalk.

3.2.5 RF connector design

If an external antenna is required, designers should use a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 5 suggests several RF connector plugs that designers can use to connect RF coaxial cables based on the declaration of the respective manufacturers.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 5: U.FL compatible plug connector

The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Typically, the RF plug is available as a cable assembly. Different types of cable assemblies are available, and the user should select the cable assembly best suited for the application. The key characteristics of an appropriate plug include:

- RF plug type: Select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Select thicker cables – typically those with a thickness between 0.8 mm to 1.37 mm, to minimize insertion loss.
- Cable length: The standard cable length is typically 100 mm or 200 mm; custom lengths are available on request. Select shorter cables to minimize insertion loss.
- RF connector terminating the other side of the cable: for example, another U.FL (for board-to-board connection) or SMA (for panel mounting).

SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect the U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors suggests that the usage of reverse polarity connectors (RP-SMA) on Wi-Fi and Bluetooth end products make it more difficult for end users to replace the antenna with higher gain versions that exceed regulatory limits.

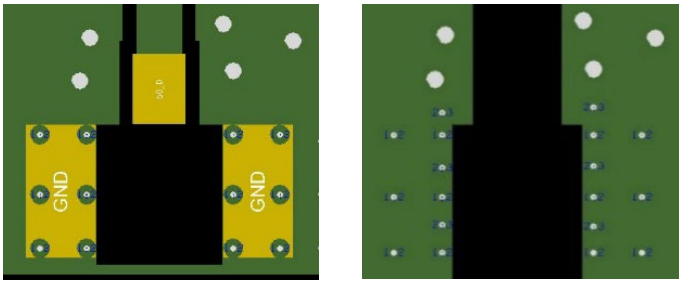

Figure 6: U.FL connector layout showing top layer (left) and inner layer 1 (right)

Strictly follow the connector manufacturer's recommended layout:

- SMA Pin-Through-Hole connectors require a void GND keep-out clearance area on all the layers around the central pin – up to annular pads of the four GND posts.
- U.FL surface mounted connectors require no conductive traces in the area below the connector between the GND land pads.

If the connector's RF pad size is wider than the microstrip, remove the GND layer beneath the RF connector to minimize the stray capacitance and keep the RF line to an impedance of 50 Ω. To reduce parasitic capacitance-to-ground for example, the active pad of the U.FL. connector must include (at the very least) a void GND keep-out clearance area on the first inner layer.

3.3 General layout guidelines

This section describes the best practice for the schematic design and circuit layout of the application.

3.3.1 Considerations for schematic design and PCB floor planning

- Low frequency signals are generally not critical to the layout and designers should focus on the higher speed buses. One exception to this general rule is when high impedance traces, such as signals driven by weak pull resistors, might be affected by crosstalk. For these and similar traces, a supplementary isolation of 4w (four times the line width) from other buses is recommended.
- Verify which interface bus requires termination and add series resistor terminations to these buses.
- Carefully consider the placement of the module with respect to antenna position and host processor.
- Verify the controlled impedance dimensions of the selected PCB stack-up. The PCB manufacturer might be able to provide test coupons.
- Verify that the power supply design and power sequence are compliant with module specifications, as described in the module's data sheet.

⚠ Take particular care not to place components close to the antenna area and follow the recommendations from the antenna manufacturer to determine the safe distance between the antenna and any other part of the system. Designers should also maximize the distance between the antenna and high-frequency buses, like DDRs and related components, or consider the use of an optional metal shield to reduce the potential interference picked up by the module antenna.

3.3.2 Component placement

- Place the module such that it provides optimum RF performance. This includes short low loss antenna connections and unobstructed antenna placement. For more information about the module placement and other antenna considerations, see also Antenna integration.
- Place bypass capacitors as close as possible to the module. Prioritize the placement of capacitors with the least capacitance so that these are closest to module pads. The supply rails must be routed through the capacitors from the power supply to the supply pad on the module.

- Do not place components close to the antenna area. Follow the recommendations of the antenna manufacturer to determine distance of the antenna in relation to other parts of the system. Designers should also maximize the distance of the antenna to High-frequency busses, like DDRs and related components. Alternatively, consider an optional metal shield to reduce interferences that might otherwise be picked up by the antenna and subsequently reduce module sensitivity.

3.3.3 Layout and manufacturing

- Avoid stubs on high-speed signals which might adversely affect signal quality. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length. Ensure that the maximum allowable length for high-speed buses is not exceeded. Longer traces generally degrade signal performance.
- For impedance matched traces, consult with your PCB manufacturer early in the project for proper stack-up definition.
- Separate the RF and digital sections of the board.
- Don't split ground layers under the module.
- Minimize the routing length. Ensure that the maximum allowable length for high-speed buses is not exceeded. Longer traces generally degrade signal performance.
- Couple all traces (including low speed or DC traces) with a reference plane (GND or power), and reference all hi-speed buses against the ground plane. If any ground reference needs to be changed, add an adequate number of GND vias in the area in which the layer is switched. This is necessary to provide a low impedance path between the two GND layers for the return current.
- Don't change the reference plane for Hi-Speed buses. If changes in the reference plane are unavoidable, add capacitors in the transition area of the reference planes. This is necessary to ensure that a low impedance return path exists through the different reference planes.
- Following the "3w rule", keep traces at a distance no less than three times that of its own width from the routing edge of the ground plane.
- For EMC purposes and the need to shield against any potential radiation, it is advisable to add GND stitching vias around the edge of the PCB. Traces on the PCB peripheral are not recommended.
- To help with the dissipation of the heat generated by the module, GND pads must have good thermal bonding to PCB ground planes.

3.4 Land pattern and solder paste stencil

The proposed layout for the land pattern and solder paste stencil is to follow the footprint dimensions of the module, which is found in the ANNA-B50 series data sheet [2]. Non-Solder Mask Defined (NSMD) pads are recommended.

The thickness of the solder paste stencil should be decided based on the entire host PCB and customer's reflow process.

3.5 ESD guidelines

Device immunity against Electrostatic Discharge (ESD) is a requirement for Electromagnetic Compatibility (EMC) conformance and use of the CE marking for products intended for sale in Europe. To bear the CE mark, all application products integrating u-blox modules must be conformance tested in accordance with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with the above directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 and the radio equipment standards ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24.

The ESD immunity test is performed at the enclosure port, defined by *ETSI EN 301 489-1* as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all-insulating and includes conductive surfaces to house the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

Any extension of the ESD immunity test to the whole device is dependent on the device classification, as defined by *ETSI EN 301 489-1*. Applicability of ESD immunity test to the related device ports or the related interconnecting cables to auxiliary equipment, depends on the device accessible interfaces and manufacturer requirements, as defined by the *ETSI EN 301 489-1*.

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in the *CENELEC EN 61000-4-2*.

☞ The terms “integral antenna”, “removable antenna”, “antenna port”, “device classification” used in the context of this guideline are defined in *ETSI EN 301 489-1*. The terms “contact discharge” and “air discharge” are defined in *CENELEC EN 61000 4-2*.

ANNA-B50 is manufactured with consideration to the specific standards for minimizing the occurrence of ESD events. The highly automated process complies with the *IEC61340-5-1 (STM5.2-1999 Class M1 devices*) standard, and designers should implement proper measures to protect devices from ESD events on any pin that might be exposed to the end user.

Compliance with standard protection level specified in *the EN61000-4-2* is achieved by including ESD protection as close to any areas accessible to the end user.

3.6 Design-in checklists

3.6.1 Schematic checklist

☐ All module pins are properly numbered and designated in the schematic (including thermal pins).
☐ Power supply design complies with the specification.
☐ Adequate bypassing is included in front of each power pin.
☐ Each signal group is consistent with its own power rail supply or proper signal translation has been provided.
☐ Unused pins are properly terminated.
☐ A pi-filter is provided in front of the antenna for final matching.
☐ Additional RF co-location filters have been considered in the design.

3.6.2 Layout checklist

☐ PCB stack-up and controlled impedance traces follow the recommendations given by the PCB manufacturer.
☐ All pins are properly connected, and the footprint follow u-blox pin design recommendations.
☐ Proper clearance is provided between the RF and digital sections of the design.
☐ Proper isolation is provided between antennas (RF co-location, diversity, or multi-antenna design).
☐ Bypass capacitors have been placed close to the module.
☐ Controlled impedance traces are properly implemented in the layout (both RF and digital) and the recommendations provided by the PCB manufacturer have been followed.
☐ 50 Ω RF traces and connectors follow the rules described in Antenna integration.
☐ Antenna design is reviewed by the antenna manufacturer.
☐ Proper grounding is provided to the module for the low impedance return path.
☐ Reference plane skipping is minimized for high frequency busses.
☐ All traces and planes are routed inside the area defined by the main ground plane.
☐ u-blox has reviewed and approved the PCB[2].

[2] Applicable only for end-products based on u-blox reference designs

4 Open CPU software

ANNA-B50 series modules are delivered without any software application. It needs to be loaded with an application to be functional. Nordic Semiconductor provides the nRF Connect SDK that can be used for development of applications for the ANNA-B50 module.

4.1 nRF Connect SDK

The nRF Connect SDK [24] is a simple-to-use Software Development Kit (SDK), which is based on the open-source Zephyr real-time operating system with Visual Studio Code used as IDE.

☞ At the time of writing the Zephyr board configuration for the u-blox EVK (`ubx_evkannab5`) is not yet published. For early adopters it is advised to modify the board definition for the Nordic Semiconductor Product Development Kit `nrf54l15dk` to fit the ANNA-B50 and the custom board developed.

4.1.1 Installation

To get started with nRF Connect SDK:

1. Install the Toolchain Manager from the nRF Connect for Desktop application [27].
2. From the Toolchain Manager, install the selected version of the nRF Connect SDK. For more information, see the nRF Connect SDK documentation [24].

4.1.2 Custom board support configuration

A board configuration that defines the module interfaces needs to be defined to use the nRF Connect SDK.

A board definition for the u-blox EVB (`ubx_evkannab5`) can be found in the u-blox open CPU GitHub repository [20]. This definition can be used as basis for any board based on ANNA-B50.

4.1.3 Support – Nordic DevZone

For support on questions related to the development of software using the nRF Connect SDK, refer to the Nordic Semiconductor DevZone forum at devzone.nordicsemi.com where both public and private questions can be posted.

4.2 Load capacitance for high-frequency oscillator

ANNA-B50 has an oscillator mounted internally in the module to provide the SoC with a high frequency clock signal. For this to work properly the load capacitors internally in the SoC must be configured with the right values. In the Zephyr OS configuration this can be done using a device tree configuration, as follows:

```
&hfxo {
    load-capacitors = "internal";
    load-capacitance-femtofarad = <14000>;
};
```

☞ This device tree node needs to be part of the board configuration for any board utilizing the ANNA-B50 modules.

See also the `ubx_evkannab5` example board definition in the u-blox open CPU GitHub repository [20].

4.3 32 kHz crystal

To implement high tolerance 32.768 clock a crystal shall be connected to ANNA-B50 modules XL1 and XL2 pins. ANNA-B5 includes internal crystal tuning capacitors that must be set for each design to align with crystal datasheet and parasitic capacitance from PCB layout. To configure the software correctly for your configuration, follow the steps in the RC oscillator configuration application note *RC oscillator configuration for nRF5 open CPU modules* [25].

☞ ANNA-B50 EVKs are delivered with an external 32.768 kHz frequency crystal mounted.

4.4 Setting output power

Output power for Bluetooth transmissions can be configured from within the nRF Connect SDK, using the following settings:

- Statically by setting `CONFIG_BT_CTLR_TX_PWR_PLUS_4=y` in the `prj.conf` file. Replace `PLUS_4` with your desired output power.
- Dynamically by using the HCI interface. For an example of how to set TX power using the HCI interface, see the Zephyr Bluetooth sample HCI Power Control.

For more information about antenna gain and regulatory compliance, see Antenna integration and Regulatory compliance.

4.5 Flashing Open CPU software

To flash ANNA-B50 modules over the Serial Wire Debug (SWD) interface an external debugger must be connected to the SWD interface of the module. Third-party tools, like J-Link Commander, J-Flash, nRF Command Line Utilities or nRF Connect Programmer, are used to flash the module.

The nRF54L15 chip in the ANNA-B50 module has the debug access port protection functionality APPROTECT enabled by default, which means that for empty modules a recovery operation (*nrfjprog –recover* or *nrfutil device recover*) is needed to be able to access the debug functionality of the module. This erases all user available non-volatile memory and disables the readback protection mechanism.

For more information about the APPROTECT and related security functionality, see the *nRF54L15, nRF54L10 and nRF54L05 data sheet* [29].

☞ SEGGER J-Link BASE external debugger works with ANNA-B50 modules.

☞ EVK-ANNA-B50x incorporates an onboard debugger, which means that it can be flashed without an external debugger.

4.6 Radio test software

This chapter describes the various test procedures for ANNA-B50, including:

- General radio testing
- Bluetooth specific testing using Direct Test Mode (DTM)
- 802.15.4 testing

These test methods involve the use of sample applications [22][21][22] provided by the ANNA-B50 chipset supplier, Nordic Semiconductor, in their nRF Connect SDK [24].

The ANNA-B50 module undergoes extensive certification and approval testing, but in some instances customers may find some extra testing necessary. Additional tests are typically necessary when:

- adding a country where the ANNA-B50 module is not yet certified
- adding a new antenna not covered by u-blox certification

4.6.1 Using software samples

The samples used to perform the different types of radio testing must be compiled for the board they are going to run on. For this purpose, u-blox provides board files that are adapted for the u-blox evaluation board (EVB). As a starting point for your testing, use the board files archived in the u-blox open CPU GitHub repository [20].

4.6.1.1 Considerations

When testing with a u-blox evaluation board be aware that it includes a mounted 32.768 kHz crystal oscillator. If your target board doesn't have this oscillator fitted, you must recompile the application with the changed settings when testing on your target board. For more information about this, see the application note *RC oscillator configuration for nRF5 open CPU modules* [25].

☞ The ANNA-B50 module and EVK-ANNA-B50 evaluation board have different pin mappings than the evaluation boards supplied by Nordic Semiconductor. Ensure that the software you use is compiled with the correct pin mapping. For more information, see the u-blox open CPU GitHub repository [20].

4.6.1.2 Compiling samples

Compile samples using nRF Connect SDK using the correct board definition to get the UART pins correctly set up. A board definition for the u-blox EVB (`ubx_evkannab5`), which can be used as basis for the definition of any board based on ANNA-B50, can be found in the u-blox Open CPU GitHub repository [20].

4.6.2 Radio test sample

The Radio test sample [22] allows the radio to be configured for transmission and reception using either modulated or constant carriers. For example, this test sample can be used to configure the radio to comply with different frequency bands (spurious emissions) and to adjust the module's output power.

4.6.2.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the ANNA-B50 module requires compiling the software with the correct pin definitions for your board.

4.6.2.2 Running the sample

This software does not use standard signaling, so regular devices like mobile phones cannot detect its signals. Instead, use another development kit running the Radio Test software as a peer device, or test with an RSSI viewer.

4.6.3 Direct Test Mode sample

The Direct Test Mode sample [21] allows the radio to be configured for transmission and reception of Bluetooth messages using different parameters. This software can be used with protocol testers that are using the DTM UART test interface as described in the *Bluetooth Core Specification* [26], *volume 6, part F*.

4.6.3.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the ANNA-B50 module requires compiling the software with the correct pin definitions for your board.

4.6.3.2 Running the sample

This software does not use standard signaling, so regular devices like mobile phones cannot detect the transmitted signals. Instead, use another development kit running the DTM Test software as a peer device. For testing it is convenient to drive the application using the Direct Test Mode application in *nRF Connect for desktop* [27], which provides a convenient GUI for controlling the device running the DTM sample.

4.6.4 802.15.4 PHY test tool

The 802.15.4 PHY test tool [23] performs *IEEE 802.15.4 RF Performance and PHY Certification tests* and provides information about the general performance evaluation of the integrated 802.15.4 radio.

4.6.4.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the ANNA-B50 module requires compiling the software with the correct pin definitions for your board.

4.6.4.2 Running the test tool

This test requires two development kits running the 802.15.4 test tool. For more information, see the documentation included with the 802.15.4 PHY test tool [23].

5 Handling and soldering

No natural rubbers, hygroscopic materials or materials containing asbestos are employed.

⚠ ANNA-B50 series modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product.

5.1 ESD handling precautions

As the risk of electrostatic discharge in the RF transceivers and patch antennas of the module is of particular concern, standard ESD safety practices are prerequisite. See also Figure 7.

Consider also:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna patch, connect the device to ground.
- When handling the Antenna pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the Antenna pin on the transceiver, be sure to use an ESD-safe soldering iron (tip).

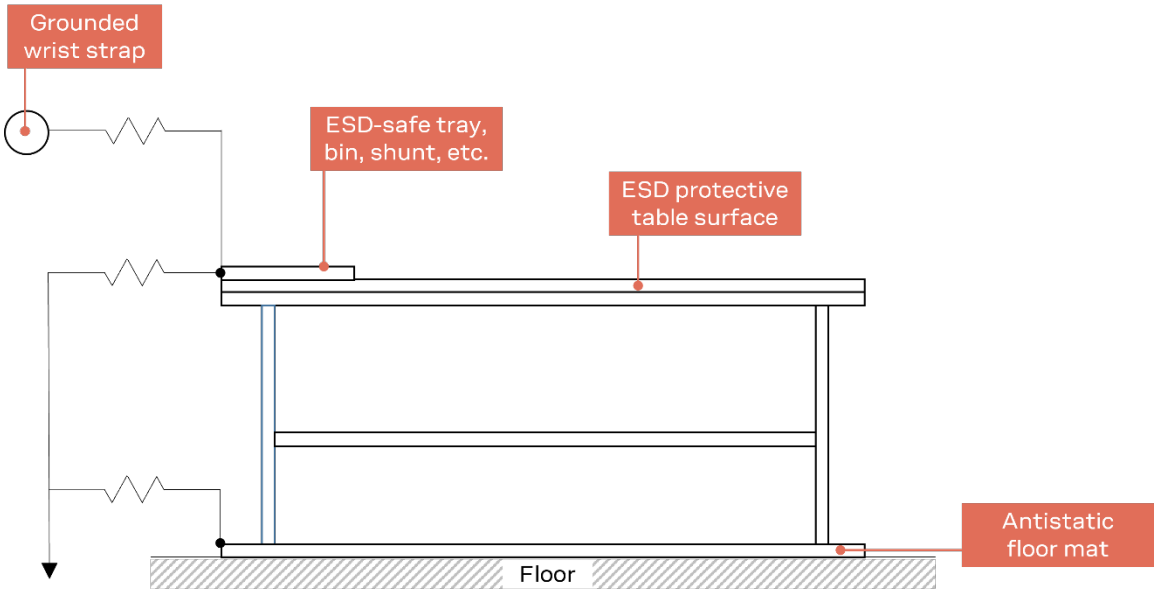

Figure 7: Standard workstation setup for safe handling of ESD-sensitive devices

5.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning, refer to the respective ANNA-B50 series data sheet [2] and Product packaging reference guide [1].

5.3 Reflow soldering process

ANNA-B50 series modules are surface mounted devices supplied in a Land Grid Array (LGA) package with gold-plated solder lands. The modules are manufactured in a lead-free process with lead-free soldering paste.

The thickness of solder resist between the host PCB top side and the bottom side of the module must be considered for the soldering process.

ANNA-B50 modules are compatible with the industrial reflow profile for common SAC type RoHS solders. No-clean soldering paste is strongly recommended.

The reflow profile is dependent on the thermal mass over the entire area of the fully populated host PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile that is used must be trimmed for each case depending on the specific soldering process and PCB layout.

⚠ The target values shown in Table 6 are only general guidelines for a Pb-free process. For further information, see also the JEDEC J-STD-020C standard [7].

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from +25 °C)	s	150
	t_S (Pre-heat)	s	60 to 120
Peak	T_L	°C	217
	t_L (time above T_L)	s	40 to 60
	T_P (absolute max)	°C	245
Cooling	Ramp-down from T_L	K/s	4
	Allowed soldering cycles	-	2

Table 6: Recommended reflow profile

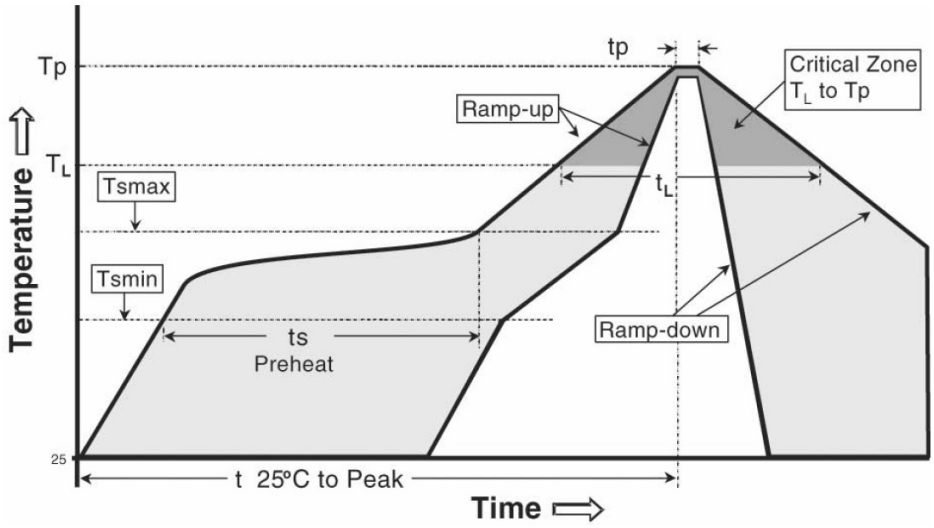

Figure 8: Reflow profile

☞ Lower value of T_P and slower ramp down rate (2–3 °C/sec) is preferred.

5.3.1 Repeated reflow soldering

For application boards with components on both sides, a two-reflow process may be required. In such cases, ANNA-B50 can be mounted in both reflow cycles. To reduce the risk of detachment due to its relatively higher weight compared to other components on the board, it is advisable to place the module on the side of the board that undergoes the final cycle. This reduces the risk of detachment due to its relatively higher weight compared to other components.

Mounting the module in an upside-down position (with the module on the underside of the board during reflow) is not recommended, as this increases the likelihood of detachment.

⚠ u-blox does not provide warranty coverage for damages to ANNA-B50 modules caused by performing more than two total reflow soldering processes (one for mounting the module and one for mounting other components).

5.3.2 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular.

For best results use a "no clean" soldering paste and circumvent the need for a cleaning stage after the soldering process.

5.3.3 Other notes

- ANNA-B50 may be used for two times reflow.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave-soldering process is allowed for boards populated with the modules. Miniature Wave Selective Solder processes are preferred over traditional wave soldering processes.
- Hand-soldering is not recommended.
- Rework is not recommended.
- Conformal coating or potting will affect the RF performance of the module and possibly reliability. It is recommended to conduct RF performance and reliability testing if applying coating or potting.
- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done so at the customer's own risk and will void the module warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding, etc.) may damage the module. The use of ultrasonic processes during the integration of the module into an end product will void the warranty.

6 Regulatory compliance

⚠ Approvals pending.

6.1 Pre-approved antennas

⚠ Approvals pending.

This section describes the external antennas that are pre-approved for use together with ANNA-B50 series modules. The currently limited list of antennas is to be extended once the scope of the module certification is decided.

☞ Note that not all antennas and accessories are approved for use in all markets/regions.

6.1.1 Single band antennas

☞ The following antennas are yet to be decided and may be changed without prior notice.

ANNA-B505	
Applicable module	ANNA-B505
Gain	TBD dBi
Impedance	N/A
Size	Integrated into module
Type	Chip antenna
Comment	
Approval	FCC*, ISED*, RED*, UKCA*, MIC*, KCC*, ANATEL*, RCM*, NCC*, and ICASA*

*Approvals pending

7 Technology standards compliance

⚠ Approvals pending.

7.1 Bluetooth SIG

The ANNA-B50 module series is qualified as a tested component against Bluetooth Core 6.0.

Product type	QDID	Listing date
ANNA-B50 RF-PHY Component (Tested)	TBD	TBD

Table 7: ANNA-B50 series Bluetooth qualified design ID

The Bluetooth SIG requires the following:

- All manufacturers of products that use Bluetooth technology are required to become members of the Bluetooth SIG.
- All end-products or end-product family that utilize Bluetooth technology must be declared with the Bluetooth SIG.

For details regarding the declaration process, see the Bluetooth qualification process for nRF5 modules, application note [28].

7.2 Matter

End-products that incorporate the Matter protocol are required to join the Connectivity Standards Alliance and certify the end-product.

7.3 Thread

End-products that incorporate the Thread protocol are required to join the Thread Group and certify the end-product.

7.4 Zigbee

End-products that incorporate the Zigbee protocol are required to join the Connectivity Standards Alliance and certify the end-product.

7.5 USB

End-products that incorporate USB technology are required to join the USB Implementors Forum (USB-IF) and certify the end-product with the USB.

8 Product testing

8.1 u-blox in-line production test

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 9 shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.

Figure 9: Automatic test equipment for module test

8.2 OEM manufacturer production test

As all u-blox products undergo thorough in-series production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a "Golden Device".

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing. Special manufacturing firmware can also be used to perform more advanced RF performance tests.

8.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test compares the signal quality of the Device under Test (DUT) with that of "Golden Device" in a location with a known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth LE device and checking that the signal level (Received Signal Strength Indicator (RSSI) is acceptable.

☞ Tests of this kind may be useful as a "go/no go" test but are not appropriate for RF performance measurements.

Go/No go tests are suitable for checking communication between the host controller and the power supply. The tests can also confirm that all components on the DUT are well soldered.

A basic RF functional test of the device that includes the antenna can be performed with standard Bluetooth LE devices configured as remote stations. In this scenario, the device containing ANNA-B50 and the antennas should be arranged in a fixed position inside an RF shield box. The shielding prevents interference from other possible radio devices to ensure stable test results.

Appendix

A Glossary

Abbreviation	Definition
ABS	Acrylonitrile butadiene styrene
ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
LE	(Bluetooth) Low Energy
CLI	Command Line Interface
CTS	Clear To Send
DCE	Data Circuit-terminating Equipment / Data Communication Equipment
DCX	Data/Command Signal
DDR	Dual-Data Rate
DFU	Device Firmware Update
DTE	Data Terminal Equipment
DTM	Direct Test Mode
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
ESD	ElectroStatic Discharge
EVB	Evaluation Board
EVK	Evaluation Kit
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
IDE	Integrated Development Environment
IEEE	Institute of Electrical and Electronics Engineers
LDO	Low Drop Out
LED	Light-Emitting Diode
LFCLK	Low Frequency, Real Time Clock
LFXO	Low Frequency, Crystal Oscillator
MAC	Media Access Control
MISO	Main Input, Sub Output
MOSI	Main Output, Sub Input
MSL	Moisture Sensitivity Level
NBU	Narrow Band Unit
NFC	Near Field Communication
NSMD	Non-Solder Mask Defined
NVM	Non-Volatile Memory
PCB	Printed Circuit Board
PIFA	Planar Inverted-F Antenna
PC	Polycarbonate
QDEC	Quadrature Decoder
QSPI	Quad Serial Peripheral Interface

Abbreviation	Definition
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indicator
RTC	Real Time Clock
RTS	Request to Send
RXD	Receive Data
SCL	Signal Clock
SDL	Specification and Description Language
SMA	SubMiniature version A
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
Thread	Networking protocol for Internet of Things (IoT) "smart" home automation devices to communicate on a local wireless mesh network
THT	Through-Hole Technology
TWI	Two-Wire Interface
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Configuration Registers
USB	Universal Serial Bus
VCC	IC power-supply pin
VSWR	Voltage Standing Wave Ratio
Zigbee	Open standard protocol, full-stack solution for most large smart home ecosystem providers

Table 8: Explanation of the abbreviations and terms used

B Antenna reference designs

This information is pending.

Related documents

[1] Packaging information reference, UBX-20027119
[2] ANNA-B50 series data sheet, UBXDOC-465451970-3932
[3] ANNA-B50 series product summary, UBXDOC-465451970-3862
[4] ANNA-B56 series product summary, UBXDOC-465451970-3918
[5] Nordic nRF54L15 data sheet, https://docs.nordicsemi.com/bundle/ps_nrf54L15/page/keyfeatures_html5.html
[6] Nordic nRF54L15 Reference Manual,
[7] EVK-ANNA-B50 user guide, UBXDOC-465451970-4643
[8] JEDEC J-STD-020C - Moisture/Reflow Sensitivity Classification for Non Hermetic Solid State Surface Mount Devices
[9] IEC EN 61000-4-2 - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[10] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[11] IEC61340-5-1 - Protection of electronic devices from electrostatic phenomena – General requirements
[12] ETSI: Audio/video, information, and communication technology equipment - Part 1: Safety requirements, IEC 62368-1:2018
[13] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
[14] ANNA-B5 EU Declaration of conformity (EU DoC),
[15] ANNA-B5 UKCA Declaration of conformity (UKCA DoC),
[16] Tag-Connect pad connector - http://www.tag-connect.com/TC2030-CTX
[17] Guidance on software or network configuration of Non-SDR devices, OET KDB 594280 D01
[18] Software security requirements for U-NII devices, OET KDB 594280 D02
[19] Guidance for modular transmitter instruction manuals and TCB certification application reviews, KDB 996369 D03
[20] u-blox short range open CPU repository, https://github.com/u-blox/u-blox-sho-OpenCPU
[21] Documentation for Direct Test Mode sample, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/bluetooth/direct_test_mode
[22] Documentation for Radio test sample, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/peripheral/radio_test
[23] Documentation for 802.15.4 PHY test tool, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/peripheral/802154_phy_test
[24] nRF Connect SDK, https://www.nordicsemi.com/Products/Development-software/nRF-Connect-SDK
[25] RC oscillator configuration for nRF5 open CPU modules, UBX-20009242
[26] Bluetooth Core Specification, https://www.bluetooth.com/specifications/specs
[27] nRF Connect for Desktop, https://www.nordicsemi.com/Products/Development-tools/nRF-Connect-for-Desktop
[28] Bluetooth® qualification process – nRF Connect SDK - Application note, UBX-21040374
[29] nRF54L15 documentation, https://docs.nordicsemi.com/category/nRF54L15-category
[30] nRF54L Pin Planner https://pinplanner.app/

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	1-Sep-2025	lber, mape	Initial version
R02	1-Apr-2026	mape, lber	Updates for document status “Advance information”

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