AN90001

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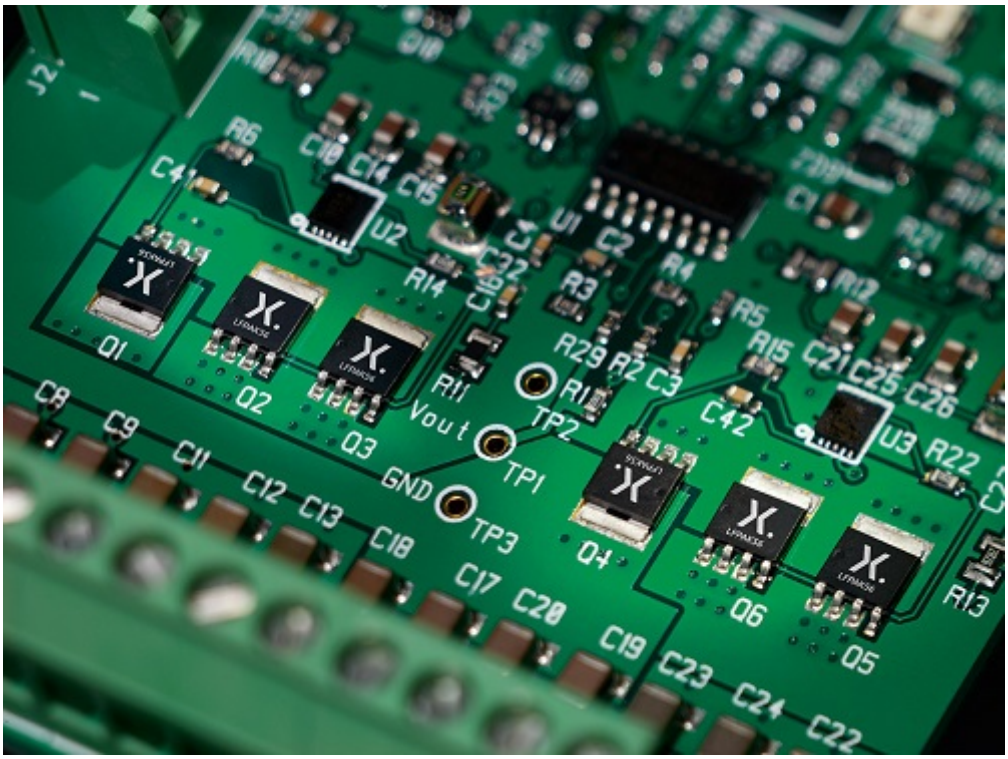
application note

Designing in MOSFETs for safe and reliable gate-drive operation



Abstract: The MOSFET gate-source threshold voltage (VGS-th) and maximum gate-source voltage (VGS-max) are key parameters that are critical to the reliable operation of MOSFETs. The threshold voltage represents the voltage at which the MOSFET starts to turn on, whilst the maximum gate-source voltage is the maximum gate-source voltage that the MOSFET can withstand safely. VGS-max ratings vary between suppliers and between MOSFETs, which can make it difficult to choose appropriate MOSFETs for the application. This application note aims to provide the designer with enough knowledge to appreciate these differences and to select an appropriate MOSFET. We also present a new methodology demonstrating where higher VGS-max ratings voltages may be applied for Nexperia's automotive grade MOSFETs.

Keywords: Silicon MOSFETs, gate drive design, VGS rating, gate oxide, gate oxide lifetime/reliability, gate-source threshold voltage rating, Time-Dependent Dielectric Breakdown (TDDB)

nexperia

1. Introduction

The MOSFET can be considered as a voltage-controlled switch. Applying a voltage (V_{GS}) across the gate and source terminals enhances the MOSFET allowing current to flow through the MOSFET-channel between the drain and source terminals. $V_{GS(th)}$ is defined as the V_{GS} for a pre-defined drain current, commonly 1 mA. Increasing the V_{GS} further causes the MOSFET to become fully enhanced. This allows more current to flow for a given drain-source voltage. A fully enhanced MOSFET will also have achieved close to its rated on state resistance $R_{DS(on)}$. Increasing the voltage beyond the full enhancement level will only result in a small reduction in $R_{DS(on)}$. Increasing the V_{GS} further to a level beyond the $V_{GS\text{-}max}$ will have direct implications for the MOSFET's reliability. This could lead to destruction of the MOSFET. The design engineer can review the MOSFET data sheet to help ensure that the MOSFET's reliability is not impaired and that it operates as expected. The data sheet gives limits and guidelines, but often the design engineer needs more detail to select a MOSFET.

This application note aims to bridge this gap. It will provide an overview of what is currently included in the data sheet concerning V_{GS} ratings and it aims to answers questions that may arise when designing in power MOSFETs.

In addition a brief introduction to the physics behind the V_{GS} ratings and the role of the gate-oxide is included. This will provide an appreciation of the reasoning behind the ratings and give confidence in the methodology employed by Nexperia to test, to qualify and to rate the MOSFET's gate-oxide capability.

An analysis of common Power MOSFET applications is also presented. This will highlight the demands imposed on the MOSFET gate-oxide by the application. Different applications have been analysed to develop a mission profile for the V_{GS}. This states what levels of V_{GS} the MOSFET will be exposed to, for how long and at what temperature. This information can then be used to select the correct MOSFET for the application, thus ensuring optimum and reliable operation.

2. Data sheet V_{GS} ratings

In an Nexperia data sheet there are typically two main parameters concerning the gate-source voltages. The first being the V_{GS} threshold value or $V_{GS(th)}$. The second is the V_{GS} rating, which in this application note will be called $V_{GS\text{-}max}$.

Some MOSFET data sheets include a value for the plateau (Miller) voltage. This is the V_{GS} voltage during switching events. Its level is poorly defined as it depends on several interdependent electrical and environmental factors. It is not important for MOSFET selection or circuit design and will not be further discussed in this application note.

2.1. V_{GS} threshold voltage - $V_{GS(th)}$

Figure 1 shows an example of data sheet $V_{GS(th)}$ values; it highlights the voltage required across the gate and source terminals to start to turn the MOSFET on. The conditions for which the $V_{GS(th)}$ is defined are specified here as the V_{GS} necessary for 1 mA of current to flow through the drain terminal. The Nexperia data sheet gives the $V_{GS(th)}$ for a range of temperatures. It also provides minimum and maximum values to account for process variation.

The $V_{GS(th)}$ is the start of MOSFET enhancement, an increase in V_{GS} is required to enhance the MOSFET further. Depending on whether a device is logic-level or standard-level, a MOSFET can be considered fully-enhanced (or fully on) when the V_{GS} is 5 V or 10 V respectively. By this point the MOSFET has achieved its rated $R_{DS(ON)}$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		2.4	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 9		-	-	4.5	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 9		1	-	-	V

Fig. 1. V_{GS} threshold values for an Nexperia automotive grade standard level device

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 9		-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 9		0.5	-	-	V

Fig. 2. V_{GS} threshold values for an Nexperia automotive grade logic level device

Other differences between standard-level and logic-level devices can be observed in their threshold-voltage values (figure 1 and 2). It is important to consider these values when selecting a MOSFET for an application. Two questions need to be answered to choose an appropriate MOSFET.

1. Can the gate-driver turn the MOSFET (fully) on?
2. Can the gate-driver turn the MOSFET (fully) off?

To answer these questions, it is necessary to take the worst case conditions in each circumstance. In order to assess question 1 we need to know what is the highest value of $V_{GS(th)}$ that the device may have. From Figures 1 and 2, we can see this occurs at the lower temperature limits. For a standard level device this can be as high as 4.5 V. If the gate-driver output is only 5 V, then a standard level device may not be suitable. This is because the MOSFET is only beginning to turn on and therefore may not operate correctly in the application. A logic level MOSFET with a maximum $V_{GS(th)}$ of ≤ 2.45 V would be more suitable.

It is important to note that $V_{GS(th)}$ has a Negative Temperature Coefficient (NTC): as the junction temperature increases, the V_{GS} for a given I_D decreases. If channel current flows because the V_{GS} is not low enough to drive the MOSFET fully OFF, I_D will increase as die temperature rises. This thermal runaway effect can ultimately cause MOSFET destruction.

Conversely, the designer must consider the upper temperature limit for turning the MOSFET off. At 175 °C a logic level device may conduct channel current at a V_{GS} ≥ 0.5 V. The gate-driver may have a minimum output voltage of 0.6 V. This is not low enough to ensure that a logic level MOSFET is turned fully off. At V_{GS} = 0.6 V channel current could still flow. In this situation it is better to select a standard level device.

2.2. The maximum V_{GS} ratings - $V_{GS\text{-}max}$

$V_{GS\text{-}max}$ is the absolute maximum gate-source voltage that can be applied to the device. These values illustrated in Figure 3 conform to the International Electrotechnical Commission's IEC60134 document -"Rating systems for electronic tubes and valves and analogous semiconductor devices". Referencing paragraph 4 of IEC60134 titled "Absolute maximum rating system" it states [1]:

"*Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions. These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.*"

This defines the allowable conditions and highlights the responsibility of the designer to ensure that the absolute maximum value is never exceeded. Reliability testing may be done at different voltage and temperature test conditions. It does not explicitly place any obligations on the manufacturer in terms of long term reliability.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage		[1]	-20	20	V

[1] Refer to application note AN90001 for further information.

Fig. 3. Maximum V_{GS} rating for a Nexperia automotive grade standard and logic level device

3. Life testing

For automotive MOSFETs, AEC-Q101 qualification is required. AEC-Q101 is a list of endurance tests the MOSFET must pass. Each test takes a sample of MOSFETs and places them under various electrical stresses and temperatures. The sample size is a minimum of 77 MOSFETs; each endurance test is repeated 3 times on a different sample of 77 MOSFETs to represent a different process batch. Surviving the endurance tests grants the tested product type Q101 accreditation, allowing the MOSFET to be used in automotive applications [2]. This can be found on all Nexperia automotive qualifed MOSFET data sheets (Figure 4).

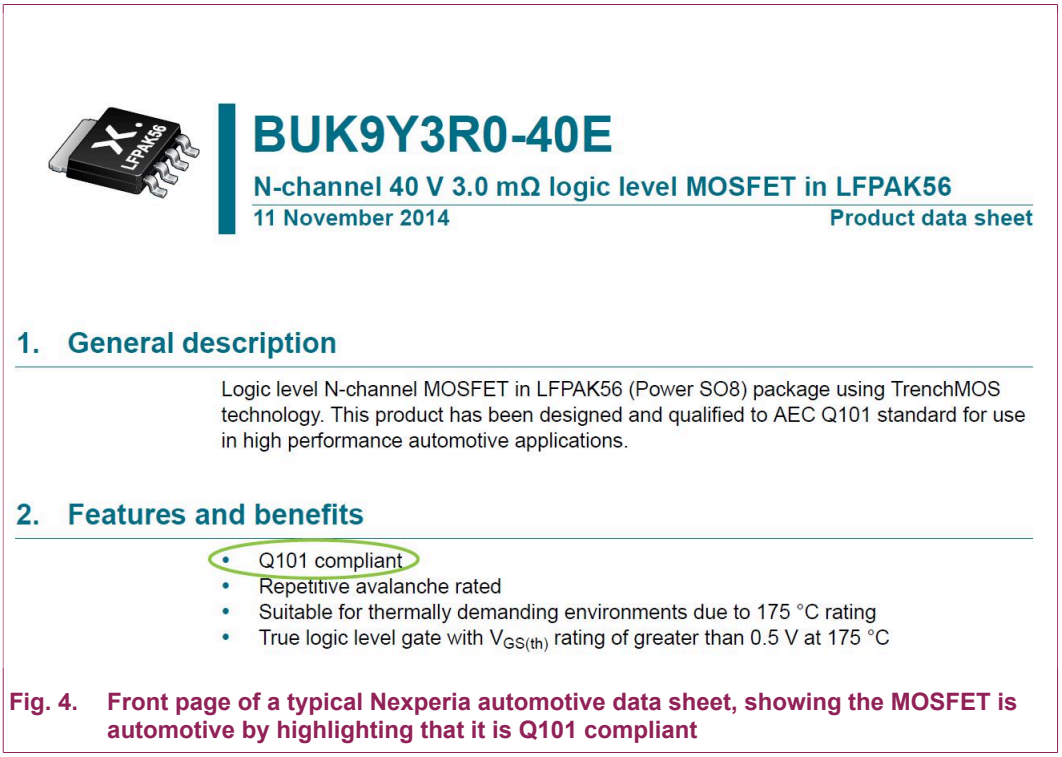


Fig. 4. Front page of a typical Nexperia automotive data sheet, showing the MOSFET is automotive by highlighting that it is Q101 compliant

To qualify the $V_{GS\text{-}max}$ ratings for Q101 the devices undergo a specified life-test procedure. The devices are placed in a chamber at the maximum rated temperature (T_{jmax}) with gate biased at 100% of the maximum voltage rating referenced in the respective qualification report for 1000 hours. These tests are performed by Nexperia to ensure that the data sheet ratings of $V_{GS\text{-}max}$ are within specification.

However, life-testing alone is inherently incapable of determining the actual capability of a MOSFET in terms of expected failed parts per million (ppm). In order to satisfy AEC-Q101 criteria no sample devices during the Q101 bias tests should fail. It is possible to extrapolate a failure rate from such data, but the maximum confidence it can provide is in the order of 11000 ppm (based on zero fails in a population of 240 devices under test and using a confidence interval of 95%). With this level of confidence it is not trivial to determine what to specify as the maximum voltage rating. Especially when in addition, Nexeria's own requirements target a sub 1 ppm defectivity level.

To achieve sub-ppm levels Nexperia has developed its own additional testing methodology. Using this, Nexperia can confidently rate the devices to satisfy the AEC-Q101 criteria, while also achieving sub 1 ppm defectivity rates (3). In order to understand this methodology an explanation of the role of a MOSFET's gate-oxide is required and is detailed below.

4. The Gate-oxide

The methodology to determine and qualify the maximum V_{GS} rating of a device is based upon characterisation of the gate-oxide. This is the layer of oxide that insulates the gate polysilicon from the source of the MOSFET and is critical to its operation. Figure 5 shows the location of the gate-oxide in the MOSFET.

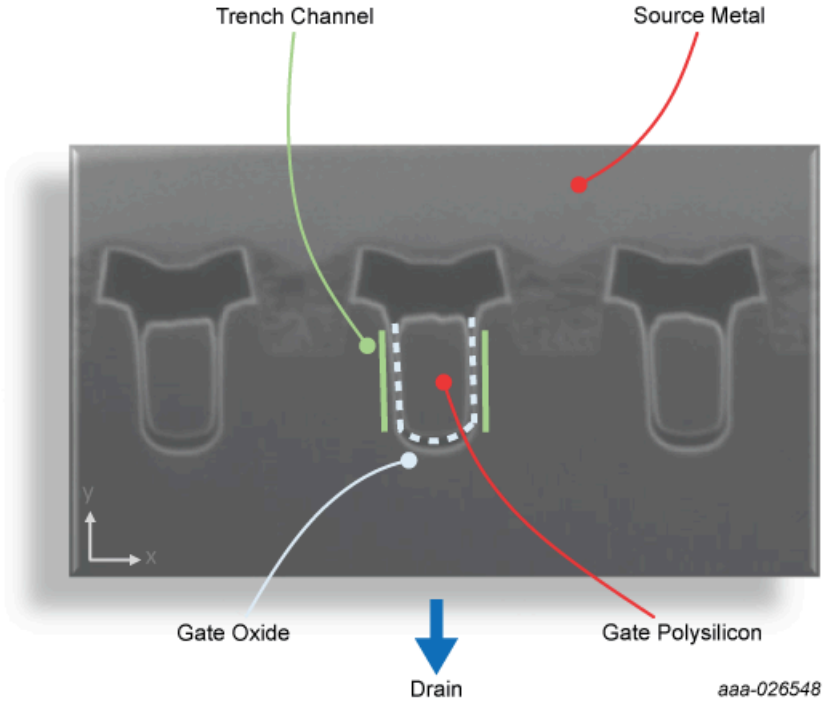


Fig. 5. Cross-section of a power MOSFET at approximately 25,000 magnification showing where the MOSFET channel forms and the location of the gate-oxide. The gate-oxide is present both sides of the trench and a channel forms next to both oxides. Current flows vertically from Drain to Source through the MOSFET channel.

When designing power MOSFETs, there are two conflicting constraints with respect to the gate-oxide thickness. Achieving a low $R_{DS(on)}$ at a low applied level of V_{GS} requires a thin gate-oxide, conversely withstanding high maximum V_{GS} requires a thick gate-oxide. In most cases, both requirements can be met and gate bias life testing can be performed at 100 % of the absolute maximum rating. However, there are some instances where this is not possible. Logic level devices are designed to provide a guaranteed $R_{DS(on)}$ at V_{GS} = 5 V. This implies a need for a gate-oxide that is thinner than for a standard level device. Consequently a logic-level gate-oxide is not capable of achieving the same maximum $V_{GS\text{-}max}$ rating as a standard-level gate-oxide. For Nexperia's automotive MOSFETs, this is typically 10 V logic-level and 20 V for standard-level devices at the maximum rated temperature, typically 175 °C.

However, caution should be exercised when comparing other manufacturers' data sheets. The $V_{GS\text{-}max}$ rating is not always given at the maximum rated temperature; instead it is often given for 25 °C. The rating given for a temperature of 25 °C may be higher than one given for 175 °C. This will make that MOSFET appear more capable on first review. Because MOSFET gate-oxide reliability decreases with increasing temperature, some older Nexperia data sheets show the capability of the MOSFET at maximum rated temperature. However more recent data sheets show the maximum capability at 25 °C to align with data sheets from other MOSFET vendors.

Exceeding the $V_{GS\text{-}max}$ rating for the gate-oxide does not mean the device will immediately fail in the application. Applying a V_{GS} to a MOSFET will develop an electric field across the internal gate-oxide (E_{OX}). The oxide electric field strength is a function of oxide thickness (T_{OX}) and V_{GS}.

$$E_{OX} = V_{GS} / T_{OX}$$

If the oxide electric field strength reaches a sufficiently high level, the gate-oxide insulation will break down and will be destroyed. However, for electric field strengths below this critical value the gate-oxide may degrade over time and ultimately fail. The rate at which this occurs depends on both the operating-temperature and the strength of the electric field within the gate-oxide. Expected oxide life-time decreases with increases in either temperature or oxide electric-field stress.

Gate-oxides need to be rated to survive for operating periods of not less than 10 years. Testing for 10 years to assess the reliability of the gate-oxide is not practical. Nexperia performs life tests under accelerated conditions to achieve quicker test results. For assessing the gate-oxide, Nexperia places a group of MOSFETs with known gate-oxide thickness under high temperatures and high oxide field strength. The MOSFETs will therefore degrade much quicker than can be expected in the application. The MOSFETs are monitored until the point of failure, which is observed as a low impedance measurement between the gate and source terminals. This is termed Time Dependant Dielectric Breakdown (TDDB).

Nexperia uses the test data from TDDB to correlate to other operating-temperatures and oxide field-strengths to determine the capability of the oxide in actual application operating conditions. This is applicable to MOSFETs with different gate-oxide thicknesses because the testing characterises oxide field-strength, not V_{GS}.

A gate-oxide production process aims to create a gate-oxide of consistent thickness throughout manufacture. However, in any real fabrication process variation will occur. This means the V_{GS} rating needs to be applicable to the MOSFET with the thinnest gate-oxide that leaves the factory. Production screens are in place that set a lower limit, which corresponds to the MOSFET with the thinnest gate-oxide. Using this value of gate-oxide thickness and the characterisation data from the accelerated TDDB tests, this MOSFET can now have its oxide rated for $V_{GS\text{-}max}$ and temperature for a given expected operating life.

For automotive MOSFET the operating requirement is outlined within AEC Q-101; 1000 hours at $V_{GS\text{-}max}$ and maximum temperature. Taking this profile into account, and knowing the thinnest oxide that can be supplied, Nexperia can confidently place $V_{GS\text{-}max}$ ratings in the data sheet.

Again, for further detail on the mechanics of gate-oxide wear out and Nexperia's methodology towards rating its gate-oxides please refer to [3].

5. Alternative operating profiles

The mission or operating-profile of a MOSFET in an actual application is rarely at the data sheet maximum temperature and at the maximum V_{GS} for 1000 hours as dictated by AEC-Q101. This combination is formulated as a compromise to allow realistic life-testing times that would protect automotive applications. The ultimate rating of a MOSFET $V_{GS\text{-}max}$ that meets AEC-Q101 may not meet the application requirements. For example the application may require 12 V V_{GS} but this exceeds the MOSFET of choice's 10 V rating, at first pass this MOSFET cannot be used in the application. However, if the operating profile of the application is outlined with greater detail it may be that the 12 V rating is required for temperatures less than 175 °C and for a cumulative lifetime duration of less than 1000 hours. Here the application criteria can be compared with the true capability of the oxide and therefore be confidently selected for the application.

This application note assess several common MOSFET topologies in order to provide an understanding of V_{GS} behaviour. From this it is possible to generate an estimate for what V_{GS} will be applied to the MOSFET and for how long; a V_{GS} profile. Using the V_{GS} profile along with operating-voltage profiles and temperature profiles a full mission profile can be created. An example is shown in Table 1. The mission profile can be used to assess the MOSFET's suitability for the application against the TDDB data.

The first set of analyses presented considers steady state stress on the gate-oxide due to a constant gate-source bias from either an external gate-driver or as a result of the steady state voltages that appear on the gate and source terminals of a MOSFET. Further analysis attempts to estimate the contribution to gate stress from transient gate-source voltages. This could result from capacitive coupling through the Miller capacitance or conduction through the MOSFET body diode. Both require detailed analysis of the application to verify compatibility with the MOSFET features.

Table 1. Example MOSFET mission profile, showing the time spent in hours at a particular V_{GS} and MOSFET junction temperature

	Time (hours)				
V_{GS} =	T_j = -40 °C	T_j = 25 °C	T_j = 80 °C	T_j = 105 °C	T_j = 125 °C
-5 V	1	5	10	1	0
2 V	10	50	100	10	2
5 V	1000	2500	5000	50	10
10 V	100	200	300	100	5
20 V	2	10	5	2	1

5.1. Application assessments

This section assesses several common topologies featuring MOSFETs and focuses on the V_{GS} behaviour. This information will help to produce the mission profile as shown in Table 1.

5.1.1. Single MOSFETs

Starting with the three application topologies shown in Figure 6. Figure 6a and 6b can be considered similar in behaviour as they are both driven gate to source. However, Figure 6c shows the MOSFET being driven gate to ground. It is possible to drive the MOSFET in this manner by ensuring the gate voltage is higher than whatever voltage is currently at the source terminal. However, it is highly recommended not to do so as will become apparent throughout the discussion.

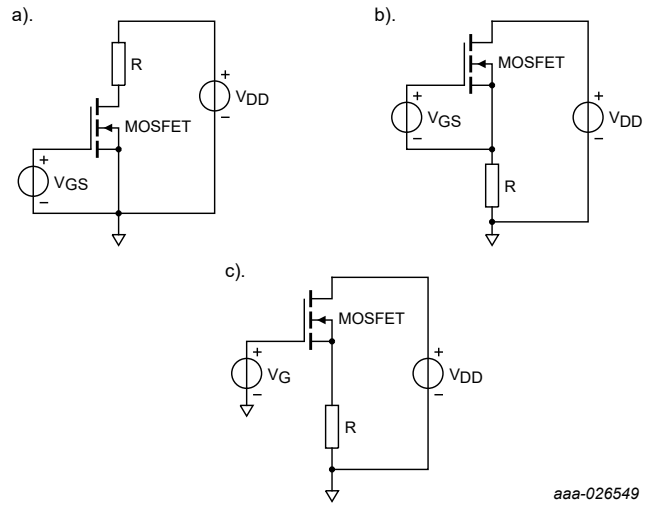


Fig. 6. a) Low side MOSFET b) High side MOSFET driven Gate to Source c) High side MOSFET driven gate to ground

In Figure 6c, when a V_G is applied, first assumptions may be that the voltage across the load resistor will be close to V_{DD} due to the low on-state resistance of a MOSFET compared to the load. However, the V_{GS} of the MOSFET is $V_{GS} = V_G – V_S$, where V_S is the voltage developed across the load in this example. This means that as V_G rises so, will V_S thus reducing the overall V_{GS} across the MOSFET. The result is a MOSFET that is not fully enhanced and therefore taking a significant portion of the V_{DD} across its drain and source terminals. The MOSFET is now dissipating a considerable amount of power and operating in linear mode, which may have thermal runaway implications. In addition, the load may not behave as expected due to it no longer having the full V_{DD} across it.

In Figure 6a the MOSFET source and gate-driver supply are both grounded and therefore provides a true V_{GS} supply. Likewise in Figure 6b, now the gate-drive is able to float above the source voltage and apply the full drive to the gate-source terminals of the MOSFET. Both the circuits in Figure 6a and 6b the MOSFETs are easily turned fully on and can achieve the low $R_{DS(ON)}$. This allows the full V_{DD} to be applied across the load and ensures correct operation of the application.

5.1.2. Half, Full and Three-Phase Bridges

Other application examples include half bridges and by extension full bridges and three phase bridges which can be found in DC-to-DC convertors and motor drives. Here, in any individual leg two MOSFETs are placed in series. When the MOSFETs are off the resistance across the drain-source terminals is not infinite and leakage paths exist. For simplification, these can be treated as resistances across the drain-source terminals. Referencing Figure 7 it can be seen that the V_{GS} on the high side (HS) MOSFET can be $-V_{DD}/2$. The time the MOSFET V_{GS} is at $V_{DD}/2$ V may be significant due to this occurring whenever the application is off and connected to the supply voltage. This will need considering in the mission profile and the MOSFET will need to be specified to meet this requirement.

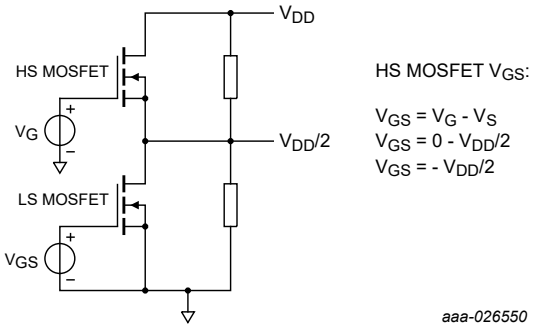


Fig. 7. Half bridge MOSFET configuration showing leakage paths and potential issues if driving High Side MOSFET with respect to ground.

When the MOSFETs are driven with respect to ground the required gate-drive needs to be at least the required V_{GS} for the MOSFET summed with the maximum voltage at the MOSFET's source terminal. For example, an automotive application typically uses a lead acid battery. Potentially the application could see 18 V from the battery and therefore the same voltage may appear on the source terminal of the high side MOSFET. This means to drive a typical SL MOSFET a gate voltage of 28 V (18 V + 10 V) with respect to ground is required to ensure the MOSFET is fully enhanced. Now the gate-drive is fixed at 28 V. However, the battery voltage may be as low as 6 V. This means the V_{GS} will be 22 V (28 V - 6 V). For a SL MOSFET this is outside its safe operating limits and has the potential to reduce its reliability in the application.

Within half bridges the extremes of the V_{GS} have been considered but the source voltage of the high side MOSFET does not depend solely upon the battery-voltage: load conditions which are variable with temperature and supply-voltage result in not knowing accurately what the source-voltage will be during considerable periods of operation of the application. This makes it very difficult to assess the V_{GS} requirement of the MOSFET when driving them with respect to ground. It is preferred and advisable to have the gate-driver referenced to the source of the MOSFET and not ground. Now, when the source voltage changes the gate-drive will be referencing this and the V_{GS} will be controlled. However, even when driving the MOSFET with respect to source there are still times when the V_{GS} is not fully dictated by the gate-driver. An assessment of transient analysis is required next.

All the applications discussed and their V_{GS} behaviour have been assessed under steady-state conditions, the next few paragraphs take into consideration the dynamic behaviour whilst the MOSFET is switching or commutating currents. In the example figures already shown the gate-drivers have been idealised as perfect voltage sources. However, all gate-drivers will have output impedances and drive current limitations adding to the complexity of transient behaviour for the application. In addition to this the PCB layout will be a factor, with track impedances contributing to the application behaviour. It is beyond the scope of this application note to discuss best layout practices beyond noting that gate-drivers should be placed as close as possible to the MOSFET it is driving. Some of these issues have been addressed in application note AN11599 - Using power MOSFETs in parallel.

The transient operation of the half bridge is now reviewed, here solely the case where the MOSFET is driven gate to source is considered. The load is inductive, representing half bridges (DCDC convertors for example) and three-phase bridges (Brushless DC motors for example). The full operation of these applications is not considered but in each, during the switching of the MOSFETs, the considerations to the gate-drive are similar.

Before describing the application behaviour, it is important to note that all MOSFETs have parasitic capacitances that couple each of the terminals, gate, drain and source (Figure 8). They are C_{GS}, C_{GD} and C_{DS} and exist as part of the MOSFET structure, playing a critical role in the transient behaviour of MOSFETs and therefore the application.

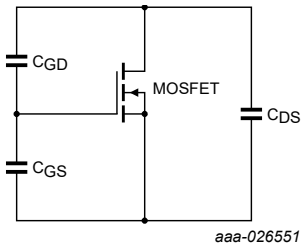


Fig. 8. Internal parasitic MOSFET capacitances

In half-bridges during an example transient event, one MOSFET is turned off and the second is turned on, this causes the switch node voltage to rise and fall. The switch node is where the source of the high side and the drain of the low side MOSFETs are connected. The dV/dt on the switch node can couple through the C_{GD} of a MOSFET and charge or discharge that MOSFET's C_{GS}, appearing as V_{GS}. Whether the V_{GS} is positive or negative depends on the sign of the dV/dt. It is the function of the driver to compensate for this change in V_{GS} by charging/discharging the V_{GS} to the set level. How effective the gate-driver is at this depends on a couple of factors, the rate of the dV/dt and how well the driver is coupled to the gate and source (how much impedance is between them). Again, being aware that the total impedance is a sum combination of package, resistance and inductances, trace parasitics and intentionally placed components (which have even more parasitics). This behaviour is shown in Figure 9. The consequences of this gate-bounce are biasing of the gate for a cumulative time which needs to be considered in any mission profile and worse, potentially causing cross conduction where both MOSFETs are on simultaneously.

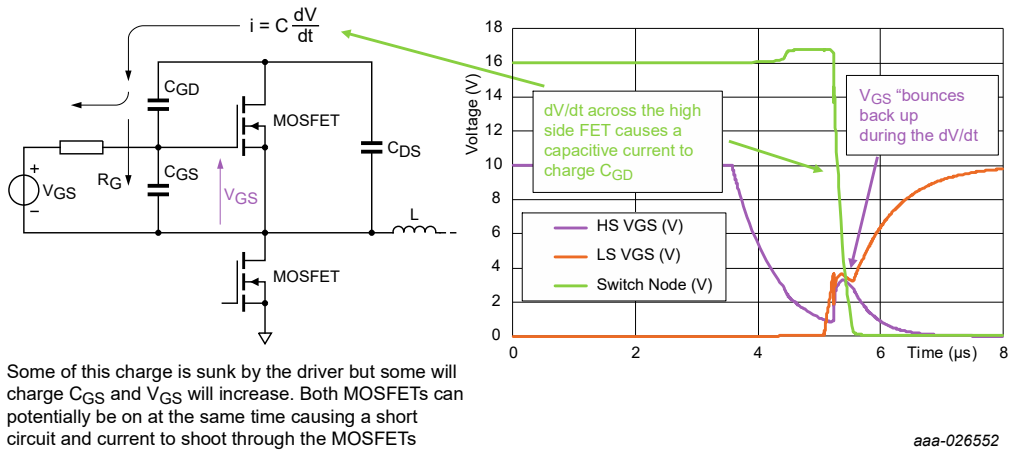


Fig. 9. Dynamic behaviour of a MOSFET half bridge

5.1.3. High side MOSFETs with Inductive loads

Other applications where V_{GS} behaviour may not be as first expected, are when driving inductive-loads. Take again the examples in Figure 6 but now replace the restive-load with an inductive one. The difference in driving methodology, that is with respect to ground or to the source, could result in either the MOSFET operating in linear mode or entering avalanche respectively. Consider now the situation where the gate-drive is referenced to ground. Also assume there is sufficient drive on the gate to compensate for an increase in source voltage, thus allowing the MOSFET to be fully enhanced. When the MOSFET is turned on current will increase through the inductor, and energy will be stored in its magnetic field. Then the gate-driver is turned off, the inductor starts to demagnetise and produces a back-EMF in order to maintain current flow. As one end of the inductor is grounded this back-EMF appears as a negative voltage on the source. The voltage will continue to decrease until the V_{GS} is great enough such that the MOSFET is partially turned on, maintaining the inductive current flow. Here the MOSFET is in linear mode, the V_{GS} is somewhere between off and fully on and the V_{DS} is significant; remembering that the source is now negative. See Figure 10 for an illustration.

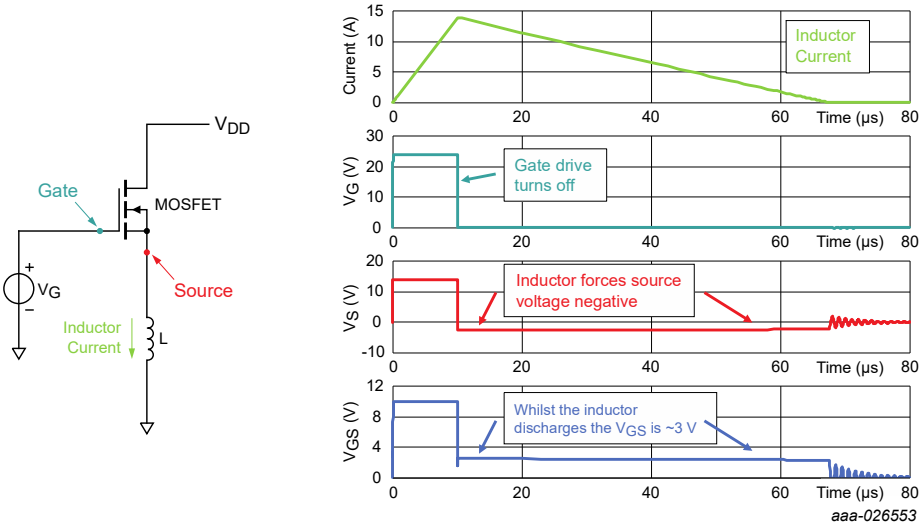


Fig. 10. Circuit and waveforms showing the V_{GS} behaviour whilst driving an inductive load and the gate of the MOSFET is driven gate to ground

Taking the previous example of driving an inductive load but with the gate being driven with respect to the source, the behaviour is similar until the MOSFET is turned off. Again the V_s will go negative until current flow is maintained, however the source is tied firmly to the gate by the driver which is operating at 0 V. No matter how negative the source goes (within operational limits) the MOSFET will stay off. Instead, the V_S will continue to decrease and therefore the V_{DS} will continue to rise. Ultimately the V_{DS} will reach the breakdown voltage of the MOSFET's internal body diode and avalanche (Figure 11). As with linear mode the power dissipation is considerable due to there being voltage and current present in the MOSFET, but avalanche is a preferable method of absorbing the inductive energy. Compared to linear mode, avalanche operation is better at sharing this power dissipation across the silicon die. Further information avalanche can be found in a MOSFET's data sheet and in more detail in application note AN10273 - *Power MOSFET single-shot and repetitive avalanche ruggedness rating*.

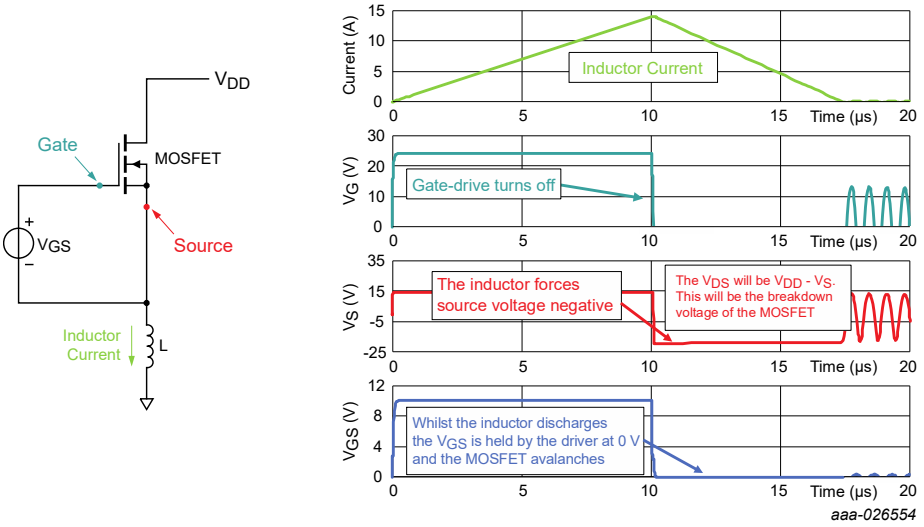


Fig. 11. Circuit and waveforms showing the V_{GS} behaviour whilst driving an inductive load and the gate of the MOSFET is driven Gate to Source

5.1.4. Motor Loads

One final application to be consider is driving motors with a single high side FET as in figure. Again the designer is recommended to drive the MOSFET with respect to ground to ensure full control of the MOSFET and application behaviour. Driving with respect to ground and the source voltage will

be near V_{DD} due to motor back EMF; all the previous considerations to driving respect to ground apply.

5.2. Application assessment summary

This application note has summarised some common application behaviours and their impact on the MOSFET's V_{GS}. The application note has shown that driving a MOSFET with respect to ground causes numerous issues and difficulties. These include operating in linear mode and not knowing what the V_{GS} may be at any point in time. This makes it difficult to formulate a mission profile to select the correct MOSFET. However, driving the gate with respect to source does not remove all of the issues; there are transient events that can induce positive or negative voltages on the V_{GS} that are not fully controlled by the gate-driver. We are still short, however, from producing the mission profile to ensure the correct selection of a MOSFET. The correct MOSFET should not be over-specified and should still operate reliably in the application for its intended life. We now need to create a mission profile.

6. Creating a mission profile

An example mission profile is shown in Table 1, it is a distribution of V_{GS} voltages at a range of temperatures and for how long. However, before generating a profile, several pieces of information need to be gathered. These include but are not limited to:

- How long the application is in operation
  - On and Off times
  - Possible fault conditions
- The distribution of operating temperatures
- The distribution of supply voltages

Along with an understanding of the application as outlined is the previous sections, this information can be used to create a mission profile. The mission profile can be assed against the TDDB data for a given MOSFET, thus determining the MOSFET's suitability for the application.

6.1. Example – Full H-bridge motor drive

An example automotive application is brushed Direct Current (DC) motors such as windscreen wiper motors or seat control motors. For this worked example the MOSFETs are driven with respect to their source terminals and not to ground.

The first part of the exercise is to gather information on how long the application will be operating for. This information can then be translated into how long the MOSFETs are on for and therefore how long they will have a V_{GS} applied. In this instance it is common for the Original Equipment Manufacturer (OEM) to stipulate the usage profile of the system and it may look like (Table 2).

Table 2. Number of motor operations and the total time spent in operation

Operations	Total operation time at 0.5 s per actuation (hours)
180,000	25

Other times when there may be a voltage present at the gate of the MOSFET is when the engine is off but the electronics are on. In the case of the motor, the two high side MOSFETs may be switched on to brake the motor. This time will add cumulatively to the mission profile (Table 3).

Table 3. Battery voltage whilst the engine is off and the time spent at this voltage whilst the electronic systems are connected to the battery

V_{GS} (V)	Time (hours)
12.5	6,000

Table 3 provides the first piece of information required to build our V_{GS} profile. We need to convert the information in Table 2 into the same. To do so, we need to know the V_{GS} the MOSFET will be driven at. The V_{GS} may be set at 10 V by a power supply or alternatively the MOSFET may be driven directly by the battery voltage. The battery voltage will have its own distribution (Table 4). Using Table 2 and Table 4 we get Table 5.

Table 4. Battery voltage distribution of the life time of the application

Battery Voltage (V)	Distribution
14.5	77%
16	15%
17	5%
18	3%

Table 5. V_{GS} profile based on battery voltage distribution and application operation time, including the V_{GS} applied to the MOSFET whilst the engine is off

V_{GS} (V)	Time (hours)
12.5	6000

V_{GS} (V)	Time (hours)
14.5	19.25
16.0	3.75
17.0	1.25
18.0	0.75
20.0	0.00825

Table 5 is now a V_{GS} profile, it shows the time spent at each V_{GS} value. However, it is missing the temperature profile to make it into a full mission profile to be assessed against the TDDB data. To generate a temperature profile the OEM and the application designer need to work together. Remember that the MOSFET may be operating a little hotter than its ambient (due to self-heating) so engineering margin may need to be added. An example is shown in Table 6.

Table 6. Ambient and junction temperature distribution of the expected life time of the application

The junction temperature is arbitrarily increased by 50 °C, this can be changed based on engineering judgment or calculation when better informed of the systems operational parameters.

T_{amb} (°C)	T_j (°C)	Distribution
-40	10	6%
23	73	20%
40	90	65%
75	125	8%
80	130	1%

Table 5 contains the V_{GS} values, and Table 6 has the temperature distribution. These two together contain the information to make Table 7, the full V_{GS} profile. For example, for 6% of the time the MOSFET junction temperature is at 10 °C. By multiplying the hours at each V_{GS} (from Table 5) by 6% the T_j = 10 °C column in Table 7 is populated. It may be the case that the higher V_{GS} voltages only occur at the lower temperatures. The profile in Table 7 will need to be updated to reflect this but can only be done so by the application designer working with the OEM.

Table 7. Full mission profile showing the time in hours for a given V_{GS} voltage and MOSFET junction temperature

	Time at V_{GS} and Temperature (hours)				
V_{GS} (V)	T_j = 10 °C	T_j = °C	T_j = 90 °C	T_j = 125 °C	T_j = 130 °C
12.5	360	1200	3900	480	60
14.5	1.155	3.85	12.5125	1.54	0.1925
16	0.225	0.75	2.4375	0.3	0.0375
17	0.075	0.25	0.8125	0.1	0.0125
18	0.045	0.15	0.4875	0.06	0.0075

The profile in Table 7 shows that for a time the MOSFET will see a V_{GS} of 18 V at elevated temperatures. Using solely the datasheet ratings a logic-level MOSFET's $V_{GS\text{-}max}$ rating of 15 V would seem to exclude it from use in this application. However, working with Nexperia to compare the profile to the logic level MOSFETs TDDB data it can be shown that the MOSFET is more than capable of operating reliably in the application. This is because the time spent at these conditions is short.

Once the design engineer has generated a V_{GS} mission profile they are encourage to contact their local Nexperia representative to receive support. Working with Nexperia, the profile can be assessed against the TDDB data and a suitable MOSFET can then be suggested.

7. Summary

The gate-source lifetime and the gate-source turn-on voltage are highly dependent on temperature so one needs to be careful in comparing datasheets from different suppliers where the stated temperature conditions for the gate-source voltages are different.

For devices that do not see the maximum gate-voltage at maximum temperature throughout their intended life, Nexperia has a methodology to provide a better assessment of the required gate-oxide rating for such an application. This would often allow better performance in other parameters without compromising reliability in the application.

This does require the so-called mission profile of the MOSFET in the application, as described in this application note.

8. Abbreviations

Table 8. Abbreviations

Symbol	Description
MOSFET	metal-oxide-semiconductor field-effect transistor
$V_{GS(th)}$	gate-source threshold voltage
V_{GS}	gate-source voltage
V_{DS}	drain-source voltage
T_j	junction temperature
V_S	source to ground voltage
V_G	gate to ground voltage
V_{DD}	application supply voltage
C_{GS}	gate-source capacitance
C_{GD}	gate-drain capacitance
AEC	Automotive Electronics Council
HS MOSFET	High side MOSFET
LS MOSFET	Low side MOSFET
SN	Switch node
IEC	International Electrotechnical Commission
TDDB	Time Dependant Dielectric Breakdown
OEM	Original Equipment Manufacturer
DC	Direct current
T_{OX}	Oxide thickness
E_{OX}	Oxide electric field strength

9. References

1. *Rating systems for electronic tubes and valves and analogous semiconductor devices.* **IEC.** IEC 60134:1961.
2. *Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors.* **AEC.** Vol. Rev D. AEC - Q101.
3. *A methodology for projecting SiO_2 thick gate oxide reliability on trench power MOSFETs and its application on MOSFETs V_{GS} rating.* **Efthymiou, E, Rutter, P and Whiteley, P.** 2015, Microelectronics Reliability.

10. Revision history

Table 9. Revision history

Revision number	Date	Description
1.1	2024-10-29	Updated the maximum V_{GS} limits in the Figure 3 and reflected this in section 2.2 and 3 description
1.0	2017-03-31	Initial version of the document

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