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APPLICATION NOTE 6748

HOW TO ADDRESS REFERENCE LONG-TERM DRIFT PERFORMANCE

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Abstract: Voltage references play an important part in driving the total system error in mixed-signal systems. This application note takes a look at the various factors that affect the long-term drift performance of these references.

Introduction

In mixed-signal systems, voltage references set the precision standard. Whether biasing an analog-to-digital converter (ADC) or digital-to-analog converter (DAC), the reference has an important role in driving the total system error. Key internal factors that dictate the overall performance of voltage references are the IC design architecture, design techniques, and fabrication process. Also important are specifications including noise, thermal hysteresis, temperature coefficient, and long-term drift (LTD).

LTD is measured as the output voltage shift from a given voltage reference at power-up and then at selected intervals over time. Data is plotted in terms of parts per million. Below is the theoretical formula of LTD:

$$LTD(ppm) = \max\left[\frac{\left(V_{OUT(tn)} - V_{OUT(t0)}\right) \times 1e^{6}}{V_{OUT(t0)}}\right]$$

where,
V_{OUT} = Voltage output of the device under test (DUT)
t_0 = first hour of measurement
t_n = nth hour of LTD data collection, where n can be as many hours as the voltage reference is powered-up

Many factors can affect a voltage reference's LTD. Some examples include package stress due to package size, mold compound, PCB stress, and external environmental factors such as temperature and humidity. Using this data, the LTD(ppm) can be practically modeled with the following function:

LTD(ppm) = f($V_{OUT(t0)}$, package stress, PCB design, PCB assembly quality, compound settling time, temperature, humidity)

Package Stress and a Pair of Shoes

A pair of shoes might serve as an appropriate analogy to explain package stress. When the shoes are comfortable, they are most likely the correct size for the foot. If the shoes are too small, however, they might seem to fit initially but they probably wouldn't be too comfortable, and over time they'd be sure to cause pain. A similar thing happens with semiconductor packages. Package stress results when a die is crammed into a package that is not suitable for the die size, a practice that can affect the device's performance over time.

Figure 1 and **Figure 2** depict LTD plots for two devices with the same core but different (SOT-23 and ceramic) packages.

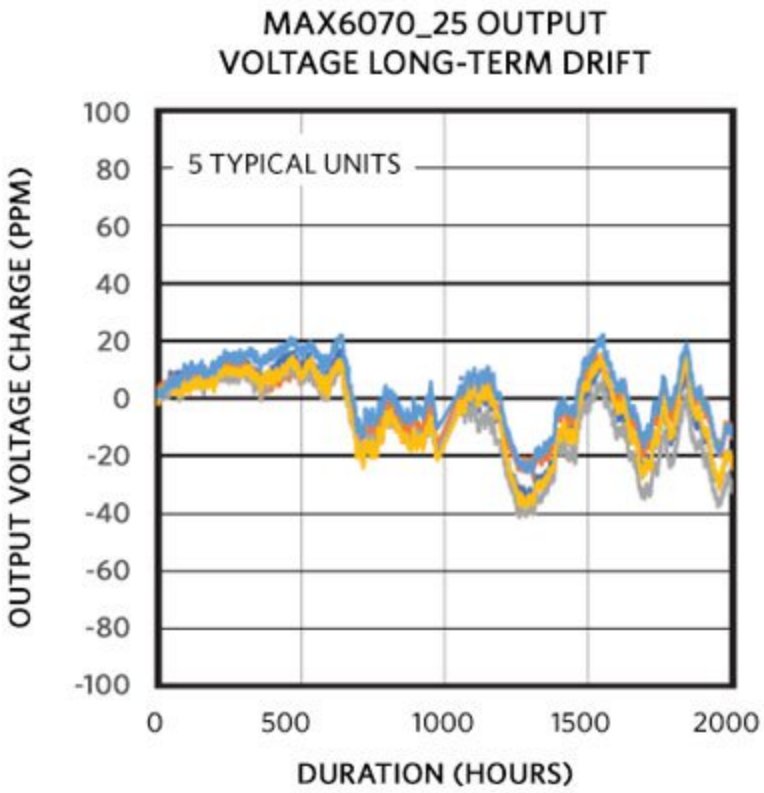

Figure 1. LTD plot for SOT-23 package.

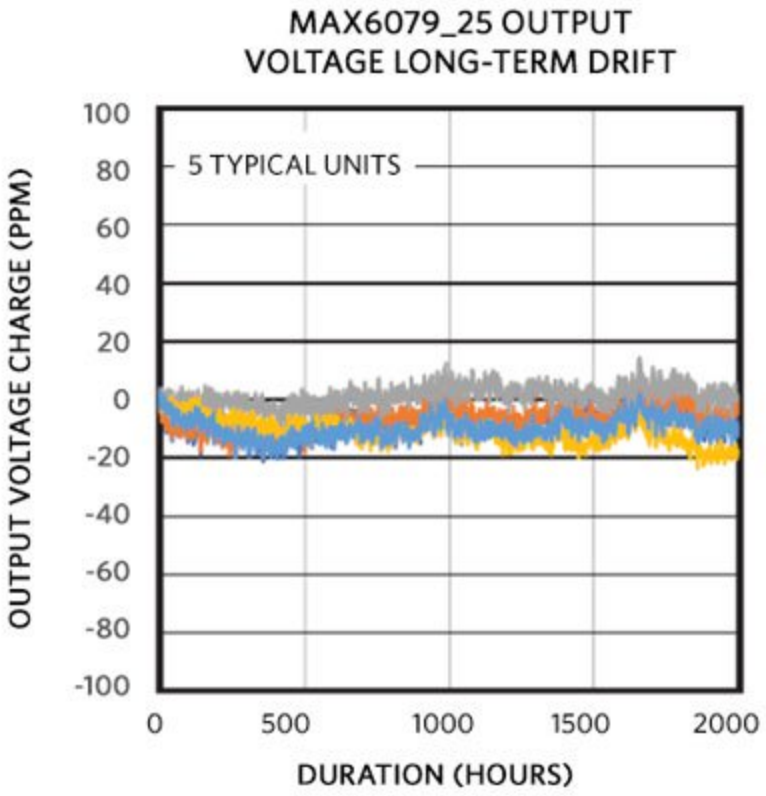

Figure 2. LTD plot for ceramic package.

Reducing Stress in the PCB Design

Some PCB designers use three- or four-sided PCB cut-out "slotting" techniques per site when designing LTD boards (**Figure 3**) to mitigate solder joint stress. Slotting the PC board is beneficial because it can thermally isolate the device under test (DUT) from surrounding circuitry, which can help reduce thermocouple effects and improve accuracy. A tab cut through the PC board on three sides of the voltage reference can reduce solder joint stress on the DUT. It’s important, of course, to ensure that measurements are consistent from site to site and board.

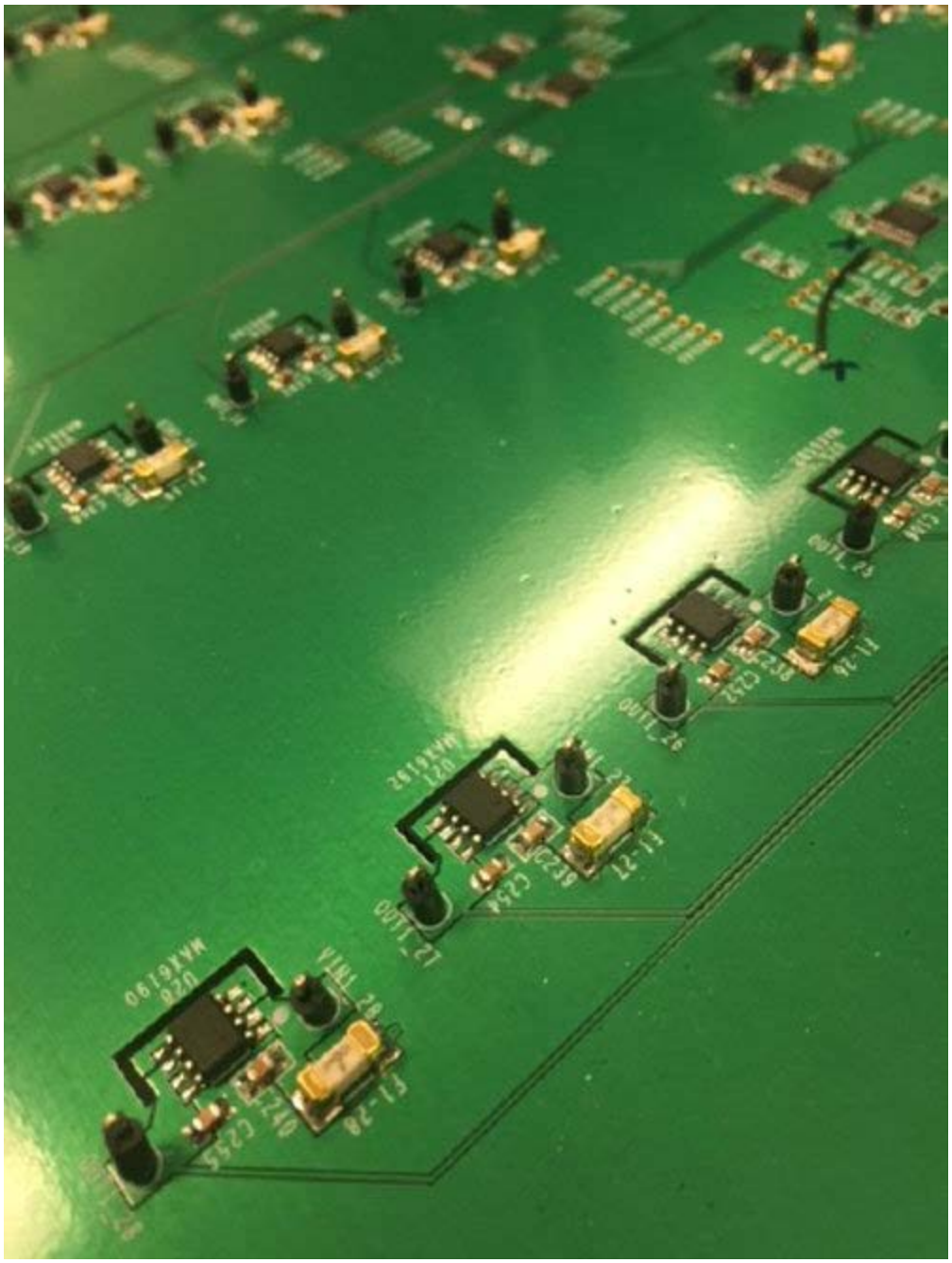

Figure 3. Three-side cut-out "slotting" to relieve solder joint stress.

Baking the PCB through several temperature cycles before attaching the DUT presents another way to reduce PCB stress. Then, before board power-up, the PCB with DUT soldered down undergoes a temperature cycle. This process de-stresses the PCB, which has gone through reflow assembly. The temperature cycle occurs within a short period after PCB reflow.

Bench Test Setup Considerations

A fully automated, multisite laboratory setup was developed to characterize the LTD of voltage references over a sample size that meets the statistical requirement for Gaussian analysis (**Figure 4**). The bench equipment was multiplexed by using onboard circuitry to power up, configure, and measure the V_{OUT} from different DUT sites, one at a time.

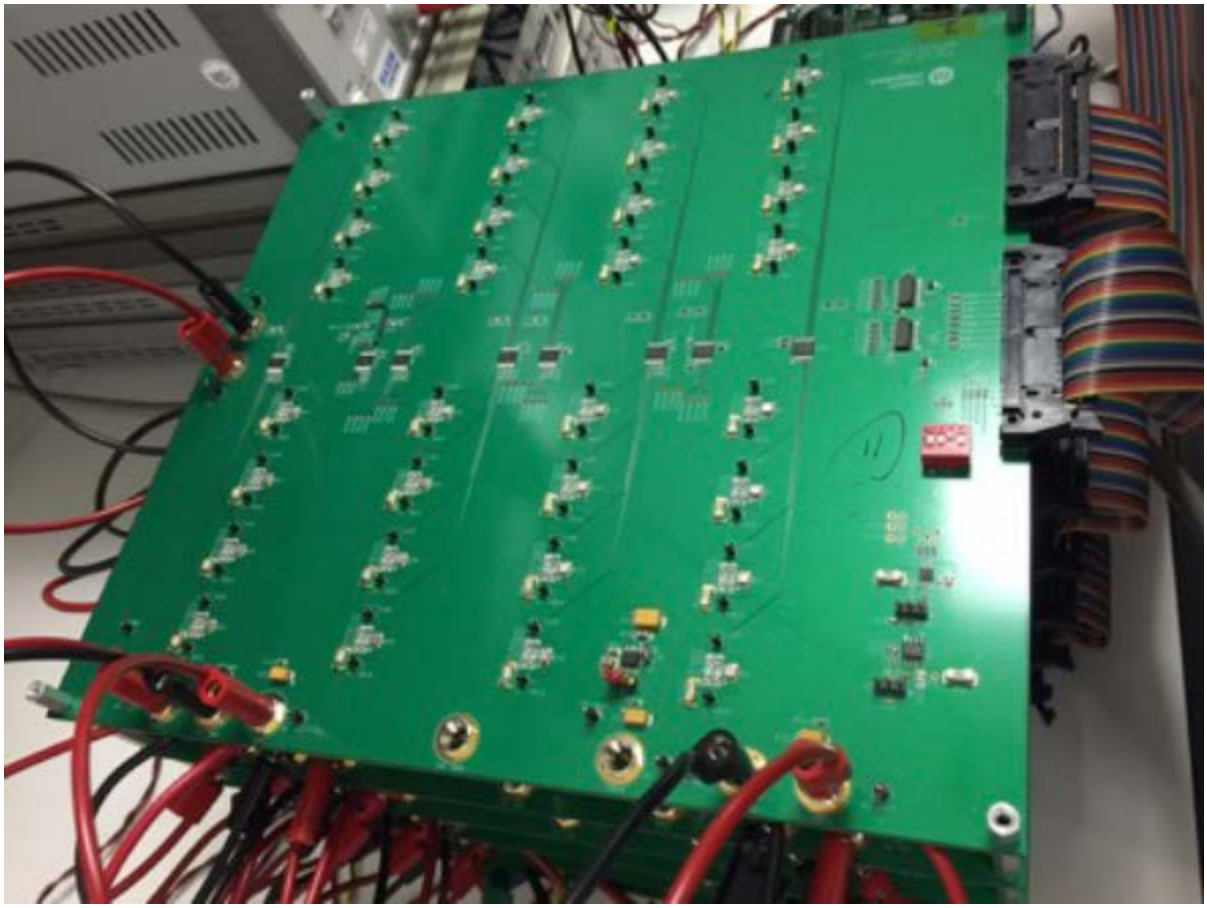

Figure 4. Multisite voltage reference PCB.

A chamber that provides environmental conditions, temperature, and relative humidity with corresponding temperature and humidity sensors adds to setup-monitoring capabilities (**Figure 5**). Automation ensures the consistency of setup configurations and reliable measurements and reduces human error in post-processing and data-logging. Pin- and package-compatible variants can be tested using the same setup. The setup is backed by an uninterruptible power supply (UPS) to avoid the DUT reset, should the power fail.

Figure 5. LTD bench setup.

Data collected consists of voltage output measurements that are later post-processed to provide the LTD measurement for each device tested. The industry standard for voltage reference LTD is 1000 hours. Automation has created an ability to exceed that benchmark by monitoring and collecting data for as many as 10,000 hours (**Figure 6**). LTD data was taken from several of Maxim's popular voltage references and the competition for comparison.

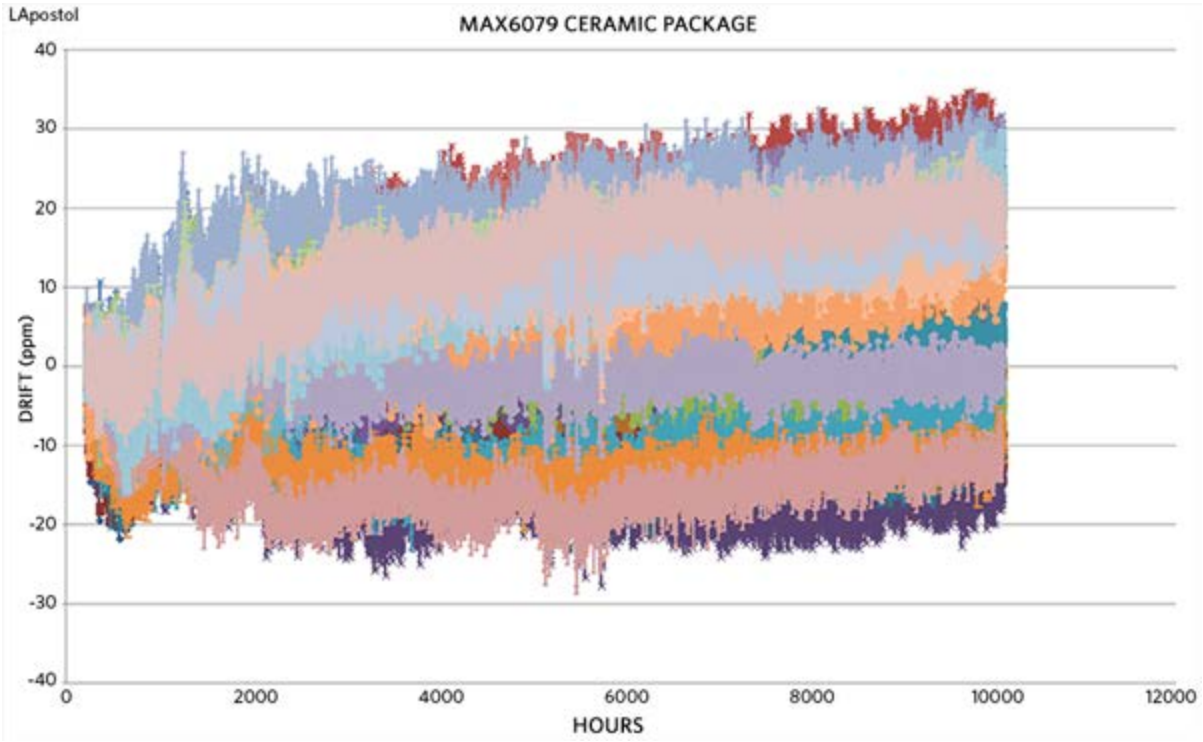

Figure 6. MAX6070 LTD over 10,000 hours.

Reflow Assembly

PCB assembly is usually done with solder reflow in the industry. The same approach is applied in experiments. This ensures that all required components undergo the same specified temperature profile, minimizing errors stemming from hand-soldering and prolonged elevated temperature exposure due to manual soldering.

Package Compound Settling

Semiconductor devices are encapsulated in packages made from plastic molding compounds consisting of epoxy resins, catalysts, hardeners, and mold release agents. For the best device performance and durability, it's prudent to evaluate different compound properties (such as glass temperature transition, flexing or bending strength, moisture absorption, and adhesion) to select the proper material.

The glass temperature transition is the temperature point at which the viscosity, thermal expansion, and heat capacity of the compound show a relatively sudden change. The molding compound with high flexural strength exerts larger stress and is not preferred for small or thin packages. As voltage reference LTD is highly affected by relative humidity (discussed later in this application note), the moisture absorption rate is one of the key compound properties to be considered.

The MAX6025AEUR+ in SOT-23 plastic package (**Figure 7**) was tested with the LTD setup. Data has shown that the package compound settles during the first 200 to 300 hours.

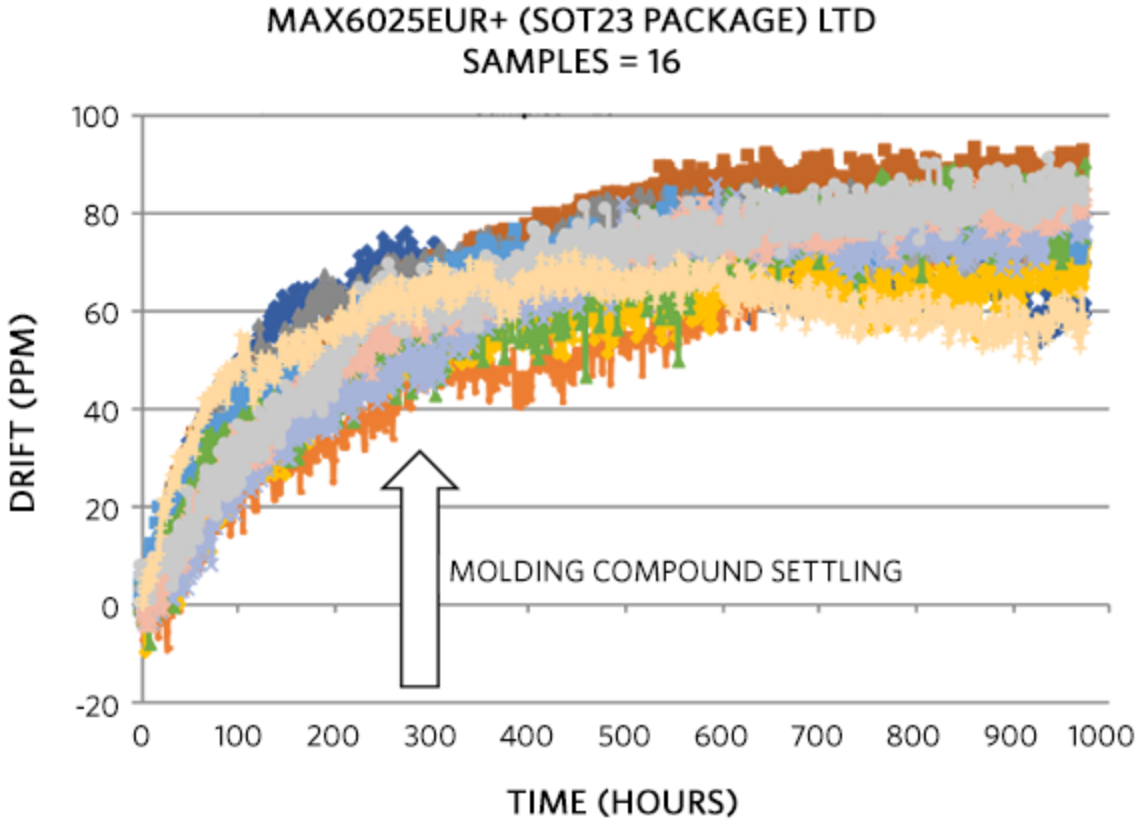

Figure 7. Package compound settles during the first 200-300 hours.

Temperature

The following temperature-dependent parameters affect the LTD performance of the voltage reference:

- Temperature coefficient (tempco)
- Thermal hysteresis

Tempco

The tempco is the maximum voltage output drift with respect to the change in temperature. It is measured by the "box" method, i.e., the maximum $\Delta V_{OUT}/ V_{OUT}$ is divided by the maximum ΔT (**Figure 8**).

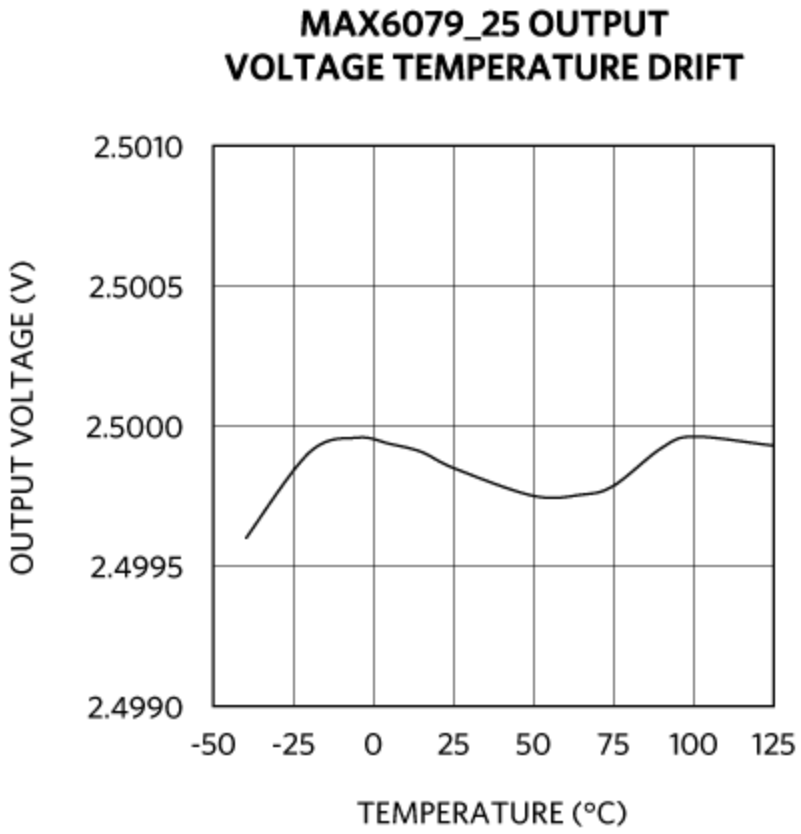

Figure 8. Typical tempco plot.

Thermal Hysteresis

Thermal hysteresis is the change of output voltage at TA = +25℃ before and after the device is cycled over its entire operating temperature range. Hysteresis is created by mechanical stress applied to the device based on whether it was previously at a higher or lower temperature (**Figure 9**).

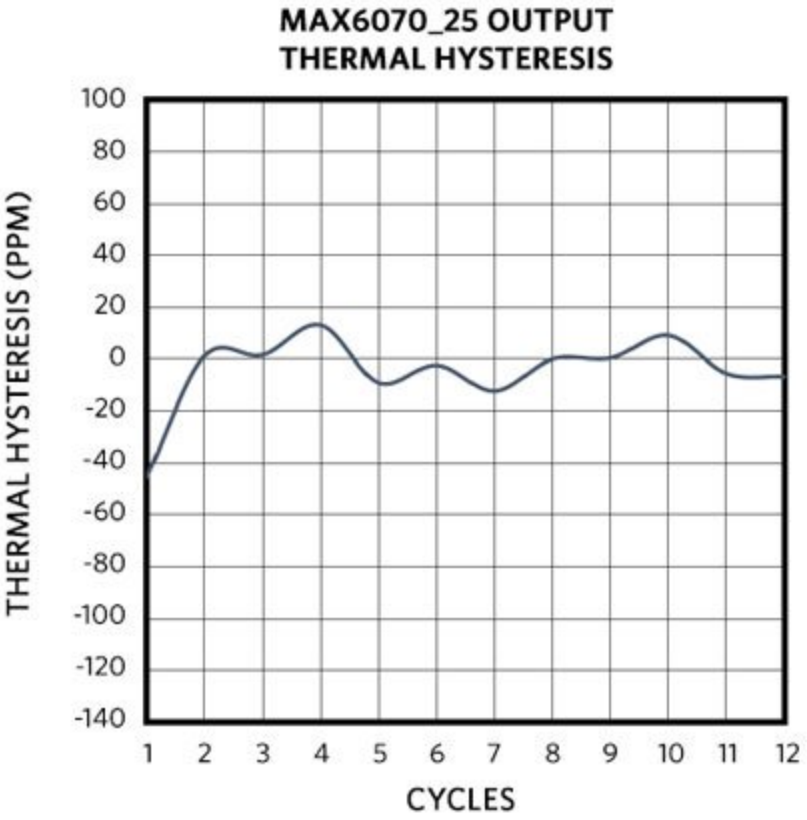

Figure 9. Typical thermal hysteresis plot.

Relative Humidity

The least understood factor affecting LTD is relative humidity, which changes with temperature and air pressure. Relative humidity is the amount of water vapor present in air and is expressed as a percentage of the amount needed for saturation at the same temperature. Though semiconductor packaging provides electrical insulation, it is not hermetically sealed (air tight) and atmospheric gas can diffuse through the porous plastic mold and openings at the lead frame. The mold after assembly contains diffused air, and water molecules can diffuse in at a slow rate. Though this effect is not obvious with instantaneous testing, the effects are prominent for a relative measurement such as LTD over an extended period.

Our lab experiment, where relative humidity moved from 40% to 25%, has shown a significant move in LTD measurement for the MAX6138AEXR25 in a SC70-3 plastic package (**Figure 10**). This occurrence depicted an inversely proportional shift in LTD because of a change in relative humidity. MAX6138EXR25 essentially behaves like a humidity tracker. The MAX6279, which is the same device core as the MAX6138 but in a ceramic test package, when subjected to the same change in relative humidity, maintained a drift of around 35ppm. Not much change in LTD was observed (**Figure 11**). This clearly indicates that ceramic, due to its non-porous material, provides a good level of immunity to the effects of moisture.

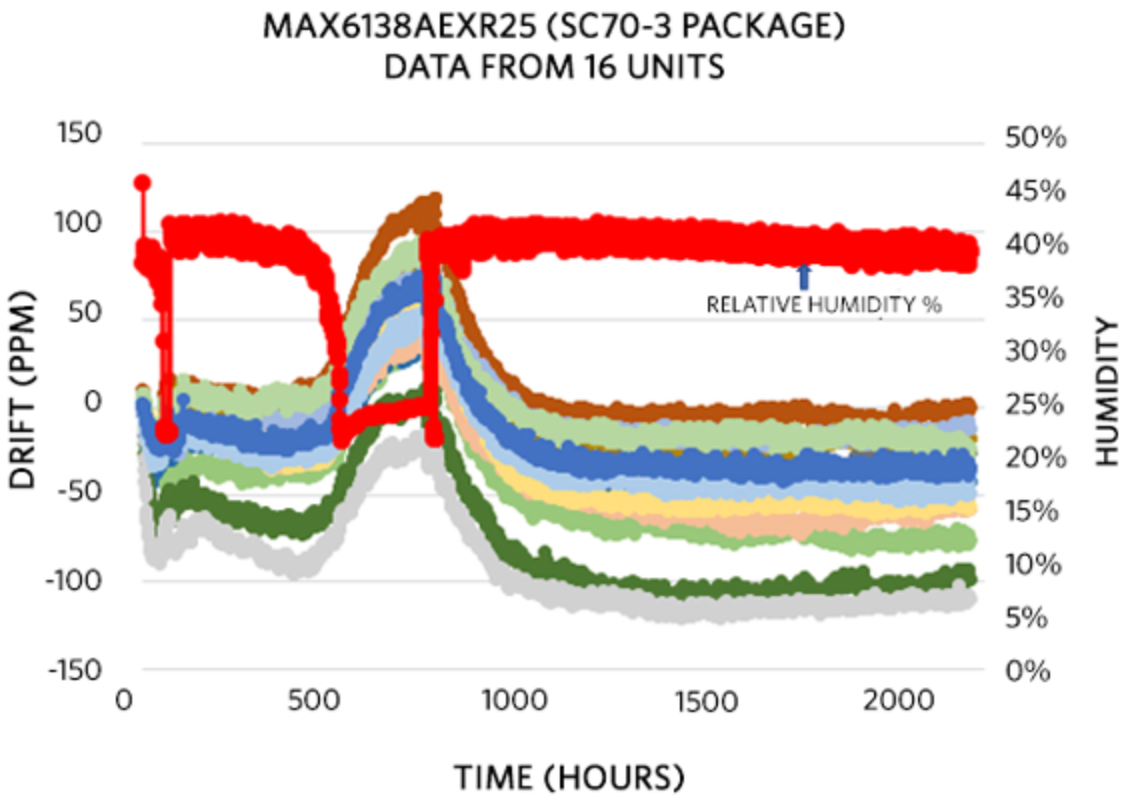

Figure 10. MAX6138AEXR25 (SC70-3 plastic package); LTD with regard to relative humidity.

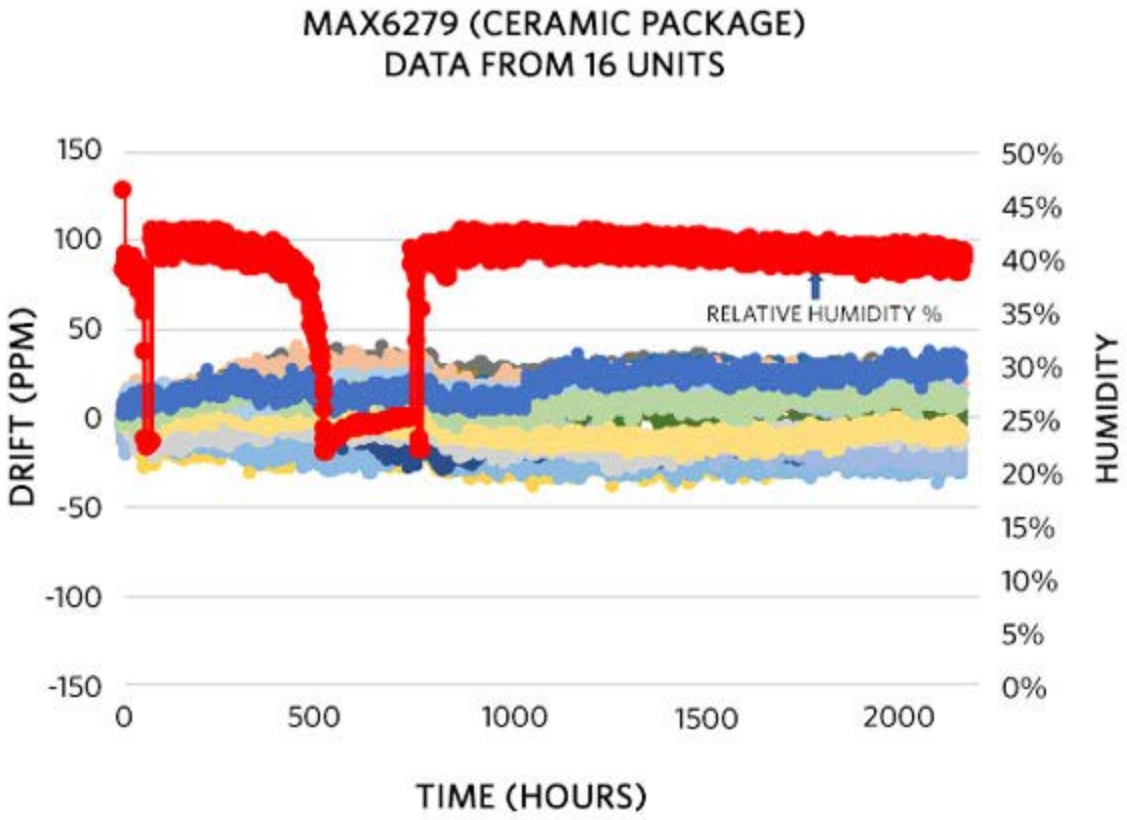

Figure 11. MAX6279 ceramic test chip LTD with regard to relative humidity.

Conclusion

Traditionally, semiconductor manufacturers show only 1000 hours of LTD data for their voltage references, which is minimal for systems running for many years. While overlooked, LTD is one of the most important specifications for industrial systems with a life span of 15 to 20 years. For a better idea of Maxim's voltage reference performance, LTD was performed on one of Maxim's popular voltage references packaged as SOT-23 (6-pin plastic) and ceramic for 10,000 hours. Since LTD performance is also dependent on external factors, it's wise for system designers to pay attention to the setup design, controls, and calibration options in addition to the right part/package selection for their application.

A similar version of this application note appeared March 26, 2018 in *EDN*.

Related Parts		
MAX6025	Precision, Low-Power, Low-Dropout, SOT23-3 Voltage References	Samples
MAX6070	Low-Noise, High-Precision Series Voltage References	Samples
MAX6138	0.1%, 25ppm, SC70 Shunt Voltage Reference with Multiple Reverse Breakdown Voltages	Samples
MAX6279	0.1%, 25ppm, Ceramic Shunt Voltage Reference	Samples

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