AN4971

Booting from External Non-Volatile Memory (NVM) on SAM9X7 MPUs

Introduction

This document describes the boot process of the SAM9X7 microprocessors (MPU).

MPUs, unlike MCUs, do not feature Flash memory, and thus depend on external Non-Volatile Memories (NVM) of different kinds for the boot process.

An on-chip ROM contains an initial boot program to launch an in-system programmer that allows a PC to load the NVM with the user application and setup the boot process. Microchip's SAM Boot Assistant (SAM-BA®) tools write the user application into the external NVM and set up the boot while running on the PC and connected to the SAM9X7 in the system through a USB, RS-232 or JTAG link. The tool suite is available on the Microchip web site, on the product page.

Secure SAM-BA Cipher, available on request, is used to prepare ciphered keys and application files for programming and to configure the Secure Boot mode on the SAM9X7, which builds a root of trust for the boot chain.

Finally, this document presents the supported types of external NVMs for the boot and discusses the technical aspects of booting from external NVMs on the SAM9X7 MPU.

Reference Documents

Document Type	Document Title	Literature Number	Available
Data Sheet	SAM9X7 Series	DS60001813	www.microchip.com

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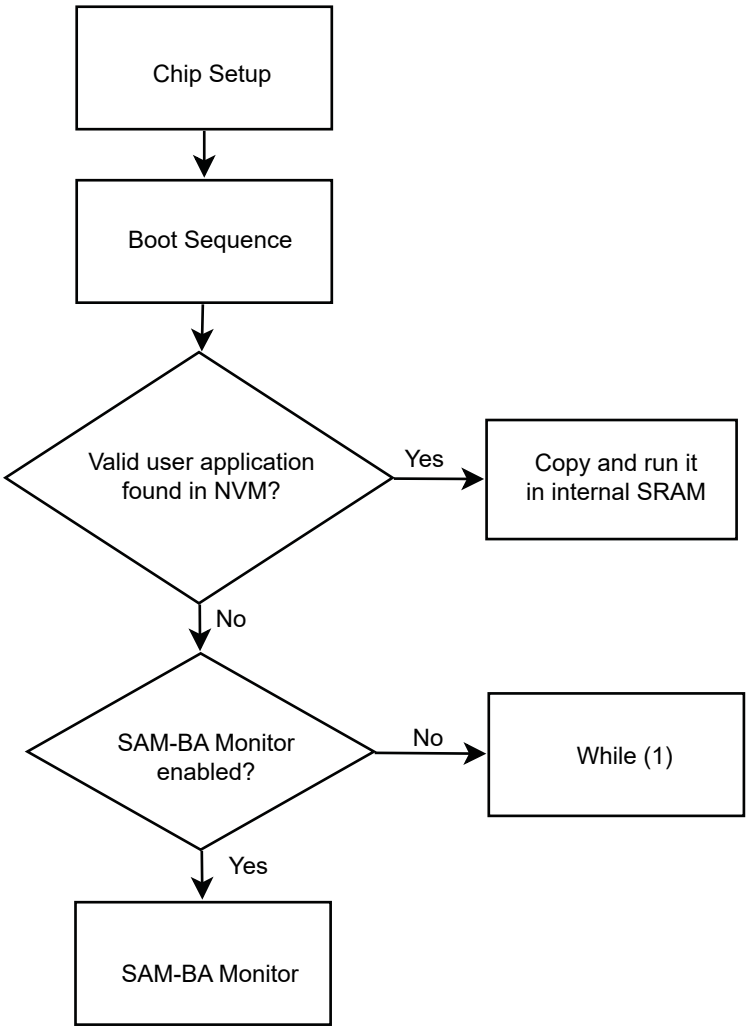
1. Role of the ROM Code

The ROM code (or Boot ROM) is stored in on-chip mask ROM and executes on power-on or after a Reset. It is responsible for loading the user application or a second-stage bootloader from an external NVM into the internal SRAM. The size of this user application is limited. Once loaded into the internal SRAM, the ROM code disables all peripheral clocks it has previously enabled, sets the PIO muxing back to its Reset state and then jumps to the address of the internal SRAM to execute the user application.

The user application should be linked so that its entry point is at the very beginning of the internal SRAM. Nevertheless, just before jumping to the user application, the ROM code also remaps the internal SRAM at address 0x0. Thus when the user application places its Arm® exception vector table at the beginning of the internal SRAM, the vectors are also seen at 0x0 by the Arm core when it needs to access them.

In the Arm9™ architecture, the 6th exception vector is reserved and the ROM code uses this 32-bit data to store the size of the user application. The ROM code fetches this value to know exactly how many bytes it should transfer from the external NVM, optimizing boot time. The ROM code also checks the other exception vector values to decide whether the user application can be considered as valid, or whether it should be skipped. The ROM code then tries to boot from the next external NVM in the boot sequence.

Figure 1-1. ROM Code Process Flow



1.1 Boot Sequence

For SAM9X7, the boot sequence is:

1. SDMMC0 IOSET1
2. SDMMC1 IOSET1
3. QSPI IOSET1
4. SPI5 IOSET1
5. NAND IOSET1

The user can configure a specific boot sequence tailored for the system by writing a Boot Configuration Packet in the One Time Programmable (OTP) memory. Refer to the product data sheet, section “Boot Configuration” for details.

If no bootable user application is found, for instance during the first boot in factory when the user application has not been written yet into the external NVM, the ROM code then executes its SAM Boot Assistant (SAM-BA) monitor, which in turn waits for a connection from the SAM-BA tool. Refer to ROM Code Process Flow.

1.2 SAM Boot Assistant (SAM-BA) In-System Programmer

The SAM-BA tool is a software program, running on a PC under Windows® or Linux®, which connects and then send commands through JTAG, USB or RS-232 to the SAM-BA monitor. This monitor is a software component of the ROM code, designed to help the customer program the user application in a supported external NVM. The SAM-BA tool may also be used to tune the boot sequence. The regular SAM-BA tool is open source and freely distributed on the Microchip website. Another tool, Secure SAM-BA Cipher, is distributed under Non-Disclosure Agreement (NDA) only and is used to prepare files to be used with the Secure Boot mode of the ROM code.

1.3 Secure Boot Mode

The Secure Boot mode extends the boot process of the ROM code to add security features and create a root of trust in the boot chain. Once the Secure Boot mode is enabled, the ROM code expects the user application in the external NVM to be ciphered and signed.

The user application is ciphered with the AES-256-CBC algorithm and signed with either AES-256-CMAC or RSA algorithm, using Secure SAM-BA Cipher to guarantee its integrity and authenticity.

The customer key is a shared secret between the customer and the microprocessor, and is written once in the OTP memory with the help of the SAM-BA tool.

The ROM code requires this customer key to decipher the user application. In the case of AES-256-CMAC, the customer key is also used to verify the signature.

Once the user application is authenticated and deciphered in the internal SRAM and before executing it, the ROM code forbids any further access to the customer key until the next Reset. This way the customer key cannot be extracted by any software running in the SoC.

To prepare the provisioning of the customer key during manufacturing, this key must be ciphered and signed with the secure SAM-BA cipher tool by the customer. Next, both the ciphered/signed user application and customer key are sent to the 3rd party manufacturer responsible for the production of the microprocessor-based design.

Then the programming of the customer boards is done by the third party manufacturer with the help of the SAM-BA tool. Only the ROM code is able to decrypt and authenticate the customer key received from the SAM-BA tool. Thus the third party manufacturer, or any other party having access to the ciphered customer key, cannot extract the plain customer key, upon which the security model relies.

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2. Supported External Non-Volatile Memories (NVM)

2.1 SDCard/e.MMC Boot

Boot may be done from SDCard or e.MMC memories connected to SDMMC0 or SDMMC1. Though SDMMC0/ SDMMC1 support up to x4 bus width, the ROM code transfers data only with a x1 bus width through SDMMC_DAT0.

The ROM code also supports e.MMC boot partitions. In order to boot from one of the two e.MMC boot partitions, the BOOT_PARTITION_ENABLE field (bits[5:3]) must be set to either 0x1 (Boot partition 1 enabled for boot) or 0x2 (Boot partition 2 enabled for boot) and the BOOT_ACK bit (bit[6]) must be set to 0x1 (Boot acknowledge sent during boot operation) in byte 129 of the Extended CSD register. Also the BOOT_BUS_WIDTH field (bit[1:0]) should be set to 0x0 (x1 bus width in boot operation mode) in byte 127 of the Extended CSD register.

The ROM code first checks if an e.MMC boot partition is enabled. If so, the maximum bootstrap size of the enabled boot partition is read by the ROM code. If no boot partition is enabled on an e.MMC or in case of a SDCard, the boot process continues with a standard SDCard/e.MMC detection. The ROM code looks for a “boot.bin” file in the root directory of the first partition, which must be formatted with a FAT12/16/32 file system.

⚠WARNING Implementing SDCard/e.MMC boot requires particular attention to the connection of the Card Detect pin. For information, refer to the section “SDCard/e.MMC Boot” of the data sheet.

2.2 Parallel NAND Flash Boot

The ROM code only supports 8-bit NAND Flash memories connected to the SMC; booting on 16-bit NAND Flash is not possible.

The correct PMECC parameters are indicated to the ROM code by writing a specific header at the beginning of the first page of the NAND Flash, just before the bootstrap. This header is built from a 32-bit word repeated 52 times. The ROM code selects the 32-bit word value with the most occurrences among the 52 values. This 32-bit word encodes precisely the memory geometry and PMECC initialization settings. Refer to the SAM9X7 data sheet, section “NAND Flash Boot: NAND Flash Detection” to get the exact layout of this 32-bit word.

2.3 SPI NOR Flash Boot

The ROM code can boot from SPI NOR Flash memories connected to any FLEXCOM interface that supports SPI, and if the SPI NOR Flash memories are compatible with either AT25, AT26 Serial Flash or AT45 DataFlash memories. Refer to the product data sheet, section “SPI Flash Boot” for more details.

2.4 QSPI NOR Flash Boot

The ROM code can boot from QSPI NOR Flash memories connected to QSPI.

Important: QSPI NAND Flash memories are not supported.

2.4.1 Software Reset of the QSPI NOR Flash Memory

QSPI limitations of the ROM code are fixed by:

1. raising the 4 I/O lines to high level during 12 QSPI clock cycles

2. sending a software Reset command sequence (66h, 99h)

before sending any other SPI command.

Step 1 causes the QSPI NOR Flash memory to exit its Continuous Read (XIP) mode, regardless of its manufacturer, whereas step 2 restores the Power-on Reset state, hence exiting the stateful 4-Byte Address mode.

Since the ROM code does not know the internal state of the QSPI NOR Flash memory (has it entered its SPI 4-4-4 mode?) when it tries to reset this memory, the ROM code first sends the reset command sequence (66h, 99h) with the SPI 4-4-4 protocol, to force an exit from the SPI 4-4-4 mode if needed, then sends the same reset command sequence but with the SPI 1-1-1 protocol. If the QSPI NOR Flash memory has not entered its SPI 4-4-4 mode, it should ignore the first Reset command sequence as it cannot decode it correctly.

Figure 2-1. Reset Command Sequence in SPI 4-4-4

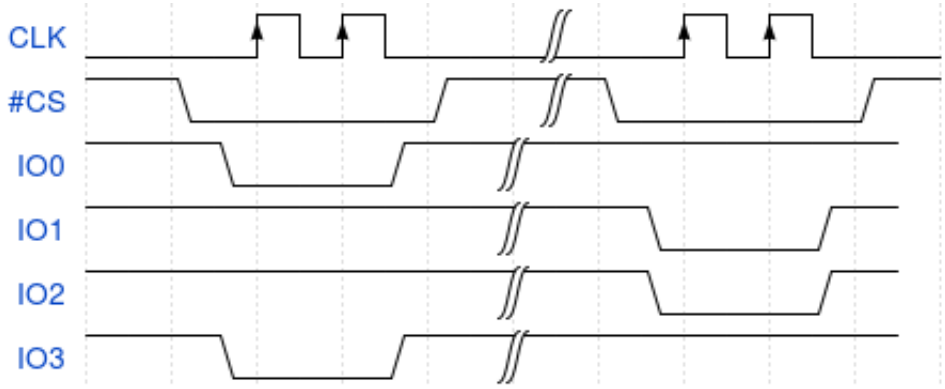
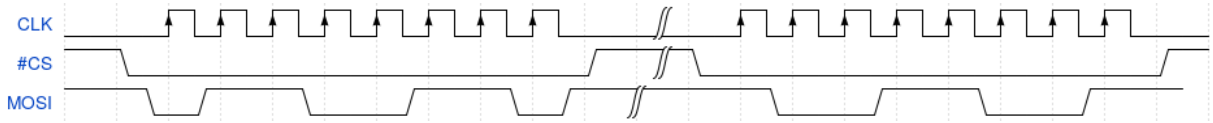


Figure 2-2. Reset Command Sequence in SPI 1-1-1



2.4.2 Probing the Read Parameters

The ROM Code relies on two mechanisms to probe any (Q)SPI NOR Flash memory connected to its QSPI controllers. First, the ROM code tries to read the Serial Flash Discoverable Parameters (SFDP) tables, hard-coded inside a ROM area of QSPI NOR Flash memories compliant with the JEDEC JESD216 specification, to learn all the required parameters to read data from those memories.

If and only if the ROM code fails to read valid SFDP tables, then it falls back into another hard-coded table stored inside the ROM code itself. To limit the size of this table in the ROM code, there is only one set of read parameters for each of the following JEDEC Manufacturer IDs:

- 01h (Spansion/Cypress)
- 20h (Micron)
- C2h (Macronix)
- EFh (Winbond)
- Others

2.4.3 Setting the Quad Enable (QE) Bit

For almost all memory manufacturers, the QE bit is non-volatile and must be set before performing any SPI command that requires the 4 I/O lines. This is the only persistent setting that the ROM code may change in the internal registers of the QSPI NOR Flash memory. All other settings are kept unchanged.

The procedure to set this QE bit is manufacturer-specific and may also change between different memory models of the same manufacturer.

Again, the ROM code first checks the SFDP tables to find out the right procedure. If no SFDP table is found, then the ROM code looks up in its own hard-coded table to get the procedure to be executed.

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More precisely, the ROM code reads bits[22:20] in DWORD15 from the Basic Flash Parameter Table (refer to JEDEC JESD216B specification) to select and then execute the relevant procedure, if any, to set the QE bit.

2.4.4 Supported QSPI Memories by Manufacturer

Table 2-1. Tested and Supported QSPI NOR Flash Memories (non-exhaustive)

Manufacturer	Memories
Microchip (SST)	SST26VF080B SST26VF016B SST26VF032B SST26VF032BA SST26VF064B
Micron	N25Q128A13 N25Q256A13 N25Q512A13 MT25QL01G
Macronix	MX25V4035FM2I MX25V8035FM2I MX25V1635FM2I MX25L3233FM2I-08G MX25L3273FM2I-08G MX25L6433FM2I-08G MX25L6473FM2I-08G MX25L12835FM2I-10G MX25L12845GMI-08G MX25L12873GM2I-08G MX25L25635MZ2I-10G MX25L25645GMI-08G MX25L25673GMI-08G MX25L51245GMI-08G MX25L51245GMI-10G MX66L1G45GMI-08G
Spansion/Cypress	S25FL127 (normal boot only; XIP fails) S25FL164 S25FL512

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3. Revision History

3.1 Rev. A - 03/2023

First issue.

Table of Contents

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