Designing an IEEE 802.3bt PoE System With PD77728

AN4896

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a Power over Ethernet (PoE) Power Source Equipment (PSE) system, based on Microchip's PD77728 PoE Controller/Manager. This document enables designers to integrate PoE capabilities (as specified in the IEEE® 802.3bt standards) into an Ethernet switch.

The PD77728 device is an 8-port, mixed-signal, and high-voltage PoE PSE device. The PD77728 supports up to Type 4, 90W output power per port. Any combination of 2-pair and 4-pair in the same system is possible and supported. Up to 12 PD77728 devices can be cascaded to provide 48, 4-pair ports.

The device supports PoE Powered Device (PD) detection, classification, power-up, and protection according to IEEE, and legacy/pre-standard PD detection. It provides real-time protection through mechanisms such as overload, under-load, over-voltage, over temperature, short-circuit, and enables operation in a standalone mode.

Microchip offers complete Evaluation Board (EVB)s. For an Evaluation Board recommendation or access to device datasheets or related application notes, consult your regional Microchip Client Engagement Manager or visit www.microchip.com/poe.

Firmware (without the boot section) and GUI are available on Microchip's Software Library.

For technical support, consult your local Embedded Solutions Engineers or go to www.Microchip.com/support.

Features

The PD77728 device and PD77728 based PSE have the following key features:

- Supported Standards
  - IEEE 802.3bt
- Supported PD Types
  - Type 1, Type 2 PDs (802.3af, 802.3at)
  - Single-signature (Type 1–4) PDs
  - Dual-signature (Type 3 and 4) PDs
  - Pre-standard (Legacy) 4-pair PDs
  - Supports non-compliant and legacy PDs
- Four Operational Modes
  - Controller mode in conjunction with PD77020 PSE Power Management Controller
  - Semi-Auto mode
  - Managed Auto mode
  - Unmanaged Auto mode
- Cascade up to 12 devices to support 96 × 2-pair ports or 48 × 4-pair ports and any 4-pair/2-pair combination
- Device Features
  - Stand-alone device supports up to 8 × 2-pair ports or 4 × 4-pair ports and any 4-pair/2-pair combination
  - Per-port integrated FET, sense resistor, and port diode
  - Total port resistance of 160 mΩ
  - Device power dissipation < 2W at full load
  - Two power rails (55V and 3.3V) for maximum power efficiency
  - Guaranteed 4-pair output power of > 90W
  - Over Supply Signal (OSS) support
  - AutoClass support
  - Supports Fast and Perpetual PoE
  - MarkHold function support
  - Host Interface through I^2C Communication
- Real-Time Protection (RTP)
- Measurements
  - Per-port voltage and current measurement
  - Accurate main power measurement
- Surge
  - Surge upto 2 kV per IEC61000-4-5-2014 without additional components
  - Surge compliance, ITU-T K.21, GR1089, IE61000-4-5-2014, EN55024
    - Up to 10 kV per IEC61000-4-5-2014
    - Up to 6 kV per ITU-T K21

- Physical Characteristics
  - Ambient temperature range –40℃ to 85℃
  - 56-pin 8 mm × 8 mm QFN package with thermal pad
  - MSL3, RoHS compliant

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1. Operational Modes

This section provides a high-level description of the following operational modes:

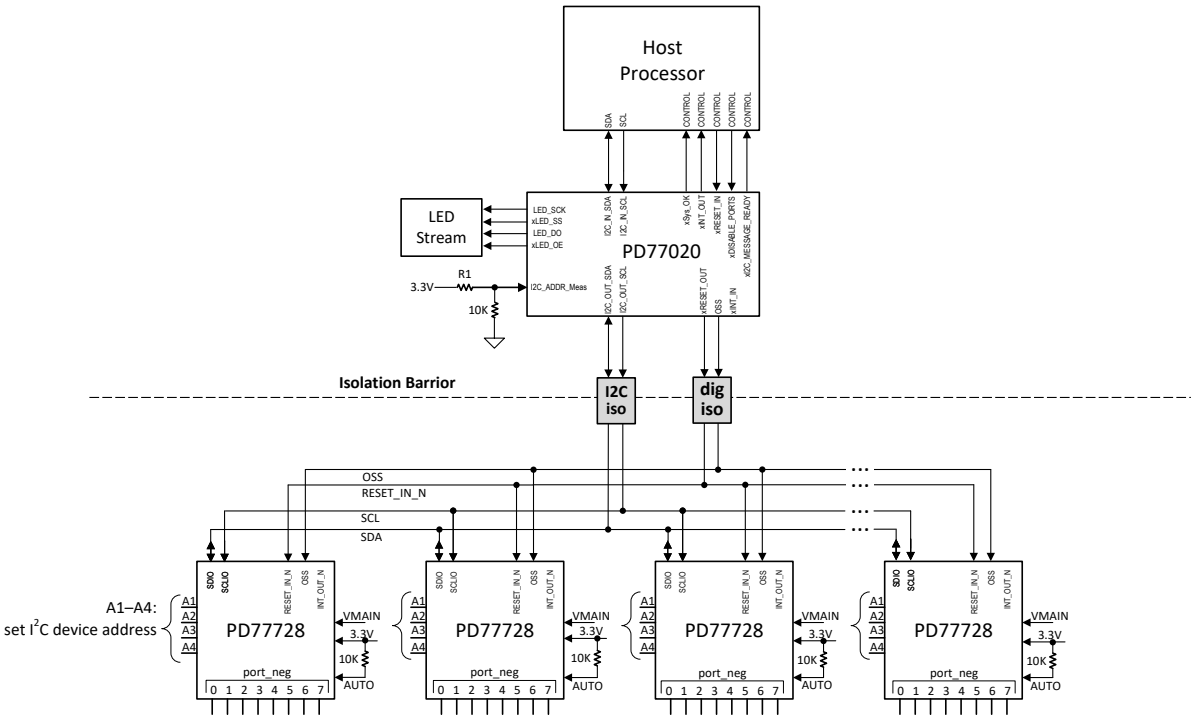
- Controller mode (with PD77020)
- Semi-Auto mode
- Managed Auto mode
- Unmanaged Auto mode

1.1 Controller Mode

This section describes the chipset operation with PD77020 PoE Power Management Controller. The PD77020 device is used in conjunction with the PD77728 device, where the PD77020 PoE Power Management Controller provides multi-port PoE functions, such as port mapping (Port Matrix), port priority, port status, and system power management.

The following figure shows the Controller mode application.

Figure 1-1. Controller Mode Application

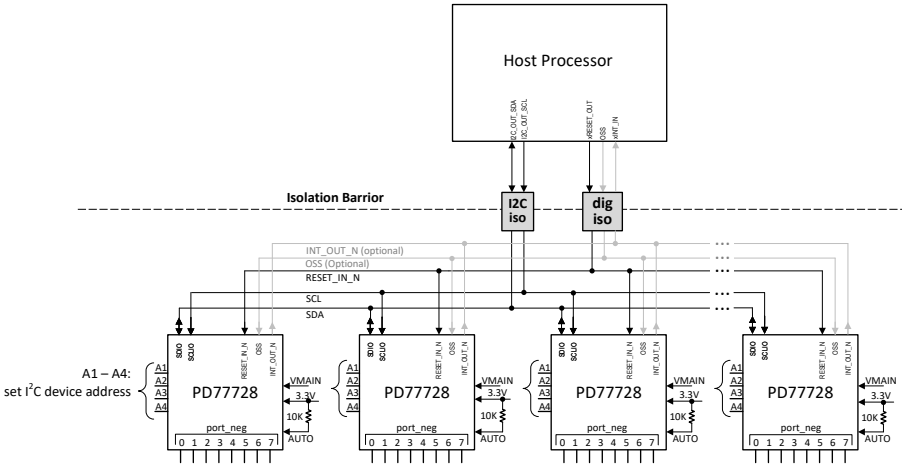


1.2 Semi-Auto Mode

In Semi-Auto mode, the device performs periodic connection check, detection, and classification, but does not power up ports without a host command. Each device has initial PSE configuration containing the Port Matrix (2P/4P configuration) and stores the port investigation results in memory for host control. The host can override these settings. In this mode, the PoE controller is responsible for the periodic or cyclic detection and classification of ports.

The following figure shows the Semi-Auto mode application.

Figure 1-2. Semi Auto Mode Application



Note: By disabling the auto mode, the PD77728 Controller/Manager can operate in semi-auto/controller mode. The auto mode is disabled when the voltage on pin 52 (AUTO) is greater than 2.096V as shown in Table 1-1.

1.3 Auto Mode

Auto mode is an operational mode where the PSE has the ability to perform the required functionality with predetermined configuration values. In this mode, the device performs connection check, detection, classification, and power-up autonomously following POR, and turning valid PoE ports ON without host intervention. A device supporting the Auto mode might either be connected to a host (1.3.1. Managed Auto Mode) or be used as a stand-alone system without any control interface (1.3.2. Unmanaged Auto Mode).

The following tasks are supported in the Auto mode:

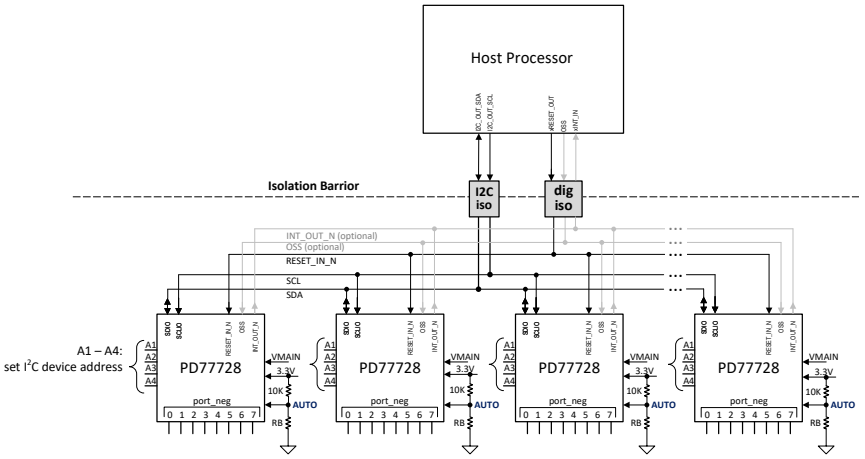
- Connection check, auto detection, classification, power-up, and power-on ports based on configuration pins
- Device-level matrix configuration

1.3.1 Managed Auto Mode

In Managed Auto mode, the device has initial PSE configuration with which the system can be operated without the host communication. However, the host communication is available which allows subsequent changes to the PSE configuration.

The following figure shows the Managed Auto mode application.

Figure 1-3. Managed Auto Mode Application

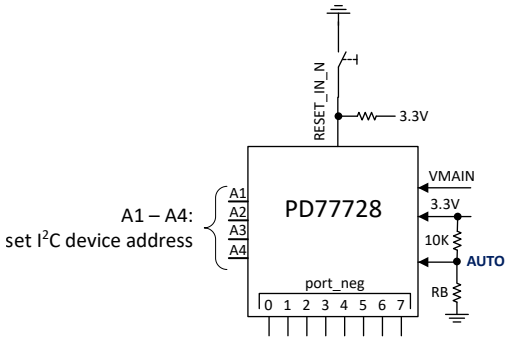


1.3.2 Unmanaged Auto Mode

In Unmanaged Auto mode, the device is a stand-alone system. The host I²C communication is not available to the device. All PSE configurations must be stored within the system and be available to the device(s) without the host communication. This is the typical application of a single device system. More than one device may be employed in this type of system, but each device operates interdependently of all other devices.

The following figure shows the Unmanaged Auto mode application.

Figure 1-4. Unmanaged Auto Mode Application



The following table lists the resistor RB values that are used to set the PSE type.

Table 1-1. AUTO Pin Configuration

Level	Level Range (V)	Mode	RB (kΩ 1%) Pin 52	Set Value (V)
0	0–0.278	Class 8	0.442	0.140
1	0.279–0.557	Class 7	1.47	0.423
2	0.558–0.847	Class 6	2.67	0.695
3	0.847–1.115	Class 5	4.22	0.979
4	1.115–1.393	Class 4-4P	6.19	1.262
5	1.394–1.693	Class 4-2P	8.87	1.551
6	1.694–1.951	Class 3-2P	12.4	1.827
7	1.951–2.23	Auto Mode disable	>17.4 or open	2.096

Note: A 10 KΩ resistor from 3.3V to AUTO pin is the top resistor value, RTOP, which along with RB creates the required voltage level at AUTO pin input.

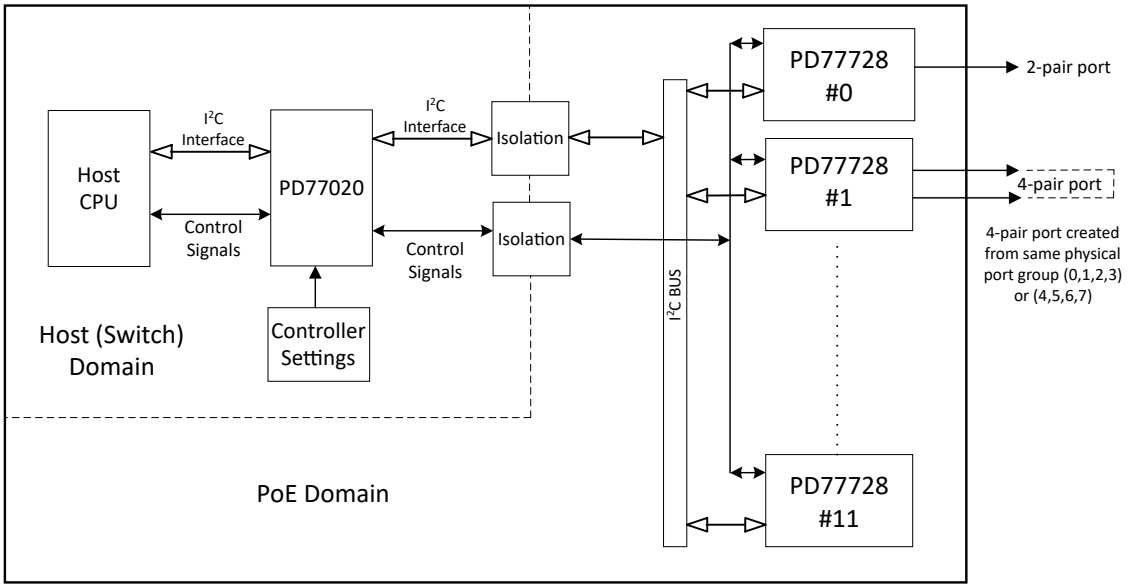
2. Functional Descriptions - Controller Mode

A typical application using the PD77020 Controller includes the following blocks.

- PoE circuit support 96 x 2-pair ports or 48 x 4-pair ports, based on up to 12 PD77728 devices as shown in the following figure.
- PD77020 Controller used to initialize, control, and monitor each PD77728 through an isolated I²C bus.
- Isolation circuit for control signals between PD77020 and PD77728 devices.

These blocks are shown in the following figure.

Figure 2-1. Controller Mode Block Diagram



2.1 Communication Interfaces

Two communication interfaces are available: an interface between the Host CPU and the PD77020 Controller and an interface between the PD77020 Controller and PD77728 PoE Controller/Managers.

Communication between the Host CPU and the PD77020 is performed through a non-isolated I²C interface. The Host CPU issues commands utilizing a dedicated serial communication protocol to the PoE controller. For more information, see the *PD77020 Serial Communication Protocol User Guide*.

Communication between the PD77020 and the PD77728 devices is via an I²C interface with 1500 V_{RMS} isolation. Isolation is a basic requirement of IEEE PoE standards. Each side of the isolator circuitry is fed by a separate power supply.

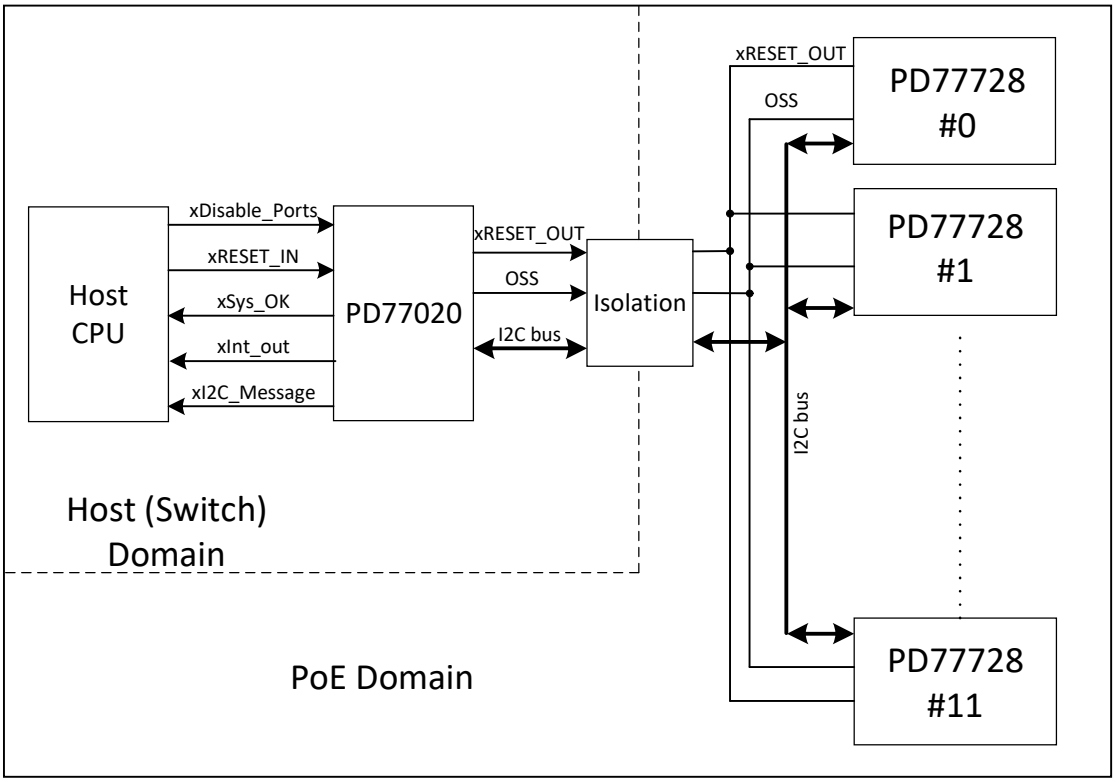
Additionally, several signals are connected between the Host CPU and the PoE controller for control and indication functions.

Note: The I²C clock (SCL) is uni-directional signal whereas I²C data (SDA) is bi-directional signal. The PD77728 supports I²C clock frequencies up to 1 MHz.

2.1.1 Host–PoE Controller Control Signals

Control signals are single hardware lines that run between the Host CPU and the PD77020 device, as shown in the following figure.

Figure 2-2. Control and Indication Signals



xDISABLE_PORTS: Control signal driven by the Host CPU disables all PoE ports. When the PD77020 Controller detects a low level voltage at xDISABLE_PORTS, it sends a disable command through the I^2C bus to all the PD77728 PoE Controller/Manager ports. The xDisable_ports pin of PD77020 is active-low.

xRESET_IN/OUT: Control signal driven by the Host CPU resets the PD77020 PoE Controller and all the PD77728 PoE Controller/Managers. When the PD77020 device detects a low-level voltage at xRESET_IN, it enters reset mode and all of its output pins switch to tri-state mode. When Reset returns to high, the PoE controller initializes and sends a RESET command (xRESET_OUT) to the PD77728 PoE managers through the isolation circuit. Connect a 10 KΩ pull-up resistor to reset signal on both the sides of the isolation block. A 47 nF filter capacitor must be connected between this pin and GND and located close to the device.

In case the Host drives the xRESET_IN pin from a push-pull output, a 1.5 KΩ resistor must be located between the Host's output and the PD77020 xRESET_IN pin 26.

xSYS_OK: Signal is generated by the PD77020 PoE Controller, indicating that the main input voltage is within range. This pin is determined by a 15-byte serial communication protocol. This pin is active-low.

xINT_OUT: Interrupt output indication. This line is asserted low when a preconfigured event is in progress. The Host configures the event that must generate an interrupt through the 15-byte protocol. When this event occurs, the xINT_OUT pin is asserted. This pin is active-low.

xI2C_MESSAGE: I^2C message ready for reading by the host. The PD77020 Controller asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I^2C read cycle only when the message is ready. This pin is active-low. After the host reads the data from the controller, this pin is asserted high.

OSS: OSS is a control pin required to turn off ports of a certain priority due to failure in one of the power supplies. A dedicated fast shut-down bus is present internal to the PD77728 device to allow fast shut-down response to the OSS signal. Both 1-bit signal priority and 3-bit signal priority are supported.

For a detailed description of OSS operation, see the *PD77728 Device Data Sheet*.

2.2 Powering

The following sections describe powering.

2.2.1 PD77020 Supply

The PD77020 PoE Controller requires a stable, filtered power for its operation coming from the system 3.3V supply in the Host Domain (3_3V_iso), so a number of decoupling capacitors are included in the design. The expected current consumption of the PD77020 PoE controller circuitry is below 20 mA.

Additionally, the PD77020 internal 1.2V VDD_CORE voltage requires decoupling capacitors. These decoupling capacitors must be layout close to pin 29 VDD_CORE.

2.2.2 PD77728 Supply

The PD77728 requires a stable 3.3V, filtered power supply in the PoE domain for operation. Connect this power supply to VDD, pin 43. The VDDA, pin 22 must be connected with a single point connection to VDD close to pin 43 and not to PCB VDD general plane, see Figure 8-6. There must be decoupling capacitors placed close to both VDD and VDDA pins. The expected current consumption is below 30 mA.

Additionally, PD77728 1.8V (VREG1P8) and 1.2V (VDDCORE) internal voltage regulators require decoupling capacitors. These decoupling capacitors must be placed close to the respective pins.

2.2.2.1 PD77728 3.3V

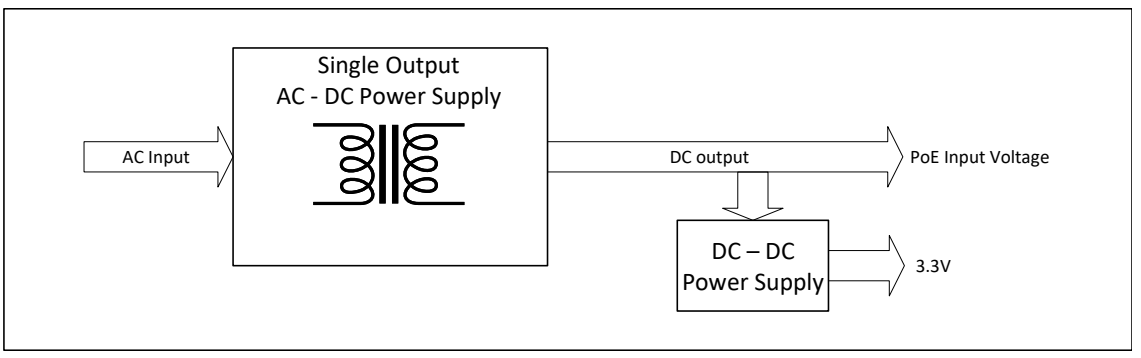
This section discusses different options for generating 3.3V power supply for PD77728, the output current ranges from 30 mA (single PD77728 device) to 360 mA (maximum 12 PD77728 devices).

A front-end AC-DC power supply is used to generate the PoE input voltage (50V to 57V). Off-the-shelf AC-DC power supplies are available with and without auxiliary/standby outputs.

2.2.2.1.1 Case - 1: AC-DC Power Supply without Auxiliary Output

When a single output AC-DC power supply is used, a DC-DC converter should step down the available PoE input voltage to 3.3V.

Figure 2-3. Single Output AC - DC Power Supply



Microchip offers several Buck controllers/regulators for stepping down input PoE to 3.3V. The Buck regulators are preferred over Buck controllers as the power switch (MOSFETs) are integrated into the silicon.

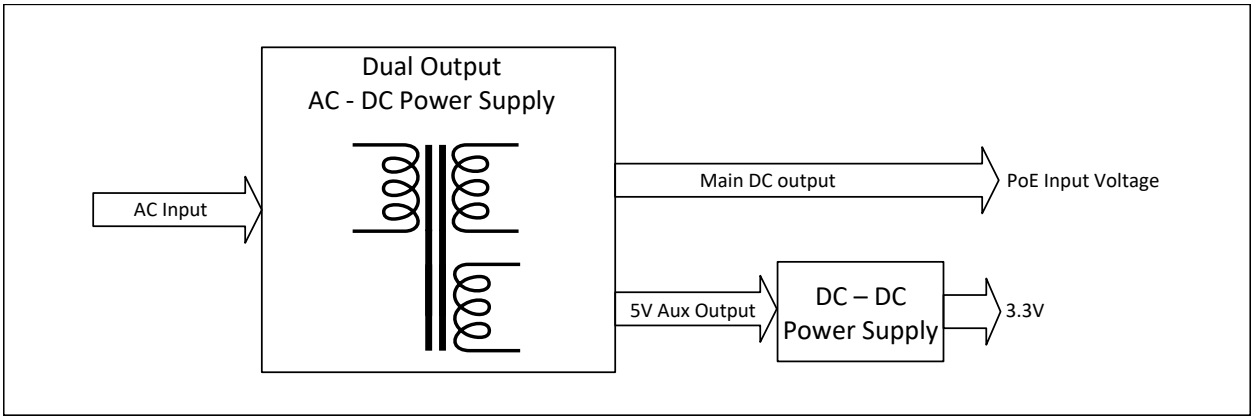
The MIC28512-1 , a synchronous step-down switching regulator with internal power switches, based 3.3V DC-DC converter is recommended when there is no auxiliary DC output available on the AC-DC power supply. A 3.3V DC-DC converter rated for 360 mA designed based on MIC28512-1 is shown in Figure 6-9 and the corresponding BOM is shown in Table 7-6. This design is adequate to power 12 PD77728 devices.

In addition to Buck controllers/regulators, Microchip offers high voltage Linear regulators to step down the input PoE to 3.3V such as LR12 and MIC5283. These LDO regulators can be used in low port count or single PD77728 IC applications, where a lower supply current is required. With an LDO solution, care must be taken to ensure adequate thermal performance.

2.2.2.1.2 Case - 2: AC-DC Power Supply with Auxiliary Output

When an AC-DC power supply with 5V Auxiliary/Standby output is used, a DC-DC converter is used to step down the 5V auxiliary output to 3.3V.

Figure 2-4. Dual Output AC - DC Power Supply



Here is an example of an AC-DC with 5V/2A standby: Module Power Supply

Microchip offers several Buck regulators, Power modules and LDO voltage regulators for stepping down the 5V to 3.3V.

The table below shows the high level comparison of the three solutions.

Table 2-1. High-level Comparison of Different Solutions

Category	Cost	Efficiency	PCB Area	Regulator Type
Buck Regulators	Moderate	High	High	Switching regulator
Power Modules	High	Moderate	Moderate	Switching regulator
LDO voltage regulators	Low	Low	Low	Linear regulator

Various Microchip offering are shown in the following table.

Table 2-2. Microchip 3.3V Regulators

Type	Product	Current
Power Module	MIC33030	400 mA
Power Module	MIC33050	600 mA
Buck Regulator	MIC23050	600 mA
Buck Regulator	MIC23030	400 mA

.....continued		
Type	Product	Current
Buck Regulator	MIC23031	400 mA
LDO Voltage Regulator	MIC5501	300 mA
LDO Voltage Regulator	MIC5365	150 mA
LDO Voltage Regulator	MIC5528	500 mA

2.2.3 Main Supply

The PoE system operates within a range of 44 V_{DC} – 57 V_{DC} (IEEE 802.3at/bt V_{MAIN} range is 50 V_{DC}–57 V_{DC}). To comply with UL SELV regulations, the maximum output voltage must not exceed 60 V_{DC}.

The main PoE power supply is connected at V_{MAIN} pin 17. For basic levels of protection (</= 2kV) connect the PoE power supply to both VMAIN_7 pin 7 and VMAIN_36 pin 36. For Enhanced levels of protection (>2 kV) leave pin 7 and 36 floating. For more information, request for *AN4813 Surge Protection for Systems Based on PD77728 8-Port PSE PoE Controller/Manager*.

2.2.4 Hot-Swap Circuit

The hot-swap circuit is crucial for applications where DC hot plug is present because absence of such a circuit causes the DC voltage to oscillate (ring), which may lead to application malfunctions.

The hot-swap circuit based on MIC2587 for a system with 12 PD77728 devices is shown in Figure 6-10 and Table 7-7. Consult Microchip for an option based on a discrete solution.

2.2.5 Grounds

Several grounds are utilized in the system: PoE domain analog (AGND) and local analog (LAGND), PoE domain digital (DGND) and local digital (LDGND), chassis, and host domain floating. See Figure 8-6 and Figure 8-9.

AGND: The negative rail of input PoE is termed as AGND. Connect only PD77728 device EPAD to AGND.

LAGND: Quiet local AGND use for each individual PD77728 to have a low current quiet connection to IREF (pin 14), VMAIN (pin 17), and VDDA (pin 22) decoupling capacitors. To avoid current loops, LAGND must be connected in a single point to AGND near the PD77728 EPAD. LAGND must be connected to DGND via a 470 nF and 1 nF capacitor and optional back to back diodes. See Figure 8-6.

DGND: The ground connection used for PD77728 digital signals (pins 43 to 56) is DGND. The decoupling capacitors connected to VDD and VDDCORE pins are connected to DGND.

LDGND: The ground connection for VREG1P8 decoupling capacitors is LDGND. Connect LDGND and DGND at single point.

All these grounds—AGND, LAGND, DGND, and LDGND—are the same ground, electrically. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

The power supplies AGND ground connector enables a current path back to the power supply. The ground connection must be capable of carrying all current back to power supplies.

Host Domain Floating: The PD77020 PoE controller relates to the host domain floating ground, which is isolated from the PoE domain grounds.

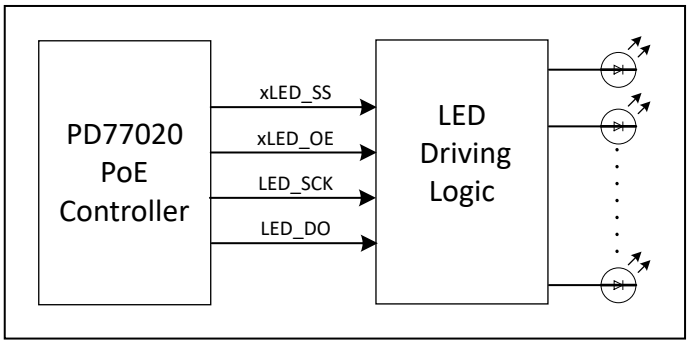
Chassis Ground: The chassis ground is connected to the switch's chassis ground. This ground plane must be 1500 V_{RMS} isolated from PoE circuitry.

2.3 LED Support

LED support for port status indication is accomplished by utilizing the LED_SCK, xLED_SS, LED_DO, and xLED_OE signals on the PD77020 controller. Bus behavior is 1 MHz synchronous serial communication (clock and data) in one direction (write only) that transmits the status up to 48 logical ports.

The following figure shows the LED support.

Figure 2-5. LED Support



2.4 Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended that each power supply is capable of generating a logic signal, indicating its operate/fail status.

The following table lists the PD77020 pins used for emergency power management.

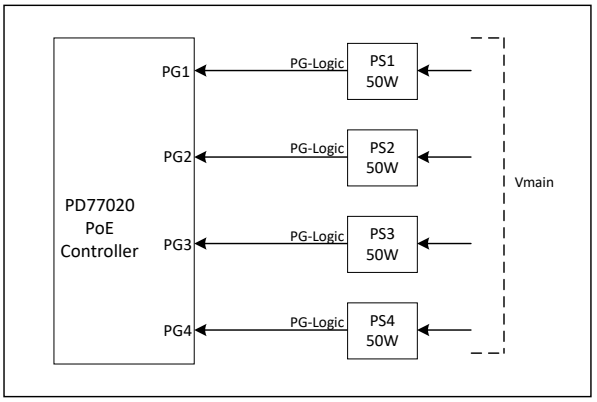
Table 2-3. Emergency Power Management Pins

PD77020 Pin Number	Signal	Description
17	PG1	Power Good 1
18	PG2	Power Good 2
19	PG3	Power Good 3
20	PG4	Power Good 4

The PoE circuit allocates power to the system in 16 programmed power levels (power banks). Power bank values are based on each supplies' available power and on the state of the logic signals PG[1..4] coming from power supplies. If PG pin is not used, the pin must be connected to GND or VDD.

The following figure shows the connections between the logic signals of the power supplies and the PoE manager.

Figure 2-6. Power Good



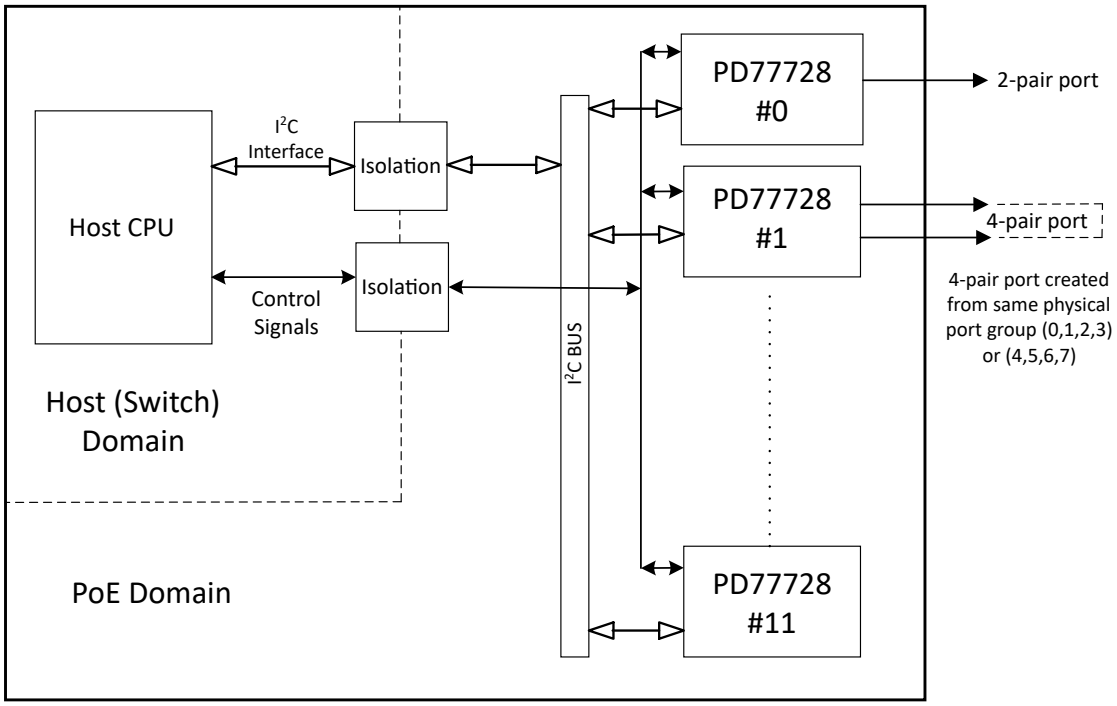
Note: The system V_{MAIN} capacitor must hold the voltage from dropping for 50 µs until the emergency power management reacts.

3. Functional Descriptions - Auto and Semi-Auto Mode

The following figure shows a typical managed auto/semi-auto mode application including the following blocks.

- PoE circuit, either 4-pair or 2-pair, based on PD77728 Controller/Manager.
- Host CPU, used to initialize, control, and monitor each of PD77728 through isolated I²C bus.
- Isolation circuit for I²C interface, control signals (RESET and OSS signals) between Host CPU and PD77728 devices.

Figure 3-1. Managed Auto/Semi-Auto Mode Block Diagram



Note:
Host CPU is present in managed auto/semi-auto modes only. There is no host device in unmanaged auto-mode. For more information, see 1.3.2. Unmanaged Auto Mode.

3.1 Communication Interfaces

The Host CPU communicates with the PD77728 device(s) via an I²C interface with 1500 V_{RMS} isolation. Isolation is a basic requirement of IEEE PoE standards. Each side of the isolation circuitry is fed by a separate power supply. The Host CPU issues commands, utilizing a dedicated serial communication protocol to the PD77728 Controller/Manager.

Additionally, there are several signals connected between the Host CPU and the PD77728 device for control and indication functions.

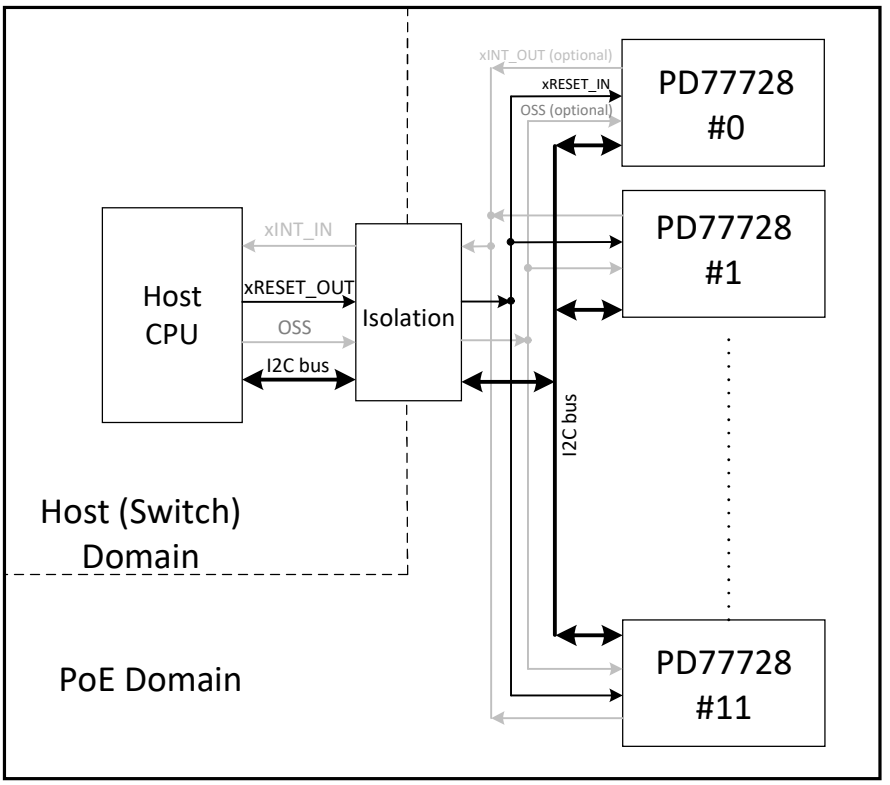
The PD77728 port I²C address is programmed through pins A1, A2, A3, and A4 (pins 48–51). For more information, see Table 4-1.

Note: The I²C clock (SCL) is uni-directional signal whereas, I²C data (SDA) is bi-directional signal. The PD77728 supports I²C clock frequencies up to 1 MHz. The I²C clock stretch is not required by the Host CPU, while communicating with the PD77728 device.

3.1.1 Host–PD77728 Control Signals

Control signals are single hardware lines that run between the Host CPU and the PD77728 device.

Figure 3-2. Control Signals – Managed Auto/Semi-Auto Mode



xRESET_IN: Control signal driven by the Host CPU resets all the PD77728 PoE Controller/Managers. When the PD77728 device detects a low-level voltage at xRESET_IN, it enters RESET mode and all of its output pins switch to tri-state mode. Connect a 10 KΩ pull-up to xRESET_IN pin of PD77728. A 47 nF filter capacitor must be connected between this pin to GND, close to the device. In case the host drives the RESET pin from a push-pull output, a 1.5 KΩ resistor must be located between the host's output and the PD77728 xRESET_IN.

OSS: OSS is an optional control pin enables to turn off ports of a certain priority due to failure in one of the power supplies. A dedicated fast shut-down bus is present internal to the PD77728 device to allow fast shut-down response to the OSS signal. Both 1-bit signal priority and 3-bit signal priority are supported.

xINT_OUT: Interrupt output indication. This line is asserted low when a preconfigured event is in progress. The host configures the event that must generate an interrupt through the 15-byte protocol. When this event occurs, the xINT_OUT pin of PD77728 is asserted. This pin is active-low. If unused, leave PD77728 xINT_OUT pin unconnected.

3.2 PD77728 Powering

For information on PD77728 powering, see 2.2.2. PD77728 Supply, 2.2.3. Main Supply, 2.2.4. Hot-Swap Circuit, and 2.2.5. Grounds.

4. PoE Manager Circuitry

The PD77728 performs a variety of internal operations and PoE functions, requiring a minimal number of external components.

4.1 PD77728 Circuitry

The PD77728 performs a variety of internal operations and PoE functions, requiring a minimal number of external components. For PD77728 device configuration in Auto and Semi-Auto Modes (without PD77020), see 6.1. Managed Auto and Semi-Auto Modes. For PD77728 device configuration in Controller mode, see 6.2. Controller Mode.

4.1.1 Reference Current Source

The reference for internal voltages within the PD77728 is set by a precision resistor, 10 kΩ. The resistor precision must be 0.1%.

4.1.2 Port Channel Resistance

The total channel resistance of a PD77728 port is 160 mΩ (typical). This resistance includes sense resistor and MOSFET $R_{DS(on)}$.

4.1.3 Front-End Components

A front-end, per-line capacitor is required. The capacitor value can be between 47 nF and 220 nF. Using 220 nF is recommended to improve the PSE immunity to 50 Hz/60 Hz noise. All other components such as reverse diode, port protection, sense resistor, and switching MOSFET are internal.

4.1.4 PD77728 I²C Address Select

The port I²C address is programmed through pins A1, A2, A3, and A4 (pins 48–51). Tie each pin to VDD or DGND, as listed in the following table, to set the I2C address.

Note: The I²C address is a 7-bit address.

Table 4-1. I²C Address Select

A4	A3	A2	A1	Ports	I²C Address
0	0	0	0	0–3	0x20
				4–7	0x21
0	0	0	1	0–3	0x22
				4–7	0x23
0	0	1	0	0–3	0x24
				4–7	0x25
0	0	1	1	0–3	0x26
				4–7	0x27
0	1	0	0	0–3	0x28
				4–7	0x29
0	1	0	1	0–3	0x2A
				4–7	0x2B
0	1	1	0	0–3	0x2C
				4–7	0x2D
0	1	1	1	0–3	0x2E
				4–7	0x2F

.....continued					
A4	A3	A2	A1	Ports	I²C Address
1	0	0	0	0–3	0x30
				4–7	0x31
1	0	0	1	0–3	0x32
				4–7	0x33
1	0	1	0	0–3	0x34
				4–7	0x35
1	0	1	1	0–3	0x36
				4–7	0x37
1	1	0	0	0–3	0x38
				4–7	0x39
1	1	0	1	0–3	0x3A
				4–7	0x3B
1	1	1	0	0–3	0x3C
				4–7	0x3D
1	1	1	1	0–3	0x3E
				4–7	0x3F

4.2 Line Transformer

A line transformer that is dedicated to PoE (with consideration to the desired PoE current for the specific applications) must be used.

5. 4-Pair Ports for IEEE 802.3bt

This section describes the basic steps to configure PSE systems to support IEEE 802.3bt 4-pair applications based on the PD77728 device.

5.1 Background

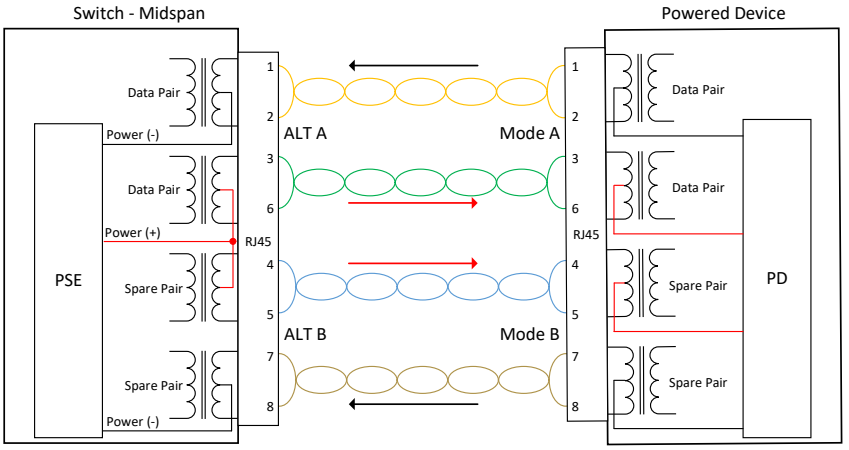
The IEEE 802.3af standard describes Power Source Equipment (PSE) power of 15W over 2-pair and the IEEE 802.3at standard describes PSE power of 30W over 2-pair. To increase the maximum PoE power supplied by the PSE to the Powered Device (PD), 4-pair ports utilize all four pairs of the structured RJ45 wires.

The IEEE 802.3bt-2018 standard, introduced the Type 3 and Type 4 PSE/PD capable of supporting 60W/90W output power using two PSE ports on all wires of the RJ45 cable.

The PD77728 supports up to 45W per 2-pair or 90W per 4-pair (Type 3 or Type 4).

The Data Pair is defined as **Alternative A** at the PSE side and **Mode A** at the PD side. The Spare Pair is defined as **Alternative B** at the PSE side and **Mode B** at the PD side. This is illustrated in the following figure.

Figure 5-1. PoE 4-Pair Architecture



5.2 Hardware Setup

The following sections describe how to set up the hardware.

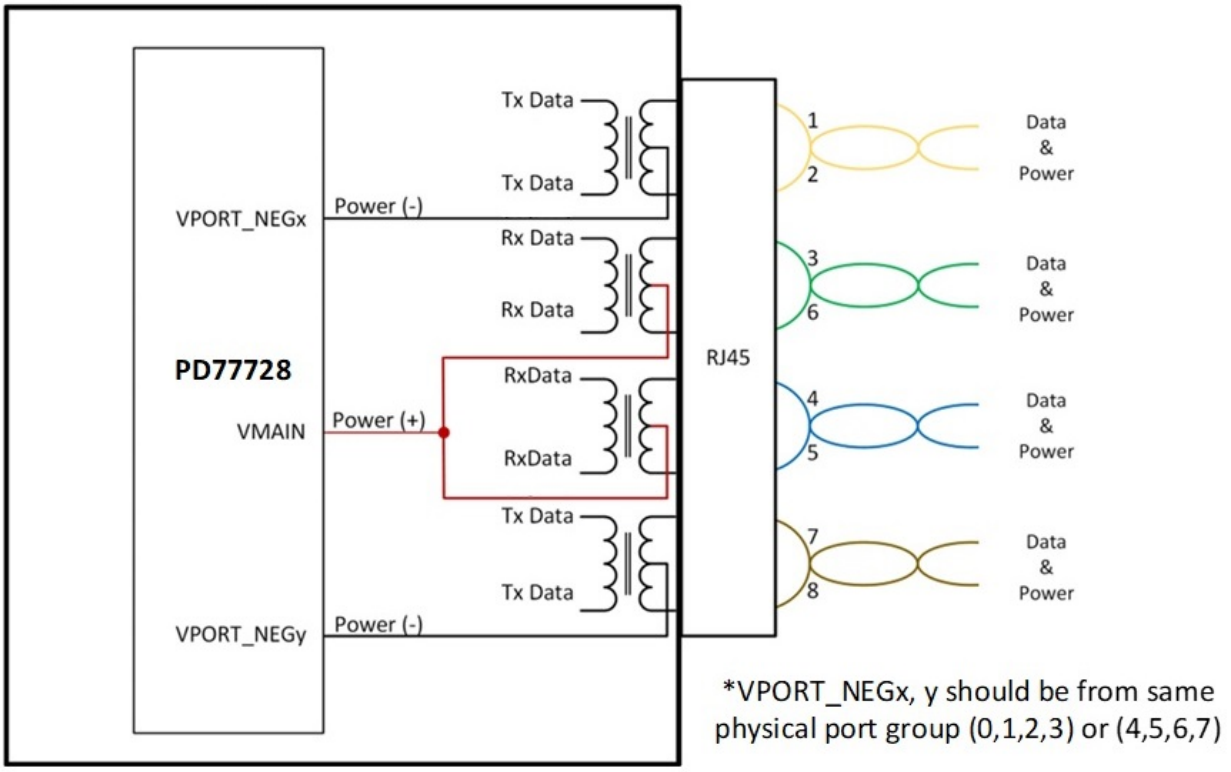
5.2.1 PSE

When operating in 4-pair, power is delivered to the PD on both pair sets (ALT-A and ALT-B), that is, two physical ports are combined to create a single logical 4-pair port required for the 4P operation. When operating in 4P mode, the two physical ports that create the one logical four pair port must be chosen from the same physical PD77728 IC. In addition, the logical 4P port must be created from the same physical port group (0, 1, 2, 3) or (4, 5, 6, 7). For example, a logical 4P port from physical ports 0 and 3 is allowed, but a logical 4P port from physical ports 0 and 4 is not allowed.

Note: To clarify, physical port 0 of PD77728 means PORT_NEG0 (pin# 3) and physical port 1 means PORT_NEG1 (pin #5) and so on.

This configuration is shown in the following figure.

Figure 5-2. 4-Pair Implementation



5.2.2 Polarity

Type 4 is limited to a “fixed polarity”, that is the IEEE 802.3bt strictly defines the connection of the positive V_{MAIN} voltage and return (PORT_NEG) paths to the physical pairs. For Type 3 applications, the standard is flexible allowing a variety of connection options. See the following table.

Table 5-1. Allowed Polarity

Pair Set	TIA/EIA 568-A	TIA/EIA 568-B	Alternative	Type 3			Type 3 or Type 4
1–2	Green	Orange	Data (Alt A)	PORT_NEGx	VMAIN	VMAIN	PORT_NEGx
3–6	Orange	Green		VMAIN	PORT_NEGx	PORT_NEGx	VMAIN
4–5	Blue	Blue	Spare (Alt B)	PORT_NEGy	PORT_NEGy	VMAIN	VMAIN
7–8	Brown	Brown		VMAIN	VMAIN	PORT_NEGy	PORT_NEGy

5.2.3 PD Side

The following figures describe how to physically connect 4-pair ports to a Signal Signature PD and how to physically connect to a Dual Signature PD.

Figure 5-3. PD 4-Pair SSPD Implementation

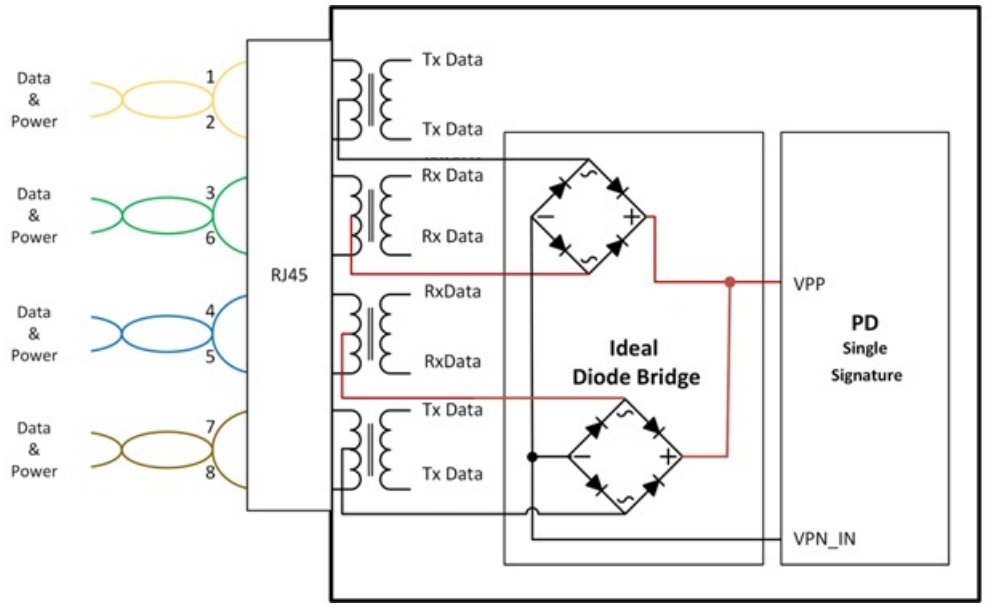
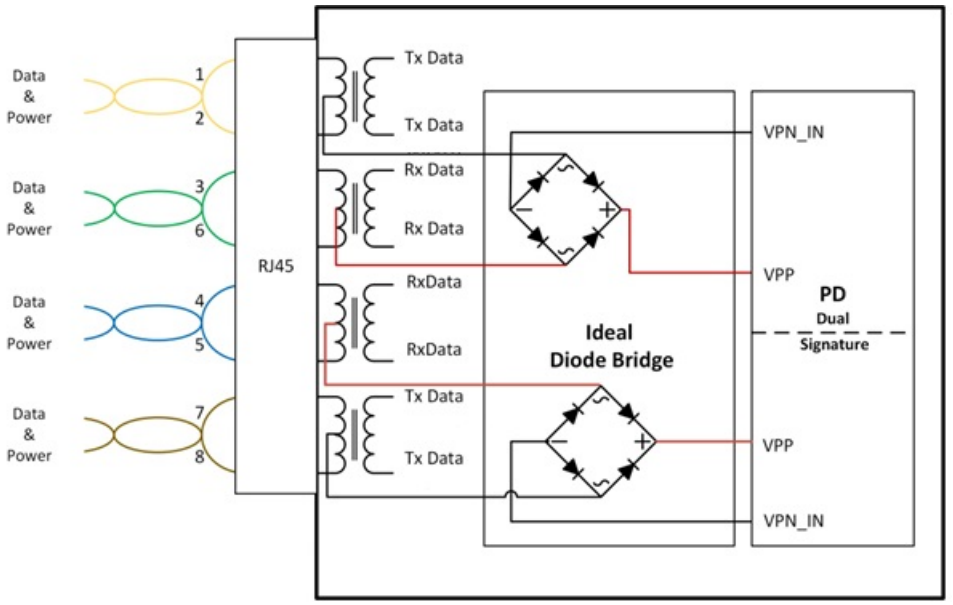


Figure 5-4. PD 4-Pair DSPD Implementation



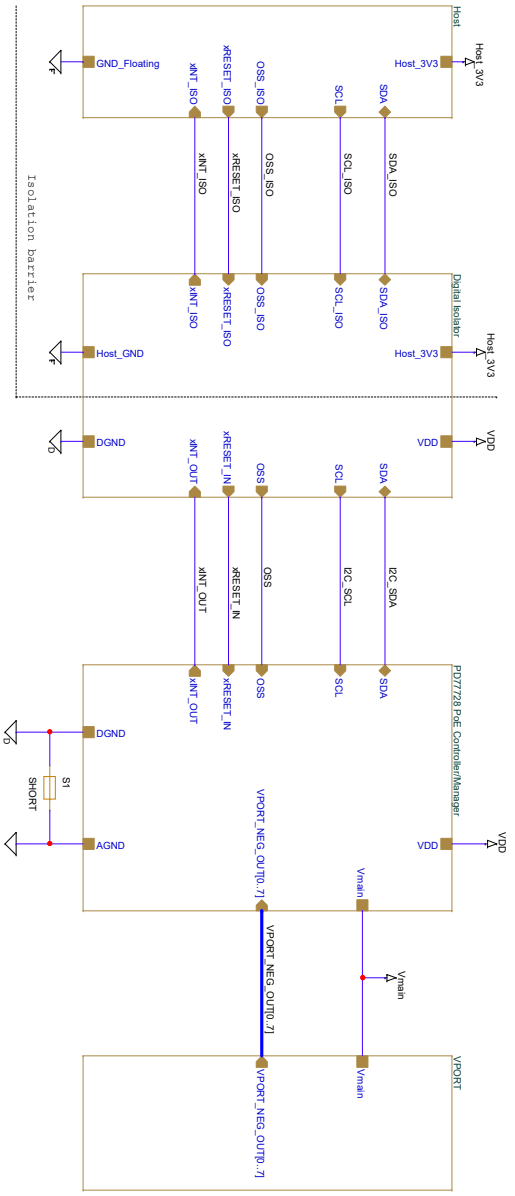
6. Schematics

The following section shows the detailed device-level schematic for various Operating Modes.

6.1 Managed Auto and Semi-Auto Modes

The following section shows the detailed device-level schematic of a 4-physical port system based on one PD77728 device, operating in Auto and Semi-Auto Modes. This schematic meets 2 kV basic surge requirements as defined in EN 61000-4-5:2014. For a higher level of surge protection, request for *AN4813: Surge Protection for Systems Based on PD77728 8-Port PSE PoE Controller/Manager*.

Figure 6-1. System Main Blocks – Auto and Semi-Auto Modes



The following figure shows the PD77728 Controller/Manager circuitry.

Figure 6-2. 8-Port PoE Controller/Manager Circuitry – Auto and Semi-Auto Modes

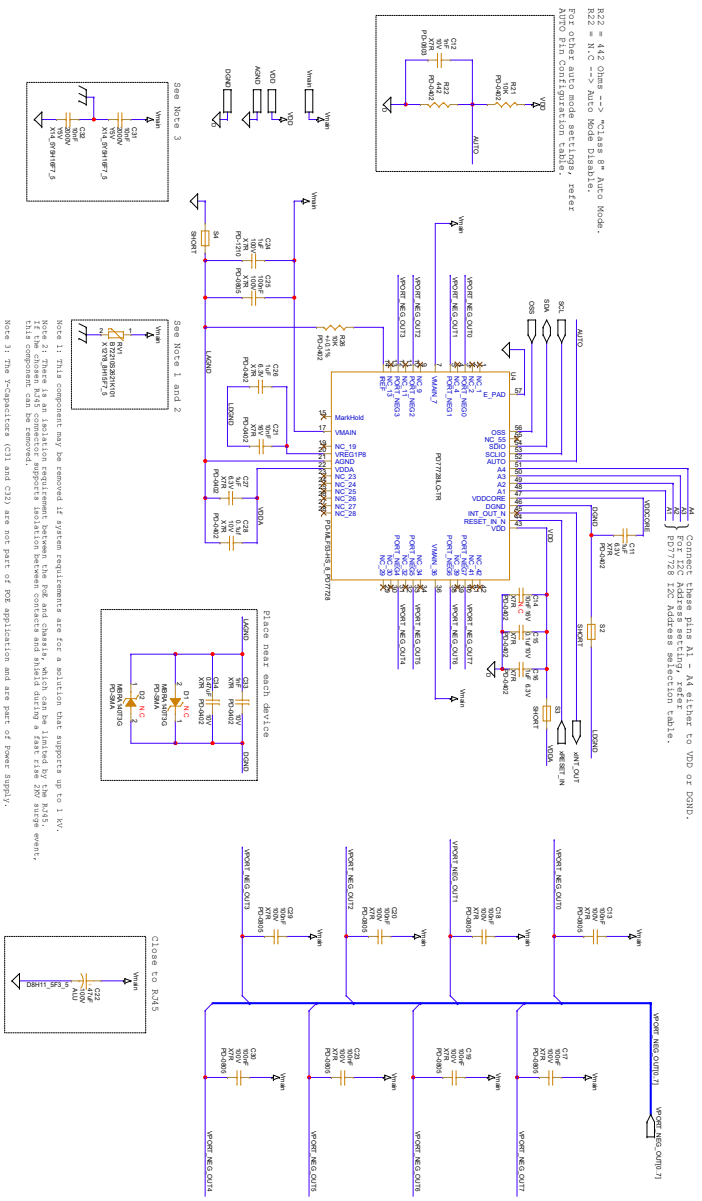
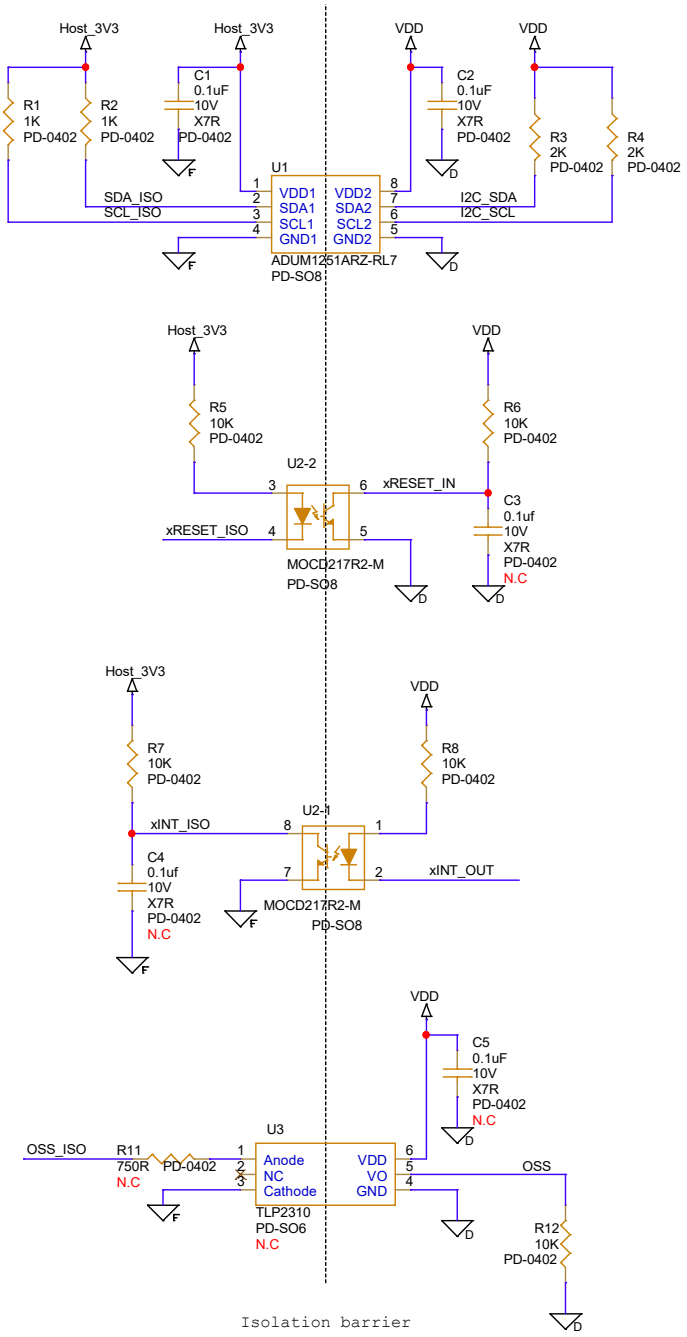


Figure 6-3. Digital Isolator Circuitry



6.2 Controller Mode

The following section shows the detailed device-level schematic of a 8-physical port system based on two PD77728 device, operating in Controller Mode. This schematic meets 2 kV basic surge requirements as defined in N 61000-4-5:2014. For a higher level of surge protection, request for *AN4813: Surge Protection for Systems Based on PD77728 8-Port PSE PoE Controller/Manager*.

Figure 6-4. System Main Blocks – Controller Mode

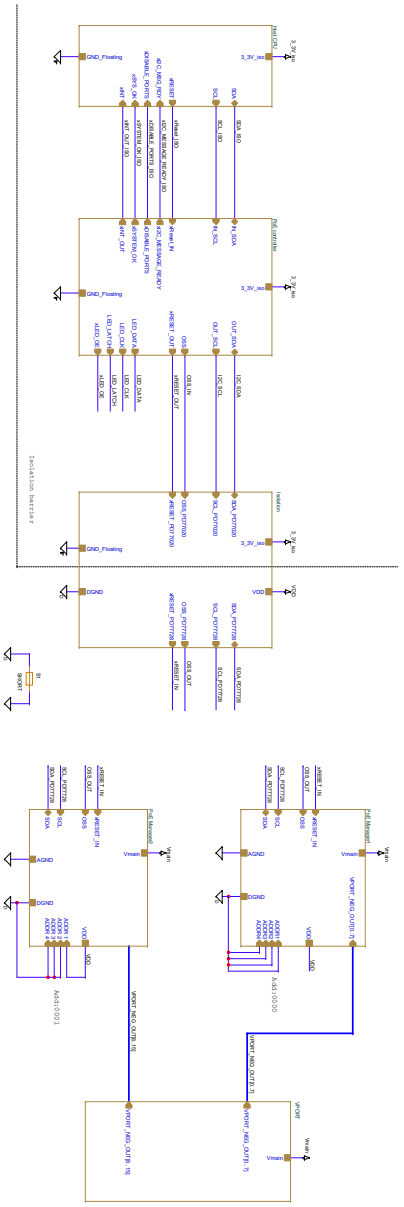


Figure 6-5. PD77020 Controller Circuitry - Controller Mode

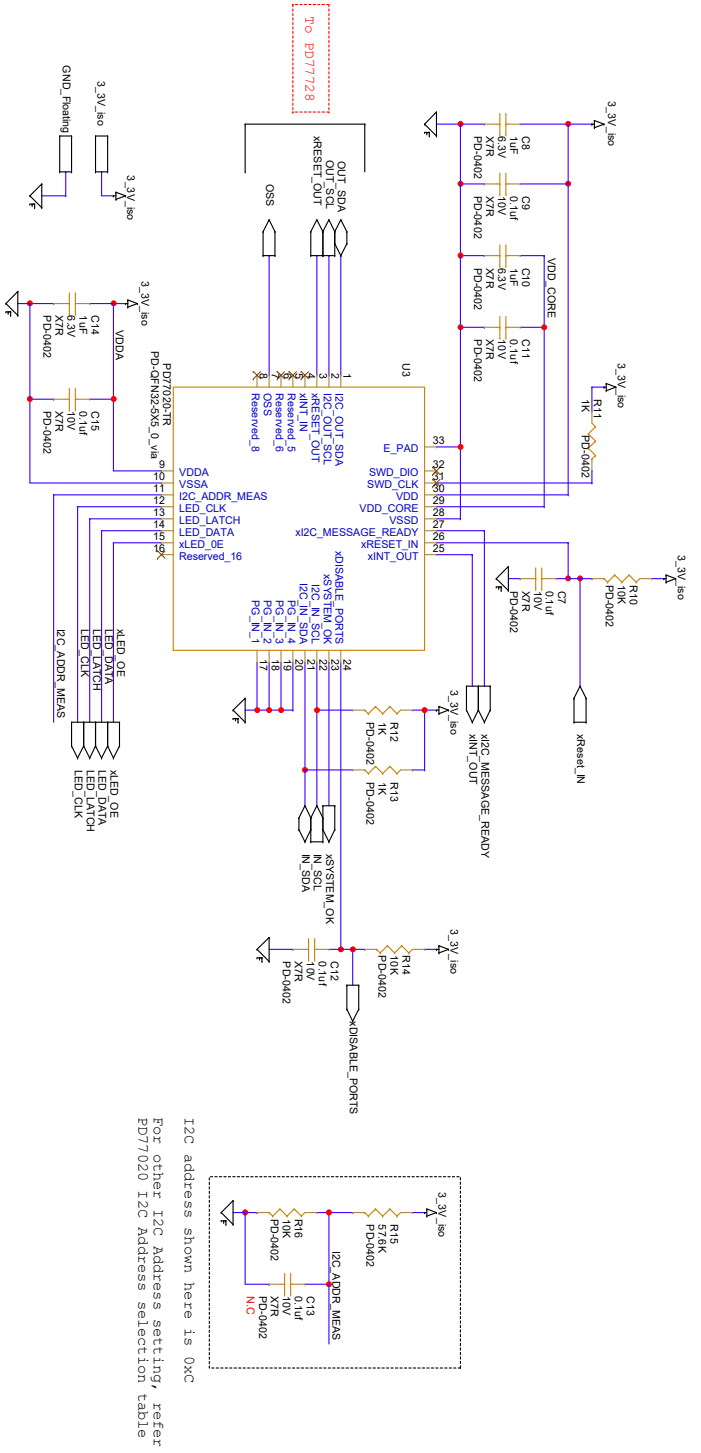
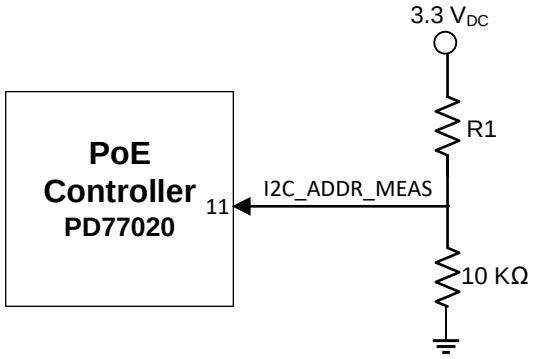


Figure 6-6. PD77020 I²C Address Selection



The following table lists the specific value of R1 to set the I²C address.

Table 6-1. PD77020 I²C Address Selection

I²C Address (Hexadecimal)	R1–KΩ (1%)
0x4	147
0x8	86.6
0xC	57.6
0x10	43.2
0x14	34
0x18	26.7
0x1C	22.1
0x20	18.2
0x24	15.4
0x28	13
0x2C	11
0x30	9.31
0x34	7.87
0x38	6.49
0x3C	5.49

Figure 6-7. PD77728 Controller/Manager Circuitry - Controller Mode

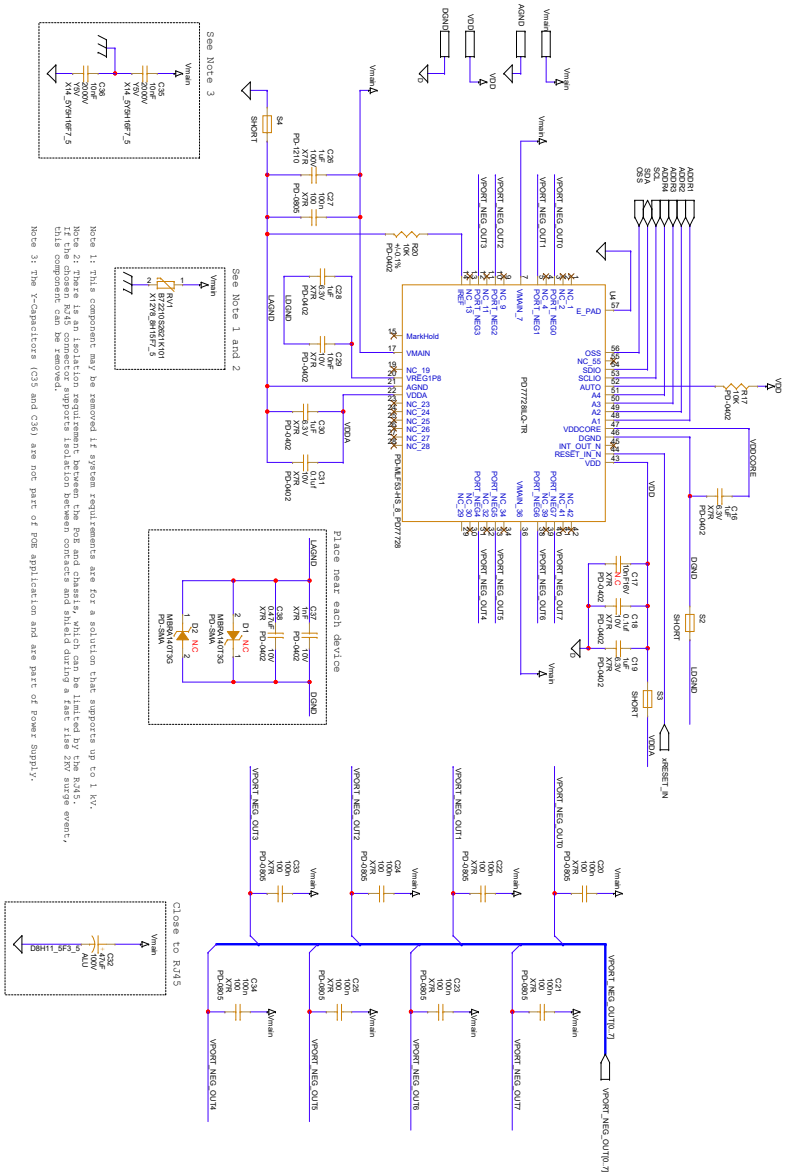
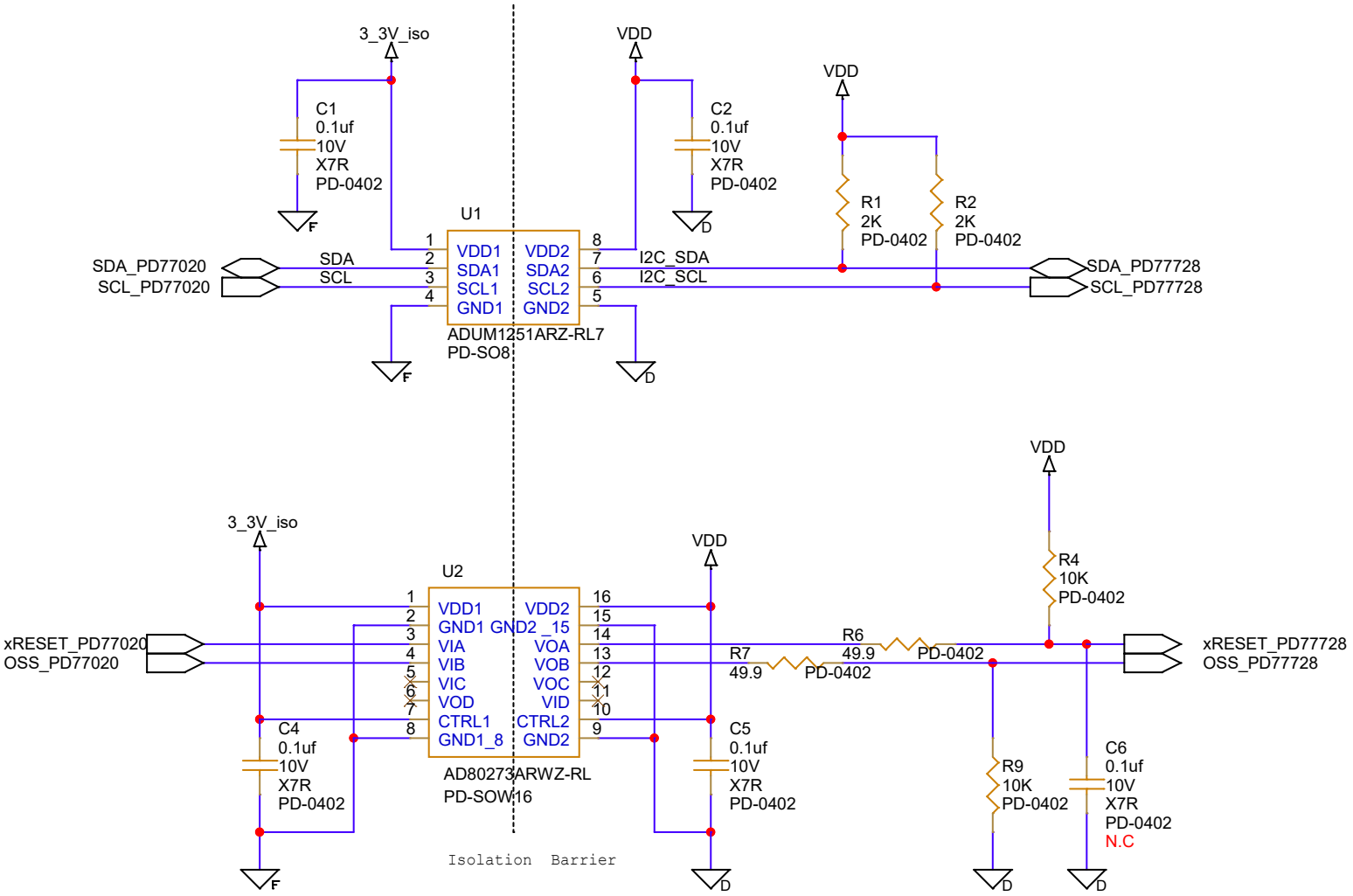


Figure 6-8. Digital Isolation Circuitry - Controller Mode



Note: In the above circuit, a digital isolator AD80273ARWZ-RL is used for isolating xRESET and OSS signals. Refer Figure 6-3 for alternative circuit using an optocoupler for xRESET signal and a high-speed optocoupler for OSS.

Figure 6-9. 3.3V Power Supply Based on MIC28512

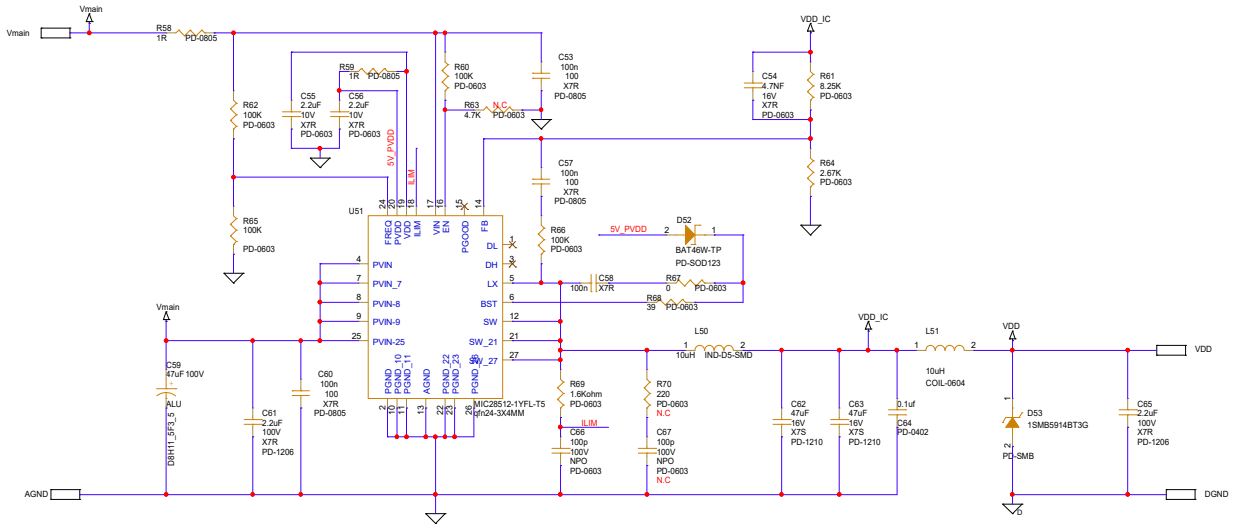
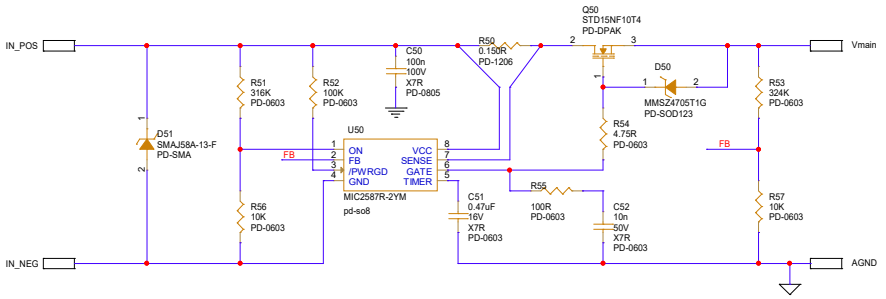


Figure 6-10. Hot-swap Circuit Based on MIC2587



7. Bill of Materials

The following section shows the detailed bill of materials for various Operating Modes.

7.1 Managed Auto and Semi-Auto Modes

The following section shows the Bill of Material (BOM) for Managed Auto and Semi-Auto Modes.

Table 7-1. 8-Port PoE Controller/Manager Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C11, C16, C26, C27	1 uF	CAP CER 1 uF 6.3V X7R 0402	Samsung	CL05B105KQ5NQNC
1	C12	1 nF	CAP CRM 1 nF 10V 10%X7R 0402 SMT	Yageo	CC0402KRX7R6BB102
9	C13, C17 - C20, C23, C25, C29, C30	100 nF	Capacitor, X7R, 100nF 100V 10% 0805	Samsung	CL21B104KCFSFNE
2	C15, C28	0.1 uF	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Walsin	0402B104K100CT
1	C21	10 nF	Capacitor,CER, X7R, 10nF 10V 10% 0402 SMT	Yageo	CC0402KRX7R6BB103
1	C22	47 uF	CAP ALU 47 uF 100V 20% 8X11.5 105C P=3.5mm T/H	Rubycon	100PX47M EFC T7 8X11.5
1	C24	1 uF	CAP CER 1 uF 100V 10% X7R 1210 SMT	AVX	12101C105KAT2A
1	R21	10K	Resistor, 10K, 1%, 1/16W 0402	Rohm	MCR01MZPF1002
1	R22	442	RES 442OHM 1% 1/10W 0402 SMD	KOA	RK73H1ETTP4420F
1	R26	10K	RES 10K Ω 0.1% 1/16W 0402 SMT	Stackpole Electronics Inc	RNCF0402BTE10K0
1	U4	PD77728ILQ-TR	IC PD77728 PoE PSE Controller/Manager	Microchip	PD77728ILQ-TR
1	RV1	B72210S2621K101	VARISTOR 625 VRMS, 825 VDC 3.5KA 10 MM	EPCOS	B72210S2621K101
2	C31, C32*	10 nF	CAP CER 10 nF 2KV +80-20% P = 7.5, D = 14.5	TDK	CK45-E3DD103ZYGNA
1	C33	1 nF	Capacitor,CER, X7R, 1 nF 10V 10% 0402 SMT	Walsin	0402B102K100CT
1	C34	0.47 uF	CAP CER 0.47UF 10V X7R 0402 SMT	Yageo	CC0402KRX7R6BB474

Note: *The Y-capacitors (C31 and C32) are not part of PoE application and are part of Power Supply.

Table 7-2. Digital Isolator Circuit Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	C1 - C2	0.1 uF	CAP CRM 100n 10V 10% X7R 0402 SMT	Walsin	0402B104K100CT
2	R1, R2	1K	RES TCK FLM 1K 1% 62.5mW 0402 SMT	Royal Electronic Factory Co.,Ltd.	0402WGF1001TCE
2	R3, R4	2K	RES TCK FLM 2K 1% 62.5mW 0402 SMT	Yageo	RC0402FR-072KL
4	R5 - R8	10K	Resistor, 10K, 1%, 1/16W 0402	Rohm	MCR01MZPF1002
1	U1	ADUM1251ARZ	IC Hot-Swap I2C Isolator 2Ch one-Direct SO-8	Analog Devices	ADUM1251ARZ-RL7
1	U2	MOCD217R2-M	IC Optoisolator Dual channel SO8	Onsemi	MOCD217R2-M

7.2 Controller Mode

The following section shows the Bill of Material (BOM) for Controller Mode.

Table 7-3. PD77020 Controller Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
5	C7, C9,C11, C12, C15	0.1 uf	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Nic Components	NMC0402X7R104K10TRP
3	C8, C10, C14	1 uF	CAP CER 1 uF 6.3V X7R 0402	Yageo	CC0402KRX7R5BB105
3	R10, R14, R16	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
3	R11, R12, R13	1K	RES TCK FLM 1K 1% 62.5 mW 0402 SMT 100 PPM	Royal Electronic Factory Co.,Ltd.	0402WGF1001TCE
1	R15	57.6K	Resistor, 57.6K, 1%, 1/16W 0402	Rohm	MCR01MZPF5762
1	U3	PD77020-TR	PD77020 PoE PSE Power Management Controller	Microchip	PD77020-VVVV[1]SS[2]-TR

Notes:

1. Firmware revision.
2. Firmware parameters options.

Table 7-4. PD77728 Circuitry/Manager Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C16, C19, C28, C30	1 uF	CAP CER 1 uF 6.3V X7R 0402	Samsung	CL05B105KQ5NQNC
2	C18, C31	0.1 uf	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Walsin	0402B104K100CT
9	C20, C21, C22, C23, C24, C25, C27, C33, C34	100n	Capacitor, X7R, 100 nF 100V 10% 0805	Samsung	CL21B104KCFSFNE
1	C26	1 uF	CAP CER 1 uF 100V 10% X7R 1210 SMT	AVX	12101C105KAT2A
1	C29	10 nF	Capacitor,CER, X7R, 10 nF 10V 10% 0402 SMT	Yageo	CC0402KRX7R6BB103
1	C32	47 uF	CAP ALU 47 uF 100V 20% 8X11.5 105C P = 3.5 mm T/H	Rubycon	100PX47M EFC T7 8X11.5
2	C35, C36*	10 nF	CAP CER 10 nF 2KV +80-20% P = 7.5, D = 14.5	TDK	CK45-E3DD103ZYGNA
1	C37	1 nF	Capacitor, CER, X7R, 1 nF 10V 10% 0402 SMT	Walsin	0402B102K100CT
1	C38	0.47 uF	CAP CER 0.47UF 10V X7R 0402 SMT	Yageo	CC0402KRX7R6BB474
1	RV1	B72210S2621K101	VARISTOR 625 VRMS, 825 VDC 3.5 KA 10 MM	EPCOS	B72210S2621K101
1	R17	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
1	R20	10K	RES 10K Ω 0.1% 1/16W 0402 SMT	Stackpole Electronics Inc	RNCF0402BTE10K0
1	U4	PD77728ILQ-TR	IC PD77728	Microchip	PD77728ILQ-TR

Note: *The Y-capacitors (C35 and C36) are not part of PoE application and are part of Power Supply.

Table 7-5. Digital Isolation Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C1, C2, C4, C5	0.1 uf	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Nic Components	NMC0402X7R104K10TRP
2	R1, R2	2K	RES TCK FLM 2K 1% 62.5 mW 0402 SMT	Yageo	RC0402FR-072KL
2	R4, R9	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
2	R6, R7	49.9	RES TCK FLM 49.9R 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-49R9-ELF
1	U1	ADUM1251ARZ-RL7	IC Hot-Swap I^2C Isolator 2Ch one-Direct SO-8	Analog Devices	ADUM1251ARZ-RL7
1	U2	AD80273ARWZ-RL	IC Dig.Isol VDD1-3ch/ VDD2-1ch 1 Mbps 3.3/5V SO16	Analog Devices	AD80273ARWZ-RL

Table 7-6. 3.3V Power Supply Based on MIC28512

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C53,C57,C58,C60	100n	Capacitor, X7R, 100 nF 100V 10% 0805	Samsung	CL21B104KCFSFNE
1	C54	4.7 nF	CAP CRM 4.7 nF 16V 10% X7R 0603 SMT	Kemet	C0603C472K4RACTU
2	C55,C56	2.2 uF	Capacitor,X7R, 2.2 uF, 10V, 10% 0603	TDK	C1608X7R1A225K080AC
1	C59	47 uF	CAP ALU 47 uF 100V 20% 8X11.5 105C P=3.5 mm T/H	Rubycon	100PX47M EFC T7 8X11.5
2	C61,C65	2.2 uF	CAP CRM 2.2 uF 100V 10% X7R 1206 SMT	AVX	12061C225KAT4A
2	C62,C63	47 uF	CAP CRM 47 uF 16V 10% X6S 1210 SMT	Murata	GRM32EC81C476KE15L
1	C64	0.1 uf	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Walsin	0402B104K100CT
1	C66	100p	CAP CRM 100 pF 100V 5%NPO 0603 SMT	AVX	06031A101JAT2A
1	D53	1SMB5914BT3G	ZENER DIODE SMB 3.6V/3W/ 104.2 mA	ON Semiconductor	1SMB5914BT3G
1	L50	10 uH	FIXED IND 10 uH 2.35A 64 mOhm SMD	Shenzhen Codaca Electronic Co., Ltd	CWPA5040-100M-MIC
1	L51	10 uH	Fixed Inductors 10 uH 1.45A 100mOhm SMT	Bourns	SDR0604-100ML
2	R58,R59	1R	RES 1R 125 mW 1%0805 SMT MTL FLM	Stackpole Electronics Inc	RMCF0805FT1R00
4	R60,R62,R65,R66	100K	RES 100K 62.5 mW 1%0603 SMT MTL FLM	ASJ	CR16-1003FL
1	R61	8.25K	RES 8.25K 62.5 mW 1% 0603 SMT	ASJ	CR16-8251FL
1	R64	2.67K	RES 2.67K 62.5 mW 1%0603 SMT MTL FLM	Yageo	RC0603FR-072K67L
1	R67	0R	RES TCK FLM 0R 62.5 mW 5% 0603 SMT	Samsung	RC1608J000CS
1	R68	39R	RES 39R 1/10W 5% 0603	Panasonic	ERJ3GEYJ390V
1	R69	1.6K	Resistor, 1.6KOhm, 1%, 1/16W 0603	Rohm	MCR03EZPFX1601
1	U51	MIC28512-1YFL-T5	IC REG BUCK 4.6V to 70V input 2A FCQFN24	Microchip	MIC28512-1YFL-T5
1	D52	BAT46W-TP	Diode Schottky 100v 150 mA 200 mW SOD123F SMT	Micro Commercial Co	BAT46W-TP

Table 7-7. Hot-swap Circuit Based on MIC2587

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	C50	100n	Capacitor, X7R, 100 nF 100V 10% 0805	Vishay	VJ0805Y104KXBAT
1	C51*	4.7 uF	Capacitor,X7R, 0.4 µF, 16V, 10% 0805	Samsung	CL21B475KOFNFNE
1	C52	10n	CAP CRM 10 nF 50V 10%X7R 0603 SMT	Samsung	CL10B103KB8NNNC
1	D50	MMSZ4705T1G	DIODE ZENER 18V 500MW SOD-123	ON-Semiconductor	MMSZ4705T1G
1	D51	SMAJ58A-13-F	DIO TVS 58V 40A SRG400WPK SMA SMT	Diodes Inc.	SMAJ58A-13-F
1	Q50	STD15NF10T4	TRN FET NCH 100V 23A0.065R D-PAK	STMicroelectronics	STD15NF10T4
1	R50*	0.150R	RES 0.15 OHM 1/4W 1% 75 ppm 1206 SMT	Vishay	WSL1206R1500FEA
1	R51	316K	Resistor, 316K, 1%, 1/16W 0603	ASJ	CR16-3163FL
1	R52	100K	RES 100K 62.5 mW 1%0603 SMT MTL FLM	Panasonic	ERJ3EKF1003V
1	R53	324K	RES TCK FLM 324K 62.5 mW1% 0603 SMT	Samsung	RC1608F3243CS
1	R54	4.75R	RES 4.75R 0.1W 1%0603 SMT MTL FLM	Samsung	RC1608F4R75CS
1	R55	100R	RES TCK FLM 100R 62.5 mW 1%0603 SMT	Yageo	RC0603FR-07100RL
2	R56,R57	10K	RES 10K 62.5 mW 1%0603 SMT MTL FLM	Yageo	RC0603FR-0710KL
1	U50	MIC2587R-2YM	IC HOT SWAP CTRLR GP 8SOIC	Microchip	MIC2587R-2YM

Note: *The resistor and capacitor value must be tuned as per the application current limit. A system with 12 PD77728 devices is considered as example here. Contact Microchip for design guidance.

8. Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a PoE system based on Microchip's PD77728 8-channel PoE Controller/Manager.

8.1 Isolation and Termination

According to PoE standards, certain isolation requirements need to be met in all the PoE equipment. In addition, EMI limitations must be considered, as specified in the FCC and European EN regulations. These requirements are considered by the PoE switch vendors while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met because of the unique combination of data and power circuitries.

The following sections define the requirements and provide recommendations for their implementation to assist designers in meeting those requirements, while also integrating Microchip's PoE chipset.

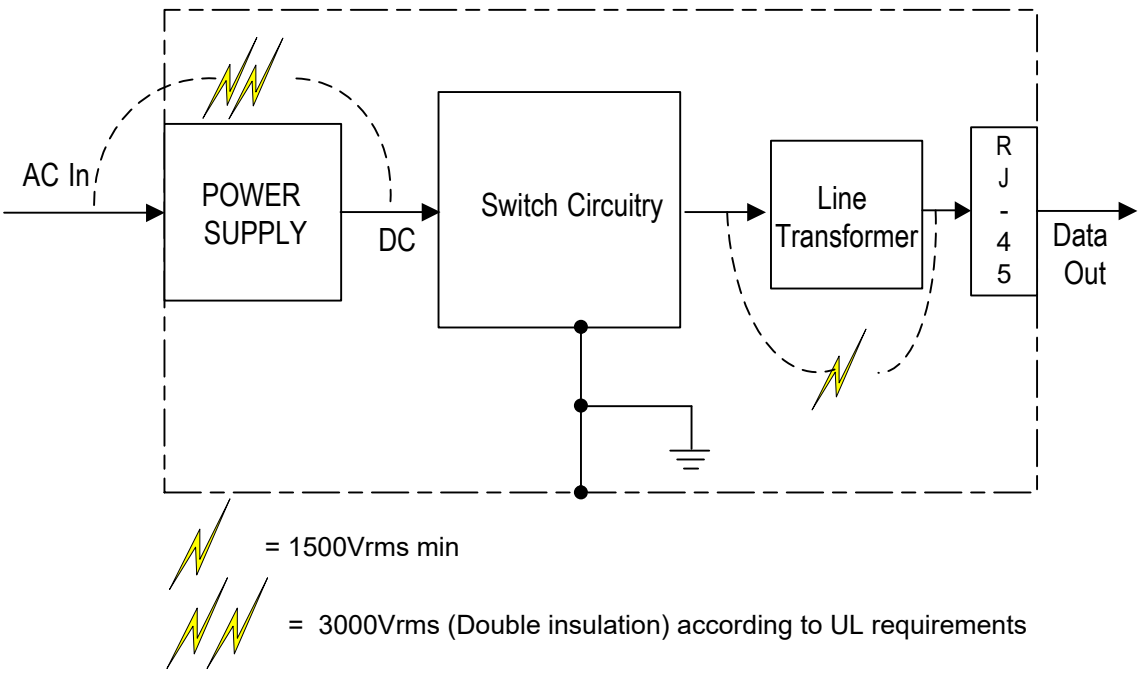
8.1.1 Isolation

As specified in the IEEE PoE standards, 1500 V_{RMS} isolation is required between the switch's main board circuitry (including protective and frame ground) and the Media Dependent Interface (MDI).

8.1.2 High-Voltage Isolation

For a switch with no PoE circuitry, isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated line transformers, as shown in the following figure.

Figure 8-1. Standard Switch Circuitry

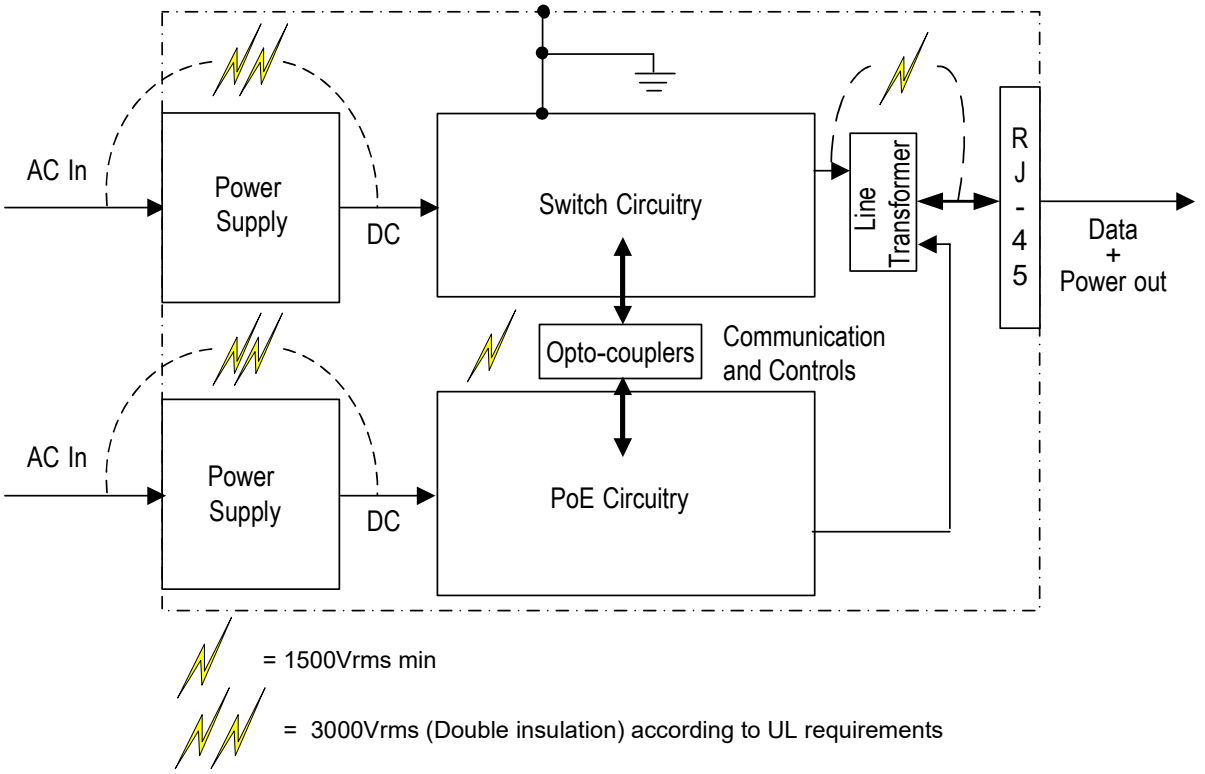


When integrating PoE circuitry into a switch, the output power can be supplied through the central tap of the line transformer's secondary side. This connectivity can bypass the line transformer's isolation if the PoE ground or DC input is connected to the switch's circuitry/ground.

To comply with these isolation requirements, the PoE managers must be isolated in regard to all other switch circuitries. Use one of the following two methods.

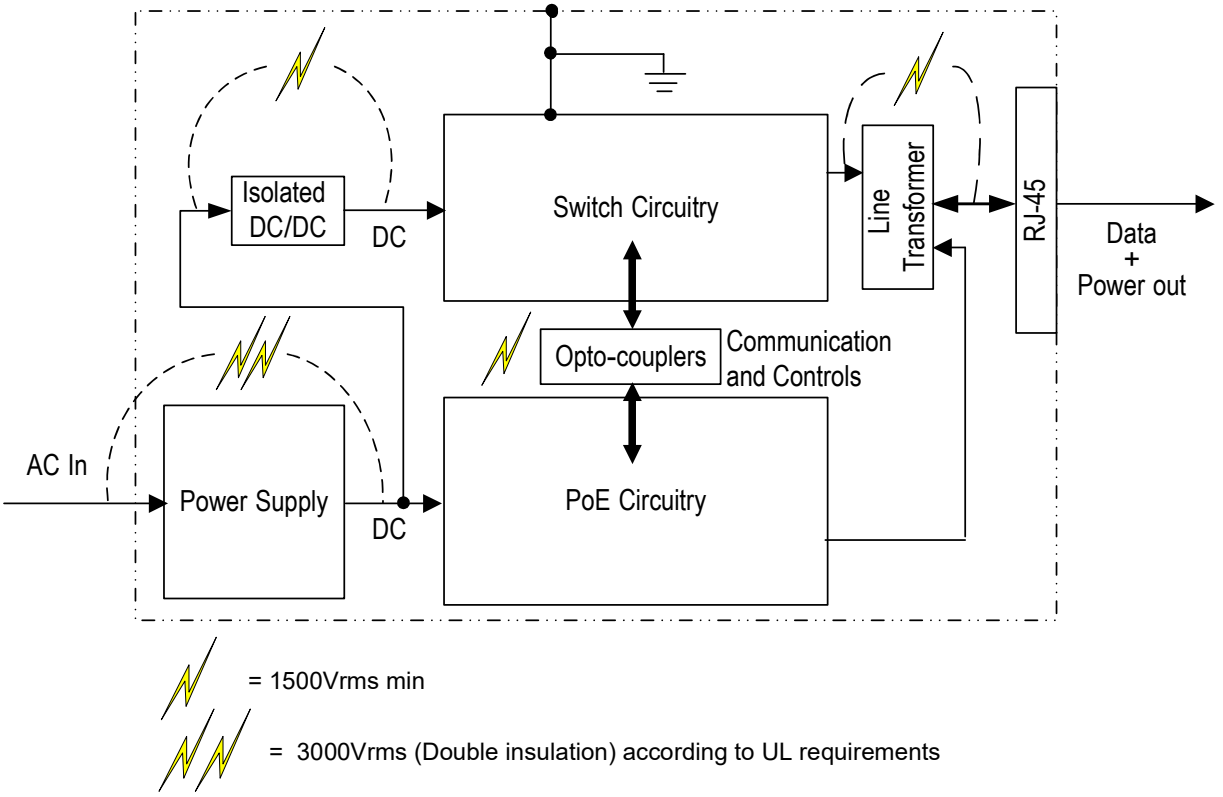
Method 1: Use a separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry, as shown in the following figure.

Figure 8-2. Switch Circuitry with Two DC Source



Method 2: Use a single system AC/DC PSU for the switch and PoE circuit while isolating the switch with additional isolated DC/DC circuitry. Use isolated serial communication port between the PoE circuitry, and the switch's circuitry, as shown in the following figure.

Figure 8-3. Switch Circuitry with Single DC Source

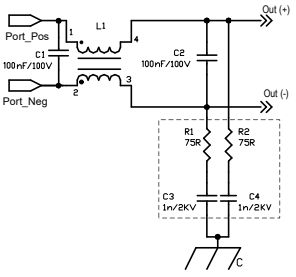


To maintain 1500 V_{RMS} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

8.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry, as shown in the following figure.

Figure 8-4. Recommended EMI Filter



Note: In most PoE systems, it is recommended to use 0Ω resistors for R1 and R2. However, certain systems may benefit from 75Ω resistors. Filtering provisions must be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes the following.

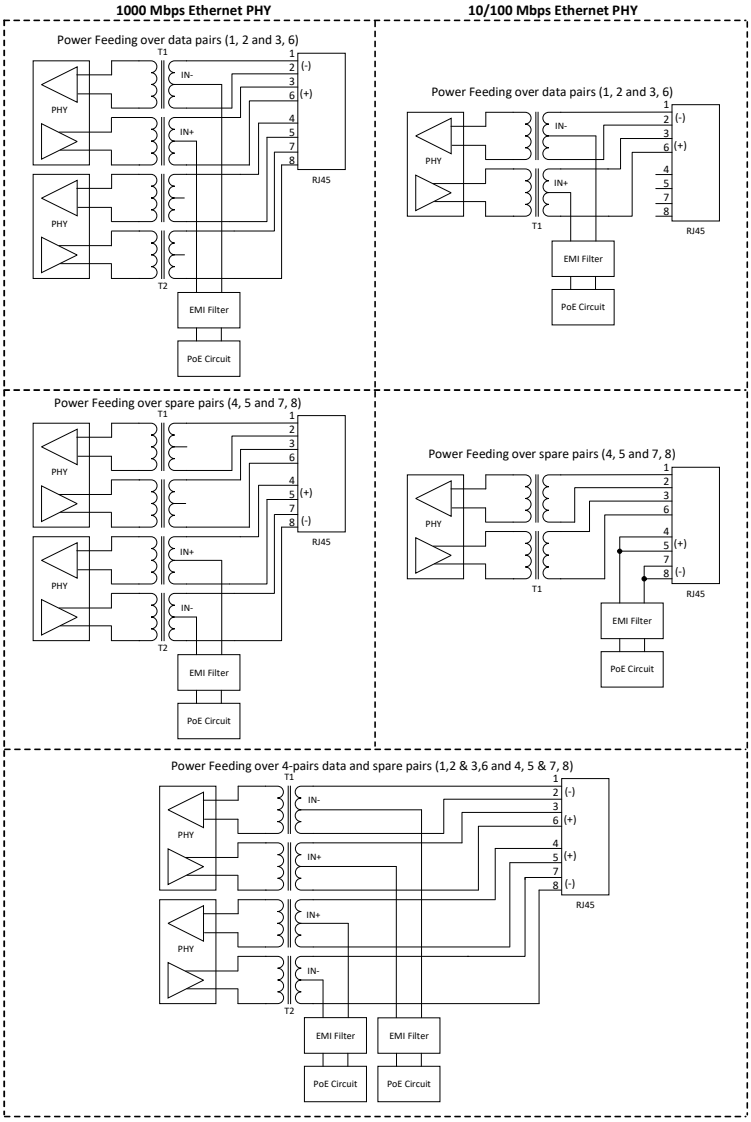
- A common mode choke for conducted EMI performances (such as, ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

As each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note: For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs, the spare pairs, or both the data and spare pairs. All methods are shown in the following figure where an MDI-X (or Auto MDI-X) connection is associated with the switch.

Figure 8-5. Output Ports Design Details



8.1.4 Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 V_{RMS} isolation between PoE voltages and frame ground (EGND). The RJ45 jack assemblies have a metal cover of 80 mils that almost reaches to the PCB surface. Maintain an 80 mils traces clearance between EGND traces for the RJ45 modular jack assembly metal cover and adjacent circuit paths/components. To prevent 1500 V_{RMS} isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ45 connector assemblies.

PoE technology involves voltages as high as 57 V_{DC}. Therefore, plan adjacent traces for 100 V_{DC} operational creepage. Operational creepage must be maintained to prevent breakdown between traces carrying these potentials.

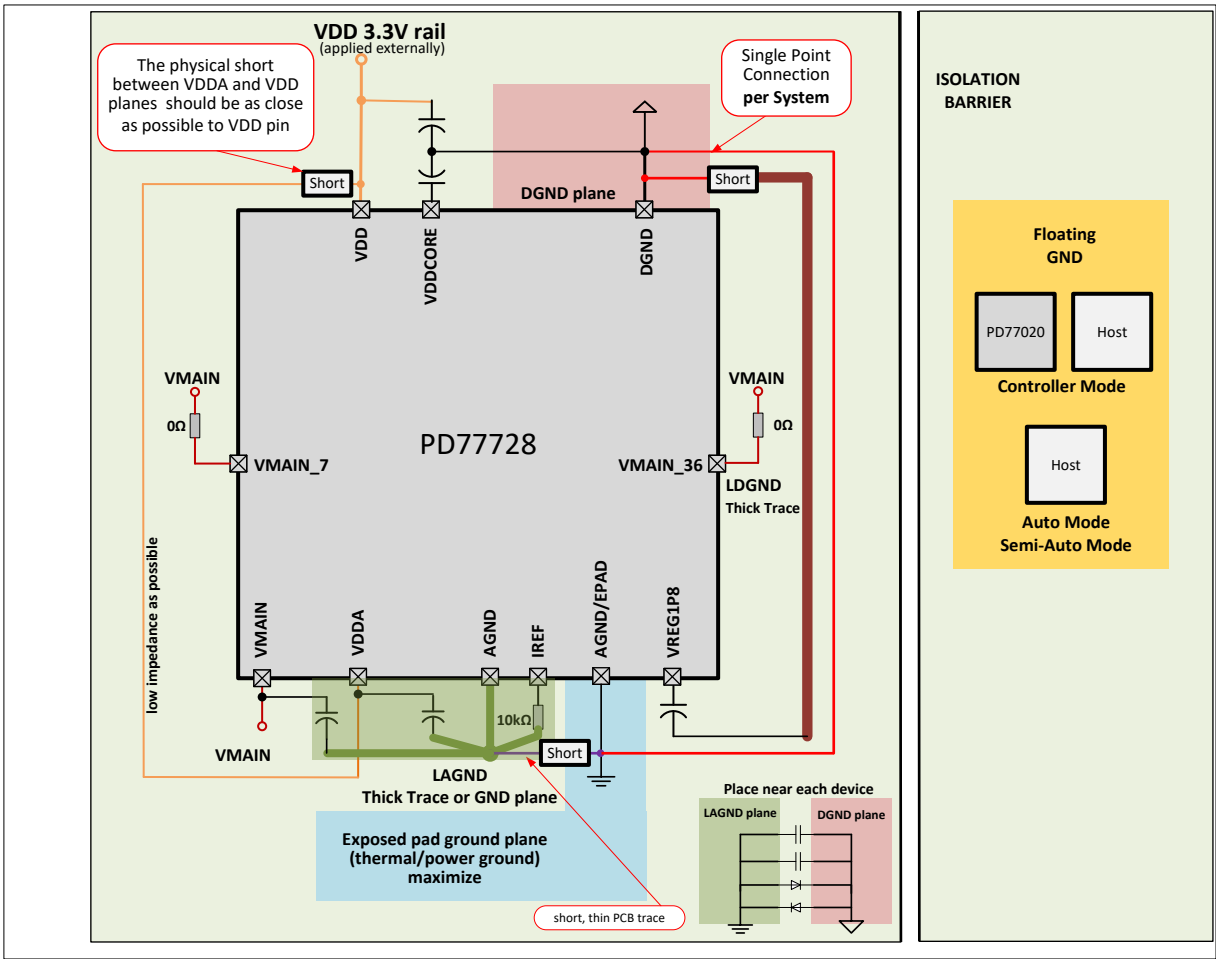
8.2 Guidelines

Microchip's PD77728 PoE Controller/Manager is designed to simplify the integration of PoE circuitry into switches based on the IEEE PoE standards. The pinout arrangement has been configured for optimal PCB routing.

Figure 8-6 shows the various circuits and elements surrounding the PD77728 PoE manager. This block diagram includes the following peripheral elements.

- **V_{MAIN} 7 and 36 pins:** Connect to V_{MAIN} (pin 17) through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection. See *AN4813: Surge Protection for Systems Based on PD77728 8-Port PSE PoE Controller/Manager*.
- **V_{DD}, pin43:** Connect VDD to main 3.3V power supply on the board. Connect VDD decoupling capacitors to DGND.
- **V_{DDCORE}, pin47:** Internal 1.2V regulator, connect 1.0 µF low ESR capacitor to DGND.
- **V_{REG1P8}, pin20:** Internal 1.8V regulator, connect 1.0 µF low ESR capacitor to LDGND.
- **V_{MAIN}, pin17:** Connect VMAIN to positive rail of input PoE. Connect 1 µF (100V, X7R) capacitor to LAGND.
- **V_{DDA}, pin22:** Connect VDDA to VDD using a single point connection, preferably the PCB shorting point placed close to VDD trace. Connect VDDA decoupling capacitors to LAGND.
- **AGND, pin21:** Connect to LAGND.
- **IREF, pin14:** Connect IREF resistor to LAGND.
- **EPAD:** Connect EPAD to AGND.
- **DGND and LAGND capacitor:** Requires a 1 nF and 470 nF per IC between LAGND and DGND. Leave a population option for two back-to-back diodes to improve EMC/EMI immunity, if required.
- **Per port connection:** See 4.1.3. Front-End Components.
- **LAGND and AGND short**: LAGND and AGND need to have a single connection near the EPAD.
- **LDGND and DGND short**: LDGND and DGND need to have a single connection.

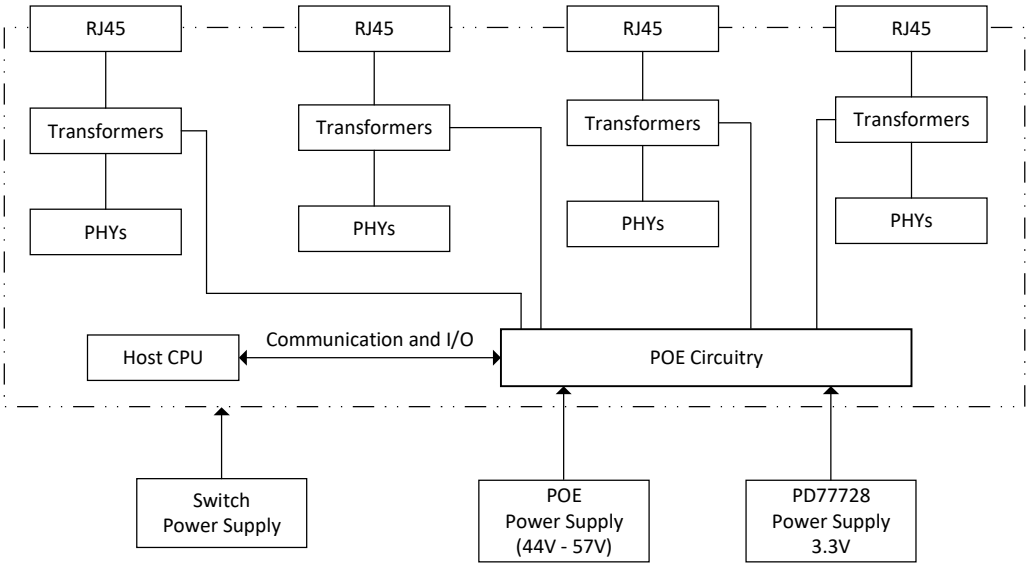
Figure 8-6. Component Identification for PD77728 Circuitry



8.2.1 Locating PoE Circuitry in a Switch

To minimize the length of high current traces as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's line transformers. The circuit can be fully integrated into the switch's PCB, or can be easily placed on top of the switch using a daughter board. Typical integration of PoE modules inside a switch is shown in the following figure.

Figure 8-7. PoE Circuitry Inside the Switch



8.2.2 Ground and Power Planes

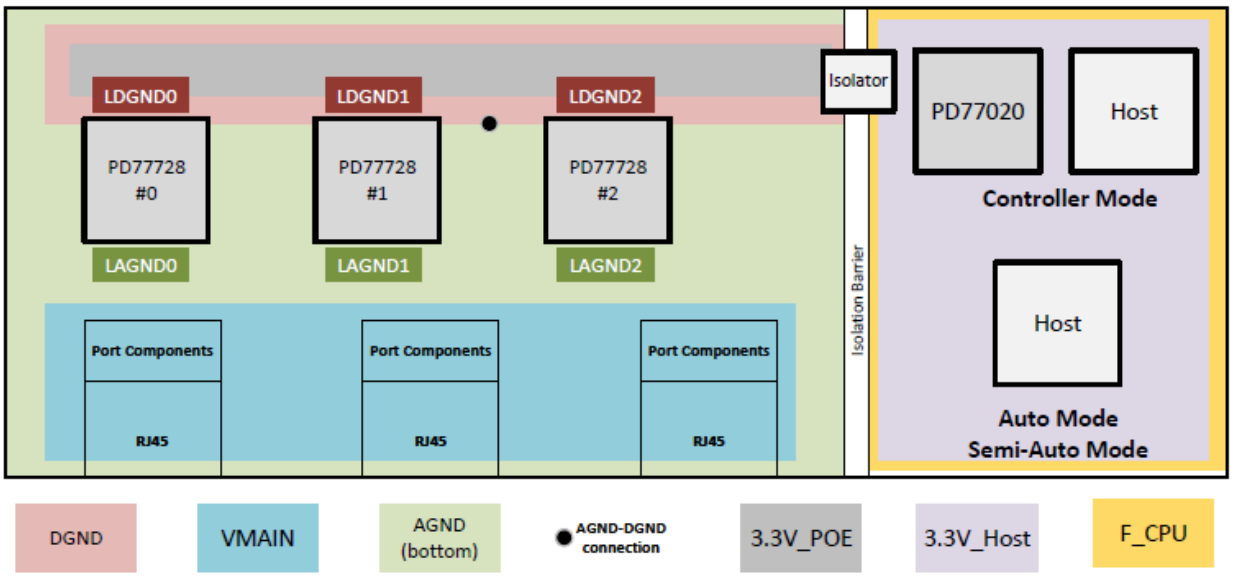
As the PoE solution is a mixed-signal (analog and digital) circuitry, care must be taken when routing the ground and power signals lines.

The reference design assumes a four-layer board such as, top, mid1, mid2, and bottom. The main planes are VMAIN/AGND and DGND.

Ground planes are crucial for proper operation and must be designed in accordance with the following guidelines.

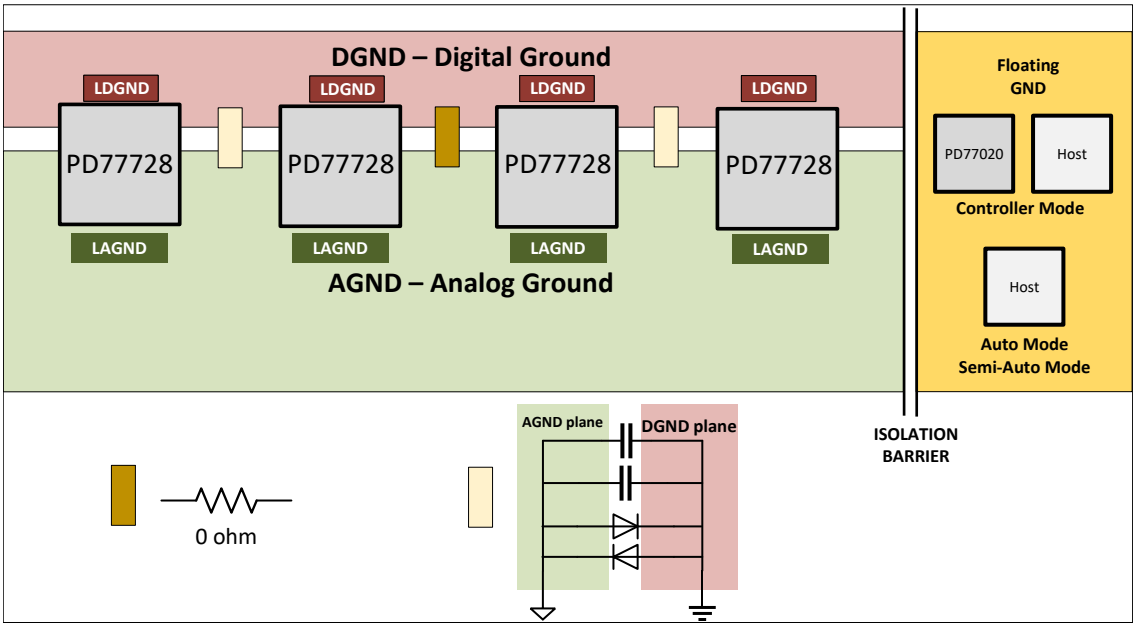
- Separate analog ground (AGND) and digital ground (DGND), with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD77728. The AGND must be located on external layer.
- Separate local grounds (LAGND/LDGND) and system grounds (AGND/DGND), with a gap of atleast 20 mils.
- Connect LDGND to DGND using a single point connection, preferably the PCB shorting point placed close to DGND trace.
- Connect all LAGND connections at single point using star connection. The LAGND is connected to EPAD using a short, thin PCB trace under IC for equipotential with AGND.
- Earth ground is used to tie in the metal frame of the RJ45 connectors. This ground must be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds, as shown in the following figure.

Figure 8-8. Ground and Power Planes



- To connect various digital ground (DGND) points extend the DGND surface under pins 43–56 of the PD77728 Controller/Managers.
- A focal interconnection point for the digital and analog grounds must be located at about the middle of the overlapping section, as shown in the following figure.

Figure 8-9. Single-Point Connection Between DGND and AGND



- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inversed Schottky diodes near each PoE manager between the analog and digital layers, as shown in the following figure. The capacitors form low impedance paths for digital driving signals.
- The power and return (ground) planes for the V_{MAIN} supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using wide copper lands.

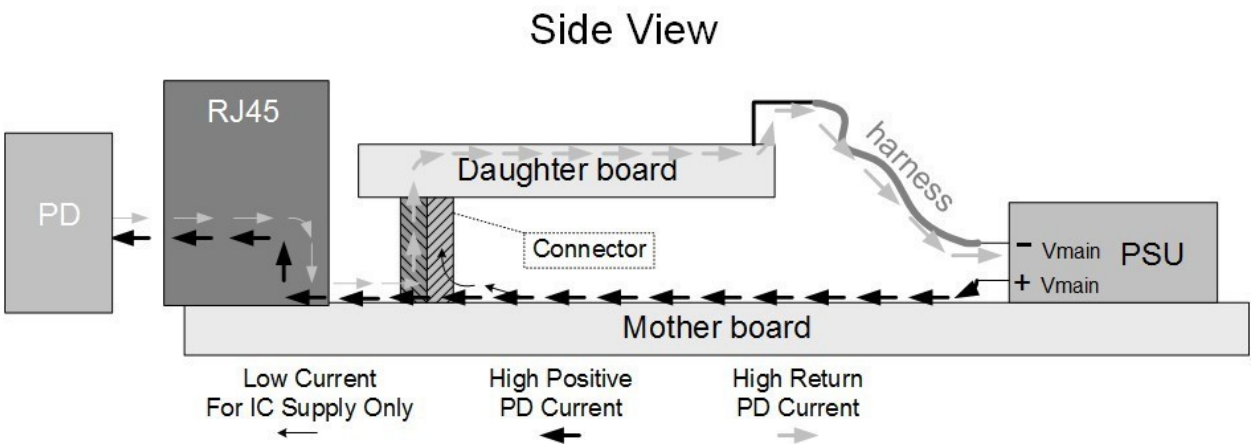
Use the following design guidelines while routing the Power planes.

- Separate V_{MAIN} and VDD signals, with a gap of at least 20 mils.
- Separate PORT_NEGx and VDD signals, with a gap of at least 20 mils.

8.2.3 Current Flow Through the PoE Application Utilizing a Daughter Board

When implementing the PoE circuitry on a daughter board, the high current path to the load (PD) does not have to be routed through the daughter board but only the return path, as shown in the following figure.

Figure 8-10. Blocks Identification for PD77728 Circuitry (Side View)



The port's DC current flows in an application utilizing a PoE DB as follows.

1. Coming from the switch's power supply positive to the center taps of the line transformer through a mother board wide trace (not through the DB).
2. From the center tap of the line transformer through the switch's RJ45 to the PD side.
3. The return current from the PD flows through RJ45 and the line transformer to the DB PoE circuitry.
4. From the DB analog ground (AGND), the current flows back to the switch's power supply negative through harness.

Note: The positive port's heavy current flows directly to the PD side without going through the PoE controllers/managers on the DB.

8.2.4 Conductor Routing

The following sections describe the conductor routing guidelines.

8.2.4.1 General Guidelines

The conductor (or printed lands) routing is performed as practiced in the general layout guidelines, specifically listed as follows.

- Conductors that deliver a digital signal are routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

8.2.4.2 Port Outputs

For robust design, the port output traces are 45-mil wide to handle maximum current and port power. However, to obtain a 10 °C (maximum) copper rise under 1A per port, set the minimum width for traces in accordance with the layer location and copper thickness, listed as follows.

- For two-ounce copper, external layer: 15 mils

- For two-ounce copper, internal layer: 20 mils
- For one-ounce copper, external layer: 25 mils
- For one-ounce copper, internal layer: 40 mils
- For ½ ounce copper, external layer: 30 mils
- For ½ ounce copper, internal layer: 55 mils (20 °C copper rise)

Additionally, the following port output guidelines must be considered.

- The port output traces must be short and parallel to each other to reduce RFI pickup and keep the series resistance low.
- The PoE port outputs must be connected to the switch's pulse transformers as shown in Figure 8-5. The common mode choke and Bob Smith termination (resistor-capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is located as close as possible to the pulse transformer.
- Route the I^2C communication clock (SCK) line coming from the PoE controller carefully so that it does not disturb the other lines. Two ground lines (connected to DGND) can be routed alongside the clock line to isolate it from the rest of the lines.

8.3 Specific Component Placement

The following section provides placement details for specific components.

8.3.1 Peripheral Components

To minimize heat transfer among various components, a gap between them must be maintained. The system designer must monitor the thermal performance during the designing phase and ensure that the maximum temperatures of the various components meet all requirements specified in the data sheet.

8.3.2 PD77020 Controller and Peripherals

For PD77020, see the Microchip *SAM D21 Family Datasheet* for recommendations related to the PoE controller layout guidelines. Locate the filtering capacitors for V_{DD} and for V_{DDA} close to power and ground pins.

8.3.3 PD77728 PoE Controller/Manager and Peripherals

The side of the PoE manager that includes pins 43–56 must face the DGND plane. These pins function as communication and control pins for the manager; connect between the PoE manager and the PD77020 PoE controller through isolation circuitry.

Locate the bypass capacitors for the PoE manager supply input close to the relevant pin. If two bypass capacitors are placed on the same line, then locate the lower valued capacitor closer to the pin on the same layer and place the higher valued capacitor at a more distant location.

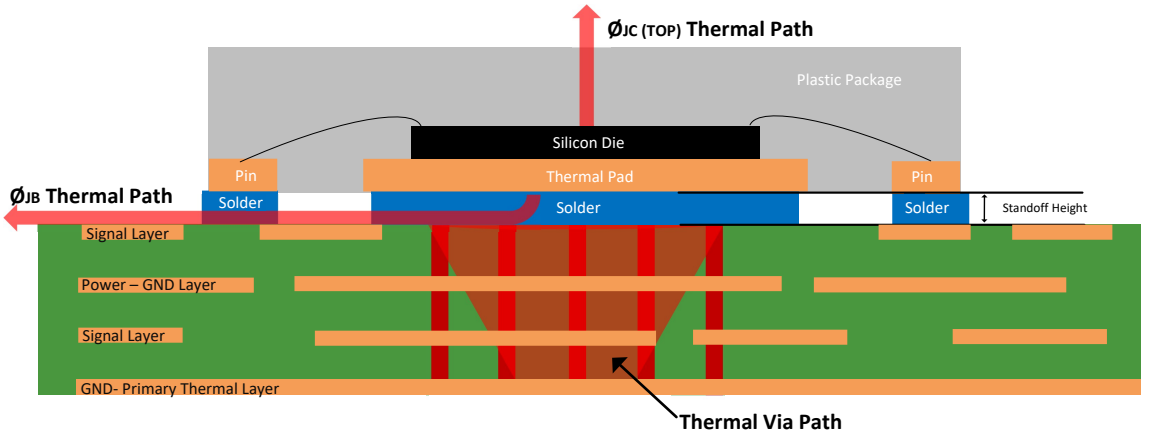
8.3.4 V_{MAIN} Capacitors

It is a good design practice to have 47 µF capacitors near each RJ45 gang over V_{MAIN}, to prevent noise and spikes events to penetrate the V_{MAIN} rail.

9. Thermal Pad Design

For proper heat dissipation, the recommended footprint/layout guidelines must be followed.

Figure 9-1. Heat Dissipation in PCB



Three thermal paths are available for heat to flow from the IC.

- Heat flow from the junction to the package side and pins. This parameter is a package parameter and is defined by ØJB in the device datasheet.
- Heat flow from the junction to the package top surface. This parameter is a package parameter and is defined by ØJC (TOP) in the device datasheet.
- Heat flow from the junction to the package bottom surface (the thermal pad) through the thermal vias to the various thermal ground planes. This is the most significant thermal path. The thermal resistance of this path is determined by the package e-pad design and the PCB construction: Number of PCB layers, number of thermal vias, construction of thermal vias, and size and location of the copper thermal plane. This is the primary heat flow path and it is important to follow footprint recommendations.

The footprint that details the solder mask, copper layers, and recommended paste mask is detailed in the PD77728 datasheet.

- As per IPC7093 standard, standoff must be minimum of 2 mil (0.050 mm), with a Microchip recommended target of 2.5 mil (0.0635 mm). For this reason, a paste mask stencil thickness of 5 mils must be considered.
- Thermal vias must be unplugged with a diameter approximately 0.33 mm. Microchip recommends a 6 × 6 via array and no solder paste covering on the bottom PCB layer.
- Thermal pad solder paste is a 3 × 3 array with “streets” in-between the array.

Important: It is important to have streets to allow for outgassing during the reflow process to help achieve a uniform standoff height.

The PCB copper thermal planes must be of maximum practical area on as many PCB layers as possible.

See the device datasheet for package footprint guidelines.

10. References

The following documents can be obtained from Microchip Power over Ethernet.

- *PD77728 8-port PSE Controller/Manager Datasheet*
- *PD77020 PoE PSE Power Management Controller*

Consult Microchip for *Surge Protection 8-Port PSE Controller/Manager PD77728*.

The following are available on Microchip's Software Library.

- *Firmware (without the boot section) and GUI*
- *PD77020 Communication Protocol User Guide*

In addition, the following non-Microchip documents can be consulted.

- *IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet*
- *IEEE802.3af-2003 Standard, DTE Power via MDI*
- *IEEE802.3at-2009 Standard, DTE Power via MDI*

Technical support for Microchip PoE products is available at the Microchip Technical Support Portal.

11. Revision History

Revision	Date	Description
B	09/2023	The following list of changes are made in Revision B of the document. • Updated 2.1. Communication Interfaces. • Updated 2.2.2. PD77728 Supply. • Added 2.2.2.1. PD77728 3.3V section. • Updated 2.2.4. Hot-Swap Circuit. • Updated Figure 6-3 and Figure 6-8. • Added Figure 6-9 and Figure 6-10. • Updated Table 7-2. • Added Table 7-6 and Table 7-7.
A	06/2023	Initial release.

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