Improving Batwing Power Dissipation

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Allegro MicroSystems' stepper motor ICs are power ICs encapsulated in DIP (dual in-line), SOIC (small outline integrated circuit), and PLCC (plastic leaded chip carrier) packages. The silicon die is directly bonded to a heat-spreading lead frame (batwing) for efficient heat transfer to an external heat sink, or to a copper ground plane on the printed wiring board.

Determining the needed amount of PWB copper area for heat sinking is a simple procedure, by following a few basic guidelines.

A. Determine the total IC power to be dissipated (P_D). This can be approximately calculated by:

$$I_{CC} \times V_{CC} \quad \text{(logic)}$$
$$+$$
$$I_{BB} \times V_{BB} \quad \text{(driver, no load)}$$
$$+$$
$$I_{OUT} \times V_{CE(sat)} \quad \text{(source driver)}$$
$$+$$
$$I_{OUT} \times V_{CE(sat)} \quad \text{(sink driver)}$$

or refer to Application Note 29501.4, Computing IC Temperature Rise.

B. Specify maximum operating ambient temperature, T_A. This should include factors such as heating from other components, air circulation, etc.

C. Specify maximum junction temperature, T_J, the temperature of the chip at maximum operating current. No strict rules exist — typically one should design for a maximum continuous junction temperature of 100°C to 130°C taking into consideration that every 10°C rise in junction temperature approximately halves the expected life of the device and every 10°C decrease in junction temperature doubles the life of the device. The absolute maximum allowable junction temperature is 150°C.

The maximum value of junction-to-ambient thermal resistance, $R_{\theta JA}$, can now be calculated as:

$$R_{\theta JA} = (T_J - T_A)/P_D$$

Graphs showing the junction-to-ambient thermal resistance, for various batwing packages, as a function of the total area of a copper ground plane heat sink on a PWB are given at www.allegromicro.com.

In order to verify the thermal design, it is useful to make an estimate of the real chip temperature. This can be done by attaching a thermocouple, or some other miniature temperature sensor, onto the batwing ground terminals of the IC under test, and measuring the "tab" temperature, T_T. The chip (junction) temperature can now be calculated:

$$T_J = T_T + (P_D \times R_{\theta JT})$$

where $R_{\theta JT}$ is the thermal resistance from junction to the batwing terminal.

The junction-to-tab thermal resistance is specified as 6°C/W for the SOIC, DIP, and PLCC packages.

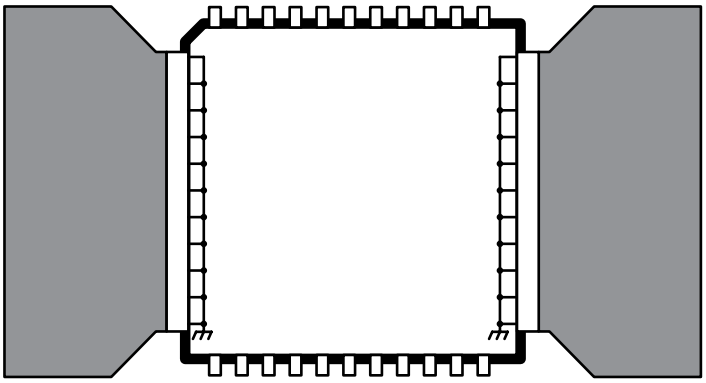

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Figure 1: Batwing PLCC, Package Code EB, with Copper-Foil Heat Sink

NOTE 1: Package power dissipation, and the requirements for heat sinking, can be considerably reduced by using external fast-recovery Schottky diodes in parallel with the internal flyback diodes. The diodes must be rated to withstand the supply voltage and load current.

NOTE 2: The original batwing (DIP) package had a copper lead frame that was continuous through the package and completely webbed between two or three lead tips on each side. Because this construction required slotted holes in the PWB, the batwing webbing was shortened to the seating plane with no noticeable effect on thermal resistance. Over time, the webbing was further reduced to the shoulder and then internal to the package. If the internal silicon die is directly mounted on the lead frame for heat transfer through the leads to an external heat sink or to a copper ground plane on the PWB, these (DIP, SOIC, or PLCC) devices are still called “batwing” packages.

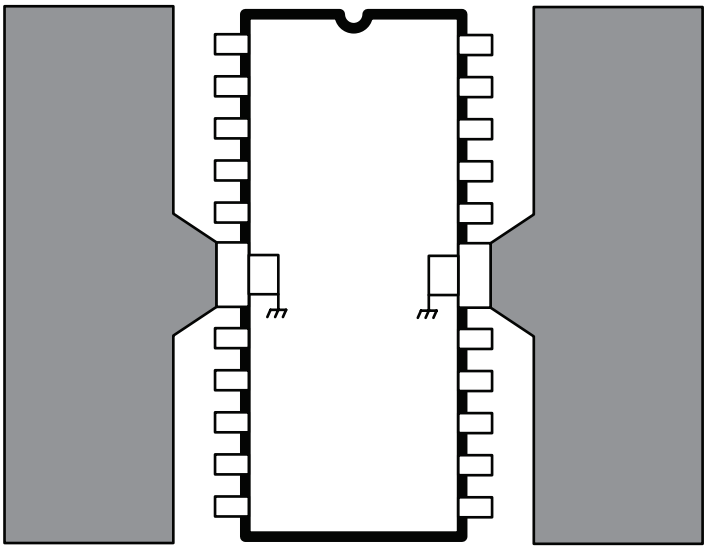

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Figure 2: Batwing DIP, Package Code B, with Copper-Foil Heat Sink

Revision History

Revision No.	Revision Date	Description of Revision
1	June 30, 2014	Updated document formatting

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