AN251216

Thermal networks of ART LDMOS devices

AMPLEON

Rev. 1 — 1 January 2026

Application note

Document information

Info	Content
Keywords	RC thermal, Models, Foster, Cauer, Zth, Rth, power amplifier
Abstract	This application note presents a modeling approach for capturing the thermal behavior of ART LDMOS RF power devices using compact RC networks. Based on an electrical analogy, the method enables efficient prediction of junction temperature and transient thermal response. The extracted models support integration into circuit simulations and system-level thermal analysis, facilitating reliable and thermally optimized RF power designs.

Revision history

Rev	Date	Description
AN251216#1	20260101	Initial version.

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1. Introduction

The thermal behavior of RF power amplifier devices plays a critical role in ensuring reliable performance and device integrity within their specified safe operating area. Accurate temperature prediction supports both circuit design optimization and system-level thermal management.

A practical approach to modeling thermal performance is to use RC thermal networks, which describe the transient temperature response of a device through an equivalent electrical analogy. These compact models can be implemented using Foster or Cauer representations, both of which reproduce the measured thermal impedance characteristics. They can be directly applied within a SPICE environment or imported into any other electrical simulator for transient or steady-state simulation.

In addition to their use in circuit-level analysis, compact RC thermal networks can be integrated into system-level thermal simulations. This enables customers to incorporate device-level thermal models into their complete assembly stack-ups such as PCBs, heat spreaders, and mechanical enclosures for accurate junction temperature prediction under realistic conditions.

This application note provides an overview of the Foster and Cauer modeling approaches, explains their derivation from measured thermal impedance data, and presents examples of how to apply them in thermal simulations. More detailed guidance on the extraction of the RC parameters from measurement and simulation data can be found in AN221014: Thermal Characteristics of ART LDMOS Power Transistors.

2. Thermal impedance

The thermal impedance denoted $Z_{th}(t)$, represents the time-dependent temperature response of the device to a power dissipation pulse. It is a key quantity for describing transient thermal behavior and is the basis for deriving the equivalent RC model.

When an RF power transistor is exposed to a continuous power pulse lasting longer than approximately one second, the device reaches thermal equilibrium and the thermal impedance reaches its plateau value, known as the steady-state thermal resistance R_{th}. This parameter defines the permanent temperature rise per unit power at steady-state operation.

For shorter pulse durations, the temperature rise lags the applied power due to the thermal inertia of materials in the die and package. This delay allows the device to tolerate higher power levels during short bursts without exceeding its thermal limits. The transient thermal impedance $Z_{th}(t)$ curves therefore provide valuable information on the allowable power levels for various pulse widths and duty cycles.

3. Junction temperature rise

To evaluate the junction temperature rise (ΔT_j) of an RF device, both the dissipated power and pulse characteristics must be known. For square power pulses, the temperature rise can be determined directly from the thermal impedance curve by multiplying the peak dissipated power (P_{diss}) by the corresponding value of $Z_{th}(t)$:

$$\Delta T_j = Z_{th}(t) * P_{diss} \quad (1)$$

For constant or long-duration power, the steady-state thermal resistance R_{th} is used in place of $Z_{th}(t)$.

For complex or arbitrary waveforms, such as modulated or sinusoidal power pulses, the thermal response can be calculated using a convolution integral that accounts for the full temporal variation of power dissipation and the device's transient response. In practice, power profiles are often approximated as a series of rectangular pulses, and the resulting temperature rise is obtained by superposition of their individual effects. This method provides sufficient accuracy for most design evaluations.

4. Foster and Cauer RC thermal models

4.1 Cauer model

The Cauer model is a ladder network in which thermal capacitances are connected to a common thermal ground corresponding to ambient temperature. This configuration mirrors the physical structure of the device, where each RC pair represents a distinct layer or thermal interface such as the semiconductor die, solder attach, substrate, and package.

As shown in Fig. 1a, the Cauer model provides direct access to internal temperature nodes and can be readily connected to external thermal networks, including system-level models of printed circuit boards or heat sinks. This makes the Cauer model more versatile and physically interpretable than the Foster representation.

4.2 Foster model

The Foster model is obtained by fitting the measured $Z_{th}(t)$ curve with a series of exponential terms, each represented by an RC pair. The resulting network forms a parallel RC chain, as illustrated in Fig. 1b.

Although the Foster representation is mathematically straightforward and convenient for quick analysis, the parameters R_i and C_i do not correspond to specific physical locations or material layers within the device. Consequently, Foster models are not suitable for extending or combining with other thermal networks.

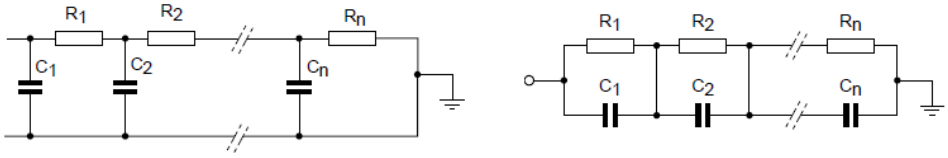


Figure 1. (a) Cauer and (b) Foster RC thermal networks

5. RC thermal modeling: Example and application

5.1 Datasheet thermal information

To demonstrate the application of RC thermal modeling, the ART2K0FE LDMOS transistor is used as an example. The device's thermal characteristics, including the thermal resistance between junction and case $R_{th(j-c)}$ and the transient thermal impedance $Z_{th(j-c)}$ for specific pulse time and duty cycle, are provided in the product datasheet listed in Table 1. The transient thermal impedance curves covering range of pulse times and duty cycles are also presented in Fig. 2. Based on these data, both Foster and Cauer networks have been extracted and are summarized in the SPICE netlist shown in Fig. 3.

Table 1. Thermal characteristics of ART2K0FE

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 95 °C	0.077	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 95 °C; t_p = 100 µs; δ = 10 %	0.018	K/W

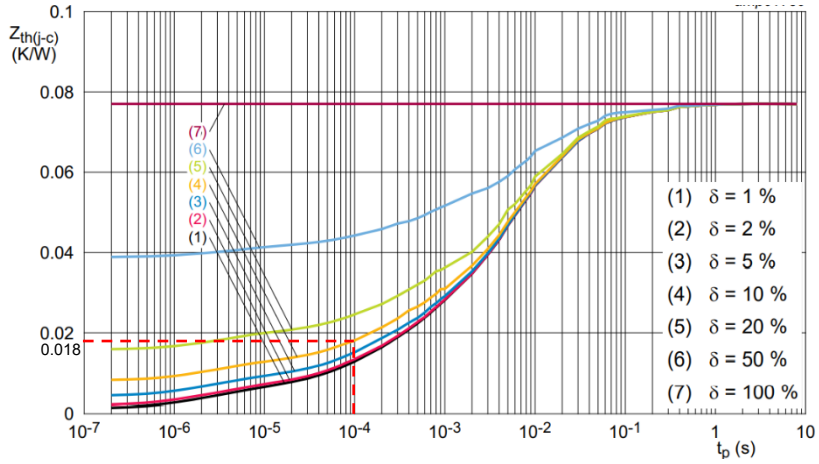


Figure 2. Transient thermal impedance from junction to the case as a function of pulse duration and duty cycle for the ART2K0FE

```
************************************************************
* Stages= 6
* Rth junction-to-case= 0.077 K/W
* R2= 0.999424 Max. difference= 0.0012585 K/W
************************************************************
.SUBCKT FOSTER 1 7
C0 1 2 0.00200
R0 1 2 0.00117
C1 2 3 0.01557
R1 2 3 0.00092
C2 3 4 0.01286
R2 3 4 0.00157
C3 4 5 0.01514
R3 4 5 0.01603
C4 5 6 0.30527
R4 5 6 0.00961
C5 6 7 0.35357
R5 6 7 0.04894
.ENDS FOSTER
```

```
************************************************************
* Stages= 6
* Rth junction-to-case= 0.077 K/W
* R2= 0.999424 Max. difference= 0.0012585 K/W
************************************************************
.SUBCKT CAUER 1 7
C0 1 0 0.00140
R0 1 2 0.00229
C1 2 0 0.00428
R1 2 3 0.00470
C2 3 0 0.00969
R2 3 4 0.00986
C3 4 0 0.00479
R3 4 5 0.00629
C4 5 0 0.16421
R4 5 6 0.02725
C5 6 0 0.36094
R5 6 7 0.02784
.ENDS CAUER
```

Figure 3. ART2K0FE Foster and Cauer model netlist

5.2 Temperature rise calculation

As an example of how to determine the junction temperature rise during pulsed operation, the transient thermal impedance curve provided in the device datasheet can be used. For a pulse width of 100 µs and a 10% duty cycle, the curve indicates a

junction-to-case transient thermal impedance of approximately $Z_{th(j-c)}\ (100\ \mu s, 10\%)\ \approx\ 0.018\ K/W$. With a peak power dissipation of $P_{diss}\ =\ 800$ W, the resulting junction temperature rise during each RF pulse is calculated as:

$$\Delta T_{j-c} = Z_{th(j-c)} * P_{diss} = 0.018\ \frac{K}{W} * 800W = 14.4\ K \qquad (2)$$

Therefore, with an assumed case temperature T_c = 85 °C, the junction temperature under pulsed operation becomes:

$$T_j = T_c + \Delta T_{j-c} = 85\ °C + 14.4\ °C = 99.4\ °C \qquad (3)$$

The case temperature represents the maximum temperature at the backside of the device flange, theoretically corresponding to the highest solder temperature between the transistor and the heatsink.

For long-duration or continuous-wave (CW) operation, the steady-state junction-to-case thermal resistance $R_{th(j-c)}$ must be used instead of the transient impedance. Using the datasheet value $R_{th(j-c)}\ =\ 0.077\ K/W$ and an average power dissipation $Pdiss\ =\ 440\ W$, the steady-state junction temperature rise is:

$$\Delta T_{j-c} = R_{th(j-c)} * P_{diss} = 0.077\ \frac{K}{W} * 440W = 33.9\ K \qquad (4)$$

Therefore, at T_c = 85 °C, the steady-state CW junction temperature is:

$$T_j = T_c + \Delta T_{j-c} = 85\ °C + 33.9\ °C = 118.9\ °C \qquad (5)$$

5.3 Simulation in electrical platform

These RC networks reproduce the measured transient thermal impedance behavior of the device and can be used in thermal-only simulations to estimate junction temperature rise in response to transient power dissipation. In such simulations, the network can be excited by a time-varying power waveform, and the resulting voltage at the junction node (T_j) reflects the temperature increase above ambient. The internal Cauer model uses Pin 1 as the junction temperature node, and Pins 6 and 7 as ambient reference points. For simple test conditions, both ambient pins may be tied to a constant voltage source representing a fixed ambient temperature (T_{amb}).

As a practical example, the RC thermal model of the ART2K0FE device has been implemented and simulated in Keysight ADS or other SPICE-compatible tools, as shown in Fig. 4 for Keysight ADS. In this setup, two versions of the Cauer network, one with three stages and one with six stages, were modeled and driven with a pulsed power waveform under different pulse durations. The simulation evaluates the transient junction temperature rise over time for a fixed duty cycle of 10%. The results in Fig. 5. illustrate the effectiveness of using the RC thermal network in transient thermal simulations, with temperature waveforms generated for pulse widths ranging from 0.01 ms to 10 ms. The simulation captures the thermal accumulation and cooling between pulses, demonstrating how the RC network translates power input into time-dependent temperature behavior. More RC stages better predict the temperature response, particularly for shorter pulse durations where the thermal time constants of different package layers become more influential. This example confirms the applicability of compact thermal models in system-level simulation tools, where they can be used to study dynamic thermal effects under realistic operating conditions.

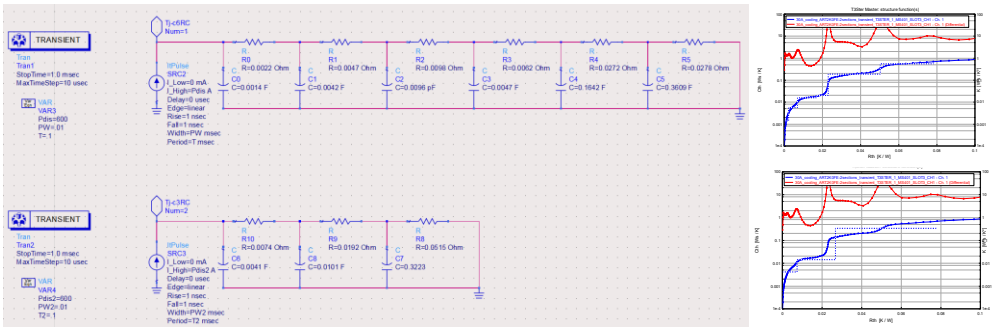
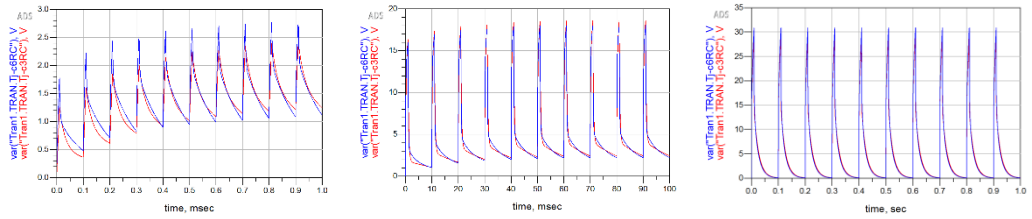


Figure 4. ADS modeling of Cauer RC thermal network based on the fitted 6-stage and 3-stage structure function



Pulse time = 0.01 ms | Pulse time = 1 ms | Pulse time = 10 ms

Figure 5. Transient temperature profile of 3-red and 6-blue stages at D=10% for various pulse times

5.4 Extension with external thermal network

When thermal effects beyond the device itself need to be included, such as those from PCB, interface material, or heatsink, the model can be extended by connecting the internal RC network to an external thermal network. In this case, Pin 6 of the internal Cauer model is connected to the first node of the external thermal network representing the system-level thermal stack-up, while Pin 7 remains tied to ambient. The final node of the external thermal network must also be connected to ambient to ensure proper termination of the thermal path. This configuration allows designers to evaluate the combined thermal performance of the device and its operating environment, including the effect of different board materials, copper layouts, and cooling strategies.

5.5 Integration into FEM thermal model

In addition to these circuit-based approaches, the RC thermal model can also be embedded in a system-level thermal finite element method (FEM) simulation. In this case, the RC ladder is used to model the die-to-case thermal path and is applied as a compact boundary condition at the mounting interface of the transistor in the FEM model. The dissipated power is applied at this boundary, and the RC network determines the junction temperature rise as a function of time and system-level heat flow. This method eliminates the need for detailed meshing of the die and package structure, significantly reducing simulation time while maintaining fidelity with measured device behavior.

This hybrid approach enables integration of verified device-level thermal performance into complete assembly simulations, allowing accurate prediction of junction temperature in complex thermal environments. For these implementations, the RC parameters are

entered directly into the simulation tool, or imported as a behavioral model script. The junction temperature computed by the compact model can then be monitored for thermal design optimization or reliability assessment.

5.6 Integration into electro-thermal circuit model

The compact RC thermal model can be integrated into the transistor subcircuit to enable dynamic electro-thermal simulation. In this configuration, the dissipated power is treated as a current that flows into the RC thermal network, and the resulting voltage represents the temperature rise at the junction. This voltage, typically assigned to the node T_j, is then used to influence temperature-dependent electrical parameters within the model.

The RC network is implemented normally in SPEAR model as a 3rd order Foster network, representing the internal thermal path from junction to case. It connects the junction temperature node to ambient through a ladder of resistor and capacitor. It can be extended with additional stages to model external thermal components such as PCBs or heatsinks. For accurate operation, it is essential that the final node of the thermal network is connected to ambient through a defined impedance. Leaving the thermal node floating or incorrectly terminated will result in simulation errors or non-convergence.

This configuration enables the device to respond to its own power dissipation during simulation. Junction temperature rises dynamically as power is applied and feeds back into the electrical model as shown in Fig. 6., allowing realistic simulation of heating effects under modulated signals or pulsed operation. To align with pulsed measurement results, the self-heating coefficient can be adjusted below 1.0 to reflect lower average thermal loading based on duty cycle and pulse time.

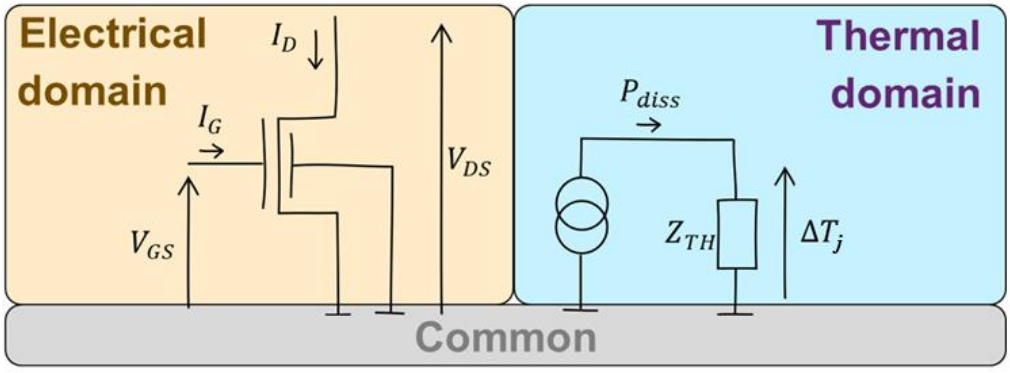


Figure 6. Self-heating and thermal impedance in SPEAR device modeling

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Date of release: 1 January 2026
Document identifier: AN251216#1