AN12004

FXLS896xAF / FXLS897xCF Sensor Data Change Detection (SDCD) block overview and example

Rev. 2 — 30 October 2020 Application note

Document information

Information	Content
Keywords	FXLS896xAF, FXLS897xCF, accelerometer, Sensor Data Change Detection (SDCD), inertial event detection
Abstract	This document details the utilization of the Sensor Data Change Detection (SDCD) block within the FXLS896xAF and FXLS897xCF 3 axis accelerometer devices

1 Introduction

The Sensor Data Change Detection (SDCD) block of FXLS896xAF and FXLS897xCF is an efficient and flexible inertial event detection function with the ability to detect inertial events such as motion/no-motion, high-g/low-g, tap, freefall and transient acceleration events, etc. This application note discusses in detail the features of the embedded block in real world application use cases. A series of examples with sample register configurations is covered to help users get started quickly.

2 SDCD block

2.1 Function overview

The SDCD function within FXLS896xAF and FXLS897xCF incorporates a flexible digital window comparator useful for implementing several different interrupt event generation functions. The SDCD block operates in either relative or absolute modes and features user programmable thresholds, debounce time, event polarity detection and interrupt generation logic.

Simply stated, the acceleration data input (X[n], for example) to the SDCD block is compared against a set of user programmable upper and lower thresholds (see Figure 1) in absolute or relative mode. For simplicity, only the absolute mode of operation is presented. The relative mode of operation is covered in Section 2.5 "Reference update modes".

- When an outside-of-thresholds (OT) event is enabled in the SDCD configuration register, a motion detection interrupt is generated whenever the input signal is greater in magnitude than the upper or lower threshold for the set debounce time (see Section 2.3 "Programmable debounce counter" for more details). In this example, the debounce counter is set to zero and the interrupt is generated as soon as the condition evaluates to true.
- When a within-thresholds (WT) event is enabled in the SDCD configuration register, a motion detection interrupt is generated whenever the input signal is between the upper and lower thresholds.

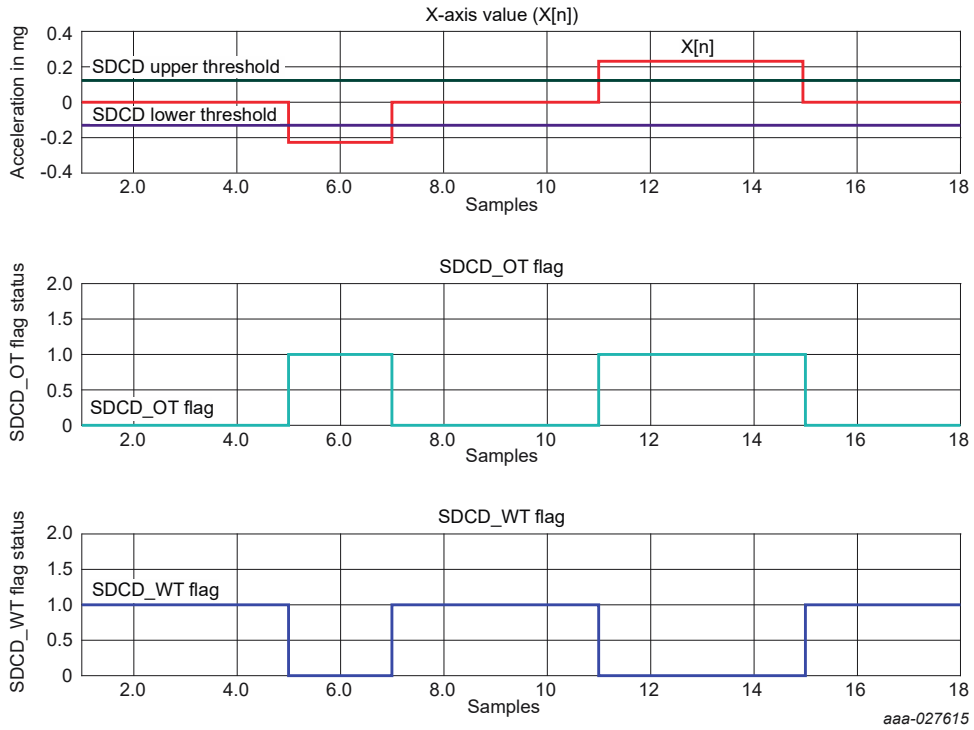

Figure 1. Outside-of-thresholds and within-thresholds event

Note: *The SDCD OT and WT interrupts can be triggered in real time or in latched mode. Details on interrupt logic are described in* Section 2.4 "Interrupt logic".

Block Diagram

The high level SDCD block diagram is shown in Figure 2.

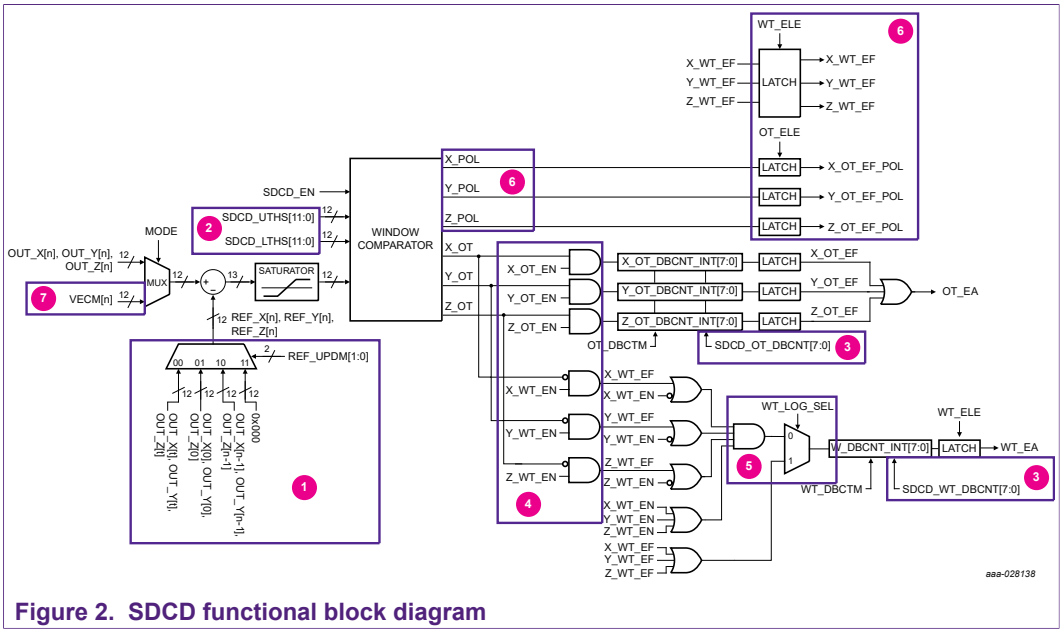

Figure 2. SDCD functional block diagram

Figure 2 numerically identifies key features. The key features are described as:

1. Relative or Absolute SDCD modes. Refer to Section 2.5 "Reference update modes".
2. Programmable upper or lower thresholds. The sensitivity of the threshold registers is same as the device's sensitivity for the currently selected full scale range (FSR).
3. Independent programmable debounce counters for both OT and WT event conditions. The counter time step is equal to the currently selected output data rate (ODR) period for the device.
4. Independent selection of axes for OT and WT interrupt logic.
5. WT event logic selection (AND/OR) for the enabled axes.
6. Event polarity detection and interrupt latching feature.
7. Vector magnitude result can be optionally used as an input to the SDCD function using the X-Axis channel.

2.2 Programmable thresholds

The SDCD block's upper and lower thresholds are encoded in 12-bit 2's complement format from addresses 33h to 36h (see Table 1). The scaling for the threshold registers is the same as the sensitivity of the selected FSR. The FSR is configured in the SENS_CONFIG1 (15h) register.

Example: If FSR is set to ±16 g mode, 1 LSB in the SDCD threshold register corresponds to 7.81 mg.

Threshold in mg = Threshold in counts × sensitivity

Note: *The SDCD_UTHS[11:0] must always be set to a higher value than SDCD_LTHS[11:0] to ensure the SDCD circuit functions correctly and produces meaningful results.*

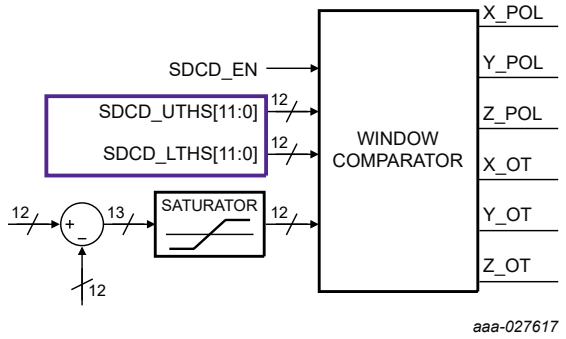

Figure 3. Programmable thresholds

Table 1. SDCD programmable threshold registers

Name	Address	Access	Comment	Accessibility
SDCD_LTHS_LSB	33h	R/W	SDCD lower threshold value LSB - sdcd_lths[7:0]	Read: always Write: Standby mode only
SDCD_LTHS_MSB	34h	R/W	SDCD lower threshold value MSB - sdcd_lths[11:8].	Read: always Write: Standby mode only
SDCD_UTHS_LSB	35h	R/W	SDCD upper threshold value LSB - sdcd_uths[7:0]	Read: always Write: Standby mode only
SDCD_UTHS_MSB	36h	R/W	SDCD upper threshold value MSB - sdcd_uths[11:8]	Read: always Write: Standby mode only

2.3 Programmable debounce counter

Two sets of programmable debounce counter registers, SDCD_OT_DBCNT and SDCD_WT_DBCNT, are available for OT and WT event detection. The counter step period is equal to the selected ODR period in low power mode (LPM) and high performance mode (HPM) modes, and to the effective ODR period (measurement + idle time) in flexible performance mode (FPM) mode.

Note: *When BT_MODE = VDD, the use of HPM and FPM modes is not advised. Use only the default LPM mode.*

Debounce period (ms) = Debounce count × (1/ODR(Hz))

These registers set the minimum number of debounce counter periods needed to recognize an SDCD event condition as true.

For example, when ODR = 100 Hz (10 ms period), and debounce count for the OT event is 5, then the debounce time period is 5 × 10 = 50 ms.

A transition from Standby to Active, Active to Standby, or Auto-WAKE/SLEEP mode automatically resets the internal SDCD OT and WT counters.

Table 2. SDCD programmable timer registers

Name	Address	Access	Comment	Accessibility
SDCD_OT_DBCNT	31h	R/W	Debounce count threshold register for SDCD OT event detection.	Read: always Write: Standby mode only
SDCD_WT_DBCNT	32h	R/W	Debounce count threshold register for SDCD WT event detection.	Read: always Write: Standby mode only

Example: Consider the graph shown in Figure 4, showing the OT event enabled, ODR is set to 100 Hz and debounce time is set to 20 ms (i.e. SDCD_OT_DBCNT equals 2). Thus, when the input signal is greater than the SDCD threshold for the set debounce time period, an interrupt is flagged.

When the debounce count is set to 0 (Figure 1), the interrupt is generated as soon as the input signal meets the threshold criteria for the OT or WT events. The interrupt is also cleared as soon as the condition becomes false.

Debounce count behavior:

Note: *The debounce counter can be decremented without clearing the interrupt.*

The debounce counters can be programmed to either decrement or clear once the event condition becomes false. See examples below. The debounce counter behavior is selected using the OT_DBCTM and WT_DBCTM bits in the SDCD_CONFIG2 (address 30h) register.

Table 3. SDCD_CONFIG2 register

Bit	7	6	5	4	3	2	1	0
Read	SDCD_EN	REF_UPDM[1:0]		OT_ DBCTM	WT_ DBCTM	WT_ LOG_SEL	MODE	REF_UPD
Write								
Reset (BT_MODE = 0)	0	0	0	0	0	0	0	0
Reset (BT_MODE = 1)	1	1	0	1	1	0	0	0

In case 1, the debounce counter behavior is set to clear the event flag as soon as the condition becomes false.

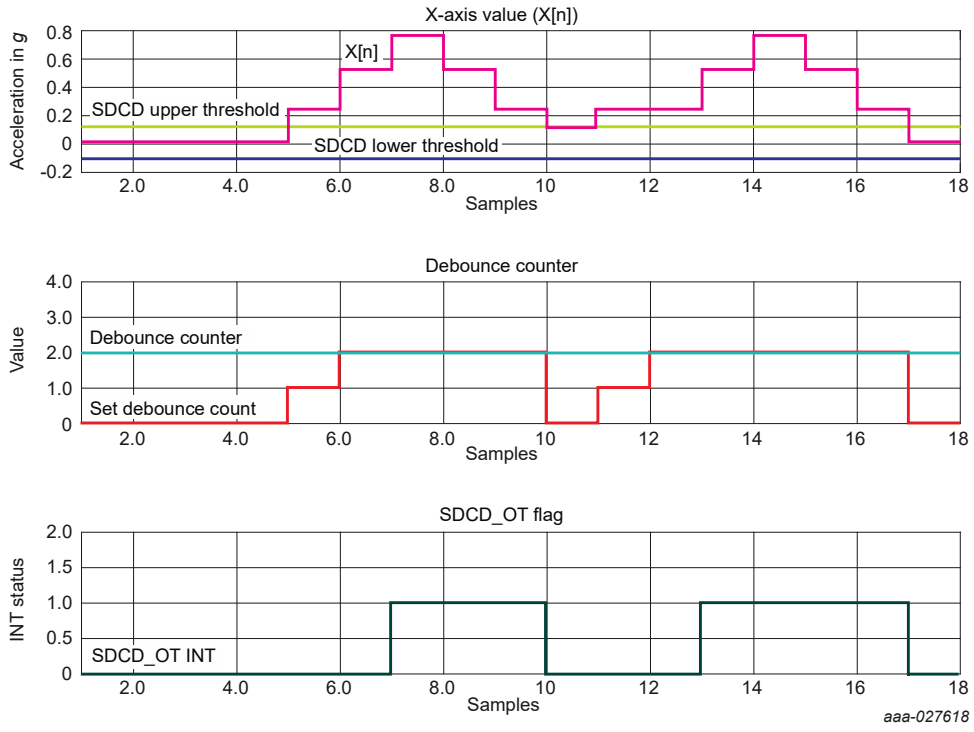

Figure 4. Case 1: Debounce behavior set to clear

With case 2, the debounce behavior is set to decrement. If the condition evaluates to false, the interrupt doesn't clear immediately but instead the debounce count decrements on every ODR period where the condition does not evaluate to true. Once the debounce counter reaches zero, the interrupt is cleared.

Note: *In both cases, the interrupt event flag is not latched and reflects motion detection interrupts in real time. Further details on the interrupt generation logic are provided in* Section 2.4 "Interrupt logic".

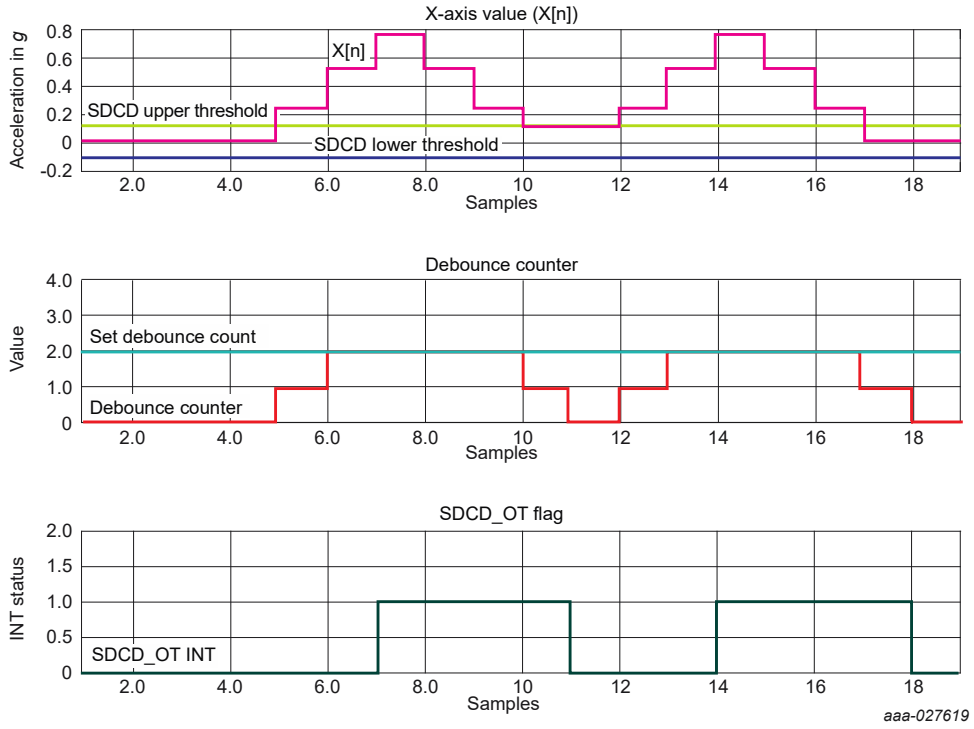

Figure 5. Case 2: Debounce behavior set to decrement

2.4 Interrupt logic

Interrupt generation for OT and WT events can be enabled independently for each axis. This is done using the X/Y/Z_OT_EN and X/Y/Z_WT_EN bits in the SDCD_CONFIG1 register (address 2Fh)

Table 4. SDCD_CONFIG1 register

Bit	7	6	5	4	3	2	1	0
Read	OT_ELE	WT_ELE	X_OT_EN	Y_OT_EN	Z_OT_EN	X_WT_EN	Y_WT_EN	Z_WT_EN
Write								
Reset BT_MODE = 0	0	0	0	0	0	0	0	0
Reset BT_MODE = 1	0	0	1	1	1	0	0	0

Event latching:

Setting the OT_ELE, WT_ELE bits in the SDCD_CONFIG1 register latches the event interrupt. Once the interrupt is latched, the event flags (X/Y/Z_OT_EF, X/Y/Z_WT_EF) in the SDCD_INT_SRC1/2 registers can only be cleared by reading these interrupt source registers. Note that when latching is enabled, the event flag is only asserted when the event condition transitions from false to true, meaning once the event flag is

set, the event condition must first become false before a subsequent true event can be recognized again.

Figure 6 illustrates the interrupt behavior when latching is enabled or disabled. In this example, the outside-of-thresholds event is enabled and debounce count is set to zero.

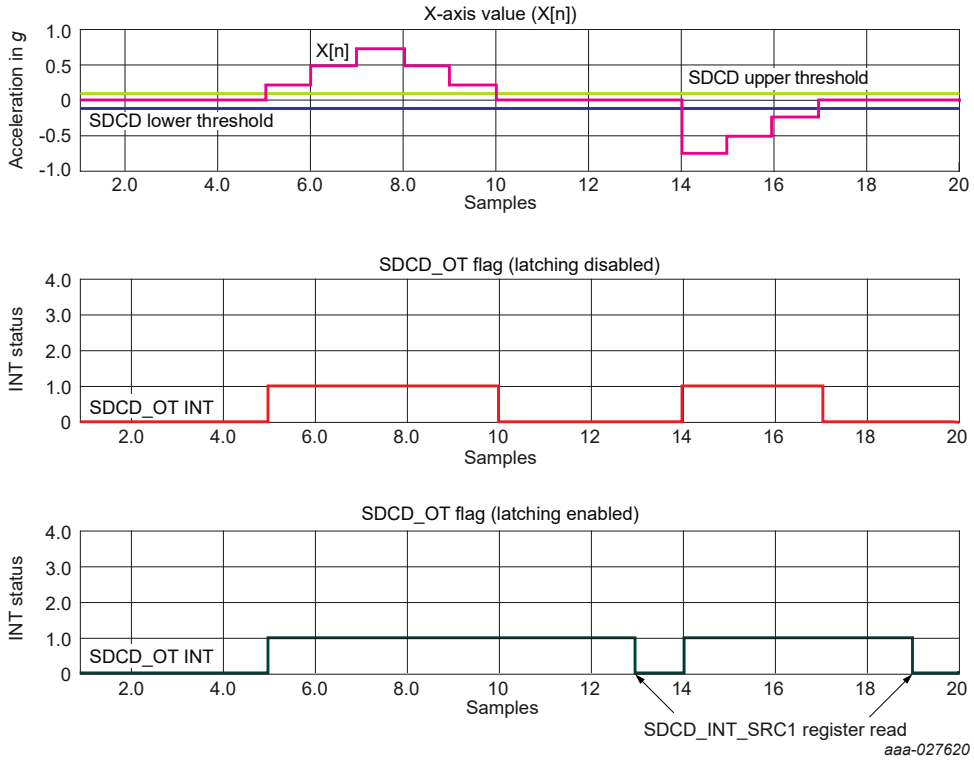

Figure 6. Interrupt latching

Interrupt usage when BT_MODE pin state = VDD or GND

Table 5 contains parameters worth noting while using interrupts from the SDCD block.

Table 5. Interrupt usage

Parameter	BT_MODE=VDD	BT_MODE=GND
Default interrupt configuration	Open drain	Push-pull
Interrupt polarity	Active low. Falling edge marks event detection	Active high. Rising edge marks event detection
Pin routing	Motion detection interrupts can only be routed to INT1 pin as only boot interrupt can be routed to INT2.	Motion detection interrupts can be routed to either INT1 or INT2 pins
ODR	Max ODR is 100 Hz because the data ready interrupt is signalled for $T_{PULSE-MOT}$ seconds (5 ms typ) for every data sample.	No limitation
Interrupt latching	If interrupt is latched, the physical interrupt will pulse for only 5 ms and will retrigger again in the next ODR period (if interrupt flag is still uncleared)	No such pulsing behavior for interrupt.

Logic selection

The WT_LOG_SEL bit in the SDCD_CONFIG2 register allows to do logical decisions (AND/OR) on the enabled axes. An example of use of this feature is detecting freefall (see Section 3), where a "within" threshold event has to be detected on all three axes at the same time for an interrupt to be triggered. The logical AND condition would be the appropriate WT logic setting for this use case.

2.5 Reference update modes

The input to the window comparator is the difference between the current acceleration value and a programmable reference value as shown in Figure 7. Depending on the selected reference update mode, a corresponding reference value will be chosen. The mode selection is effected through the REF_UPDM[1:0] bits in the SDCD_CONFIG2 register.

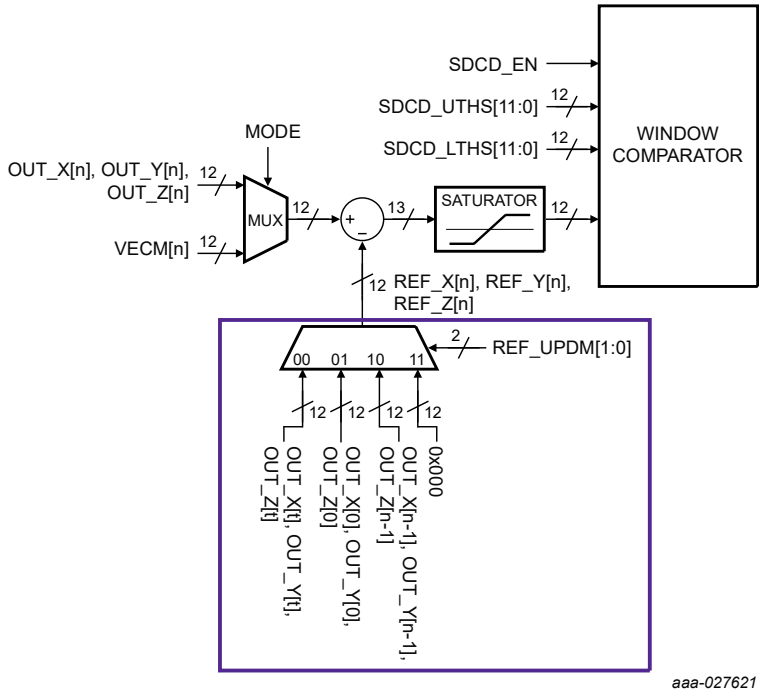

Figure 7. SDCD reference update modes

REF_UPDM[1:0] selection:

- 0b00: The function stores the first 12-bit X/Y/Z decimated and trimmed input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values after the function is enabled (SDCD_EN is set to 1). The REF_X/Y/Z values are updated with the current 12-bit X/Y/Z decimated input data (OUT_X/Y/Z[n]) at the time the SDCD_OT_EA flag transitions from false to true.
- 0b01: The function stores the first decimated and trimmed X/Y/Z acceleration input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values when the SDCD function is enabled; the REF_X/Y/Z values are then held constant and never updated until the SDCD function is disabled and subsequently enabled, or asynchronously when the REF_UPD bit is set by the host.

At any point, the internal reference values can be updated with the current X, Y, Z acceleration values by setting the trigger bit REF_UPD in the SENS_CONFIG2 register.

- 0b10: The function updates the SDCD_REF_X/Y/Z values with the current decimated and trimmed X/Y/Z acceleration input data after the function evaluation. This allows for acceleration slope detection with Data(n) to Data(n–1) to be used as the input to the window comparator. Figure 8 shows the SDCD block usage in relative mode.
- 0b11: The function uses a fixed value of 0 for each of the SDCD_REF_X/Y/Z registers, making the function operate in absolute comparison mode.(Example Figure 1, Figure 4, Figure 5 shows the SDCD block usage in absolute mode)

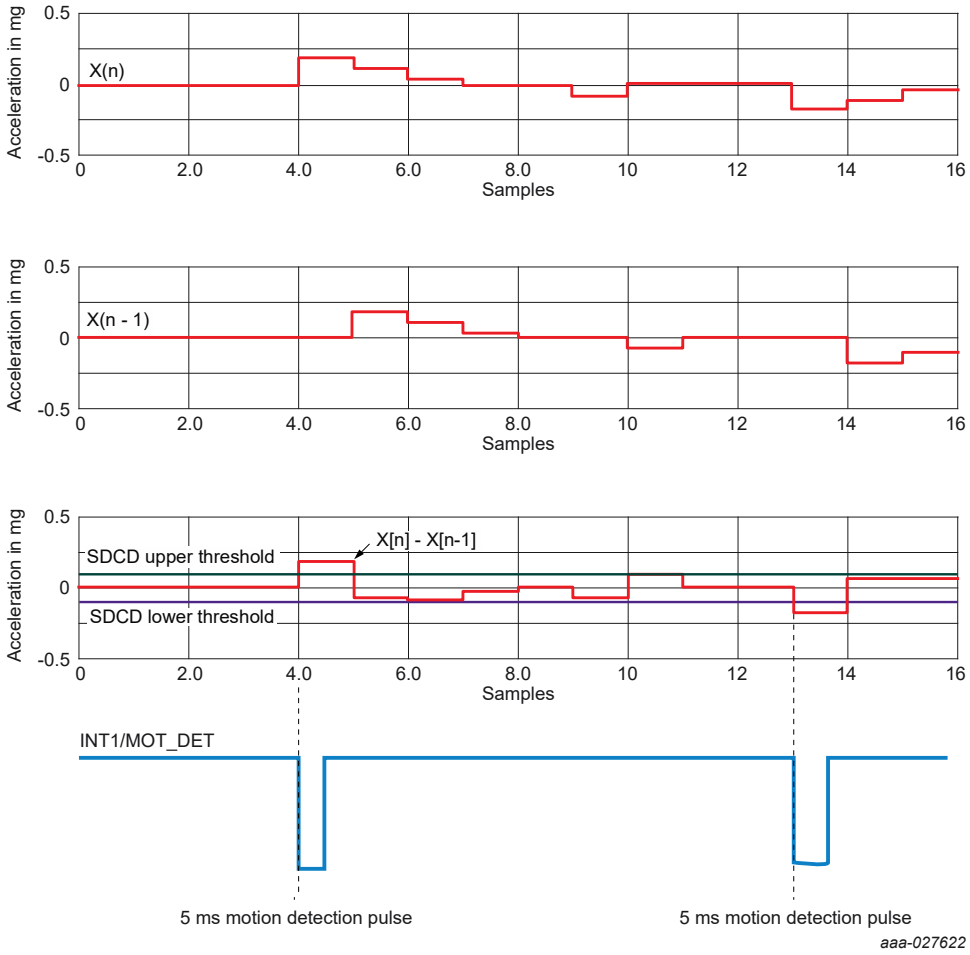

Figure 8. SDCD relative operation mode

Note: *It is possible to use the vector magnitude input to the SDCD block through the X-axis channel. The X-axis channel parameters (X/Y/Z_OT_EN, X/Y/Z_WT_EN) have to be used to act on the vector magnitude signal. The vector magnitude result is used as an input as soon as the MODE bit in SDCD_CONFIG2 register is set, and the vector magnitude function is enabled by setting SENS_CONFIG5[VECM_EN] = 1.*

3 Example use cases

This section illustrates five popular dynamic motion based use cases (Table 6) and will cover sample register configuration steps (with BT_MODE = GND) and device behavior for each case.

Table 6. SDCD configurations for example use cases

Trigger	Shake	Motion to No-Motion	Twist	Free-fall	Jerk/ Transient/Tap
Application	**Smart Inhaler**	**Smartwatch deep sleep mode**	**Smartwatch wake mode**	**Human fall detection**	**Smartwatch menu cycling**
Action	**Indicate to the user to shake the unit well before use**	**Deactivate Smartwatch display**	**Activate Smartwatch display**	**Send out a medical alert**	**Cycle through menu items**
OT/WT	OT	WT	WT	WT	OT
Axes Enabled	X	XYZ	XZ	XYZ	XYZ
WT_LOG_SEL	OR	AND	AND	AND	OR
Ref_updm	0b11 (absolute)	0b10 (Relative N-(N-1))	0b01 (Relative-fixed Ref)	0b11 (absolute)	0b10 (Relative N-(N-1))
UTHS	2.5 g	0.1 g	-1 g	0.2 g	2 g
LTHS	-2.5 g	-0.1 g	-3 g	-0.2 g	-2 g
Debounce	10 ms	2.55 s	10 ms	100 ms	0
ODR	400 Hz	100 Hz	200 Hz	100 Hz	25 Hz

3.1 Shake event detection

Example use case: Smart Inhaler - Indicate to the user to shake the unit well before use.

Motion and its signature:

A typical shake motion is unidirectional and involves four consecutive side to side shake movements of the device,each indicated by four half sine signatures on the shake axis (X Axis in this case). To detect the signature, a reasonably high data rate (400 Hz) is required and the SDCD block can be operated under absolute mode with threshold levels set to ±2.5 g for identifying a shake event.

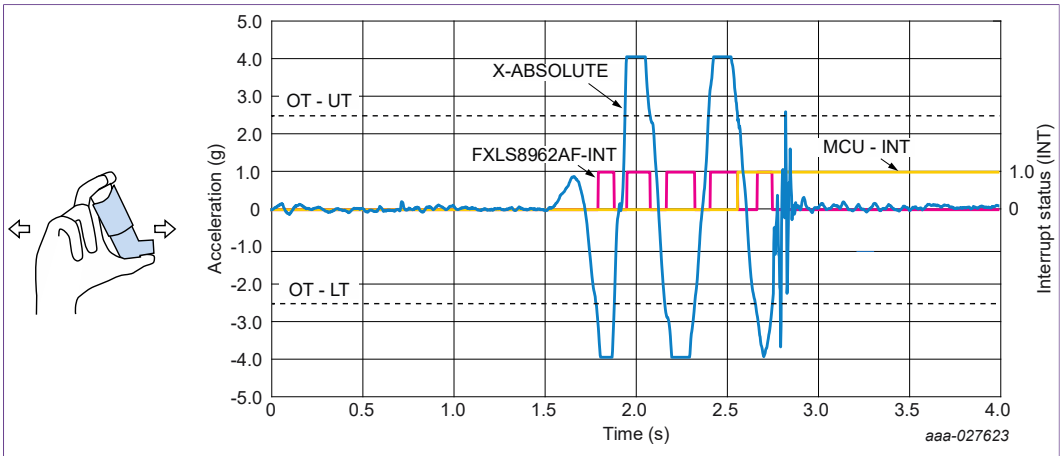

Figure 9. Shake motion and its signature

Table 7. Register configuration for shake motion event detection

Register	Value	Description
15h	02h	FSR = 4 g and Standby mode
17h	33h	Wake ODR = 400 Hz and Sleep ODR = 400 Hz
2Fh	20h	Enable X axis only for SDCD OT function
30h	F0h	Enable SDCD function, Enable Absolute Reference Mode and set OT Debounce counter to clear immediately when threshold criteria is false
31h	04h	Debounce time = 4 × (1/400) = 10 ms
33h	FEh	*Registers 33h and 34h set the OT LOWER threshold. In this case it is set to hex2dec (FAFE) × 1.95 mg/LSB =* ***-2.5 g*** *(1.95 mg/LSB in 4 g mode).*
34h	FAh	
35h	02h	*Registers 35h and 36h set the OT UPPER threshold. In this case it is set to hex2dec (0502) × 1.95mg/LSB =* ***+2.5 g***
36h	05h	
20h	A0h	Enabling DRDY_EN and SDCD_OT_EN
21h	80h	Routing DRDY interrupt to INT2 pin
15h	03h	FSR = 4 g and ACTIVE = 1

Observation:

The SDCD block triggers an interrupt every time the threshold of ±2.5 g was met (with debounce time of 10 ms) and MCU can generate an interrupt after receiving four consecutive interrupts from FXLS896xAF/FXLS897xCF which denotes the shake gesture.

3.2 Motion to no-motion event detection

Example use case: Put the MCU in smartwatch to deep sleep mode when the device is at rest.

Motion and its signature:

The transition from motion to no motion is a relatively simple activity to detect compared to other activities. WT detection in the SDCD block can be used on the axes in relative mode for a set debounce time to determine if no motion had occurred. In this example, to detect a motion to no-motion event, WT value of ±100 mg is used and the debounce

count is set for at least 255 consecutive samples. When ODR=100 Hz, debounce time equals 2.55 s, meaning when there is no activity for 2.55 s, an interrupt is triggered.

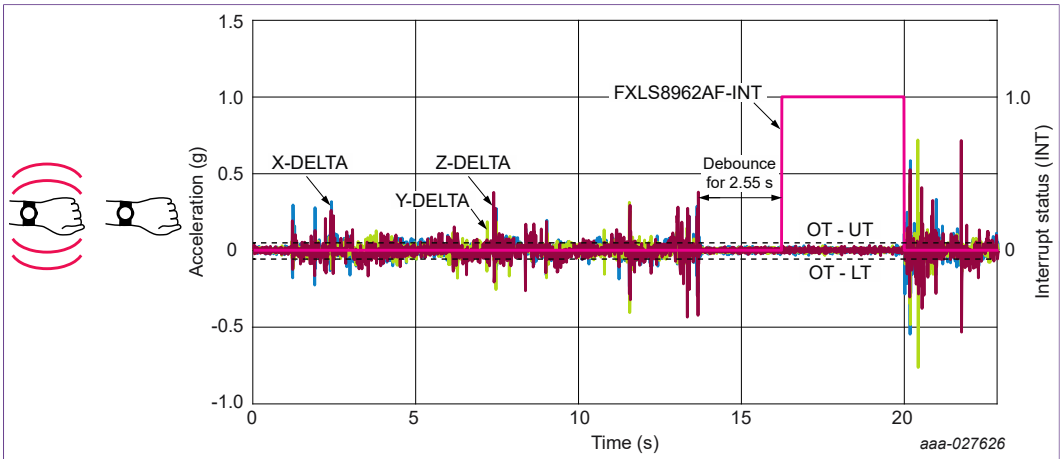

Figure 10. Motion to no-motion event detection

Table 8. Register configuration for motion to no-motion event detection

Register	Value	Description
15h	02h	FSR = 4 g and Standby mode
17h	55h	Wake ODR = 100 Hz and Sleep ODR =100 Hz (Reg 16h = 00h low power mode by default)
2Fh	07h	Enabling SDCD WT for all 3 axes X, Y, Z
30h	C8h	Enabling SDCD and Relative Data (N) – Data (N-1) mode for motion to no-motion detection
32h	FFh	Debounce time is 255 samples corresponding to 2.55 s for setting and clearing motion to no-motion event detection
33h	CCh	*Registers 33h and 34h set the OT LOWER threshold. In this case it is set to hex2dec (FFCC) × 1.95 mg/LSB =* ***–100 mg*** *(1.95 mg/LSB in 4 g mode).*
34h	FFh	
35h	34h	*Registers 35h and 36h set the OT UPPER threshold. In this case it is set to hex2dec (0034) × 1.95 mg/LSB =* ***+100 mg***
36h	00h	
20h	90h	Enabling DRDY_EN and SDCD_WT_EN
21h	80h	Routing DRDY interrupt to INT2 pin
15h	03h	FSR = 4 g and ACTIVE = 1

Observation:

The SDCD block triggers a rising interrupt when the threshold of < ±100 mg is met (with debounce of 255 samples).

3.3 Twist motion event detection

Example use case: Turn on smartwatch display screen by twisting the hand.

Motion and its signature:

A typical twist motion involves acceleration in any two orthogonal axes. For example, in a smartwatch use case, the two axes in the accelerometer are under motion for a twisting activity as follows:

- Z- and X-axis showing activity, with the Y-axis remaining relatively stationary
- Z- and Y-axis showing activity, with the X-axis remaining relatively stationary

As shown in Figure 11, when delta values (nth and the initial reference sample) are plotted for the axes, a typical twist motion would show X and Z values having a delta of ~–1 g to –3 g from their initial reference position (polarity of thresholds depends on axis orientation and should be determined accordingly).

For a twist activity based smartwatch display application, the suitable reference position would occur when the wrist is facing up and parallel to the ground (where X and Y reads 0 g and Z reads 1 g). Since this reference position is fixed, REF_UPDM[1:0]=01h is the reference update mode that can be used in the SDCD block.

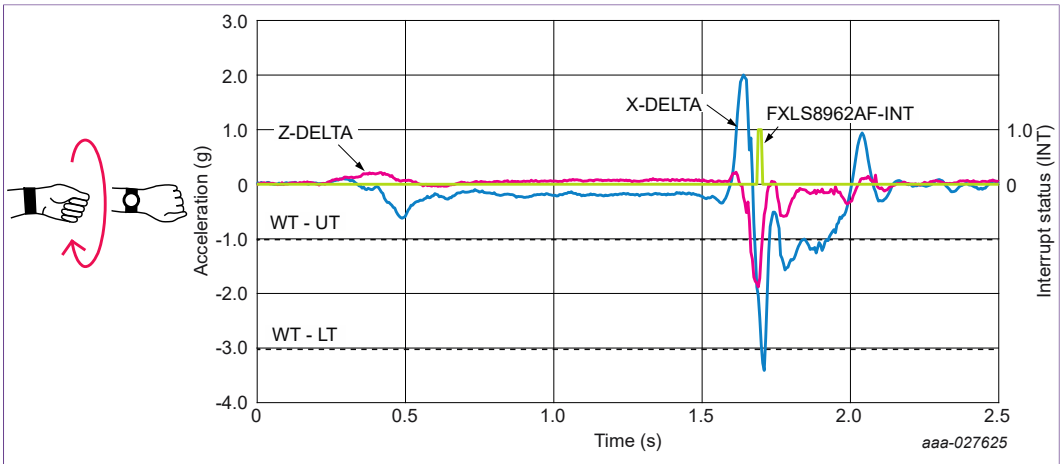

Figure 11. Twist motion and its signature

Table 9. Register configuration for twist motion event detection

Register	Value	Description
15h	02h	FSR = 4 g and Standby mode
17h	44h	Wake ODR = 200 Hz and Sleep ODR = 200Hz (Reg 16h = 00h low power mode by default)
2Fh	05h	Enable X and Z axis only for SDCD WT function
30h	A8h	Enabling SDCD function, WT logical AND, relative fixed reference mode and set WT Debounce counter to clear immediately when threshold criteria is false.
32h	02h	Debounce time = 2 × (1/200) = 10 ms
33h	FEh	*Registers 33h and 34h set the OT LOWER threshold. In this case it is set to hex2dec (F9FE) × 1.95 mg/LSB =* ***–3g*** *(1.95 mg/LSB in 4 g mode).*
34h	F9h	
35h	00h	*Registers 35h and 36h set the OT UPPER threshold. In this case it is set to hex2dec (FE00) × 1.95 mg/LSB =* ***–1g***
36h	FEh	
20h	90h	Enabling DRDY_EN and SDCD_WT_EN
21h	80h	Routing DRDY interrupt to INT2 pin
15h	03h	FSR = 4 g and ACTIVE = 1

Observation:

FXLS896xAF/FXLS897xCF triggers an interrupt every time the WT of ~–1 g to ~–3 g is met on X and Z axes simultaneously (with debounce time of 10 ms). This interrupt is an indicator of the twist movement of the wrist from a fixed position.

3.4 Freefall motion event detection

Example use case: Human fall detection.

Motion and its signature:

A typical freefall event would cause all three axes in the accelerometer to read 0 g as the MEMS in the sensor is subjected to zero acceleration during freefall. Thus to detect a freefall event, a WT event detection can be used in SDCD block. The thresholds can be defined as low as ±200 mg and absolute reference mode shall be used. Since we are expecting a WT event in all three axes during freefall, the WT_LOG_SEL bit is set to enable AND logic operation on the axes event flags. Note that debounce time is set to 100 ms to identify the freefall event from a reasonable height.

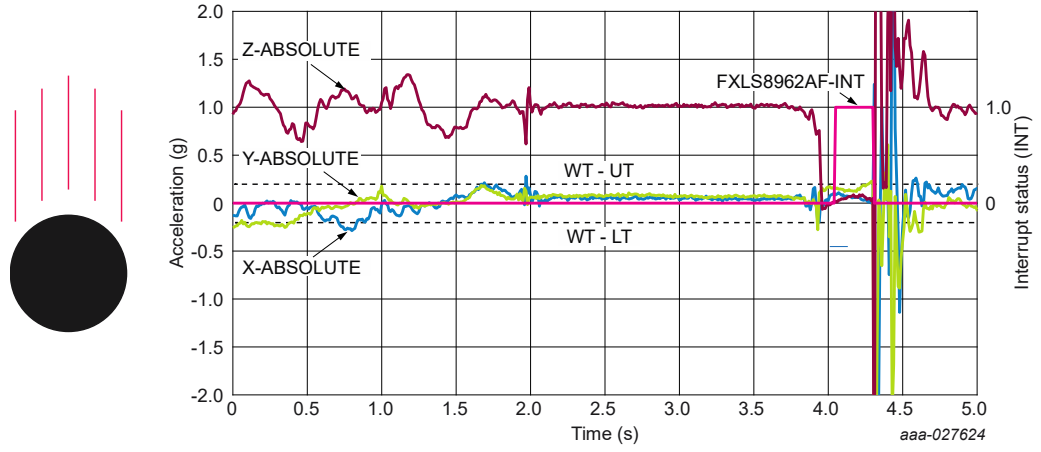

Figure 12. Freefall motion and its signature

Table 10. Register configuration for freefall event detection

Register	Value	Description
15h	02h	FSR = 4 g and Standby mode
17h	55h	Wake ODR = 100 Hz and Sleep ODR = 100 Hz
2Fh	07h	Enabling SDCD WT for all 3 axes X, Y, Z
30h	E8h	Enable SDCD function, enable absolute reference mode and set WT logic selection to AND. Debounce behavior is set to clear immediately when threshold criteria evaluates to false.
32h	0Ah	Debounce time is 10 samples corresponding to 100 ms
33h	99h	*Registers 33h and 34h set the OT LOWER threshold. In this case it is set to hex2dec (FF99)x1.95 mg/LSB =* ***-200 mg*** *(1.95mg/LSB in 4g mode).*
34h	FFh	
35h	67h	*Registers 35h and 36h set the OT UPPER threshold. In this case it is set to hex2dec (0067)x1.95 mg/LSB =* ***+200 mg*** *(1.95mg/LSB in 4g mode).*
36h	00h	
20h	90h	Enabling DRDY_EN and SDCD_WT_EN
21h	80h	Routing DRDY interrupt to INT2 pin
15h	03h	FSR = 4 g and ACTIVE=1

Observation:

FXLS896xAF/FXLS897xCF triggers a rising interrupt when the WT of < ±200 mg is met (with debounce time of 100 ms).

3.5 Transient / tap motion event detection

Example use case: Cycle through the display menu in smartwatch by tapping on it.

Motion and its signature:

A typical transient motion involves a sudden jerk exceeding ±2 g in any of the X-axis, Y-axis and Z-axis with respect to the previous sample as a reference. Thus, the SDCD reference mode REF_UPDM[1:0]=10h is used. This allows for acceleration slope detection with Data(n) to Data(n–1) always used as the input to the window comparator.

Note the FXLS896xAF/FXLS897xCF is configured to go into sleep mode when inactive for more than 0.64 seconds and transitions to wake mode on seeing transient activity as observed from the ‘WAKE=0/SLEEP=1’ trace in Figure 13.

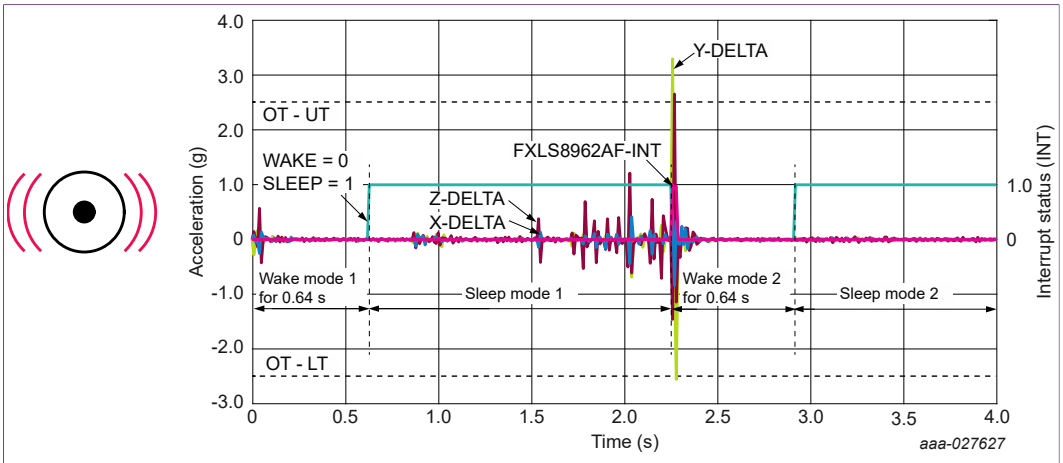

Figure 13. Tap event and its signature

Table 11. Register configuration for transient/tap event detection

Register	Value	Description
15h	02h	FSR = 4 g and Standby mode
17h	57h	Wake ODR=100 Hz and Sleep ODR = 25 Hz
2Fh	38h	Enabling SDCD OT for all 3 axes X, Y, Z
30h	C0h	Enabling SDCD and Relative Data (N) – Data (N-1) mode for transient detection
31h	00h	Debounce time = 0 for transient detection
33h	FFh	*Registers 33h and 34h set the OT LOWER threshold. In this case it is set to hex2dec (FBFF) × 1.95 mg/LSB =* ***–2g*** *(1.95 mg/LSB in 4 g mode).*
34h	FBh	
35h	01h	*Registers 35h and 36h set the OT UPPER threshold. In this case it is set to hex2dec (0401) × 1.95 mg/LSB =* ***+2g***
36h	04h	
20h	A0h	Enabling DRDY_EN and SDCD_OT_EN
21h	80h	Routing DRDY interrupt to INT2 pin
1Eh	40h	***Note:*** *Registers 1Eh and 1Fh enable the ASLP function and set the sleep mode transition timer. In this case it is set to hex2dec (0040) × 10 ms (100 Hz Wake ODR) =* ***0.64 s***
1Fh	00h	
18h	21h	Enable SDCD outside of thresholds event Auto-WAKE/SLEEP transition source enable
15h	03h	FSR = 4 g and ACTIVE = 1

Observation:

FXLS896xAF/FXLS897xCF triggers an interrupt every time the WT of > ±2 g is met (with debounce time of 10 ms) which in turn transitions the part from sleep to wake mode or prevents part from entering sleep mode.

4 Revision history

Table 12. Revision history

Rev	Date	Description
v.2	20201030	• Revised the document title from "FXLS89x2 Sensor Data Change Detection (SDCD) block overview and examples" to "FXLS896xAF / FXLS897xCF Sensor Data Change Detection (SDCD) block overview and example." • Global: revised "FXLS89x2" to "FXLS896xAF and FXLS897xCF" or "FXLS896xAF/ FXLS897xCF" throughout the document.
v.1	20180201	Initial release

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Date of release: 30 October 2020
Document identifier: AN12004