AN10896

Mounting and Soldering of RF transistors in Air Cavity Packages

AMPLEON

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Application note

Document information

Info	Content
Keywords	Air Cavity Packages, heat sink, footprint, surface mount, reflow soldering, component handling, exposed heat spreader, SMDP, NSMDP, bolt down.
Abstract	This application note provides a general mounting recommendation/guideline suitable for Air cavity Packages.

Revision history

Rev	Date	Description
AN10896#8	20250203	Overall revision
AN10896#7	20240523	Overall revision
AN10896#6	20220915	Package “SOT467A” was removed from table 5
AN10896#5	20220202	Overall revision
AN10896#4	20160217	Overall revision, include below modifications: • The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.
AN10896#3	20130607	Added ACP, rework & updated reflow
AN10896#2	20121113	Added notification on use of flux cleaners for air cavity packages in section 5.1 Added G to table 2 (page 23).
AN10896#1	20100504	Initial release

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1. Introduction

1.1 General (mounting recommendations RF power)

This document is intended to guide customers in ways how to solder Air Cavity RF Power transistors. Each customer has its own way of designing applications and mounting the devices, so therefore not possible to cover all specific requirements. The intention of this document is to have a general mounting recommendation/guideline.

1.2 Definition

The following words in this document:

- “Heat sink” refers to the heat sink located under the PCB, the application heat sink forms the part of the thermal path that carries heat away from the device to the cooling air.
- “Exposed heat spreader” is used for plastic molded devices and is designed for attachment to the customer board.
- "Flange" (also a heat spreader) is used for the ACC and ACP and are designed for attachment to the customer board.
- "Eared" is a flange with 2 slotted holes allowing bolt down.
- "Earless" is a flange used for devices that are being soldered.
- "Foot Print or Solder land" refers to the area on which to solder the device.
- “Printed Circuit Board (PCB)” refers to the electrical interconnection between the RF power devices and other electrical components that are part of a PA.

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1.3 Main product groups

This document covers the different Air cavity packages families offered by Ampleon and is divided in two main product groups: “Air Cavity Ceramic” (ACC) and “Air Cavity Plastic” (ACP).

1.3.1 ACC (Air Cavity Ceramic packages)

The traditional package for RF power transistors is the ACC with a ceramic lid. The package is made of three main parts: flange, ringframe and lid. The flange is brazed with the ringframe at high temperature and the resulting component is known as a header. After assembly (die and wires) the package is closed by gluing the lid on top.

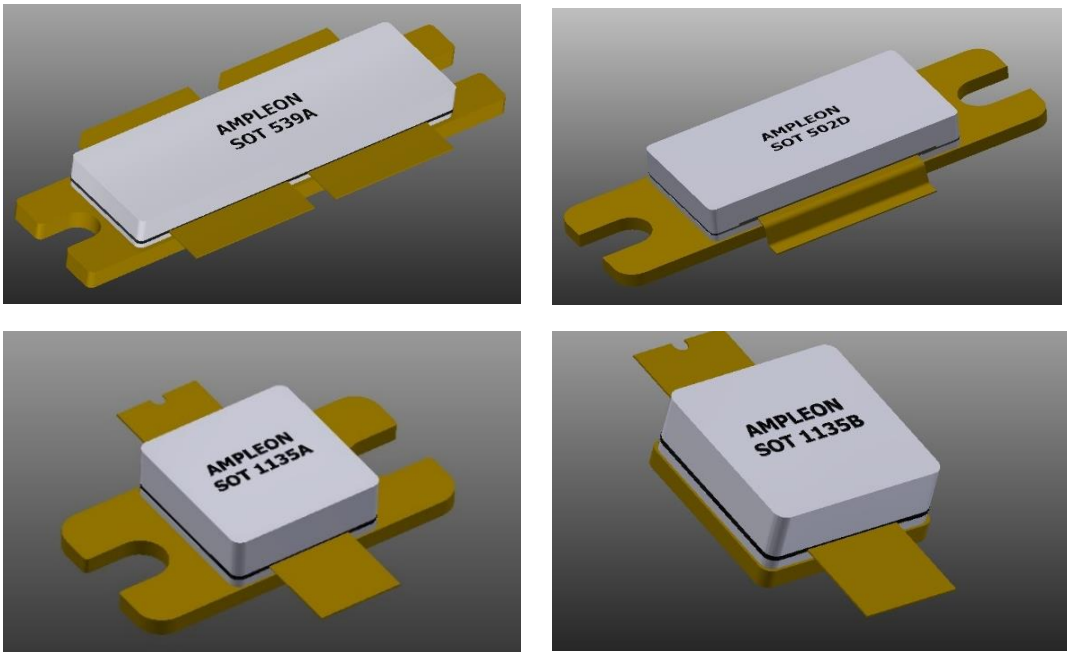

Figure 1. Typical ACC packages; Ear- and Ear-less, straight and gullwing leads

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1.3.2 ACP (Air Cavity Plastic packages)

The structure of ACP is similar to ACC but the lid and ringframe are glued and are made of a polymer instead of ceramic.

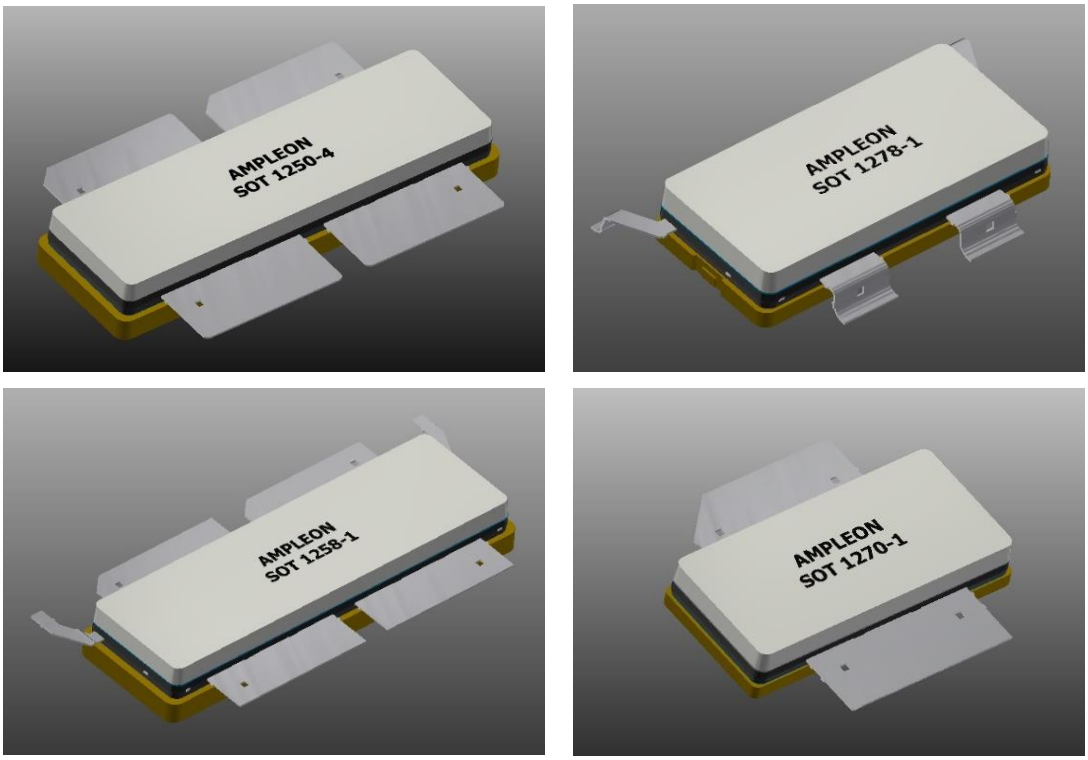

Figure 2. Typical ACP examples Straight-Lead and Gullwing Package types

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2. Application board

Depending on the power management, and device type there are number of different configurations, below some of the most common ones.

2.1 Straight leads packages

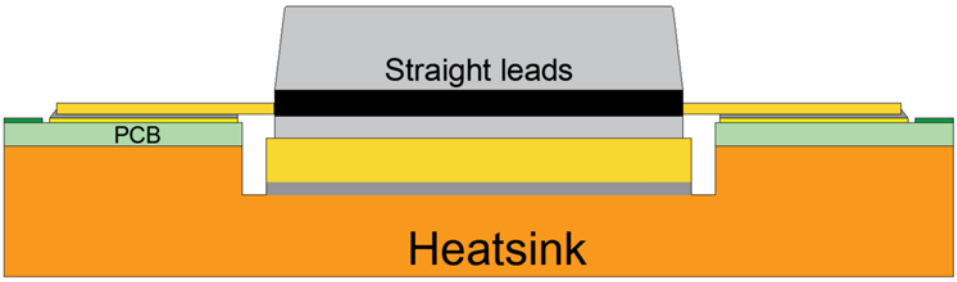

Figure 3. PCB bonded to a heat sink with a cavity, intended for straight leads package

2.2 Gullwing packages

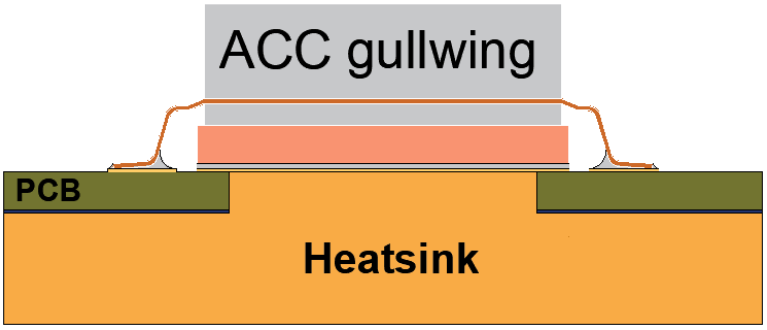

Figure 4. PCB bonded to a heat sink with a pedestal, intended for gullwing high-power packages

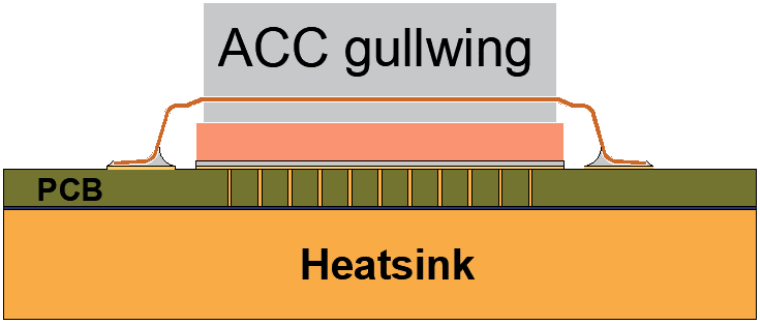

Figure 5. PCB with vias bonded to a heat sink, intended for gullwing low-power packages

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3. Board design

3.1 PCB land pad design

Design should satisfy requirements for electrical, thermal and reliability performance, board level assembly and board level testing.

The dimensions given in this section are for the solderable portion of the PCB /package.

3.1.1 Straight leads packages

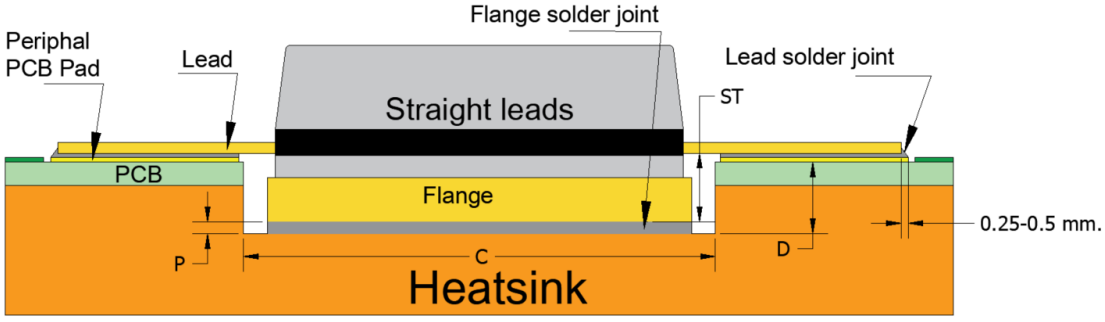

Figure 6. Straight leads package cross section

Looking to the cross-section view of an air-cavity package (Figure 7) we recommend the outside edge of the solder pad should be longer than the outside tip of the leads by a minimum of 0.25 mm.

The pad area should be at least 0.15 mm from the edge of the cavity (pull back), PCB manufacturer should provide a design rule on this dimension.

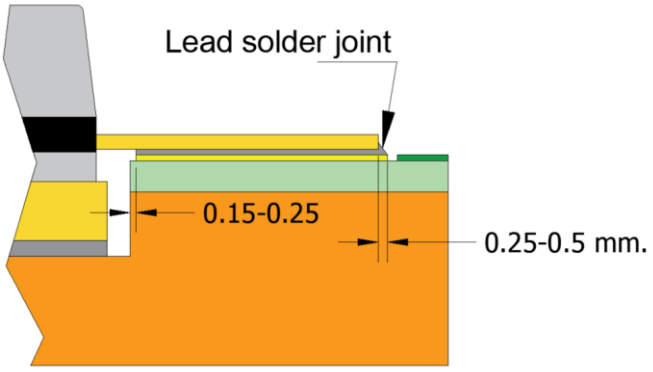

Figure 7. Straight leads package cross section view detail

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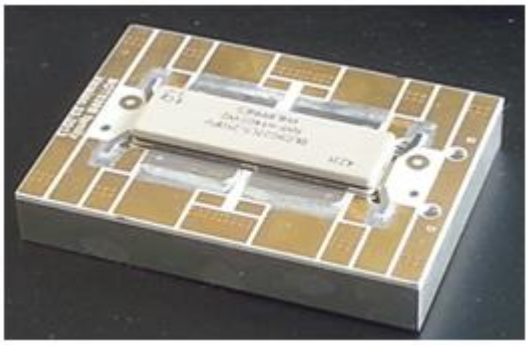

Figure 8. Example of a straight leads package on a test board

3.1.1.1 Heatsink cavity

The heat sink design depends primarily on dissipated heat and on the other components located on the PCB. These vary from one application to another, therefore no general recommendations on the size and thickness of the heat sink.

The package body is placed through an aperture in the PCB onto the heat sink.

The dimensions of the aperture in the PCB should be such that the package can be easily inserted through it by manual or automatic processes.

Cavity width/length opening (Figure 9).

C= Nominal cavity aperture dimension (X&Y directions) = Maximum package body size + Pick & Place placement capability + cavity tolerance/2.

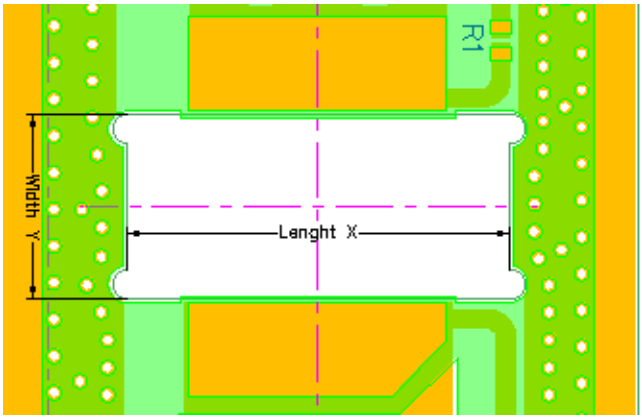

Figure 9. PCB Cavity aperture X & Y directions

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Heatsink cavity depth (D) = Package Stand off (ST) + Preform thickness (P) – solder thickness under lead (L) - Gap lead to solder before reflow (G).

Typical recommended values:

- Preform thickness (P) = 200 - 400 microns.
- Solder thickness under lead (L) = 150 microns.
- Gap lead to solder before reflow (G) = 0 to 100 microns.

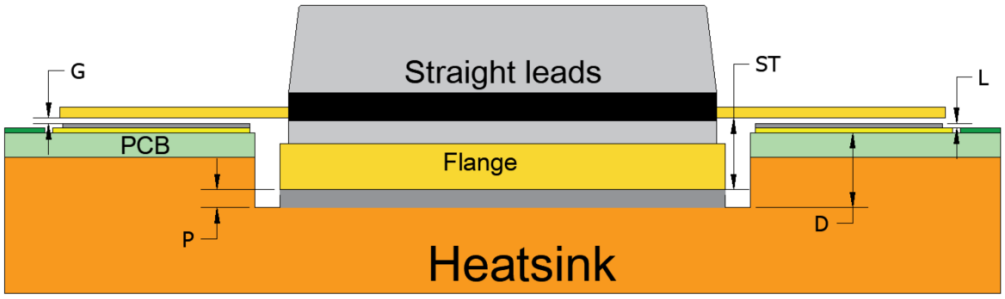

Figure 10. Heatsink cavity depth

Due to its importance factor on product performance and product reliability this dimension tolerance should be minimized as much as possible, Ampleon recommends a maximum cavity depth tolerance of +/- 0.08 mm.

We also advice to limit bottom surface roughness (Ra < 6 microns).

All of these parameters will vary due to their tolerances. Determining the cavity depth is a simple calculation of a worst-case tolerance stack up; however, it might end up in a value simply too large for normal production (the leads will likely lay too high above the PCB).

A more common approach is to make use of the Square Root of Sum of the Square method. Use the actual distribution of all valid parts, in case these are not available take the actual specification.

3.1.2 Gull wing packages

Looking to the cross section view of a Gullwing package (Figure 11) we recommend to extend PCB heel and toe extensions pads 0.25 to 0.50mm, this will allow a good filet at both sides of the lead.

A larger heel pad may cause an excess solder condition on the inside of the lead reducing flexibility and increasing stresses on the solder joint.

Pad width should be approximately 60 % of the lead pitch, in case of single lead, PCB pad should be extended 0.125mm to both sides.

Soldering of Gullwing package should ensure proper contact on the governing interfaces. Solder thickness on pad and leads should consider the package's outline drawing tolerances such as Q-height, Lead angle and Gauge plane as presented in Figure 12. Force application during attachment and/or soldering jig may also help to ensure proper contact on the governing interfaces.

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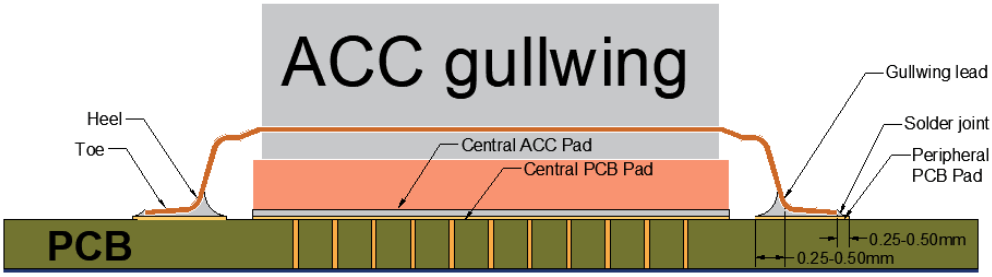

Figure 11. Cross section view of an ACC GW package

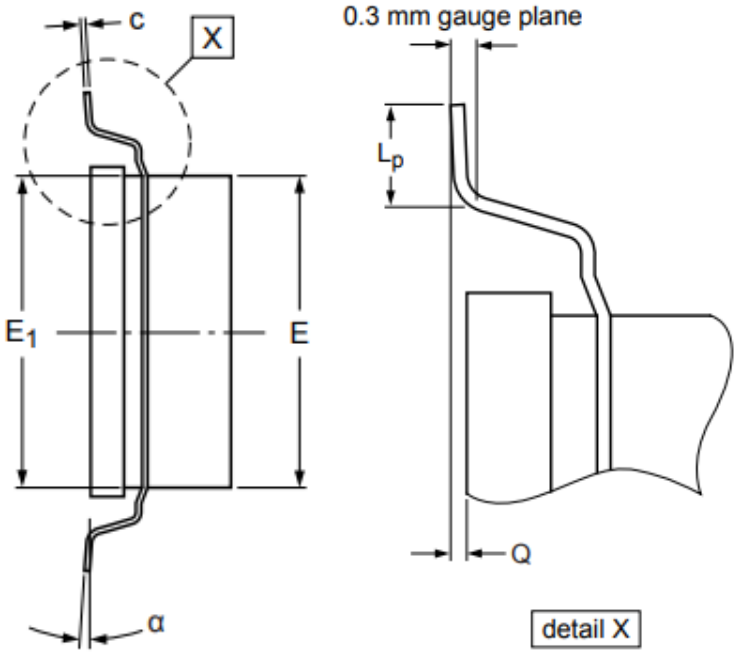

Figure 12. Package outline drawing of ACC GW package

3.2 PCB land pattern solder mask

The industry has two common concepts on the opening of solder resist:

- Non solder mask defined (NSMD) the solder mask openings are larger than the exposed metal pad (Figure 13).
- Solder mask defined (SMD) the solder mask overlaps the underlying metal pad, which is slightly larger than the solder mask opening (Figure 14).

Selection of NSMD versus SMD should be based on complexity of the board design and board supplier capability for solder mask registration and tolerance.

Solder mask design should follow PCB manufacturer design rules, typically the copper to solder mask and solder mask overlap is 0.075 mm.

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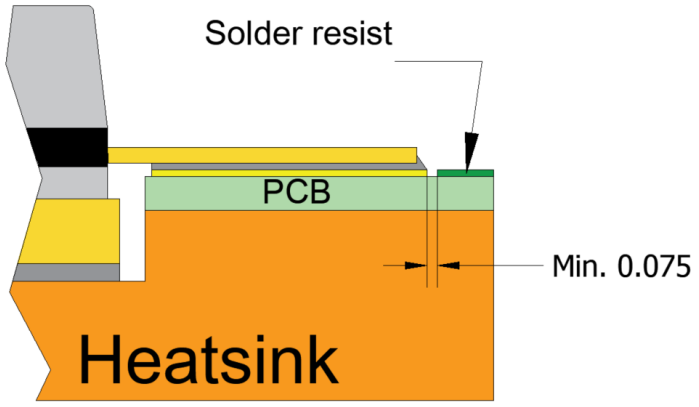

Figure 13. NSMD cross section of a straight leads package

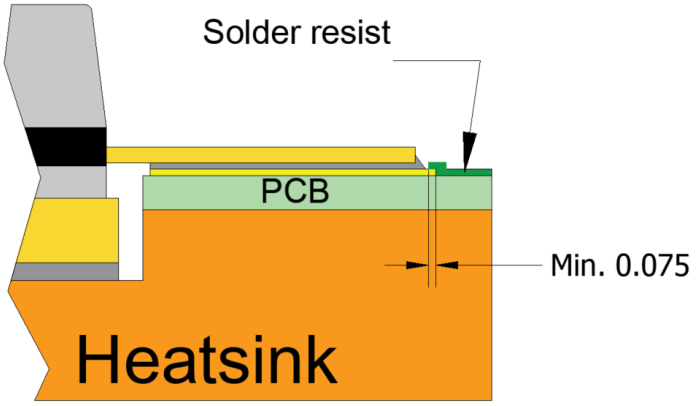

Figure 14. SMD cross section view of a straight leads package

Even if the metal pad on the PCB extends beyond the dimensions, it is recommended that a solder mask dam is used to define the solderable area for the lead (Figure 15). This prevents the solder overflow from the lead and wetting the remaining trace.

Minimum recommended dam width is 0.2mm.

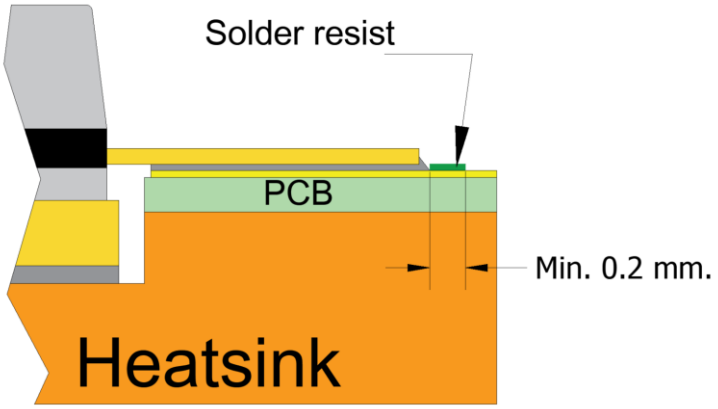

Figure 15. Solder mask dam cross section view a straight leads package

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4. Solder paste printing

For applying solder paste you can use either stencil or silk screen printing techniques taking care of standard process control. The aperture dimensions, that is, the length and width and the depth (the stencil thickness) should be made fit for each package type and balanced according to the used stencil thickness. Stencil thickness is dictated by all components on the board. The aperture length and width should be selected such that it fits the stencil process.

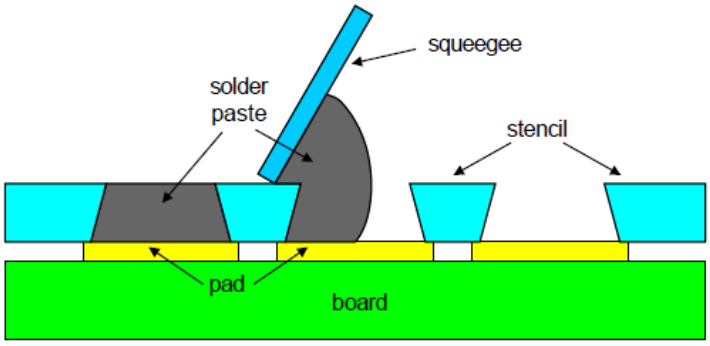

Figure 16. Stencil printing

4.1 Stencil thickness

It is possible to use a stencil that has a different thickness at different locations, an example of this is the step-stencil. This, however, is only recommended if there is no other solution. Stencils (Figure 17) are commonly made from metal Nickel alloy; they may be either electro-formed or laser-cut (preferred).

Typical stencil thickness is given in Table 1.

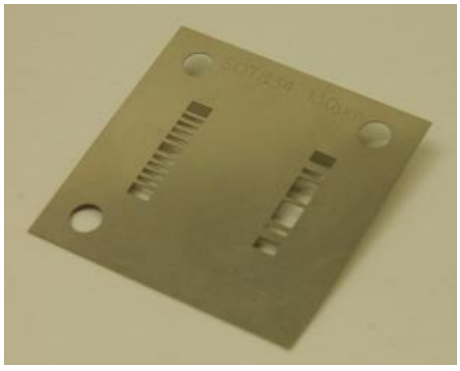

Figure 17. Stencil example

Table 1. Typical stencil thickness

Semiconductor package pitch	Stencil thickness
≥ 0.5 mm	120 μm to 200 μm
0.4 mm to 0.5 mm	100 μm to 125 μm

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In most cases, the package will be mounted on a PCB after the rest of the substrate has been populated. A typical process flow includes:

- Solder paste printing.
- Solder preform placement (where required).
- Component placement (including the OMP package).
- Reflow.
- Inspection.

The height of the solder on the PCB pads will depend on the stencil that was used for printing.

4.1.1 Stencil aperture

A general rule is that the stencil apertures must be 0.025mm smaller than the solder lands, on all sides. In other words, the solder paste lays 0.025 mm inward from the solder land edge. This usually results in stencil aperture dimensions that are 0.05mm smaller than the corresponding solder land dimensions.

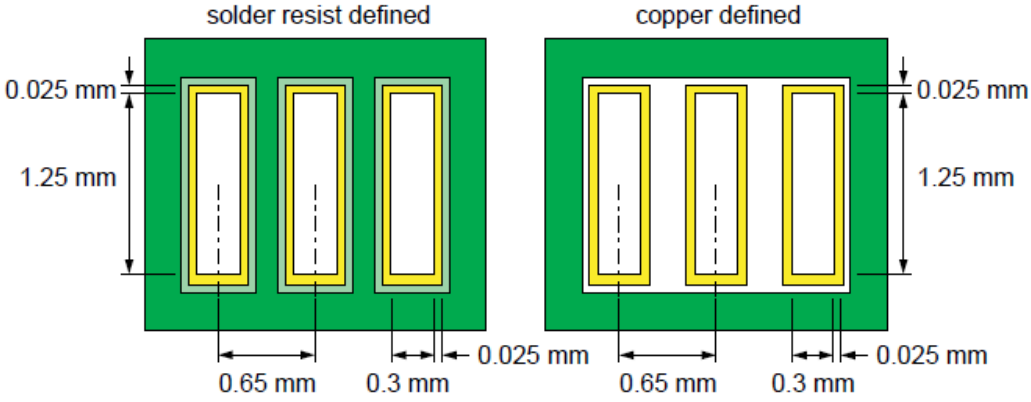

Figure 18. Solder paste printing on NSMDP and SMDP

An exception lies with the very large solder lands, such as when printing solder paste on a heat sink land. In that case, it is advised to print an array of smaller solder paste deposits, these deposits cover approximately 50-80 % of the total land area. It is also advised to keep the solder paste away from the edges of this land. This concept combined with other important factors (solder paste, reflow profile setting and stencil thickness) will allow flux to outgas properly and may help minimize the solder voids. Figure 19 shows an example of solder paste printing straight leads.

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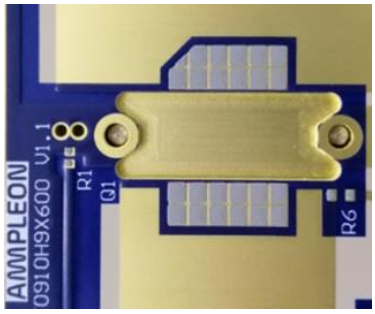

Figure 19. Example of solder paste printing straight leads

Depending on the solder paste used, the solder paste deposits printed on a large land may not always coalesce completely. In some cases, individual solder joints can still be recognized between the exposed die pad and solder land on the board. It is possible that voids remain in the solder joints. Whether or not voids or incomplete coalescing of the solder are a problem, depends on the application.

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5. Solder materials

There are several materials that ensure a good thermal and electrical conductive interface. Table 2 gives a summary of the possible combinations. The cells marked “X” are typically used in the industry while those marked ”O” are optional.

Table 2. Overview of solder pastes and preforms used

Solder type	Air cavity			
	Eared		Earless	
	Leads	Flange	Leads	Flange
Solder paste	X	O	X	O
Solder preform	O	-	O	X
Thermal paste	-	O	-	-

5.1 Solders

In line with European legislation, it is recommended to use a Pb-free solder paste or preform, although exemptions are granted for selected applications.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes/preforms have a wide range of melting temperatures.

As a substitute for SnPb solder, the most common Pb-free paste/preforms used is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 to 4 % of Ag and 0 to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of more than 235 °C (Table 3).

Table 3. Minimum peak temperature for soldering per alloy (JEDEC J-STD-020)

Solder	Melting temperature	Minimum peak reflow temperature (measured at the solder joint)
SAC	217 °C	235 °C
PbSn	183 °C	215 °C

Care should be taken when selecting a solder and note that solder types are categorized by solder sphere size. For small packages or fine pitch applications solder paste type 3 or better are recommended.

A no-clean solder paste or preform does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

Ampleon advises using a preform with pre-applied flux for flange to heat sink attachment. It reduces voids and ensures the required amount of solder. Preforms with pre-applied flux are available in the market.

In case separate flux (manually, like with a brush, pen or dipping) is applied in combination with a preform, extra care needs to be taken not to use excessive amounts of flux. These might increase the chance of voids in the solder joint.

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For more information on the solder paste and solder preforms, please contact your solder supplier.

Flux cleaners

It is not recommended to use flux cleaning fluids for air cavity packages.

No-clean solder paste and no-clean solder wire are recommended, so the PCB and the package do not have to be cleaned after reflow or manual soldering.

5.2 Thermal paste/preform

The eared (bolt down) ceramic packages are typically using a thermal paste or preform to improve the thermal conductivity, meaning better than a metal on metal contact. A “metal to metal” contact area is very small (could be ~ 2 % depending on the roughness). Applying pressure by bolt down will increase this contact area, but still those areas not being in contact are filled up by air, known as a bad heat conductor.

Filling these air pockets with a thermal interface material will increase the contact area further resulting in a better thermal conductivity.

Solder offers the best thermal contact but can create other problems such as trapped flux (voids) and TCE mismatch (bow).

Ampleon does use thermal grease for the evaluation of eared (bolt down) and solder preforms for the earless devices.

For production reasons (efficiency) customers use thermal preforms, such as metal foils (like copper) and graphite containing pads. Point of attention when pads are used:

- Check for galvanic corrosion in the application.
- Keep the pad size close to the size of the backside of the device. Too short pads give additional stress when bolting down the flange and might even cause cracking of the package.
- The hardness and ductility of the thermal preform material should be considered to prevent package stress during the bolt down process.

5.3 Solder amount

This document does not give recommendation about the amount of solder to be used for every type of product, however it is important to take notice of the gold plating. In 9.2.4 the information needed to prevent gold embrittlement can be found.

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6. Reflow soldering procedure

Ampleon advises to use a convection oven rather than a conduction or radiation oven. A convection oven provides a uniform heat and a very controlled temperature (± 2°C). Moreover, it allows soldering a wide range of products due to the temperature uniformity. During the reflow soldering process all parts of the board are subjected to an accurate temperature/time profile.

A temperature profile essentially consists of three phases:

- **Pre-heat:** the board is warmed up to a temperature that lies lower than the melting point of the solder alloy.
- **Reflow**: the board is heated to a peak temperature well above the melting point of the solder, but below the temperature at which the components and boards are damaged.
- **Cooling down:** the board is cooled down, so that soldered joints freeze before the board exits the oven.

The peak temperature during reflow has an upper and a lower limit.

6.1 Lower limit of peak temperature

The minimum peak temperature must at least be high enough for the solder to make reliable solder joints. This is determined by solder paste characteristics; contact your paste supplier for details.

6.2 Upper limit of peak temperature (Body related)

The maximum peak temperature must be lower than the temperature at which the components are damaged. This is defined by MSL testing of the package. The maximum body temperature during reflow soldering depends on the body size and on the demand to respect the package MSL.

The maximum allowed body temperature depends on the package dimension and should be in accordance with the JEDEC recommendations. Table 4 shows the classification temperature (Tc) for a Pb-free process according to JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface Mount Devices).

Table 4. JEDEC J-STD-020 - Tc for a Pb-free process

Pb-Free Process - Classification Temperatures (T_c)			
Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

classification temperature (T_c) – The maximum body temperature at which the component manufacturer guarantees the component MSL as noted on the caution and/or bar code label per J-STD-033.

The package thickness and dimension can be obtained in the package's outline drawing. The recommended maximum body temperature is published in Ampleon's website documentation.

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6.3 Upper limit of peak temperature (Board related)

The maximum peak temperature must be lower at which the boards are damaged.

This is a board characteristic; please contact your board supplier for details.

6.4 Reflow Profile

The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, in which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature, as this would result in component and/or board damage. Even if the cold and hot spots start the reflow phase with roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some tweaking of the oven temperature settings and conveyor belt speeds. In extreme cases, even the board layout may have to be optimised to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. For reflow soldering with SAC, the peak temperature should be higher than 235 ºC.

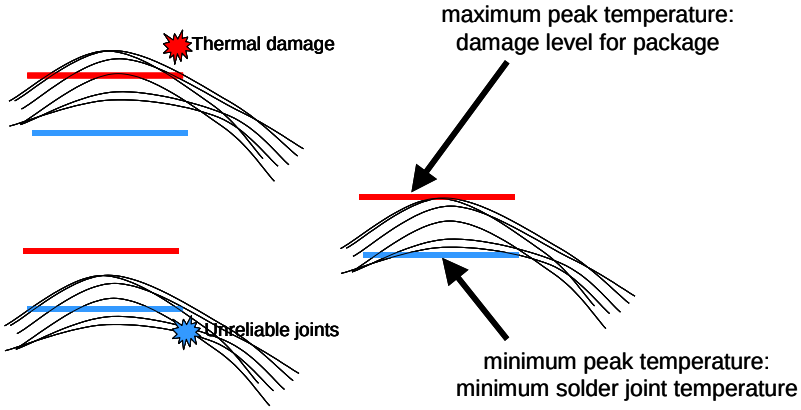

Figure 20. Fitting both the hot and cold spots into the required peak temperature range

The black lines in Figure 20 represent the actual temperature profiles for a number of different spots on a board. The bottom line represents the cold spot, and the top line corresponds to the hot spot. The blue line represents the minimum allowed peak temperature, and the red line is the maximum allowed peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, resulting in damage. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

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6.5 An example of a reflow profile using SAC solder:

The reflow soldering profile should be calibrated with 2 thermocouples on package: one under package flange and one on top package cap to prevent a temperature offset. In addition, a third thermocouple on top of package leads is recommended for further optimization of the profile.

Peak temperature in any of package main parts (leads, flange, and cap) should not exceed recommended Tc values. Exceeding that temperature may degrade the device characteristics or may even damage the device

All reflow activities were performed in a belt oven with an inert atmosphere (Nitrogen - N2). During calibration, the zone temperature and belt speed are varied and the temperature of the device temperature monitored and compared to the JEDEC recommendations (Table 5 and Figure 21) and solder paste supplier recommendations.

Long preheat or soaking time will allow flux to outgas properly and may help minimize the solder voids of a typical Pb-free solder paste.

Table 5. SAC Reflow profile classification (JEDEC J-STD-020)

Profile Feature	Pb free Assembly (SAC alloys)
Preheat Soak • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{min} to Ts_{max}) (ts)	 • 150 ºC • 200 ºC • 60 – 120 seconds
Ramp-up rate (T_L to T_P)	3 ºC/second max
Time 25 ºC to Peak Temperature (Device supplier Maximum)	8 minutes max
• Liquidus temperature (T_L) • Time maintained above Liquidus temperature (t_L)	• 217 ºC • 60-150 seconds
Time (t_p) within 5 ºC of the specified (T_c).	30 seconds
Ramp-down Rate (T_P to T_L)	6 ºC/seconds max

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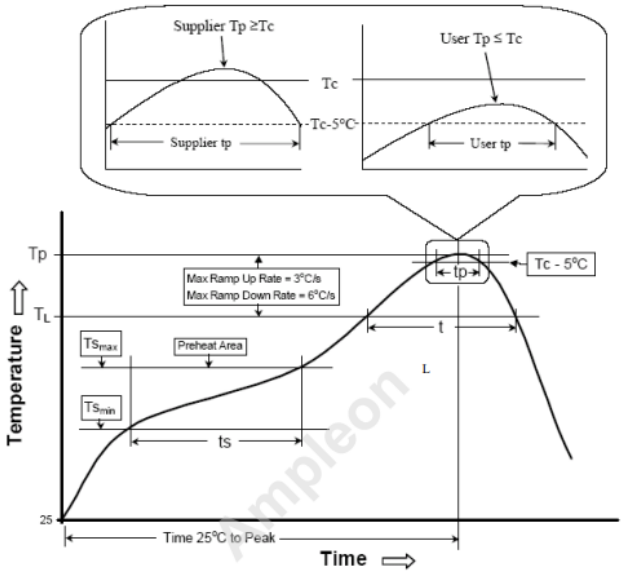

Figure 21. Classification profile based on JEDEC (JEDEC J-STD-020)

7. Inspection

Non-destructive vision/optical inspection methods are preferred to verify soldering quality.

Common methods for design and process development purposes are:

- Manual or automatic optical inspection.
- Examination by X-ray.
- SAM (Scanning Acoustic Microscope).
- Cross-sectional analysis.

7.1 Optical inspection

Easiest method for solder joint inspection is through optical inspection to look for solder joint profile and visual defects like shorts, misalignment.

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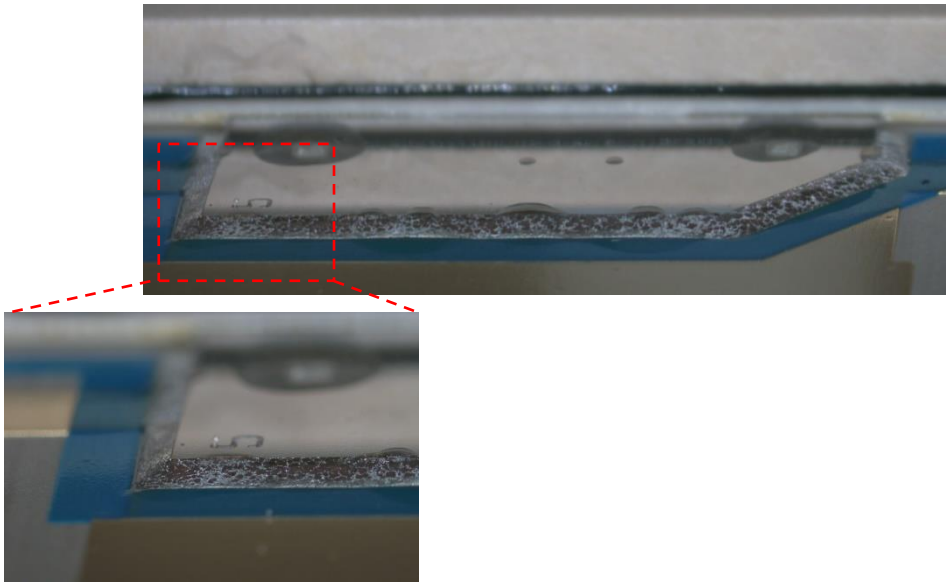

Figure 22. Visual appearance straight leads device (Pb-free solder joints)

7.2 X-ray

It's an efficient inline control to detect soldering defects such as poor soldering, bridging, voiding and missing parts. Some defects such as broken solder joints are not easily detectable by X-ray.

Void levels do provide confidence in the materials and soldering process.

Figure 23 shows typical X-ray where it can be seen the voiding under package leads/flange.

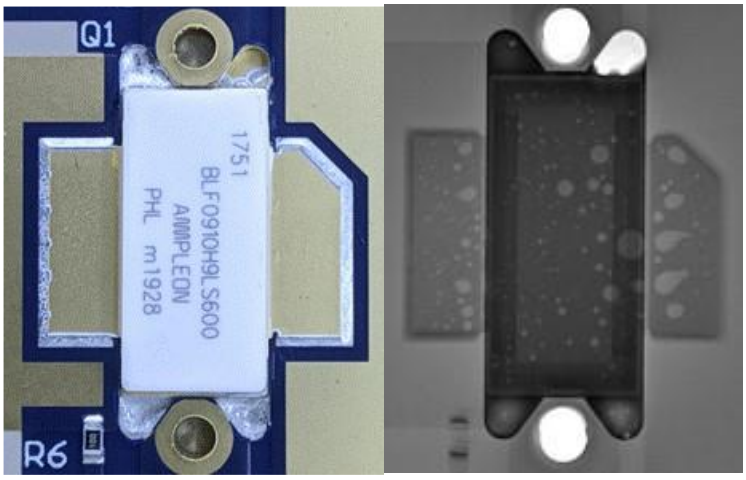

Figure 23. X-ray lead-PCB interface

Generally, the extent of voiding depends on the board pad size, the stencil layout, the solder paste, the reflow profile, the via layout and solderability of PCB/package.

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General considerations to minimize X-ray impact to the electrical performance of semiconductor ICs are provided in Appendix 9.3 of this document.

7.3 SAM (Scanning Acoustic Microscope)

This method is used to examine in particular the interface between the exposed heat spreader/flange and the heatsink, as it is not easily detectable by x-ray. Variability in gray scale (dark – bright) indicates presence of voids.

The solder interface between the flange and heatsink have been inspected as shown in Figure 24.This provides information on the quality of the soldered interface (based on the level of voids). It shows very low level of voids. This technique can also be applied to assess the soldering quality of the leads to the PCB.

The introduction of finished PCBs into a DI water bath is considered a reliability risk, if parts will be used after SAM, dry bake should be performed, 8 hours at 125°C (typical conditions may differ depending on application).

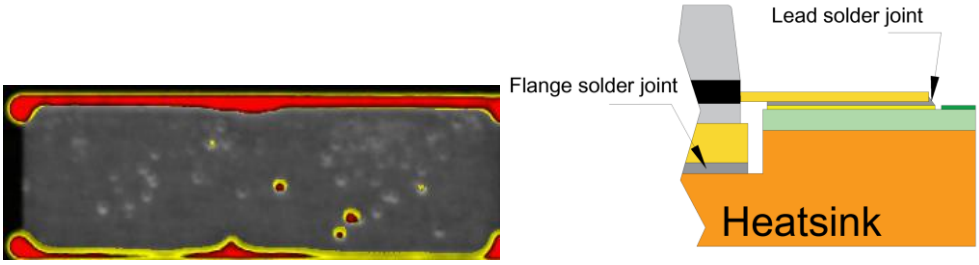

Figure 24. SAM of soldered interface between flange & heat sink

7.4 Cross-sectional analysis

Cross-sectioning can offer detailed information about the solder joint quality.

Since it's a destructive method, cross-sectioning during monitoring is naturally not practical and it's indicated for development and failure analysis.

Figure 25 shows typical cross section of ACP component.

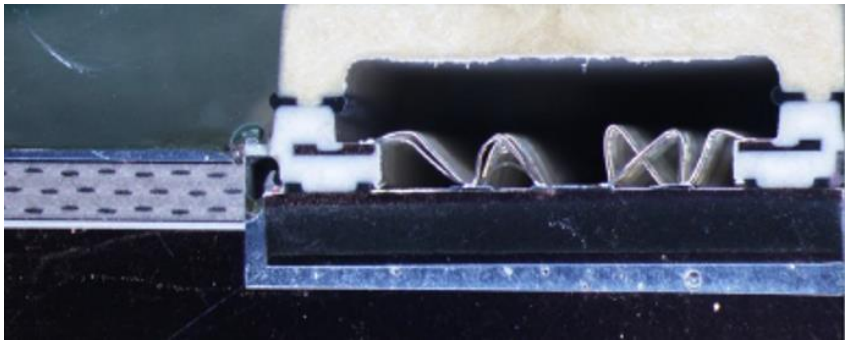

Figure 25. ACP cross section

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8. Mounting procedure

8.1 Manual mounting eared devices

8.1.1 Package placement

Even though an eared packages is not passed through a reflow oven, it may be heated by a soldering iron or bar. Therefore, to avoid issues due to moisture sensitivity, it is best to store the packages in dry environment or in Nitrogen.

Using an in-house method, apply an even layer of thermal compound to the bottom of the package flange. This thermal compound will improve the thermal conductivity between the metal surfaces of the flange and the heat sink. The layer must be thin, and it must be evenly spread out before placing the package, so that no air bubbles are trapped. Use of excessive thermal compound is not desirable, as it adds a “layer” of thermal resistance. In addition, excess thermal compound may leak out of the heat sink cavity when the package is bolted to the heat sink – this could contaminate the PCB near the package.

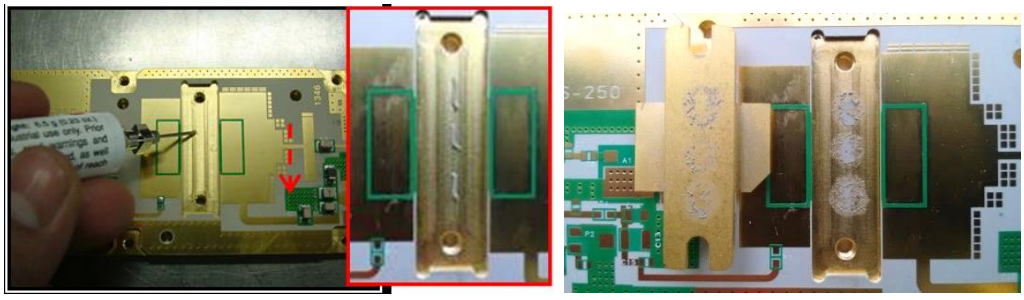

Figure 26. Example of applying 3 small lines of silver conductive grease on the cavity center. Photo on right side package removed after bottle down showing silver conductive paste spread

Place the package in its position, with the flange sticking through the PCB and into the cavity in the heat sink. Package alignment is done visually, by adjusting the position so that the package leads are exactly aligned with the PCB pads.

In order to ensure a good interconnection between the flange and the bottom of the heat sink cavity, the package is bolted down onto the heat sink. The holes in the heat sink may have thread, in which case the bolt is fixed to the heat sink itself. They may also be plain, in which case nuts are used to tighten the bolts. Both situations are illustrated in Figure 27.

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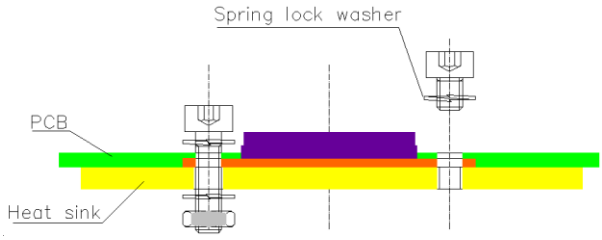

Figure 27. Bolting down

Do not use hexagonal bolts, as these may interfere with some of the smaller flange-mount packages during the bolting step.

The force applied when tightening the bolts is important to ensure a good contact between the flange and the heat sink. It is recommended to tighten the bolts in two steps to ensure the packages free from damages during mounting:

- First, both bolts should be tightened (finger tight).
- Second, the bolts should be fully tightened to the recommended torque with a controlled torque wrench, such as a torque screwdriver. Excessive torque may damage the device. The range of torques (calculated for M3) recommended for flange packages.

Table 6 Torque

Torque	Minimum value	Maximum value
Nm	0.60	0.75

Washers are recommended in order to spread the force equally. In addition, use of spring-lock washers will make sure that the bolts do not come loose with vibrations when the product is used.

8.1.1.1 Soldering the leads

Soldering the leads to the PCB pads is largely a question of good workmanship, as it is done manually. Use a soldering iron, or bar, with a tip that is at least as wide as the leads. The width should be smaller than the package width, to eliminate the risk of accidentally touching other components on the PCB.

Use a soldering iron or bar that is ESD-safe.

Use solder wire. Use an alloy that has a melting temperature that is not higher (and preferably lower) than the solder that was used on the rest of the PCB. Set the soldering iron or bar to the temperature specified by the solder supplier. Flux containing solder wire is preferred.

Using the iron or bar, apply solder to the PCB pad, around the package lead. Make sure that the solder has melted completely and apply enough solder to ensure a good joint. If there is a small gap between the lead and the pad apply extra solder to fill this. Throughout this process care must be taken that the soldering iron or bar makes contact with neither the package body nor the neighboring components. The solder may not touch the package body. Proper joint formation should be verified by visual inspection through a microscope. If there is a gap between the leads and the PCB pad, check the

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filling by the solder. Also, an angle of 20° – 30° degrees indicates good wetting, for lead-free solders.

8.2 Manual mounting earless devices

8.2.1 Reflow mounting

For these packages, it is critical the leads make good contact with the pads on the PCB, and that – at the same time – the flange makes good contact with the heat sink. For these reasons, although not mandatory the package is usually bolted to the board with a fixture, during reflow.

Next section only describes the procedure using a fixture during reflow.

8.2.1.1 Fixture on cap during reflow

Where an external load is required during reflow soldering, it could also be applied on the cap of the transistor. As a result, a jig should be designed accordingly to apply a uniform load (up to 1.5kg) over the transistor cap , avoid point-loading on the cap, as example shown in Figure 28.

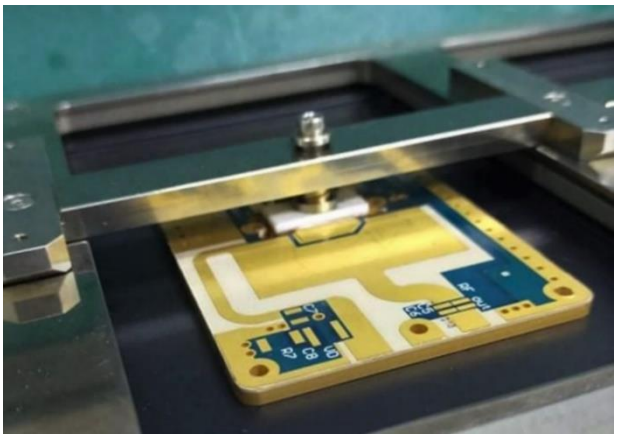

Figure 28. Reflow soldering jig applying uniform load on the transistor cap

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8.2.2 Reflow soldering

The most important step in reflow soldering is when the solder paste deposits melt and soldered joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile with varied times.

A rough indication of the recommended minimum peak temperatures for SnPb and SAC alloys is given in Table 3, however, these values should be verified with your solder paste supplier.

After reflow, check that the solder in the heat sink cavity does not make contact with the package body.

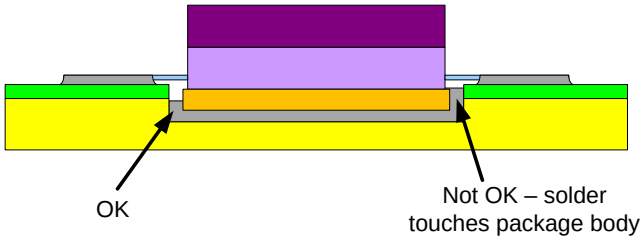

Figure 29. Inspection of solder inside the cavity

Although repair of solder joints is generally possible, it can be challenging and require proper optimization. Difficulty will vary depending on package type and PCB design.

A package lead or a land pad in case of a leadless package not soldered properly may be repaired by heating it with the tip of a soldering iron. In that case, it is sufficient to heat the lead/pad until the solder melts completely, and a new device should not be necessary.

The soldering iron temperature must be set such that the package surface temperature doesn't exceed its maximum allowed temperature. Soldering iron should also be ESD compliant.

In other situations, if a defective component is observed after board assembly, there may be a need to replace the package. In that case, the rework process should consist of the following steps:

- Removal of old package.
- Site preparation.
- Solder application.
- New package placement.
- Soldering new package.

8.3 Removal of eared package

- Unscrew the bolts holding down the eared package.
- Remove the old package using a soldering iron tip. If the package is going to be submitted to failure analysis, use a soldering iron that is ESD-safe.

It is essential that both leads are heated simultaneously, while a vacuum wand nozzle is attached to the top of the package body, for lifting it off.

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The process steps are as follows:

- Set the soldering iron or bar to a temperature that is high enough to melt the solder. This value depends on the solder that was used to attach the package.
- Attach a vacuum wand nozzle to the top of the package body.
- When the soldering iron has reached the desired temperature, place it over the package so that both package leads are heated simultaneously.
- Watch carefully as the soldering iron or bar heats the solder joint.
- As soon as the solder melts, lift the package off the PCB using the vacuum wand. Do not lift the package before the solder in the joints has melted completely, as this may damage the package and the PCB.

Throughout this process, care must be taken that the soldering iron or bar does not make contact with the package body or the neighboring components.

Although a hot air gun with a dedicated nozzle could theoretically be used, this is not recommended.

If a soldering iron with a suitable tip is not available, it is possible to remove the old package by de-soldering the leads one lead at a time. In that case, apply the iron to one of the leads, and wait until the solder in the joint has melted completely. Then, lift the package. As the other lead is still soldered to the PCB, this will result in damage. Next, de-solder the other lead. Due to the potential damage of this method, it is not preferred if the package is going to be submitted for failure analysis.

After the old package has been removed, check whether excess thermal compound has remained in the cavity in the heat sink. If this is the case, remove the heat sink from the PCB and discard it.

8.4 Removal of the earless package

For removal of earless packages, it is recommended to use a hot plate in combination with hot air heat transfer (Figure 30 - setup for bottom and top heating)

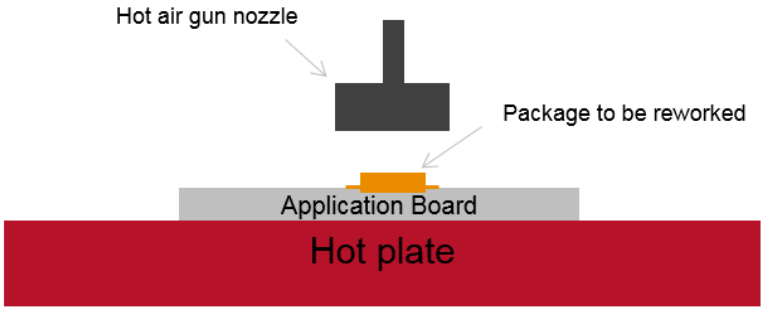

Figure 30. Setup schematic – package removal

Rework station equipment should be able to control:

- Temperature and time for bottom heating.
- Temperature, time, distance and air flow for top heating.

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- Temperature profile should be adaptable to different packages sizes and thermal masses.
- Ensure that the peak temperature and temperature ramps are according with the standard reflow process.
- High mechanical forces shouldn't be applied to remove or move component, this can compromise future failure analysis on the component or/and PCB. It is recommended to use vacuum pipette (ESD safe).

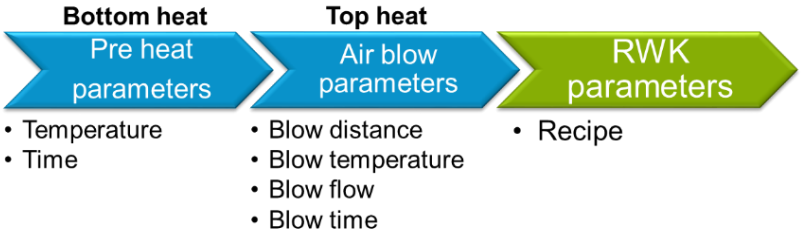

Figure 31. Key rework station parameters

The process steps are as follows:

- Dry-bake (remove moisture from the PCB) for 8 hours at 125°C (typical conditions, may differ depending on application).
- Pre heat (uniform temperature in board) on hotplate with a temperature of 125°C (typical conditions, may differ depending on application).
- Reflow component to rework using the hot air. The Nozzle size and heat flow should be optimized to keep heat flow localized and still allow the melting of the solder on the component.
- Package removal: as soon as the solder melts, lift the package off the PCB using a vacuum nozzle. Do not lift the package before the solder in the joints has melted completely, as this may damage the package and the PCB.

Throughout this process, care must be taken that there are no contacts with neighboring components.

8.5 Site preparation

After the package has been removed, the PCB pads and heatsink cavity must be prepared for the new package. Excess solder and/or flux remains should be removed. Ideally this is done on an appropriate de-soldering station. Alternatively, use a soldering iron set to the temperature specified for the solder that was originally used to attach the package.

For earless package clean the pads/cavity using the soldering iron and solder wick, or another in-house technique.

For eared packages clean the pads using the soldering iron and solder wick, or another in-house technique. Remains of heatsink compound on heatsink cavity should be cleaned using with alcohol (IPA) and not with any corrosive chemical (i.e. acetone).

Note: use a temperature that is needed to just liquefy the solder but that does not damage the PCB.

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After most of the solder has been removed from a solder land, a very thin layer of solder will be left, on top of a few intermetallic layers. In the case of Cu pads, for example, there will be layers of Cu_3Sn, Cu_6Sn_5, and finally solder, on top of the Cu (see Figure 32). The top layer of solder is easily solder-able.

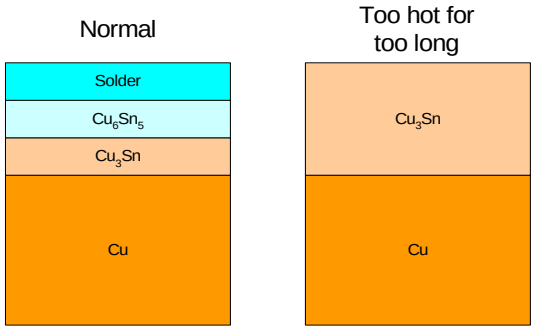

Figure 32. Overheating and Cu_3Sn formation

If, however, the pad is heated too much during removal of the rejected IC package, and during site preparation, the top two layers will also be converted into Cu_3Sn (Figure 32), in that case, there will only be the Cu_3Sn inter-metallic layer on top of the Cu. Unfortunately, Cu_3Sn is hardly wettable. As a result, it will become very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress, that the solder lands are heated only as much as is absolutely necessary.

8.6 Solder application

A mini stencil is preferable method to apply solder.

Stencil should have same design as the stencil used in normal assembly of the component (thickness, apertures, pattern).

In case space constrains due to other components nearby and mini stencil cannot be used, solder paste dispense method can be used. Make sure that solder volume is consistent across all packages leads/pads.

After solder application solder volume must be visually controlled.

8.7 Placement of the new package

If the heat sink was discarded, mount a new heat sink. Next, mount a new package in much the same way as the original package was mounted. Re-use of removed packages is not recommended.

In case manual mounting, use a good optical system (e.g. microscope with min 25x magnification) for placement and alignment of package.

8.8 Soldering of the new package

New package should be soldered to the PCB in the same manner as the original package.

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In case reflow furnace is not possible, same method as used for the package removal can be used (hot plate combined with hot air nozzle), heating/cooling profile should have ramp rates and peak temperatures similar to the initial reflow.

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9. Appendices

9.1 MSL

MSL (Moisture Sensitivity Level).

If there is moisture trapped inside a surface mount package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package's MSL, depends on the package characteristics and on the temperature it is exposed to during reflow soldering.

MSL level are determined according JEDEC standard J-STD-020 [1]. Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every product, this MSL is given on a packing label on the shipping box. An example of a packing label is given in Figure 33.

Figure 33. Example of MSL information on packing label

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, to remove any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are always to be respected. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partial assembled boards, between two reflow steps, be stored longer than indicated by the MSL level.

The semiconductor package floor life depends on the MSL level and should be accordance to the J-STD-020.

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9.2 ESD

Damage to semiconductors from Electro Static Discharge (ESD) is a major cause of rejects and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is recommended that the following ESD precautions be complied with.

Generally, ESD devices are marked with warning sign as in Figure 34.

Figure 34 ESD warning signal.

9.2.1 Workstations for handling ESD sensitive components

Figure 35 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed:

- Workbench and floor surface should be lined with anti-static material
- Persons at a workbench should be earthed via a wrist strap and a resistor
- All mains-powered equipment should be connected to the mains via an earth leakage switch
- Equipment cases should be grounded
- Relative humidity should be maintained between 40 % and 50 %
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) “Protection of Electrostatic Sensitive Devices” (see 11), which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

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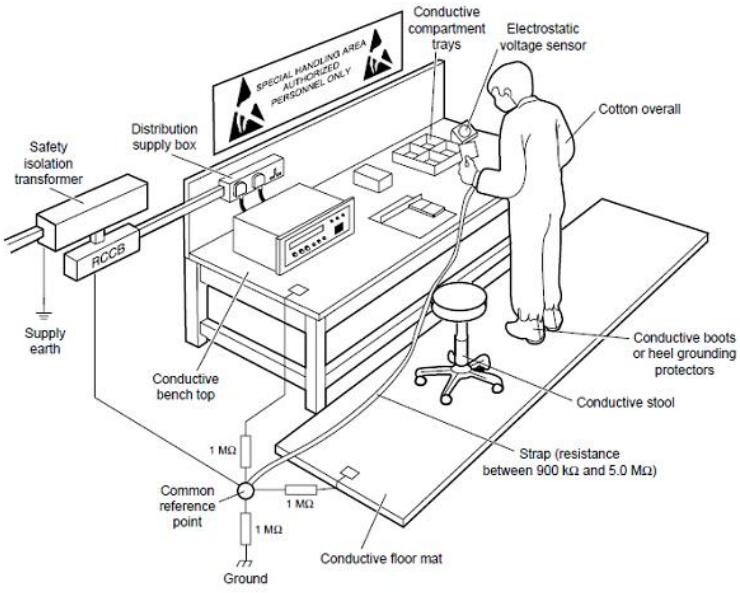

Figure 35. Example of a work station

9.2.2 Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials.

Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be re-packed in conductive or anti-static packing or carriers.

9.2.3 PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Standard precautions for manual handling of electrostatic-sensitive devices need to be followed.

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9.2.4 Gold embrittlement

Some air cavity packages such ACC have flange gold plated. To avoid brittle AuSn inter-metallics (reliability) in the solder joints enough solder should be applied. The level of gold within the solder joint may not exceed 4% by weight.

9.3 X-ray considerations

X-ray can affect the electrical performance of semiconductor ICs, a phenomenon documented in scientific literature. X-ray tool vendors provide application notes on methods to minimize X-ray impact on semiconductors. Customers are strongly advised to consult their X-ray tool vendor for specific guidance, as the impact depends on various factors such as spectrum, filters, collimators, and software settings.

General considerations to minimize X-ray impact:

- Minimize the total X-ray dose. Ampleon has conducted X-ray inspection to verify good soldering on a board. This can be achieved with a dose << 1 Gy. A maximum dose of <<1 Gy is recommended including rework. Maximum dose depends on the x-ray spectrum. Internal evaluations by Ampleon have shown that the dose needed to make sharp pictures has a negligible effect on the electrical characteristics of its products. However, these findings are for reference only and do not constitute a warranty or guarantee.
- Use collimators to reduce secondary exposure.
- Apply filters to minimize the softer part of the X-ray spectrum, which has the most significant impact.
- Regularly monitor the X-ray dose to prevent overexposure due to tool malfunction.
- Inspect the device from the back, allowing the application board and/or flange or lead frame to absorb a significant part of the X-ray radiation.
- Assess potential electrical performance shifts caused by X-ray exposure to verify the product performance remains within specified limits. Special attention should be given to Idq (quiescent current), caused by a shift in Vt (threshold voltage). X-ray can lead to a Vt shift caused by charging of the gate oxide in LDMOS devices. These charges can be released during lifetime. The shift in Idq caused by X-ray needs to be well within the requirements from application perspective.

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10. Abbreviations

Table 7. Abbreviations

Acronym	Description
SnPb (solder)	Sn (Tin) Pb (Lead)
SAC (solder)	Sn (Tin) Ag (Silver) Cu (Copper)
MSL	Moisture Sensitivity Level
RH	Relative Humidity
NSMD	Non Solder Mask Defined
SMD	Solder Mask Defined
PCB	Printed Circuit Board
ACC	Air Cavity Ceramic
ACP	Air Cavity Plastic

Acronym	Description
ACC	Air Cavity Ceramic
ACP	Air Cavity Plastic
CTE	Coefficient Thermal Expansion
ENIG	Electroless Nickel Immersion Gold
ESD	Electrostatic discharge
JEDEC	Joint Electron Device Engineering Council
MSL	Moisture Sensitivity Level
NSMD	Non Solder Mask Defined
OSP	Organic Solder-ability Preservative
PCB	Printed Circuit Board
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
SAC (solder)	Sn (Tin) Ag (Silver) Cu (Copper)
SAM	Scanning Acoustic Microscope
SMD	Solder Mask Defined
SnPb (solder)	Sn (Tin) Pb (Lead)

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11. References

[1] IPC/JEDEC J-STD-020

Joint IPC/JEDEC Standard for Moisture/Reflow, Sensitivity Classification for Non hermetic Surface Mount Devices

[2] IPC-7351

Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[3] EN 100015/CECC 00015

Protection of Electrostatic Sensitive Devices, European Standard

[4] 3997.750.04888

Quality reference handbook, Ampleon

[5] IPC-A-610

Acceptability of Electronic Assemblies, IPC

[6] MIL-STD-883

Test Methods standard microcircuit

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12. Legal information

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