Endurance, Data Retention and Field Immunity of STT-MRAM

1. Introduction

Spin Transfer Torque Magneto-Resistive Random Access Memory (STT-MRAM) based on perpendicular magnetic tunnel junction (pMTJ) is by far the most promising emerging non-volatile memory (NVM) technology with a unique combination of low power, fast read/write speeds and practically unlimited endurance. This application note presents studies on time-dependent dielectric breakdown (TDDB), data retention and field immunity properties of STT-MRAM based on Avalanche's proprietary pMTJ technology. The results of the studies show projected endurance of $>10^{16}$ write cycle, 10 years data retention at 125°C, the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe. This suggests that STT-MRAM meets and exceeds the requirements of most memory use cases for data storage, code storage, and scratchpad memories for embedded and high-performance computing applications, such as last-level caches (LLC).

2. Endurance

Endurance specifies the cumulative number of program/erase cycles of memory devices without unrecoverable errors. Endurance is a ubiquitous issue in Flash memories and relates to the product's end-of-life. Each program/erase operation introduces defects in the flash memory cell structure (oxide) that accumulate over time. At some point, defect-induced errors prevent the flash cell from normal operation, rendering it unusable.

STT-MRAM, on the other hand, does not store charge and uses magnetic states instead for storage. Programming is achieved by pulsing a current through an MTJ element, causing the magnetization direction of the storage layer to switch (up/down) by Spin Transfer Torque (STT) effect. Reading is done by sensing different MTJ resistance states (low/high depending on the storage layer magnetization directions) owing to Tunneling Magneto-Resistance (TMR) effect. Two different MTJ resistance states represent data "1" and "0," respectively. Since MTJ has a thin tunnel barrier which can degrade owing to voltage stress, the endurance of STT-MRAM is limited by Time-dependent Dielectric Breakdown (TDDB). This is analogous to CMOS gate oxide lifetime limitation owing to TDDB.

3. Retention

Retention is the ability of an NVM device to maintain and provide on-demand the programmed state of any memory cell for a minimum period of time. In general, the capability of any NVM cell to return correct data is influenced by many factors, such as temperature, voltage and cumulative program/erase cycles, etc.

As mentioned in the Endurance section, STT-MRAM does not have charge cycling based wear-out mechanisms. However, STT-MRAM has decreasing data retention at elevated temperatures owing to temperature-dependence of magnetic anisotropy. In order to compensate for the loss of thermal stability at high temperatures, magnetic anisotropy of the devices must be increased. This in turn leads to larger write currents at lower temperatures, thus reducing the efficiency of the memory. Avalanche's proprietary pMTJ design maintains low write current/voltage without compromising data retention.

4. Field immunity

In certain applications, the memory device may potentially be exposed to stray or external magnetic field. Since MRAM stores data using magnetic moment, it is more sensitive to the magnetic field than charge based devices. Field immunity is a parameter that describes how well the MRAM works when exposed to external magnetic field.

There are two types of immunity field we need to consider for MRAM. Firstly, when MRAM is exposed to the external magnetic field, the energy barrier of MRAM will be altered, which will impact the electrical switching performance of the MRAM. The maximum magnetic field under which the MRAM is still functional is called operation immunity field. Secondly, when MRAM is exposed to very high magnetic field, the magnetic field will flip the magnetic moment of the storage layer in pMTJ, which leads to loss of data in the memory. The maximum magnetic field under which the data in MRAM can be maintained without corruption is called standby immunity field.

Avalanche takes into account the potential external magnetic field impact on STT-MRAM with advanced pMTJ design and circuit design. Avalanche STT-MRAM achieves the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe with less than sub-ppm raw error rate impact.

5. Avalanche's STT-MRAM - Endurance, Retention, Field immunity

The cycling endurance of an STT-MRAM product depends on the write voltage and must be set far above the mean switching voltage to ensure a low write error rate. Figures 1 shows empirical TDDB data of Avalanche's 64Mbit STT-MRAM device.

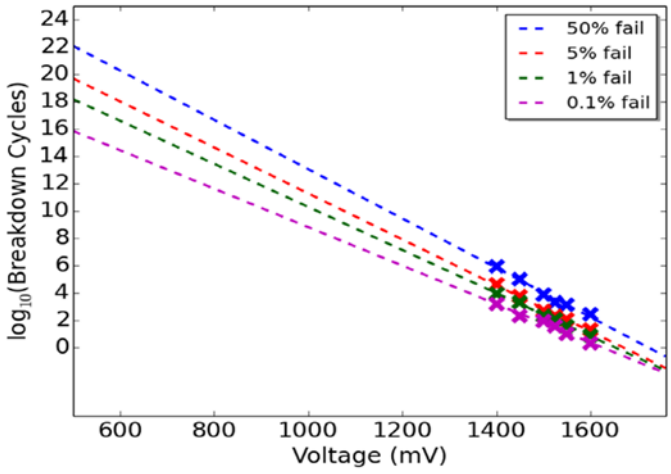

Figure 1: Typical Endurance Data for pMJT test structures

As can be seen, $1x10^{16}$ write cycles can be achieved using a 500 mV write pulse.

Retention, which is another important characteristic of STT-MRAM, is the length of time the data can be retained after written. 10 years is the industry norm for non-volatile memories. Figure 2 shows empirical data for Avalanche's 64Mbit device.

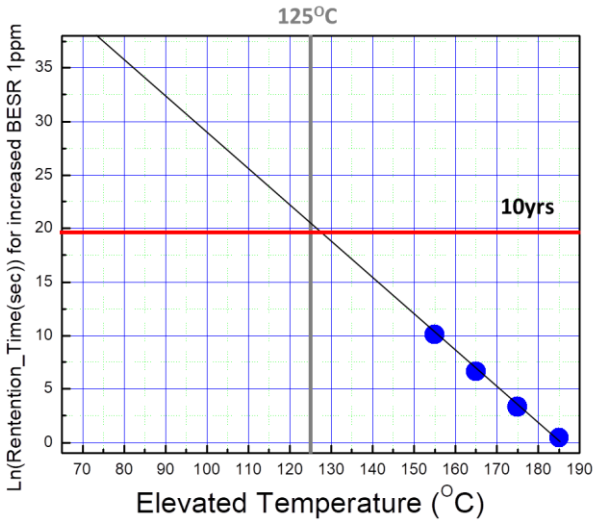

Figure 2: Typical Retention Data for 64Mbit pMJT STT-MRAM device

As can be seen, 10 years data retention is achieved at 125°C.

Field immunity can be characterized by testing MRAM in the presence of external magnetic field. Figure 3 shows Avalanche STT-MRAM achieves the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe with less than sub-ppm raw error rate impact. Duration of applied field is 1 hour in standby mode.

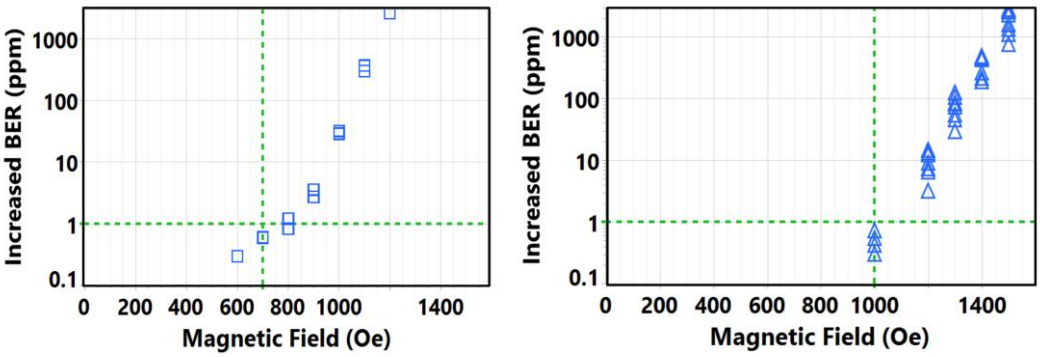

Figure 3: Field immunity results for chip in operation (left chart) and standby (right chart) mode

6. Avalanche's STT-MRAM products

Avalanche offers five STT-MRAM product families that address different stand-alone and embedded applications as shown in Figure 4 and discussed in the following section. The product families are:

eSRAM: eSRAM products are embedded, non-volatile, true random access memories that allow both reads and writes to occur randomly in memory. eSRAM is a scratch pad memory ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance, high performance and a scalable memory technology. eSRAM is offered with the industry standard AMBA 3 AHB-Lite interface.

eNVM: eNVM products are also embedded, non-volatile, true random access memories similar to eSRAM but have a much higher temperature profile (solder reflow). eNVM is ideal for program and data storage. eNVM is offered with the industry standard AMBA 3 AHB-Lite interface.

SP-NVSRAM: SP-NVSRAM products are standalone and are ideal for scratch pad applications. They offer random access, low latency, low power, infinite endurance and high performance. SP-NVSRAM uses an SPI interface and is available in small packages.

MD-AVRAM: MD-AVRAMs are standalone, mid-density, persistent RAM products built around industry leading DDR4/5 interface. MD-AVRAM offers extremely high performance, provide low latency and are ideal for replacing low density DRAMs.

HD-AVRAM: HD-AVRAM products are similar to MD-AVRAM products and are offered in much higher densities. HD-AVRAM has slightly lower endurance of $1x10^{10}$ write cycles owing to a highly scalable next generation switching mechanism.

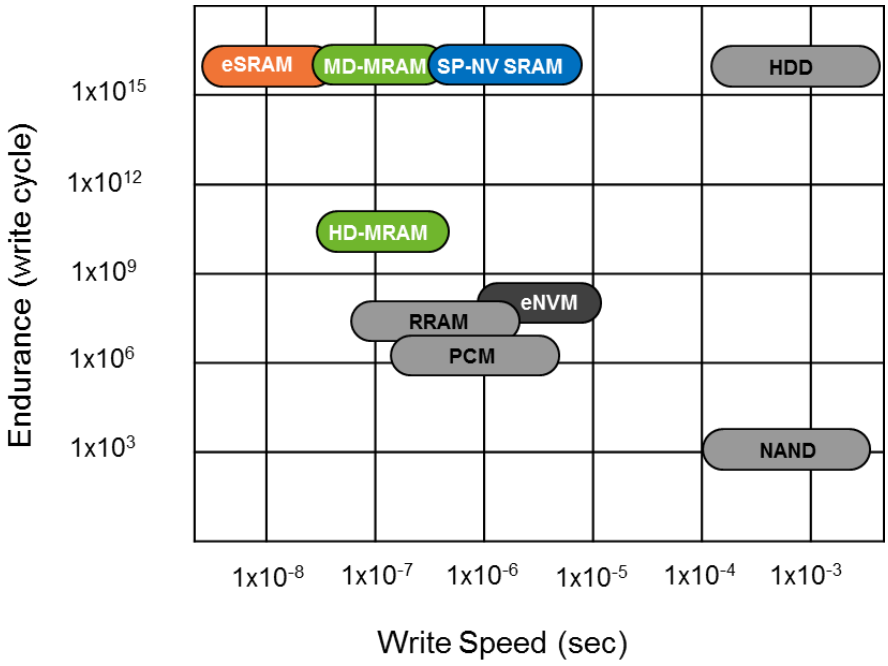

Figure 4: Avalanche Products Overview

7. Use Models

a. Data Logging Memory (SP-NVSRAM)

A data logger is an electronic device that records data over time via external instruments and sensors. Its primary benefit is the ability to autonomously collect data. Upon activation, data loggers measure and record information for the duration of the monitoring period. A few of their critical properties are as follows:

- Data loggers have relatively low sampling rates (~1MHz).
- Data loggers are standalone devices and require non-volatile, large (~megabits) density to accommodate days/months of uninterrupted data acquisition.
- Data loggers are battery-backed devices with energy harvesting (solar power, etc.) to supplement the power source. Power consumption must be low to support >10-yr battery lifetime.
- Data loggers are extremely reliable. In other words, as long as power is on, they will not fail to log data for any reason. In the event of power loss, the logged data will not be lost.

Table 1: Data Logging Memory Requirements

Requirements	Read Access Time (ns)	Write Time (ns)	Frequency of Operation (MHz)	Data Endurance (Cycles)	Data Retention (Years)
Data Logging Memory	100	100	10	$1x10^{16}$	10

Avalanche's SP-NVSRAM family meets these requirements and can be used as data logger memory of choice.

Table 2: Avalanche's SP-NVSRAM characteristics

Device Operation	Values	Units
Density range	8 – 64	Megabits
Read (Word: 32 bits)	10.0	ns
Write (Word: 32 bits)	20.0	ns
Frequency of Operation	100	MHz
Endurance	$1x10^{16}$	cycles
Retention	10	years
Standby	50.0	µA
Hibernate Power Mode	1.0	µA
Read (Word: 32 bits)	2.0	mA
Write (Word: 32 bits)	10.0	mA

b. IoT Memory (eSRAM, eNVM)

IoT devices are computing gadgets that connect wirelessly to a network and have the ability to transmit data. Their rapid development has created a number of exciting new opportunities and challenges for designers with one consideration that cannot be overlooked: the need for the devices to have memory that can store boot code and data. Some of the must have requirements are as follows:

- **Cost.** Cost is a concern in any project; the more expensive the memory selection, the more expensive the final device.
- **Size.** Most IoT devices are small, and thus the embedded technology must also be small. The amount of space required for memory processing must also be kept to a minimum, as more silicon wafer space is required, the more cost goes up.
- **Power Consumption.** Most IoT devices either run on small batteries or rely on energy harvesting for recharging. For this reason, it's important to choose an option that uses the least amount of power and voltage during both active use and standby.
- **Startup time.** Users want excellent device performance. So memory performance needs to be sufficient to allow for a quick startup. Implementing a code-in-place option reduces the time required to boot up, as well as overall BOM since there is less need for RAM with substantial on-chip storage.

Table 3: IoT Memory Requirements

Requirements	Read Access Time (ns)	Write Time (ns)	Frequency of Operation (MHz)	Data Endurance (Cycles)	Data Retention (Years)
IoT Memory (Boot Code & Data Storage)	10	20	100	$1x10^{16}$	10

Avalanche's eSRAM and eNVM families meets these requirements and can be used as IoT memory of choice.

Table 4: Avalanche's E-SRAM, E-NVM characteristics

Device Operation	eSRAM Values	eNVM Values	Units
Density range	8 – 64	8 – 64	Megabits
Read (Word: 32 bits)	10.0	10.0	ns
Write (Word: 32 bits)	20.0	200.0	ns
Frequency of Operation	100	100	MHz
Endurance	$1x10^{16}$	$>10^{6}$	cycles
Retention	10	10	years
Standby	50.0	50.0	µA
Hibernate Power Mode	1.0	1.0	µA
Read (Word: 32 bits)	2.0	2.0	mA
Write (Word: 32 bits)	10.0	10.0	mA

c. Persistent Memory (MD-AVRAM, HD-AVRAM)

Persistent memory (PM) is simply data storage memory that does not lose data when the power is disconnected. PM storage is in the system (outside the main processor) and has lower performance than conventional DRAM. It sits in the system DIMM slots and as mentioned before, doesn't lose data upon power loss.

In the data storage hierarchy, PM is positioned between DRAM and SSD/HDD main storage. Its performance is similar to or lower than DRAM; it can have higher latency. PM's capacity can be larger than DRAM.

Avalanche's is currently developing MD-AVRAM (1-16Gb) and higher density HD-AVRAM product families to meet these requirements as the persistent memory of choice.

8. Summary

Avalanche's STT-MRAM technologies meet and exceed the requirements of most memory use cases with incumbent technologies and can be used in low power as well as high performance applications.