Application Note AN-2189

400GBase-DR4 QSFP-DD EEPROM Application Note Rev A01

Introduction

The purpose of this application note is to document the EEPROM contents of II-VI's 400 Gigabit Ethernet DR4 QSFP-DD modules.

This application note applies to 400GBase-DR4 QSFP-DD II-VI part number FTCD4523E2PCM, FTCD4533E2PCM, FTCD4523E2PCM-4A and FTCD4533E2PCM-4A.

	FTCD4523E2PCM FTCD4533E2PCM	FTCD4523E2PCM-4A FTCD4533E2PCM-4A
ApSel 1	4x100G	400G
ApSel 2	400G	4x100G

All registers are supported per CMIS REV 4.0 Common Management Interface, which are applicable for a SM (separable module) with host to module management communication based on a Two-Wire-Interface (TWI),and per SFF-8024 REV 4.2 Specification for SFF Committee Cross Reference to Industry Products. The EEPROM mapping below is meant to be an inclusive listing of what is supported by the transceiver.

Applicable Documents, Standards and MSA's

a. CMIS, Common Management Interface Specification, Rev 4.0, April 30th, 2019
b. QSFP-DD Specification for QSFP Double Density 8X Pluggable Transceiver, Rev 5.0, July 2019
c. SFF-8679, QSFP 4x Base Electrical Specification, Rev 1.8, October 5th ,2018
d. SFF-8024, SFF Module Management Reference Code Tables, Rev 4.7, January 14th ,2020
e. IEEE802.3cu, 100 Gb/s and 400 Gb/s over SMF at 100 Gb/s per Wavelength

How to use this Application Note

Please refer to the CMIS 4.0 and SFF-8024 documents for information on the available EEPROM memory content. The memory is arranged in a single address, multiple page approach. The 7-bit device address on the Two-Wire-Interface (TWI), is 0100000b(A0h). The EEPROM pages, implemented for FTCD4523E2PCM, FTCD4533E2PCM, FTCD4523E2PCM-4A and FTCD4533E2PCM-4A 400GBase-DR4 QSFP-DD transceiver are shown below. Included are description of each field and values/default values for each memory location. Dynamic values (DDM) in the EEPROM map are kept blank which will be populated with the instantaneous values at the times of accessing those specific memory locations.

II-IV Specific Implementation:

a. Aux2 monitor is implemented for Laser Temperature Monitor.
b. Only one instance of Command Data Block (CDB) is implemented with support for only Bank 0. As other banks are not implemented, the bank select byte (byte 126, Lower page 00h) is read only. Memory pages 13h and 14h are implemented in this Bank, providing loopback controls and internal pattern generator/error checker access. These pages can be accessed using page select byte 127 of Lower Memory page.
c. FTCD4523E2PCM-4A and FTCD4533E2PCM-4A QSFP-DD: Presence of valid data input signal across all eight (8) input electrical lanes are must to finish the DSP initialization.
d. FTCD4523E2PCM and FTCD4533E2PCM QSFP-DD: Presence of valid data input signal across two (2) input electrical lanes are must to finish the DSP initialization.

Revision	Date	Change
A0	03/01/2021	Initial release
A1	03/12/2021	Change Table 1 (Lower Page 00H) 0x1A = 0x40 to 0x1A = 0x60 (change optical modulation amplitude to average power)

Contents

TABLE 1: LOWER MEMORY PAGE 00H (CONTROL AND STATUS ESSENTIALS)

Lower Page 00h is required and includes interrupt flags and monitor results arranged to enable single block read operations for time-critical data. (See CMIS-4.0 Table 8-2 to Table 8-14)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
0	00	0	8	RO	Identifier	See SFF-8024	QSFP-DD	18	QSFP-DD	18
1	01	0	8	RO	Version ID	CMIS Version; upper nibble is the whole number part, lower is decimal	40	40	40	40
2	02	7	1	RO	Flat_Mem	Upper memory flat or paged 0b=Paged memory (pages 00h, 01h, 02h, 10h and 11h are implemented) 1b=Flat memory (only page 00h implemented)	Paged	04	Paged	04
		6	1		Reserved	Reserved				
		4	2		Reserved	Reserved				
		2	2		TWI Max Speed	TWI maximum speed supported 01b=Module supports up to 1 MHz	Up to 1 MHz		Up to 1 MHz	
		0	2		Reserved	Reserved				
3	3	4	4	RO	Reserved	Reserved		00		00
		1	3		Module state	Current state of Module (see Table 8-3, CMIS 4.0)	0		0	
		0	1		Interrupt	Digital state of Interrupt output signal 1b=Interrupt not asserted (default) 0b=Interrupt asserted	0		0	
4	4	7	1	RO	Bank 0 lane 8 flag summary	1b=one or more of the flag bits from bank 0, lane 8 is set.	0	00	0	00
		6	1		Bank 0 lane 7 flag summary	1b=one or more of the flag bits from bank 0, lane 7 is set.	0		0	
		5	1		Bank 0 lane 6 flag summary	1b=one or more of the flag bits from bank 0, lane 6 is set.	0		0	
		4	1		Bank 0 lane 5 flag summary	1b=one or more of the flag bits from bank 0, lane 5 is set.	0		0	
		3	1		Bank 0 lane 4 flag summary	1b=one or more of the flag bits from bank 0, lane 4 is set.	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		2	1		Bank 0 lane 3 flag summary	1b=one or more of the flag bits from bank 0, lane 3 is set.	0		0	
		1	1		Bank 0 lane 2 flag summary	1b=one or more of the flag bits from bank 0, lane 2 is set.	0		0	
		0	1		Bank 0 lane 1 flag summary	1b=one or more of the flag bits from bank 0, lane 1 is set.	0		0	
5	5	7	1	RO	Bank 1 lane 8 flag summary	1b=one or more of the flag bits from bank 1, lane 8 is set.	0	00	0	00
		6	1		Bank 1 lane 7 flag summary	1b=one or more of the flag bits from bank 1, lane 7 is set.	0		0	
		5	1		Bank 1 lane 6 flag summary	1b=one or more of the flag bits from bank 1, lane 6 is set.	0		0	
		4	1		Bank 1 lane 5 flag summary	1b=one or more of the flag bits from bank 1, lane 5 is set.	0		0	
		3	1		Bank 1 lane 4 flag summary	1b=one or more of the flag bits from bank 1, lane 4 is set.	0		0	
		2	1		Bank 1 lane 3 flag summary	1b=one or more of the flag bits from bank 1, lane 3 is set.	0		0	
		1	1		Bank 1 lane 2 flag summary	1b=one or more of the flag bits from bank 1, lane 2 is set.	0		0	
		0	1		Bank 1 lane 1 flag summary	1b=one or more of the flag bits from bank 1, lane 1 is set.	0		0	
6	6	7	1	RO	Bank 2 lane 8 flag summary	1b=one or more of the flag bits from bank 2, lane 8 is set.	0	00	0	00
		6	1		Bank 2 lane 7 flag summary	1b=one or more of the flag bits from bank 2, lane 7 is set.	0		0	
		5	1		Bank 2 lane 6 flag summary	1b=one or more of the flag bits from bank 2, lane 6 is set.	0		0	
		4	1		Bank 2 lane 5 flag summary	1b=one or more of the flag bits from bank 2, lane 5 is set.	0		0	
		3	1		Bank 2 lane 4 flag summary	1b=one or more of the flag bits from bank 2, lane 4 is set.	0		0	
		2	1		Bank 2 lane 3 flag summary	1b=one or more of the flag bits from bank 2, lane 3 is set.	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	1		Bank 2 lane 2 flag summary	1b=one or more of the flag bits from bank 2, lane 2 is set.	0		0	
		0	1		Bank 2 lane 1 flag summary	1b=one or more of the flag bits from bank 2, lane 1 is set.	0		0	
7	7	7	1	RO	Bank 3 lane 8 flag summary	1b=one or more of the flag bits from bank 3, lane 8 is set.	0	00	0	00
		6	1		Bank 3 lane 7 flag summary	1b=one or more of the flag bits from bank 3, lane 7 is set.	0		0	
		5	1		Bank 3 lane 6 flag summary	1b=one or more of the flag bits from bank 3, lane 6 is set.	0		0	
		4	1		Bank 3 lane 5 flag summary	1b=one or more of the flag bits from bank 3, lane 5 is set.	0		0	
		3	1		Bank 3 lane 4 flag summary	1b=one or more of the flag bits from bank 3, lane 4 is set.	0		0	
		2	1		Bank 3 lane 3 flag summary	1b=one or more of the flag bits from bank 3, lane 3 is set.	0		0	
		1	1		Bank 3 lane 2 flag summary	1b=one or more of the flag bits from bank 3, lane 2 is set.	0		0	
		0	1		Bank 3 lane 1 flag summary	1b=one or more of the flag bits from bank 3, lane 1 is set.	0		0	
8	8	7	1	RO	L-CDB block 2 complete	Latched flag to indicate completion of the CDB command for CDB block 2. Clear on Read (See Page 01h, Byte 163 bit 7)	0	00	0	00
		6	1		L-CDB block 1 complete	Latched flag to indicate completion of the CDB command for CDB block 1. Clear on Read (See Page 01h, Byte 163 bit 7)	0		0	
		3	3		Reserved					
		2	1		Data Path firmware fault	Becomes set when an integrity check of the firmware for this auxiliary device finds an error.	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	1		Module firmware fault	Becomes set when an integrity check of the module firmware finds an error.	0		0	
		0	1		L-Module state changed flag	Latched Indication of change of Module state. Clear on Read	0		0	
9	9	7	1	RO	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag. Clear on Read	0	00	0	00
		6	1		L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag. Clear on Read	0		0	
		5	1		L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag. Clear on Read	0		0	
		4	1		L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag. Clear on Read	0		0	
		3	1		L-Temp Low Warning	Latched low temperature warning flag. Clear on Read	0		0	
		2	1		L-Temp High Warning	Latched high temperature warning flag. Clear on Read	0		0	
		1	1		L-Temp Low Alarm	Latched low temperature alarm flag. Clear on Read	0		0	
		0	1		L-Temp High Alarm	Latched high temperature alarm flag. Clear on Read	0		0	
10	0A	7	1	RO	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor. Clear on Read	0	00	0	00
		6	1		L-Aux 2 High Warning	Latched high warning for Aux 2 monitor. Clear on Read	0		0	
		5	1		L-Aux 2 Low Alarm	Latched low alarm for Aux 2 monitor. Clear on Read	0		0	
		4	1		L-Aux 2 High Alarm	Latched high alarm for Aux 2 monitor. Clear on Read	0		0	
		3	1		L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor. Clear on Read	0		0	
		2	1		L-Aux 1 High Warning	Latched high warning for Aux 1 monitor. Clear on Read	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	1		L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor. Clear on Read	0		0	
		0	1		L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor. Clear on Read	0		0	
11	0B	7	1	RO	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor. Clear on Read	0	00	0	00
		6	1		L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor. Clear on Read	0		0	
		5	1		L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor. Clear on Read	0		0	
		4	1		L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor. Clear on Read	0		0	
		3	1		L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor. Clear on Read	0		0	
		2	1		L-Aux 3 High Warning	Latched high warning for Aux 3 monitor. Clear on Read	0		0	
		1	1		L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor. Clear on Read	0		0	
		0	1		L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor. Clear on Read	0		0	
12	0C	0	8		Reserved			00		00
13	0D	0	8		Custom			00		00
14	0E	0	8	RO	Module Monitor 1 Temperature MSB	Internally measured temperature signed 2's complement in 1/256-degree Celsius increments NOTE: Temp can be below 0.	0	00	0	00
15	0F	0	8	RO	Module Monitor 1: Temperature1 LSB		0	00	0	00
16	10	0	8	RO	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3-volt input supply voltage: in 100 µV increments	0	00	0	00
17	11	0	8	RO	Module Monitor 2: Supply 3.3-volt LSB		0	00	0	00
18	12	0	8	RO	Module Monitor 3: Aux 1 MSB	TEC Current or Reserved monitor	Not implemented	00	Not implemented	00
19	13	0	8	RO	Module Monitor 3: Aux 1 LSB			00		00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
20	14	0	8	RO	Module Monitor 4: Aux 2 MSB	Laser Temperature monitor Max Cooling Laser Temperature: signed 2's complement in 1/256-degree Celsius increments See Page 01h Byte 145 (CMIS Table 8-30)	Implemented	00	Implemented	00
21	15	0	8	RO	Module Monitor 4: Aux 2 LSB			00		00
22	16	0	8	RO	Module Monitor 5: Aux 3 MSB	Laser Temperature or additional supply voltage monitor	Not implemented	00	Not implemented	00
23	17	0	8	RO	Module Monitor 5: Aux 3 LSB		Not implemented	00	Not implemented	00
24	18	0	8	RO	Module Monitor 6: Custom MSB	Custom monitor		00		00
25	19	0	8	RO	Module Monitor 6: Custom LSB			00		00
26	1A	7	1	RW	Reserved	Reserved		60		60
		6	1		LowPwr	Control the module power mode. Default value = 1 (CMIS 6.3.1.1)	TRUE		TRUE	
		5	1		Squelch control	0b=Tx Squelch reduces OMA 1b=Tx Squelch reduces Pave (CMIS-4.0 Table 8-31)	TxSquelch reduces Pave		TxSquelch reduces Pave	
		4	1			1b=Forces module into low power mode (CMIS 6.3.1.3)	FALSE		FALSE	
		3	1		Software Reset	0b=Not in reset 1b=Software reset. Cleared to zero on a reset. Same as asserting the ResetL signal for the hold time, followed by its de-assertion.	FALSE		FALSE	
		0	3		Control	Custom Control	0		0	
27-28	1B-1C	0	16		Reserved	Reserved	0000	00 00	0000	00 00
29-30	1D-1E	0	16		Control	Custom Global Controls	0000	00 00	0000	00 00
31	1F	7	1	RW	M-CDB Block 2 Complete	Masking Bit for CDB Block 2 Complete Flag	FALSE	00	FALSE	00
		6	1		M-CDB Block 1 Complete	Masking Bit for CDB Block 1 Complete Flag	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	3	RO	Reserved	Reserved				
		2	1	RW	M-Data Path Firmware Fault	Masking Bit for Data Path Firmware Fault Flag	FALSE		FALSE	
		1	1		M-Module Firmware Fault	Masking Bit for Module Firmware Fault Flag	FALSE		FALSE	
		0	1		M-Module State	Masking Bit for Module State Change	FALSE		FALSE	
32	20	7	1	RW	M-Vcc3.3 Low Warning flag mask	Masking Bit for Low Warning	FALSE	00	FALSE	00
		6	1		M-Vcc3.3 High Warning flag mask	Masking Bit for High Warning	FALSE		FALSE	
		5	1		M-Vcc3.3 Low Alarm flag mask	Masking Bit for Low Alarm	FALSE		FALSE	
		4	1		M-Vcc3.3 High Alarm flag mask	Masking Bit for High Alarm	FALSE		FALSE	
		3	1		M-Temp Low Warning flag mask	Masking Bit for Low Warning	FALSE		FALSE	
		2	1		M-Temp High Warning flag mask	Masking Bit for High Warning	FALSE		FALSE	
		1	1		M-Temp Low Alarm flag mask	Masking Bit for Low Alarm	FALSE		FALSE	
		0	1		M-Temp High Alarm flag mask	Masking Bit for High Alarm	FALSE		FALSE	
33	21	7	1	RW	M-Aux2	Masking Bit for Low Warning	FALSE	00	FALSE	00
		6	1		M-Aux2	Masking Bit for High Warning	FALSE		FALSE	
		5	1		M-Aux2	Masking Bit for Low Alarm	FALSE		FALSE	
		4	1		M-Aux2	Masking Bit for High Alarm	FALSE		FALSE	
		3	1		M-Aux1	Masking Bit for Low Warning	FALSE		FALSE	
		2	1		M-Aux1	Masking Bit for High Warning	FALSE		FALSE	
		1	1		M-Aux1	Masking Bit for Low Alarm	FALSE		FALSE	
		0	1		M-Aux1	Masking Bit for High Alarm	FALSE		FALSE	
34	22	7	1	RW	M-Vendor	Masking Bit for Low Warning	FALSE	00	FALSE	00
		6	1		M-Vendor	Masking Bit for High Warning	FALSE		FALSE	
		5	1		M-Vendor	Masking Bit for Low Alarm	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		4	1		M-Vendor	Masking Bit for High Alarm	FALSE		FALSE	
		3	1		M-Aux3	Masking Bit for Low Warning	FALSE		FALSE	
		2	1		M-Aux3	Masking Bit for High Warning	FALSE		FALSE	
		1	1		M-Aux3	Masking Bit for Low Alarm	FALSE		FALSE	
		0	1		M-Aux3	Masking Bit for High Alarm	FALSE		FALSE	
35	23	0	8		Mask Reserved	Reserved				
36	24	0	8		Mask Custom	Module level flag masks	00	00	00	00
37	25	0	8	RO	CDB Block 1 Status	Status of the most recently triggered CDB command in CDB Block 1	00	00	00	00
38	26	0	8	RO	CDB Block 2 Status	Status of the most recently triggered CDB command in CDB Block 2	00	00	00	00
39	27	0	8	RO	Active Module Firmware Major Revision	Numeric representation of Active module firmware major revision	X	xx	X	xx
40	28	0	8	RO	Active Module Firmware Minor Revision	Numeric representation of Active module firmware minor revision	X	xx	X	xx
41	29	0	184	RO	Reserved	Reserved				
64	40	0	152		Custom	Custom	00000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
85	55	0	8	RO	Module Type	Module Type Encoding (CMIS Table 8-12) 02h Optical Interfaces: SMF	Optical: SMF	02	Optical: SMF	02
86	56	0	8	RO	ApSel 1 Advertising	Host Interface Code from SFF-8024 Host Electrical Interfaces	11h: 400GAUI-8 C2M (Annex 120E)	11	0Dh: 100GAUI-2 C2M (Annex 135G)	0D
87	57	0	8	RO	ApSel 1 Advertising	Media Interface Code	1Ch: 400GBASE-DR4	1C	14h: 10GFC-MM, 100GBASE-DR	14
88	58	4	4	RO	ApSel 1 Advertising	Host Lane Count	8	84	2	21
		0	4		ApSel 1 Advertising	Media Lane Count	4		1	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
89	59	7	1	RO	ApSel 1 Advertising	Permitted to start on Host Lane 8	FALSE	01	FALSE	55
		6	1			Permitted to start on Host Lane 7	FALSE		TRUE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		TRUE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		TRUE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	TRUE		TRUE	
90	5A	0	8	RO	ApSel 2 Advertising	Host Interface Code	0Dh: 100GAUI-2 C2M (Annex 135G)	0D	11h: 400GAUI-8 C2M (Annex 120E)	11
91	5B	0	8	RO	ApSel 2 Advertising	Media Interface Code	14h: 10GFC-MM, 100GBASE-DR	14	1Ch: 400GBASE-DR4	1C
92	5C	4	4	RO	ApSel 2 Advertising	Host Lane Count	2	21	8	84
		0	4		ApSel 2 Advertising	Media Lane Count	1		4	
93	5D	7	1	RO	ApSel 2 Advertising	Permitted to start on Host Lane 8	FALSE	55	FALSE	01
		6	1			Permitted to start on Host Lane 7	TRUE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	TRUE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	TRUE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	TRUE		TRUE	
94	5E	0	8	RO	ApSel 3 Advertising	Host Interface Code	FFh: End of Advertised ApSel Codes	FF	FFh: End of Advertised ApSel Codes	FF
95	5F	0	8	RO	ApSel 3 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
96	60	4	4	RO	ApSel 3 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 3 Advertising	Media Lane Count	0		0	
97	61	7	1	RO	ApSel 3 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
98	62	0	8	RO	ApSel 4 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
99	63	0	8	RO	ApSel 4 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
100	64	4	4	RO	ApSel 4 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 4 Advertising	Media Lane Count	0		0	
101	65	7	1	RO	ApSel 4 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
102	66	0	8	RO	ApSel 5 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
103	67	0	8	RO	ApSel 5 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
104	68	4	4	RO	ApSel 5 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 5 Advertising	Media Lane Count	0		0	
105	69	7	1	RO	ApSel 5 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
106	6A	0	8	RO	ApSel 6 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
107	6B	0	8	RO	ApSel 6 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
108	6C	4	4	RO	ApSel 6 Advertising	Host Lane Count	0	00	0	00
108	6C	0	4		ApSel 6 Advertising	Media Lane Count	0		0	
109	6D	7	1	RO	ApSel 6 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
110	6E	0	8	RO	ApSel 7 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
111	6F	0	8	RO	ApSel 7 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
112	70	4	4	RO	ApSel 7 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 7 Advertising	Media Lane Count	0		0	
113	71	7	1	RO	ApSel 7 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
114	72	0	8	RO	ApSel 8 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
115	73	0	8	RO	ApSel 8 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
116	74	4	4	RO	ApSel 8 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 8 Advertising	Media Lane Count	0		0	
117	75	7	1	RO	ApSel 8 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
118-121	76-79	0	32	WO	Password Change Entry Area	Password Change Entry Area	00000000	00 00 00 00	00000000	00 00 00 00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
122-125	7A – 7D	0	32	WO	Password Entry Area	Password Entry Area	00000000	00 00 00 00	00000000	00 00 00 00
126	7E	0	8	RW	Bank Select Byte	The value written to the Bank Select byte 126 determines which bank is accessed when banking is supported	00	00	00	00
127	7F	0	8	RW	Page Select Byte	A value of 00h indicates Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, etc., indicate that the page identified by the bank select byte is mapped to Bytes 128-255.	00	00	00	00

TABLE 2: UPPER PAGE 00H (ADMINISTRATIVE INFORMATION)

Upper Page 00h provides static module identity and capabilities information. (CMIS-4.0 Table 8-15 to Table 8-25)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	8	RO	Identifier	Same as Page 00h lower Byte 0	QSFP-DD	18	QSFP-DD	18
129-144	81-90	0	128	RO	Vendor Name	Vendor Name (ASCII)	FINISAR	46 49 4E 49 53 41 52 20 20 20 20 20 20 20 20 20	FINISAR	46 49 4E 49 53 41 52 20 20 20 20 20 20 20 20 20
145-147	91-93	0	24	RO	Vendor OUI	Vendor IEEE Company ID	00 90 65h (36965 Decimal)	00 90 65	00 90 65h (36965 Decimal)	00 90 65

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
148-163	94-A3	0	128	RO	Vendor PN	Part Number Provided by QSFP Vendor (ASCII)	FTCD4523E2PCM-4A	46 54 43 44 34 35 32 33 45 32 50 43 4D 2D 34 41	FTCD4523E2PCM	46 54 43 44 34 35 32 33 45 32 50 43 4D 20 20 20
							FTCD4533E2PCM-4A	46 54 43 44 34 35 33 33 45 32 50 43 4D 2D 34 41	FTCD4533E2PCM	46 54 43 44 34 35 33 33 45 32 50 43 4D 20 20 20
164-165	A4-A5	0	16	RO	Vendor Rev.	Revision level for part number provided by vendor (ASCII)	XX	xx xx	XX	xx xx
166-181	A6-B5	0	128	RO	Vendor SN	Serial number provided by vendor (ASCII)	A123456	41 31 32 33 34 35 36 20 20 20 20 20 20 20 20 20	A123456	41 31 32 33 34 35 36 20 20 20 20 20 20 20 20 20
182-183	B6-B7	0	16	RO	Date Code_Year	ASCII code, two low order digits of year. (00=2000).	00	30 30	00	30 30
184-185	B8-B9	0	16	RO	Date Code_Month	ASCII code, digits of month (01=Jan through 12=Dec)	00	30 30	00	30 30
186-187	BA-BB	0	16	RO	Date Code_Day	ASCII code, day of month (01-31)	00	30 30	00	30 30
188-189	BC-BD	0	16	RO	Date Code_Lot code	ASCII code, vendor specific lot code, may be blank	00	30 30	00	30 30
190-199	BE-C7	0	80	RO	CLEI code	Common Language Equipment Identification code		00 00 00 00 00 00 00 00 00 00		00 00 00 00 00 00 00 00 00 00
200	C8	5	3	RO	Module Power Consumption	See QSFP-DD MSA hardware specification (Table 8) 0101(05h): Power class 6	Power class 6 (< 12 W) Bit 7-5: 101	A0	Power class 6 (< 12 W) Bit 7-5: 101	A0
		0	5		Reserved	Reserved	00		00	
201	C9	0	8	RO	Module Power Consumption	Max power consumption in units of 0.25 W (rounded up)	48	30	48	30
202	CA	6	2	RO	Cable Length (Copper or Active)	Multiplier for value in bits 5-0. 00 = multiplier of 0.1 11 = multiplier of 100	multiplier of 0.1	00	multiplier of 0.1	00
		0	6		Cable Length (Copper or Active)	Link length base value. To calculate actual link length use multiplier in bits 7-6.	0		0	
203	CB	0	8	RO	Media Connector Type	Type of connector present in the module. See SFF-8024 for codes.	MPO 1x12	0C	MPO 1x12	0C

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
204	CC	0	8	RO	Copper Cable Attenuation	Passive copper cable attenuation at 5GHz in 1dB increments	0	00	0	00
205	CD	0	8	RO	Copper Cable Attenuation	Passive copper cable attenuation at 7GHz in 1dB increments	0	00	0	00
206	CE	0	8	RO	Copper Cable Attenuation	Passive copper cable attenuation at 12.9GHz in 1dB increments	0	00	0	00
207	CF	0	8	RO	Copper Cable Attenuation	Passive copper cable attenuation at 25.8GHz in 1dB increments	0	00	0	00
208-209	D0-D1	0	16	RO	Reserved	Reserved				
210	D2	7	1	RO	Near end implementation	Lane 8 (0b=Implemented. 1b=Not implemented)	1	F0	1	F0
		6	1		Near end implementation	Lane 7 (0b=Implemented. 1b=Not implemented)	1		1	
		5	1		Near end implementation	Lane 6 (0b=Implemented. 1b=Not implemented)	1		1	
		4	1		Near end implementation	Lane 5 (0b=Implemented. 1b=Not implemented)	1		1	
		3	1		Near end implementation	Lane 4 (0b=Implemented. 1b=Not implemented)	0		0	
		2	1		Near end implementation	Lane 3 (0b=Implemented. 1b=Not implemented)	0		0	
		1	1		Near end implementation	Lane 2 (0b=Implemented. 1b=Not implemented)	0		0	
		0	1		Near end implementation	Lane 1 (0b=Implemented. 1b=Not implemented)	0		0	
211	D3	5	3	RO	Reserved	Reserved				
		0	5		Far end implementation	CMIS Table 8-23 for config code of discrete far end connectors	0	00	0	00
212	D4	0	8	RO	Media Interface Technology	Media interface technology	1310 nm EML	06	1310 nm EML	06
213-220	D5-DC	0	64	RO	Reserved	Reserved				
221	DD	0	8	RO	Custom	Custom	00	00	00	00
222	DE	0	8	RO	Checksum	The checksum code is the low order 8 bits of the arithmetic sum	FTCD4523E2PCM-4A Checksum = 122	7A	FTCD4523E2PCM Checksum = 56	38

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
						of all byte values from byte 128 to byte 221, inclusive	FTCD4533E2PCM-4A Checksum = 123	7B	FTCD4533E2PCM Checksum = 57	39
223-255	DF-FF	0	264	RW	User Custom Info	User Custom Info (non-volatile)	00	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

TABLE 3: UPPER PAGE 01H (ADVERTISING)

Page 01h contains advertising fields that define properties that are unique to the module. Presence of this page is advertised in bit 7 byte 2 of lower Page 00h. All fields on this upper Page 01h are read only and static. (CMIS-4.0 Table 8-25 to Table 8-39)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	8	RO	Inactive Module Firmware Revision	Major Revision	0	00	0	00
129	81	0	8	RO	Inactive Module Firmware Revision	Minor Revision	0	00	0	00
130	82	0	8	RO	Module Hardware Revision	Major Revision	X	xx	X	xx
131	83	0	8	RO	Module Hardware Revision	Minor Revision	Y	yy	Y	yy
132	84	6	2	RO	Length (SMF)	Link length multiplier for SMF fiber 00 = 0.1 (1 to 6.3 km)	FTCD4523E2PCM-4A **0.1 km** Bit 7-6 = 00 Bit 5-0 = 000101	05	FTCD4523E2PCM **0.1 km** Bit 7-6 = 00 Bit 5-0 = 000101	05
		0	6			Base link length for SMF fiber: 500m				
		6	2		Length (SMF)	Link length multiplier for SMF fiber 01 = 1 (1 to 63 km)	FTCD4533E2PCM-4A **1 km** Bit 7-6 = 01	42	FTCD4533E2PCM **1 km** Bit 7-6 = 01	42
		0	6			Base link length for SMF fiber: 2Km				

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
							Bit 5-0 = 000010		Bit 5-0 = 000010	
133	85	0	8	RO	Length (OM5)	Link Length for OM5 Fiber, Units of 2m.	0	00	0	00
134	86	0	8	Ro	Length (OM4)	Link Length for OM4 Fiber, Units of 2m.	0	00	0	00
135	87	0	8	RO	Length (OM3 50um)	Link Length for EBW 50/125 µm Fiber, Units of 2m	0	00	0	00
136	88	0	8	RO	Length (OM2 50um)	Link Length For 50/125 µm Fiber, Units of 1m	0	00	0	00
137	89	0	8	RO	Reserved	Reserved				
138-139	8A-8B	0	16	RO	Wavelength	Nominal wavelength (Wavelength=Value/20 in nm)	26,220	66 6C	26,220	66 6C
140-141	8C-8D	0	16	RO	Wavelength Tolerance	Guaranteed range (+/- value) (Wavelength Tol.=value/200 in nm)	1,300	05 14	1,300	05 14
142	8E	7	1	RO	CMIS Implementation	Reserved		24		24
		6	1		CMIS Implementation	Pages 20h-2Fh implemented for versatile diagnostic monitoring	FALSE		FALSE	
		5	1		CMIS Implementation	Bank Page 13h-14h implemented for diagnostic features	TRUE		TRUE	
		3	2		CMIS Implementation	Reserved				
		2	1		CMIS Implementation	Page 03h Implemented	TRUE		TRUE	
		0	2		CMIS Implementation	Bank pages Implemented	Bank 0 only Implemented		Bank 0 only Implemented	
143	8F	5	3	RO	ModSelL wait time exponent	The ModSelL wait time value is the mantissa x 2^exponent expressed in microseconds.	6	DF	6	DF
		0	5		ModSelL wait time mantissa	The ModSelL wait time value is the mantissa x 2^exponent expressed in microseconds.	31		31	
144	90	4	4	RO	DataPathDeinit_MaxDuration	Encoded Max Duration of the DataPathDeinit state (CMIS Table 8-29)	100ms -500ms Bit7-4 = 0101	57	100ms -500ms Bit7-4 = 0101	57

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		DataPathInit_MaxDuration	Encoded Max Duration of the DataPathInit state (CMIS Table 8-29)	1 s to 5 s Bit4-0 = 0111		1 s to 5 s Bit4-0 = 0111	
145	91	7	1	RO	Cooling implemented	Cooled Transmitter 0b=Uncooled transmitter device 1b=Cooled transmitter	TRUE = 1	C0	TRUE = 1	C0
		5	2		Tx input clock recovery capabilities (CMIS Table 8-30)	Tx Input Clock Synchronicity 01b= Tx input lanes 1-4 and 5-8 to be in separate Tx synchronous groups	Lanes 1-2, 3-4, 5-6, 7-8 in separate synchronous groups: 02		Lanes 1-2, 3-4, 5-6, 7-8 in separate synchronous groups: 02	
		3	2		Reserved	Reserved				
		2	1		Aux 3 Monitor type	1b=Aux 3 monitor is Vcc2 0b=Aux 3 monitor is Laser Temperature	0: Laser Temperature		0: Laser Temperature	
		1	1		Aux 2 Monitor type	1b=Aux 2 monitor is TEC current 0b=Aux 2 monitor is Laser Temperature	0: Laser Temperature		0: Laser Temperature	
		0	1		Aux 1 Monitor type	1b=Aux 1 monitor is TEC current 0b=Aux 1 monitor is reserved	0: Reserved		0: Reserved	
146	92	0	8	RO	Maximum module temperature	Maximum temperature allowed, 8-bit signed 2's complement in degC	46	46	46	46
147	93	0	8	RO	Minimum module temperature	Minimum temperature allowed, 8-bit signed 2's complement in degC	00	00	00	00
148	94	0	16	RO	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10 ns rounded to the nearest 10 ns. A value of all zeroes indicates not specified.	0	00 00 00	0	00 00 00
149	95	0	8	RO	Propagation Delay LSB				0	
150	96	0	8	RO	Minimum operating voltage	Minimum operating voltage, in 20 mV increments	157	9D	157	9D
151	97	7	1	RO	Detector type	0b=PIN detector 1b=APD detector	PIN	18	PIN	18
		5	2		Rx Output Eq type	00b=Peak-to-peak amplitude stays constant, or not implemented	Peak-to-Peak constant, or Not Implemented or No Info		Peak-to-Peak constant, or Not Implemented or No Info	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		4	1		Rx Optical Power Measurement type	0b=OMA 1b=average power	Average Power: 01		Average Power: 01	
		3	1		Rx LOS type	0b=Rx LOS responds to OMA 1b=Rx LOS responds to Pave	Average Power: 01		Average Power: 01	
		2	1		RX LOS fats mode implemented	0b=Rx LOS fast mode not implemented 1b=Rx LOS fast mode implemented	FALSE		FALSE	
		1	1		Tx Disable fast mode implemented	0b=Tx Disable fast mode not implemented 1b=Tx Disable fast mode implemented	FALSE		FALSE	
		0	1		Module-Wide Tx Disable	0b=Tx Disable implemented per lane 1b=disables all Tx lanes	FALSE		FALSE	
152	98	0	8	RO	Implementation	Minimum per-lane power consumption saved in CDR bypass, units of 0.01W	0	00	0	00
153	99	7	1	RO	Rx Output Amplitude 0011b implemented	0b=Amplitude code 0011b not implemented 1b=Amplitude code 0011b implemented	TRUE	F9	TRUE	F9
		6	1		Rx Output Amplitude 0010b implemented	0b=Amplitude code 0010b not implemented 1b=Amplitude code 0010b implemented	TRUE		TRUE	
		5	1		Rx Output Amplitude 0001b implemented	0b=Amplitude code 0001b not implemented 1b=Amplitude code 0001b implemented	TRUE		TRUE	
		4	1		Rx Output Amplitude 0000b implemented	0b=Amplitude code 0000b not implemented 1b=Amplitude code 0000b implemented	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Max Tx Input Eq	Max supported Tx Input Eq control (units of 1 dB)	9		9	
154	9A	4	4	RO	Max Rx Output Eq Post-cursor	Max supported Rx Output Eq Post-cursor control (units of 1 dB)	7	77	7	77
		0	4		Max Rx Output Eq Pre-cursor	Max supported Rx Output Eq Pre-cursor control (units of 0.5 dB)	7		7	
155	9B	7	1	RO	Wavelength control implemented	0b=No wavelength control 1b=Active wavelength control implemented	FALSE	3B	FALSE	3B
		6	1		Tunable transmitter implemented	0b=Transmitter not tunable 1b=Transmitter tunable	FALSE		FALSE	
		4	2		Tx Squelch implemented	11b=User control both OMA and Pave squelch supported. (CMIS Table 8-7)	User configurable		User configurable	
		3	1		Tx Force Squelch implemented	0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented	TRUE		TRUE	
		2	1		Tx Squelch Disable implemented	0b= Tx Squelch Disable not implemented 1b= Tx Squelch Disable implemented	FALSE		FALSE	
		1	1		Tx Disable implemented	0b=Tx Disable not implemented 1b=Tx Disable implemented	TRUE		TRUE	
		0	1		Tx Polarity Flip implemented	0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	TRUE		TRUE	
156	9C	3	5	RO	Reserved	Reserved		03		03
		2	1		Rx Squelch Disable implemented	0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	1		Rx Disable implemented	0b=Rx Disable not implemented 1b=Rx Disable implemented	TRUE		TRUE	
		0	1		Rx Polarity Flip implemented	0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented	TRUE		TRUE	
157	9D	4	4	RO	Implementation	Reserved		07		07
		3	1		Tx Adaptive Input Eq Fail flag implemented	Tx Adaptive Input Eq Fail flag 0b=not implemented 1b=implemented	FALSE		FALSE	
		2	1		TX CDR LOL flag implemented	Tx CDR Loss of Lock flag 0b=not implemented 1b=implemented	TRUE		TRUE	
		1	1		TX LOS flag implemented	Tx Loss of Signal flag 0b=not implemented 1b=implemented	TRUE		TRUE	
		0	1		TX Fault flag implemented	Tx Fault flag 0b=not implemented 1b=implemented	TRUE		TRUE	
158	9E	3	5	RO	Implementation	Reserved		06		06
		2	1		Rx LOL flag implemented	Rx CDR Loss of Lock flag 0b=not implemented 1b=implemented	TRUE		TRUE	
		1	1		Rx LOS flag implemented	Rx Loss of Signal flag 0b=not implemented 1b=implemented	TRUE		TRUE	
		0	1		Reserved	Reserved				
159	9F	6	2	RO	Reserved	Reserved		0B		0B
		5	1		Custom monitor implemented	0b=Custom monitor not implemented 1b=Custom monitor implemented	FALSE		FALSE	
		4	1		Aux 3 monitor implemented	0b=Aux 3 monitor not implemented 1b=Aux 3 monitor implemented	FALSE		FALSE	
		3	1		Aux 2 monitor implemented	0b=Aux 2 monitor not implemented 1b=Aux 2 monitor implemented	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		2	1		Aux 1 monitor implemented	0b=Aux 1 monitor not implemented 1b=Aux 1 monitor implemented	FALSE		FALSE	
		1	1		Internal 3.3 Volts monitor implemented	0b=Internal 3.3 V monitor not implemented 1b=Internal 3.3 V monitor implemented	TRUE		TRUE	
		0	1		Temperature monitor implemented	0b=Temperature monitor not implemented 1b=Temperature monitor implemented	TRUE		TRUE	
160	A0	5	3	RO	Implementation	Reserved		07		07
		3	2		TX Bias current measurement and threshold multiplier	Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold (CMIS Table 8-42 and Table 8-62) 00b=multiply x1 01b=multiply x2 10b=multiply x4 11b=reserved	x1: 2 uA		x1: 2 uA	
		2	1		Rx Optical Input Power monitor implemented	Rx Output Optical Power monitor 0b=not implemented 1b=implemented	TRUE		TRUE	
		1	1		Tx Optical Input Power monitor implemented	Tx Output Optical Power monitor 0b=not implemented 1b=implemented	TRUE		TRUE	
		0	1		TX Bias monitor implemented	Tx Bias monitor 0b=not implemented 1b=implemented	TRUE		TRUE	
161	A1	7	1	RO	Implementation	Reserved		09		09
		5	2		Tx Input Eq Store/Recall buffer count	Tx Input Eq Store/Recall buffer count 00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall	Not implemented		Not implemented	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
						buffer count=2 11b=reserved				
		4	1		Tx Input Eq Freeze implemented	Tx Input Eq Freeze 0b=not implemented 1b=implemented	FALSE		FALSE	
		3	1		Adaptive Tx Input Eq implemented	Adaptive Tx Input Eq 0b=not implemented 1b=Eq implemented	TRUE		TRUE	
		2	1		Tx Input Eq fixed manual control implemented	Tx Input Eq Fixed Manual control 0b=not implemented 1b=implemented	FALSE		FALSE	
		1	1		Tx CDR Bypass control implemented	Tx CDR Bypass control 0b=not implemented 1b=implemented (if CDR is implemented, it will be enabled)	FALSE		FALSE	
		0	1		Tx CDR implemented	Tx CDR 0b=not implemented 1b=implemented	TRUE		TRUE	
162	A2	6	2	RO	Implementation	Reserved		3D		3D
		5	1		Staged Set 1 implemented	Staged Control Set 1 implemented on Page 10h	TRUE		TRUE	
		3	2		Rx Output Eq control implemented	Rx Output Eq control 00b=not implemented 01b=Pre-cursor control implemented 10b=Post-cursor control implemented 11b=Pre- and Post-cursor control implemented	Rx Output Eq Pre- and Post-cursor control implemented		Rx Output Eq Pre- and Post-cursor control implemented	
		2	1		Rx Output Amplitude control implemented	Rx Output Amplitude control 0b=not implemented 1b=implemented	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	1		Rx CDR Bypass control implemented	Rx CDR Bypass control 0b=not implemented 1b=implemented (if CDR is implemented, it will be enabled)	FALSE		FALSE	
		0	1		Rx CDR implemented	Rx CDR 0b=not implemented 1b=implemented	TRUE		TRUE	
163	A3	6	2	RO	CDB Advertisement (CMIS Table 8-35)	CDB Implemented 00b=CDB not implemented 01b=Only one instance of CDB implemented. In Pages 9Fh and A0h-AFh, Bank 0 only supported	Only one instance of CDB implemented (only Bank 0 supported)	60	Only one instance of CDB implemented (only Bank 0 supported)	60
		5	1		CDB Advertisement (CMIS Table 8-35)	CDB background operation Implemented 0b=not implemented. 1b=implemented	TRUE		TRUE	
		4	1		CDB Advertisement (CMIS Table 8-35)	CDB Auto Paging Implemented 0b=not implemented 1b=Paging and Auto page wrap implemented	FALSE		FALSE	
		0	4		CDB Advertisement (Refer to Table 8-35)	This field defines which EPL pages are implemented in the module 0=Pages A0h-AFh not implemented	Page A0-Afh not implemented		Page A0-Afh not implemented	
164	A4	0	8	RO	CDB Max TWI Bytes per write transaction (CMIS Table 8-35)	Support for longer TWI write transactions (only on CDB pages 9Fh-AFh) CdbMaxTWIWriteBytes = (Byte 164+1) * 8	15	0F	15	0F
165	A5	7	1	RO	CDB command processing option	1b: CDB commands are processed on STOP bit when CMD 128/129 registers are within the write I2C transaction 0b: CDB commands are processed on a write to Byte 129 of Page 9F.	Processed on STOP bit when CMD 128/129 registers are within the write I2C transaction	80	Processed on STOP bit when CMD 128/129 registers are within the write I2C transaction	80
		5	2		CDB Advertisement	Reserved				

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
					(CMIS Table 8-35)					
		0	5		CDB commands tNACK time	Denotes tNACK for CDB commands if above 80ms using values of 0-31b. Ignored when Byte 166 bit 7 is 0b.	0		0	
166	A6	7	1	RO	CDB tNACK time indicator	0b=tNACK in bits 6-0 also applies to CDB Generic commands. (CMIS Table 8-35)	tNACK in bits 6-0 applies to CDB	00	tNACK in bits 6-0 applies to CDB	00
		0	7		Maximum tNACK time	tNACK = (80 - XX) ms. XX is the value of this register in ms.	0		0	
167	A7	4	4	RO	ModulePwrDn MaxDuration	Maximum duration of the ModulePwrDn state 0110b: 500ms<= maximum state duration<1s (CMIS Table 8-29)	6	68	6	68
		0	4		ModulePwrUp MaxDuration	Maximum duration of the ModulePwrUp state 1000b: 5s <=maximum state duration<10s (CMIS Table 8-29)	8		8	
168	A8	4	4	RO	DataPathTxTurn Off_MaxDuration	Max Duration of DataPathTxTurnOFF State 1 ms <= maximum state duration < 5 ms	1	15	1	15
		0	4		DataPathTxTurn On_MaxDuration	Max Duration of DataPathTxTurnON State 100 ms <= MAX state duration < 500 ms	5		5	
169-175	A9-AF	0	56	RO	Reserved	Reserved				
176	B0	7	1	RO	ApSel 1 Advertising	Permitted to start on Media Lane 8 – Lane 1 (bit 7 -0)	FALSE	01	FALSE	0F
		6	1						FALSE	
		5	1						FALSE	
		4	1						FALSE	
		3	1						TRUE	
		2	1						TRUE	
		1	1						TRUE	
		0	1				TRUE		TRUE	
177	B1	7	1	RO	ApSel 2 Advertising	Permitted to start on Media Lane 8	FALSE	0F	FALSE	01

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		6	1		ApSel 2 Advertising	Permitted to start on Media Lane 7	FALSE			
		5	1		ApSel 2 Advertising	Permitted to start on Media Lane 6	FALSE			
		4	1		ApSel 2 Advertising	Permitted to start on Media Lane 5	FALSE			
		3	1		ApSel 2 Advertising	Permitted to start on Media Lane 4	TRUE			
		2	1		ApSel 2 Advertising	Permitted to start on Media Lane 3	TRUE			
		1	1		ApSel 2 Advertising	Permitted to start on Media Lane 2	TRUE			
		0	1		ApSel 2 Advertising	Permitted to start on Media Lane 1	TRUE		TRUE	
178	B2	7	1	RO	ApSel 3 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 3 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 3 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 3 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 3 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 3 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 3 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 3 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
179	B3	7	1	RO	ApSel 4 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 4 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 4 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 4 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 4 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 4 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 4 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 4 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
180	B4	7	1	RO	ApSel 5 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 5 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 5 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 5 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 5 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 5 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 5 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 5 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
181	B5	7	1	RO	ApSel 6 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 6 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		5	1		ApSel 6 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 6 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 6 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 6 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 6 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 6 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
182	B6	7	1	RO	ApSel 7 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 7 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 7 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 7 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 7 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 7 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 7 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 7 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
183	B7	7	1	RO	ApSel 8 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 8 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 8 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 8 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 8 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 8 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 8 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 8 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
184	B8	7	1	RO	ApSel 9 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 9 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 9 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 9 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 9 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 9 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 9 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 9 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
185	B9	7	1	RO	ApSel 10 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 10 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 10 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		4	1		ApSel 10 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 10 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 10 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 10 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 10 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
186	BA	7	1	RO	ApSel 11 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 11 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 11 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 11 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 11 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 11 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 11 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 11 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
187	BB	7	1	RO	ApSel 12 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 12 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 12 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 12 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 12 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 12 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 12 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 12 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
188	BC	7	1	RO	ApSel 13 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 13 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 13 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 13 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 13 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 13 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 13 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 13 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
189	BD	7	1	RO	ApSel 14 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 14 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 14 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 14 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	1		ApSel 14 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 14 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 14 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 14 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
190	BE	7	1	RO	ApSel 15 Advertising	Permitted to start on Media Lane 8	FALSE	00	FALSE	00
		6	1		ApSel 15 Advertising	Permitted to start on Media Lane 7	FALSE		FALSE	
		5	1		ApSel 15 Advertising	Permitted to start on Media Lane 6	FALSE		FALSE	
		4	1		ApSel 15 Advertising	Permitted to start on Media Lane 5	FALSE		FALSE	
		3	1		ApSel 15 Advertising	Permitted to start on Media Lane 4	FALSE		FALSE	
		2	1		ApSel 15 Advertising	Permitted to start on Media Lane 3	FALSE		FALSE	
		1	1		ApSel 15 Advertising	Permitted to start on Media Lane 2	FALSE		FALSE	
		0	1		ApSel 15 Advertising	Permitted to start on Media Lane 1	FALSE		FALSE	
191-222	BF-DE	0	256	RO	Custom	Custom	00000000000000000000000000000000000000000000000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00000000000000000000000000000000000000000000000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
223	DF	0	8	RO	ApSel 9 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
224	E0	0	8	RO	ApSel 9 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
225	E1	4	4	RO	ApSel 9 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 9 Advertising	Media Lane Count	0		0	
226	E2	7	1	RO	ApSel 9 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
227	E3	0	8	RO	ApSel 10 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
228	E4	0	8	RO	ApSel 10 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
229	E5	4	4	RO	ApSel 10 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 10 Advertising	Media Lane Count	0		0	
230	E6	7	1	RO	ApSel 10 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
231	E7	0	8	RO	ApSel 11 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
232	E8	0	8	RO	ApSel 11 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
233	E9	4	4	RO	ApSel 11 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 11 Advertising	Media Lane Count	0		0	
234	EA	7	1	RO	ApSel 11 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
235	EB	0	8	RO	ApSel 12 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
236	EC	0	8	RO	ApSel 12 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
237	ED	4	4	RO	ApSel 12 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 12 Advertising	Media Lane Count	0		0	
238	EE	7	1	RO	ApSel 12 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
239	EF	0	8	RO	ApSel 13 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
240	F0	0	8	RO	ApSel 13 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
241	F1	4	4	RO	ApSel 13 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 13 Advertising	Media Lane Count	0		0	
242	F2	7	1	RO	ApSel 13 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
243	F3	0	8	RO	ApSel 14 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
244	F4	0	8	RO	ApSel 14 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
245	F5	4	4	RO	ApSel 14 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 14 Advertising	Media Lane Count	0		0	
246	F6	7	1	RO	ApSel 14 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
247	F7	0	8	RO	ApSel 15 Advertising	Host Interface Code	0h: Undefined	00	0h: Undefined	00
248	F8	0	8	RO	ApSel 15 Advertising	Media Interface Code	0h: Undefined	00	0h: Undefined	00
249	F9	4	4	RO	ApSel 15 Advertising	Host Lane Count	0	00	0	00
		0	4		ApSel 15 Advertising	Media Lane Count	0		0	
250	FA	7	1	RO	ApSel 15 Advertising	Permitted to start on Host Lane 8	FALSE	00	FALSE	00
		6	1			Permitted to start on Host Lane 7	FALSE		FALSE	
		5	1			Permitted to start on Host Lane 6	FALSE		FALSE	
		4	1			Permitted to start on Host Lane 5	FALSE		FALSE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	1			Permitted to start on Host Lane 4	FALSE		FALSE	
		2	1			Permitted to start on Host Lane 3	FALSE		FALSE	
		1	1			Permitted to start on Host Lane 2	FALSE		FALSE	
		0	1			Permitted to start on Host Lane 1	FALSE		FALSE	
251-254	FB-FD	0	32	RO	Reserved	Reserved				
255	FF	0	8	RW	Checksum	Checksum for byte 130 to 254, inclusive. Note that the module firmware revision in bytes 128 and 129 is not included in the checksum.	FTCD4523E2PCM-4A Checksum = 101	65	FTCD4523E2PCM Checksum = 101	65
							FTCD4533E2PCM-4A Checksum = 162	A2	FTCD4533E2PCM Checksum = 162	A2

TABLE 4: UPPER PAGE 02H (MODULE AND LANE THRESHOLDS)

Upper Page 02h includes module defined thresholds for module level and lane-specific monitors. The presence of Page 02h is advertised in bit 7 of byte 2 in lower page 00h. All fields on page 02h are read only and static. (CMIS-4.0 Table 8-40 to Table 8-43)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	8	RO	Temperature High Alarm threshold MSB	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256-degree Celsius increments.	75.000	4B	75.000	4B
129	81	0	8	RO	Temperature High Alarm threshold LSB			00		00
130	82	0	16	RO	Temperature Low Alarm threshold MSB		-5.000	FB	-5.000	FB
131	83	0	8	RO	Temperature Low Alarm threshold LSB			00		00
132	84	0	16	RO	Temperature High Warning threshold MSB		70.000	46	70.000	46

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
133	85	0	8	RO	Temperature High Warning threshold LSB			00		00
134	86	0	8	RO	Temperature Low Warning threshold MSB		0.000	00	0.000	00
135	87	0	8	RO	Temperature low warning threshold LSB			00		00
136	88	0	16	RO	Supply 3.3V high alarm threshold MSB	Thresholds for internally measured 3.3-volt input supply voltage: in 100 µV increments	3.63	8D	3.63	8D
137	89	0	8	RO	Supply 3.3V high alarm threshold LSB			CC		CC
138	8A	0	8	RO	Supply 3.3V low alarm threshold MSB		2.97	74	2.97	74
139	8B	0	8	RO	Supply 3.3V low alarm threshold LSB			04		04
140	8C	0	8	RO	Supply 3.3V high warning threshold MSB		3.465	87	3.465	87
141	8D	0	8	RO	Supply 3.3V high warning threshold LSB			5A		5A
142	8E	0	8	RO	Supply 3.3V low warning threshold MSB		3.1350	7A	3.1350	7A
143	8F	0	8	RO	Supply 3.3V low warning threshold LSB			76		76
144	90	0	8	RO	Aux 1 monitor high alarm threshold -- MSB	Reserved Monitor	0	00	0	00
145	91	0	8	RO	Aux 1 monitor high alarm threshold --LSB			00		00
146	92	0	8	RO	Aux 1 monitor low alarm threshold -- MSB	Reserved Monitor	0	00	0	00
147	93	0	8	RO	Aux 1 monitor Low Alarm threshold LSB			00		00
148	94	0	8	RO	Aux 1 monitor High Warning threshold MSB	Reserved Monitor	0	00	0	00
149	95	0	8	RO	Aux 1 monitor High Warning threshold LSB			00		00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
150	96	0	8	RO	Aux 1 monitor Low Warning threshold MSB	Reserved Monitor	0	00	0	00
151	97	0	8	RO	Aux 1 monitor Low Warning threshold LSB			00		00
152	98	0	8	RO	Aux 2 monitor high alarm threshold - MSB	Laser Temperature monitor signed 2's complement in 1/256 degree Celsius increments	19,200	4B	19,200	4B
153	99	0	8	RO	Aux 2 monitor high alarm threshold - LSB			00		00
154	9A	0	8	RO	Aux 2 monitor low alarm threshold-MSB		8,960	23	8,960	23
155	9B	0	8	RO	Aux 2 monitor low alarm threshold-LSB			00		00
156	9C	0	8	RO	Aux 2 monitor High Warning threshold MSB		17,920	46	17,920	46
157	9D	0	8	RO	Aux 2 monitor High Warning threshold LSB			00		00
158	9E	0	8	RO	Aux 2 monitor Low Warning threshold MSB		10,240	28	10,240	28
159	9F	0	8	RO	Aux 2 monitor Low Warning threshold LSB			00		00
160	A0	0	8	RO	Aux 3 monitor high alarm threshold-MSB	Thresholds for Laser Temperature or additional supply voltage monitor Laser Temperature monitor, signed 2's complement in 1/256-degree Celsius increments	0	00	0	00
161	A1	0	8	RO	Aux 3 monitor high alarm threshold-LSB			00		00
162	A2	0	8	RO	Aux 3 monitor low alarm threshold-MSB		0	00	0	00
163	A3	0	8	RO	Aux 3 monitor low alarm threshold-LSB			00		00
164	A4	0	8	RO	Aux 3 monitor High Warning threshold MSB		0	00	0	00
165	A5	0	8	RO	Aux 3 monitor High Warning threshold LSB			00		00
166	A6	0	8	RO	Aux 3 monitor Low Warning threshold MSB		0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
167	A7	0	8	RO	Aux 3 monitor Low Warning threshold LSB			00		00
168	A8	0	8	RO	Custom monitor High Alarm threshold MSB	Custom monitor signed or unsigned 16-bit value	0	00	0	00
169	A9	0	8	RO	Custom monitor High Alarm threshold LSB		0	00	0	00
170	AA	0	8	RO	Custom monitor low alarm threshold MSB		0	00	0	00
171	AB	0	8	RO	Custom monitor low alarm threshold LSB		0	00	0	00
172	AC	0	8	RO	Custom monitor high warning threshold MSB		0	00	0	00
173	AD	0	8	RO	Custom monitor high warning threshold LSB		0	00	0	00
174	AE	0	8	RO	Custom monitor low warning threshold MSB		0	00	0	00
175	AF	0	8	RO	Custom monitor low warning threshold LSB		0	00	0	00
176	B0	0	8	RO	Tx optical power high alarm threshold MSB	Threshold for Tx optical power unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 8.8.3, CMIS 4.0 for monitor details including accuracy	7.0000	C3	7.0000	C3
177	B1	0	8	RO	Tx optical power high alarm threshold LSB			C7		C7
178	B2	0	8	RO	Tx optical power low alarm threshold MSB		-6.8994	7	-6.8994	7
179	B3	0	8	RO	Tx optical power low alarm threshold LSB			FA		FA
180	B4	0	8	RO	Tx optical power high warning threshold MSB		4.0000	62	4.0000	62
181	B5	0	8	RO	Tx optical power high warning threshold LSB			1F		1F
182	B6	0	8	RO	Tx optical power low warning threshold MSB		-2.8997	14	-2.8997	14
183	B7	0	8	RO	Tx optical power low warning threshold LSB			09		09

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
184	B8	0	8	RO	Tx bias current high alarm threshold MSB	Threshold for Tx bias unsigned integer in 2 uA increments, times the multiplier from CMIS Table 8-33. CMIS section 8.8.3, for monitor details including accuracy	130.0	FD	130.0	FD
185	B9	0	8	RO	Tx bias current high alarm threshold LSB			E8		E8
186	BA	0	8	RO	Tx bias current low alarm threshold MSB		25.0	30	25.0	30
187	BB	0	8	RO	Tx bias current low alarm threshold LSB			D4		D4
188	BC	0	8	RO	Tx bias current high warning threshold MSB		120.0	EA	120.0	EA
189	BD	0	8	RO	Tx bias current high warning threshold LSB			60		60
190	BE	0	8	RO	Tx bias current low warning threshold MSB		40.0	4E	40.0	4E
191	BF	0	8	RO	Tx bias current low warning threshold LSB			20		20
192	C0	0	8	RO	Rx optical power high alarm threshold MSB	Threshold for Rx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 8.8.3, CMIS 4.0 for accuracy	7.0000	C3	7.0000	C3
193	C1	0	8	RO	Rx optical power high alarm threshold LSB			C7		C7
194	C2	0	8	RO	Rx optical power low alarm threshold MSB		-9.9012	3	-9.9012	3
195	C3	0	8	RO	Rx optical power low alarm threshold LSB			FF		FF
196	C4	0	8	RO	Rx optical power high warning threshold MSB		4.0000	62	4.0000	62
197	C5	0	8	RO	Rx optical power high warning threshold LSB			1F		1F
198	C6	0	8	RO	Rx optical power low warning threshold MSB		-5.9007	0A	-5.9007	0A
199	C7	0	8	RO	Rx optical power low warning threshold LSB			0A		0A
200-229	C8-E5	0	240	RO	Reserved	Reserved		00		00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
230-254	E6-FE	0	200	RO	Custom	Custom	000000000000 000000000000 000000000000 000000000000 00	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	000000000000 000000000000 000000000000 000000000000 00	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
255	FF	0	8	RO	Checksum	Checksum for byte 128 to 254	245	F5	245	F5

TABLE 5: UPPER PAGE 03H (USER NVRS)

Page 03h User EEPROM. The presence of Page 10h is advertised in bit 2 in Page 01h byte 142 (8Eh).

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	1024	RO	User EEPROM (NVRs)	User EEPROM (NVRs)	00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 00000000000000000000 0000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 000000000000000000 0000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

TABLE 6: UPPER PAGE 10H (LANE AND DATA PATH CONTROL)

The upper memory map page 10h is a banked page that contains lane dynamic control bytes. The presence of Page 10h is advertised in bit 7 in Page 00h byte 2. (CMIS-4.0 Table 8-44 to Table 8-55)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	8	RW	Host Lane Data path initialization control	Bit 7 to 0: Data path initialization control for host lane 8 to 1 respectively. 0b = Initialize 1b = De-initialize the data path associated with the host lane.	FALSE	00	FALSE	00
129	81	0	8	RW	Tx Polarity Flip	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=No polarity flip for associated lane 1b=Tx input polarity flip for associated lane	FALSE	00	FALSE	00
130	82	0	8	RW	TxDSBL Tx Disable	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=Tx output enabled for associated media lane 1b=Tx output disabled for associated media lane	FALSE	00	FALSE	00
131	83	0	8	RW	TxSquelchDSBL Tx Squelch Disable	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=Tx output squelch permitted and 1b=Tx output squelch not permitted for associated media lane when corresponding host input LOS is detected	FALSE	00	FALSE	00
132	84	0	8	RW	TxForceSquelch Tx force squelch	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=No impact on Tx behavior and 1b=Tx output squelched for associated media lane	FALSE	00	FALSE	00
133	85	0	8		Reserved	Reserved				
134	86	7	1	RW	TxInputEQFreeze Tx Input Eq Adaptation Freeze	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b= No impact on Tx input eq adaptation behavior and 1b=Tx input eq adaptation frozen at last value for associated lane	FALSE	00	FALSE	00
135	87	6	2	RW	TxInputEQAdaptStore Lane 4	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved CMIS 6.2.4.4	Reserved	00	Reserved	00
		4	2		TxInputEQAdaptStore Lane 3		Reserved		Reserved	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	2		TxInputEQAdaptStore Lane 2		Reserved		Reserved	
		0	2		TxInputEQAdaptStore Lane 1		Reserved		Reserved	
136	88	6	2	RW	TxInputEQAdaptStore Lane 8	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved CMIS 6.2.4.4	Reserved	00	Reserved	00
		4	2		TxInputEQAdaptStore Lane 7		Reserved		Reserved	
		2	2		TxInputEQAdaptStore Lane 6		Reserved		Reserved	
		0	2		TxInputEQAdaptStore Lane 5		Reserved		Reserved	
137	89	0	8	RW	RxPolarityFlip	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=No polarity flip for associated lane 1b=Rx output polarity flip for associated lane	FALSE	00	FALSE	00
138	8A	0	8	RW	RxDSBL Rx Output Disable	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=Rx output enabled for associated lane 1b=Rx output disabled for associated lane	FALSE	00	FALSE	00
139	8B	0	8	RW	RxSquelchDSBLRx Squelch Disable	Bit 7 to 0: Correspond to lane 8 to lane 1. 0b=Rx output squelch permitted and 1b=Rx output squelch not permitted for associated lane	FALSE	00	FALSE	00
140-142	8C-8E	0	24		Reserved	Reserved		00 00 00		00 00 00
143	8F	0	8	RW	Staged Set 0 lane 8 -1, Apply_DataPathInit	Bit 7 to 0: Correspond to lane 8 to lane 1. 1b=Apply Staged Control Set 0 lane 8-1 settings using DataPathInit	00	00	00	00
144	90	0	8	RW	Staged Set 0 lane 8-1 Apply_Immediate	Bit 7 to 0: Correspond to lane 8 to lane 1. 1b=Apply Staged Control Set 0 lane 8-1 settings with no Data Path State transitions	00	00	00	00
145	91	4	4	RW	Staged Set 0 Lane 1 ApSel code	ApSel Code, Lane 1 CMIS Table 8-13 or Table 8-39, lane 1	1	11	1	11
		1	3		Staged Set 0 Lane 1 Data Path ID	First lane of the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	1		Staged Set 0 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1	TRUE		TRUE	
146	92	4	4	RW	Staged Set 0 Lane 2 ApSel code	ApSel Code, Lane 2 CMIS Table 8-13 or Table 8-39, lane 2	1	11	1	11
		1	3		Staged Set 0 Lane 2 Data Path ID	First lane of the data path containing lane 2 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Staged Set 0 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2	TRUE		TRUE	
147	93	4	4	RW	Staged Set 0 Lane 3 ApSel code	ApSel Code, Lane 3 CMIS Table 8-13 or Table 8-39, lane 3	1	11	1	15
		1	3		Staged Set 0 Lane 3 Data Path ID	First lane of the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	0		2	
		0	1		Staged Set 0 Lane 3 Explicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 0 control values for lane 3	TRUE		TRUE	
148	94	4	4	RW	Staged Set 0 Lane 4 ApSel code	ApSel Code, Lane 4 CMIS Table 8-13 or Table 8-39, lane 4	1	11	1	15
		1	3		Staged Set 0 Lane 4 Data Path ID	First lane of the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	0		2	
		0	1		Staged Set 0 Lane 4 Explicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 0 control values for lane 4	TRUE		TRUE	
149	95	4	4	RW	Staged Set 0 Lane 5 ApSel code	ApSel Code, Lane 5 CMIS Table 8-13 or Table 8-39, lane 5	1	11	1	19
		1	3		Staged Set 0 Lane 5 Data Path ID	First lane of the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	0		4	
		0	1		Staged Set 0 Lane 5 Explicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 0 control values for lane 5	TRUE		TRUE	
150	96	4	4	RW	Staged Set 0 Lane 6 ApSel code	ApSel Code, Lane 6 CMIS Table 8-13 or Table 8-39, lane 6	1	11	1	19
		1	3		Staged Set 0 Lane 6 Data Path ID	First lane of the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	0		4	
		0	1		Staged Set 0 Lane 6 Explicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 0 control values for lane 6	TRUE		TRUE	
151	97	4	4	RW	Staged Set 0 Lane 7	ApSel Code, Lane 7	1	11	1	1D

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
					ApSel code	CMIS Table 8-13 or Table 8-39, lane 7				
		1	3		Staged Set 0 Lane 7 Data Path ID	First lane of the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	0		6	
		0	1		Staged Set 0 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7 1b=use Staged Set 0 control values for lane 7	TRUE		TRUE	
152	98	4	4	RW	Staged Set 0 Lane 8 ApSel code	ApSel code, Lane 8 CMIS Table 8-13 or Table 8-39, lane 8	1	11	1	1D
		1	3		Staged Set 0 Lane 8 Data Path ID	First lane of the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	0		6	
		0	1		Staged Set 0 Lane 8 Explicit Control	0b=Use Application-defined settings for lane 8 1b=use Staged Set 0 control values for lane 8	TRUE		TRUE	
153	99	0	8	RW	Tx Adapt. EQ ENBL Staged set 0, Tx controls: Adaptive input EQ Enable	Bit 7 to 0: corresponded to Tx 8 to Tx1 1b=Enable 0b=Disable (use manual fixed EQ)	TRUE	FF	TRUE	FF
154	9A	6	2	RW	Tx Adapt. EQ Recall, Lane 4	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved CMIS 6.2.4.4 for Store/Recall methodology	Do Not Recall	00	Do Not Recall	00
		4	2		Tx Adapt. EQ Recall, Lane 3		Do Not Recall		Do Not Recall	
		2	2		Tx Adapt. EQ Recall, Lane 2		Do Not Recall		Do Not Recall	
		0	2		Tx Adapt. EQ Recall, Lane 1		Do Not Recall		Do Not Recall	
155	9B	6	2	RW	Tx Adapt. EQ Recall, Lane 8	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved CMIS 6.2.4.4 for Store/Recall methodology	Do Not Recall	00	Do Not Recall	00
		4	2		Tx Adapt. EQ Recall, Lane 7		Do Not Recall		Do Not Recall	
		2	2		Tx Adapt. EQ Recall, Lane 6		Do Not Recall		Do Not Recall	
		0	2		Tx Adapt. EQ Recall, Lane 5		Do Not Recall		Do Not Recall	
156	9C	4	4	RW	Tx Fixed EQ Control (units of 1dB), Lane 2	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4)	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Tx Fixed EQ Control (units of 1dB), Lane 1		0		0	
157	9D	4	4		Tx Fixed EQ Control (units of 1dB), Lane 4		0	00	0	00
		0	4		Tx Fixed EQ Control (units of 1dB), Lane 3		0		0	
158	9E	4	4		Tx Fixed EQ Control (units of 1dB), Lane 6		0	00	0	00
		0	4		Tx Fixed EQ Control (units of 1dB), Lane 5		0		0	
159	9F	4	4		Tx Fixed EQ Control (units of 1dB), Lane 8		0	00	0	00
		0	4		Tx Fixed EQ Control (units of 1dB), Lane 7		0		0	
160	A0	0	8	RW	TxCDR ENBL Staged set 0, Tx CDR control	Bit 7 to 0: Corresponded to Tx 8 to Tx1 1b=CDR enabled, 0b=CDR bypassed	TRUE	FF	TRUE	FF
161	A1	8	1	RW	RxCDR ENBL Staged set 0, Rx CDR control	Bit 7 to 0: Corresponded to Rx 8 to Rx1 1b = CDR enabled 0b= CDR bypassed	TRUE	FF	TRUE	FF
162	A2	4	4	RW	Rx EQ Precursor Control (units of 0.5dB), Lane 2	Rx output equalization pre-cursor (See CMIS-4.0 Table 6-5)	2	22	2	22
		0	4		Rx EQ Precursor Control (units of 0.5dB), Lane 1		2		2	
163	A3	4	4		Rx EQ Precursor Control (units of 0.5dB), Lane 4		2	22	2	22
		0	4		Rx EQ Precursor Control (units of 0.5dB), Lane 3		2		2	
164	A4	4	4		Rx EQ Precursor Control (units of 0.5dB), Lane 6		2	22	2	22
		0	4		Rx EQ Precursor Control (units of 0.5dB), Lane 5		2		2	
165	A5	4	4		Rx EQ Precursor Control (units of 0.5dB), Lane 8		2	22	2	22

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Rx EQ Precursor Control (units of 0.5dB), Lane 7		2		2	
166	A6	4	4		Rx EQ Postcursor Control (units of 1dB), Lane 2	Rx output equalization pre-cursor (See CMIS-4.0 Table 6-5)	0	00	0	00
		0	4		Rx EQ Postcursor Control (units of 1dB), Lane 1		0		0	
167	A7	4	4		Rx EQ Postcursor Control (units of 1dB), Lane 4		0	00	0	00
		0	4		Rx EQ Postcursor Control (units of 1dB), Lane 3		0		0	
168	A8	4	4		Rx EQ Postcursor Control (units of 1dB), Lane 6		0	00	0	00
		0	4		Rx EQ Postcursor Control (units of 1dB), Lane 5		0		0	
169	A9	4	4		Rx EQ Postcursor Control (units of 1dB), Lane 8		0	00	0	00
		0	4		Rx EQ Postcursor Control (units of 1dB), Lane 7		0		0	
170	AA	4	4	RW	Rx Amp Control, Lane 2	Staged Set 0 Rx output amplitude (See CMIS-4.0 Table 6-6)	2	22	2	22
		0	4		Rx Amp Control, Lane 1		2		2	
171	AB	4	4		Rx Amp Control, Lane 4		2	22	2	22
		0	4		Rx Amp Control,		2		2	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
					Lane 3					
172	AC	4	4		Rx Amp Control, Lane 6		2	22	2	22
		0	4		Rx Amp Control, Lane 5		2		2	
173	AD	4	4		Rx Amp Control, Lane 8		2	22	2	22
		0	4		Rx Amp Control, Lane 7		2		2	
174-177	AE-B1	0	32	RO	Reserved	Reserved				
178	B2	0	8	RW	Stage Set 1, Apply controls: Apply_DataPathInit (8 Channels)	Bit 7 to 0: Correspond to lane 8 to lane 1. Apply Staged Control Set 1 setting using DataPathInit. 1b = Apply stage control set.	00	00	00	00
179	B3	0	8	RW	Stage Set 1, Apply controls: Apply_Immediate (8 Channels)	Bit 7 to 0: Correspond to lane 8 to lane 1. Apply Staged Control Set 1 setting with no data path state transitions. 1b = Apply stage control set.	00	00	00	00
180	B4	4	4	RW	Staged Set 1 Lane 1 ApSel code	ApSel Code, Lane 1 CMIS-4.0 Table 8-13 or Table 8-39	2	21	2	21
		1	3		Staged Set 1 Lane 1 Data Path ID	DataPath LaneStart (0b-111b), Lane 1 (CMIS-4.0 Table 8-52)	0		0	
		0	1		Staged Set 1 Lane 1 Explicit Control	Use Explicit Control, Lane 1 0b=Application-defined settings for lane 1 1b=Staged Set 1 control values for lane 1	TRUE		TRUE	
181	B5	4	4	RW	Staged Set 1 Lane 2 ApSel code	ApSel Code, Lane 2 CMIS-4.0 Table 8-13 or Table 8-39	2	21	2	21
		1	3		Staged Set 1 Lane 2 Data Path ID	DataPath LaneStart (0b-111b), Lane 2 (CMIS-4.0 Table 8-52)	0		0	
		0	1		Staged Set 1 Lane 2 Explicit Control	Use Explicit Control, Lane 2 0b=Application-defined settings for lane 2 1b=Staged Set 1 control values for lane 2	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
182	B6	4	4	RW	Staged Set 1 Lane 3 ApSel code	ApSel Code, Lane 3 CMIS-4.0 Table 8-13 or Table 8-39	2	25	2	21
		1	3		Staged Set 1 Lane 3 Data Path ID	DataPath LaneStart (0b-111b), Lane 3 (CMIS-4.0 Table 8-52)	2		0	
		0	1		Staged Set 1 Lane 3 Explicit Control	Use Explicit Control, Lane 3 0b=Application-defined settings for lane 3 1b=Staged Set 1 control values for lane 3	TRUE		TRUE	
183	B7	0	1	RW	Staged Set 1 Lane 4 ApSel code	ApSel Code, Lane 4 CMIS-4.0 Table 8-13 or Table 8-39	2	25	2	21
		1	3		Staged Set 1 Lane 4 Data Path ID	DataPath LaneStart (0b-111b), Lane 4 (CMIS-4.0 Table 8-52)	2		0	
		4	4		Staged Set 1 Lane 4 Explicit Control	Use Explicit Control, Lane 4 0b=Application-defined settings for lane 4 1b=Staged Set 1 control values for lane 4	TRUE		TRUE	
184	B8	4	4	RW	Staged Set 1 Lane 5 Explicit Control	ApSel Code, Lane 5 CMIS-4.0 Table 8-13 or Table 8-39	2	29	2	21
		1	3		Staged Set 1 Lane 5 Data Path ID	DataPath LaneStart (0b-111b), Lane 5 (CMIS-4.0 Table 8-52)	4		0	
		0	1		Staged Set 1 Lane 5 ApSel code	Use Explicit Control, Lane 5 0b=Application-defined settings for lane 5 1b=Staged Set 1 control values for lane 5	TRUE		TRUE	
185	B9	4	4	RW	Staged Set 1 Lane 6 ApSel code	ApSel Code, Lane 6 CMIS-4.0 Table 8-13 or Table 8-39	2	29	2	21
		1	3		Staged Set 1 Lane 6 Data Path ID	DataPath LaneStart (0b-111b), Lane 6 (CMIS-4.0 Table 8-52)	4		0	
		0	1		Staged Set 1 Lane 6 Explicit Control	Use Explicit Control, Lane 6 0b=Application-defined settings for lane 6 1b=Staged Set 1 control values for lane 6	TRUE		TRUE	
186	BA	4	4	RW	Staged Set 1 Lane 7 ApSel code	ApSel Code, Lane 7 CMIS-4.0 Table 8-13 or Table 8-39	2	2D	2	21
		1	3		Staged Set 1 Lane 7 Data Path ID	DataPath LaneStart (0b-111b), Lane 7 (CMIS-4.0 Table 8-52)	6		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	1		Staged Set 1 Lane 7 Explicit Control	Use Explicit Control, Lane 7 0b=Application-defined settings for lane 7 1b=Staged Set 1 control values for lane 7	TRUE		TRUE	
187	BB	4	4	RW	Staged Set 1 Lane 8 ApSel code	ApSel Code, Lane 8 CMIS-4.0 Table 8-13 or Table 8-39	2	2D	2	21
		1	3		Staged Set 1 Lane 8 Data Path ID	DataPath LaneStart (0b-111b), Lane 8 (CMIS-4.0 Table 8-52)	6		0	
		0	1		Staged Set 1 Lane 8 Explicit Control	Use Explicit Control, Lane 8 0b=Application-defined settings for lane 8 1b=Staged Set 1 control values for lane 8	TRUE		TRUE	
188	BC	0	8	RW	Tx Adapt. EQ ENBL Staged Set 1, Tx Adaptive input EQ Enable	7 to 0: corresponds to Tx 8 to Tx1 1b=Enable 0b=Disable (use manual fixed EQ)	TRUE	FF	TRUE	FF
189	BD	6	2	RW	Staged Set 1 Tx4 Tx Adapt. EQ Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved CMIS-4 6.2.4.4 for Store/Recall methodology	Do Not Recall	00	Do Not Recall	00
		4	2		Staged Set 1 Tx3 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
		2	2		Staged Set 1 Tx2 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
		0	2		Staged Set 1 Tx1 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
190	BE	6	2		Staged Set 1 Tx8 Tx Adapt. EQ Recall		Do Not Recall	00	Do Not Recall	00
		4	2		Staged Set 1 Tx7 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
		2	2		Staged Set 1 Tx6 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
		0	2		Staged Set 1 Tx5 Tx Adapt. EQ Recall		Do Not Recall		Do Not Recall	
191	BF	4	4	RW	Staged Set 1 Tx2 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 2	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Staged Set 1 Tx1 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 1	0		0	
192	C0	4	4		Staged Set 1 Tx4 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 4	0	00	0	00
		0	4		Staged Set 1 Tx3 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 3	0		0	
193	C1	4	4		Staged Set 1 Tx6 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 6	0	00	0	00
		0	4		Staged Set 1 Tx5 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 5	0		0	
194	C2	4	4		Staged Set 1 Tx8 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 8	0	00	0	00
		0	4		Staged Set 1 Tx7 Input Eq control	Manual fixed Tx input eq control (CMIS-4.0 Table 6-4) Tx Fixed EQ Control (units of 1dB), Lane 7	0		0	
195	C3	0	8	RW	TxCDR ENBL Staged Set 1 Tx CDR control	Bit 7 to 0: Correspond to Tx 8 to Tx1 1b = CDR enabled 0b= CDR bypassed	TRUE	FF	TRUE	FF
196	C4	0	8	RW	RxCDR ENBL Staged Set 1 Rx CDR Control	Bit 7 to 0: Correspond to Rx 8 to Rx1 1b = CDR enabled 0b= CDR bypassed	TRUE	FF	TRUE	FF
197	C5	4	4	RW	Staged Set 1 Rx2 Output Eq control RX2	Rx EQ Precursor Control (units of 0.5dB) Lane 2	2	22	2	22
		0	4		Staged Set 1 Rx1 Output Eq control RX1	Rx EQ Precursor Control (units of 0.5dB) Lane 1	2		2	
198	C6	4	4		Staged Set 1 Rx4 Output Eq control RX4	Rx EQ Precursor Control (units of 0.5dB) Lane 4	2	22	2	22

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Staged Set 1 Rx3 Output Eq control RX3	Rx EQ Precursor Control (units of 0.5dB) Lane 3	2		2	
199	C7	4	4		Staged Set 1 Rx6 Output Eq control RX6	Rx EQ Precursor Control (units of 0.5dB) Lane 6	2	22	2	22
		0	4		Staged Set 1 Rx5 Output Eq control RX5	Rx EQ Precursor Control (units of 0.5dB) Lane 5	2		2	
200	C8	4	4		Staged Set Rx8 Output Eq control RX8	Rx EQ Precursor Control (units of 0.5dB) Lane 8	2	22	2	22
		0	4		Staged Set 1 Rx7 Output Eq control RX7	Rx EQ Precursor Control (units of 0.5dB) Lane 7	2		2	
201	C9	4	4	WR	Staged Set 1 Rx2 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 2	0	00	0	00
		0	4		Staged Set 1 Rx1 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 1	0		0	
202	CA	4	4		Staged Set 1 Rx4 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 4	0	00	0	00
		0	4		Staged Set 1 Rx3 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 3	0		0	
203	CB	4	4		Staged Set 1 Rx6 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 6	0	00	0	00
		0	4		Staged Set 1 Rx5 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 5	0		0	
204	CC	4	4		Staged Set 1 Rx8 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 8	0	00	0	00
		0	4		Staged Set 1 Rx7 Output Eq control	Rx EQ Postcursor Control (units of 1dB) Lane 7	0		0	
205	CD	4	4	RW	Staged Set 1 Rx2 Output Amplitude	Rx Amp Control, Lane 2	2	22	2	22
		0	4		Staged Set 1 Rx1 Output Amplitude	Rx Amp Control, Lane 1	2		2	
206	CE	4	4		Staged Set 1 Rx4 Output Amplitude	Rx Amp Control, Lane 4	2	22	2	22

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Staged Set 1 Rx3 Output Amplitude	Rx Amp Control, Lane 3	2		2	
207	CF	4	4		Staged Set 1 Rx6 Output Amplitude	Rx Amp Control, Lane 6	2	22	2	22
		0	4		Staged Set 1 Rx5 Output Amplitude	Rx Amp Control, Lane 5	2		2	
208	D0	4	4		Staged Set 1 Rx8 Output Amplitude	Rx Amp Control, Lane 8	2	22	2	22
		0	4		Staged Set 1 Rx7 Output Amplitude	Rx Amp Control, Lane 7	2		2	
209-212	D1-D4	0	32	RO	Reserved	Reserved		00 00 00 00		00 00 00 00
213	D5	0	8	RW	Host Lane M- Data Path State Changed flag mask	Bits 7 to 0: Correspond to Host lane 8 to lane 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
214	D6	0	8	RW	Media Lane M-TX Fault flag mask	Masking bit for Tx Fault flag, media lane Bits 7 to 0: Correspond to Media lane 8 to lane 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
215	D7	0	8	RW	LOS flag mask M-Tx	Masking bit for Tx LOS flag Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
216	D8	0	8	RW	TX CDR LOL flag mask M-Tx	Masking bit for Tx CDR LOL flag Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
217	D9	0	8	RW	TX Adaptive Eq Fault flag mask M-Tx	Masking bit for Tx Adaptive Input Eq Fail Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
218	DA	0	8	RW	Media Lane Power High Alarm flag mask M-Tx	Masking bit for Tx output power High Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
219	DB	0	8	RW	Media Lane Power Low Alarm flag mask M-Tx	Masking bit for Tx output	FALSE	00	FALSE	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
						power Low Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked				
220	DC	0	8	RW	Media Lane Power High Warning flag mask M-Tx	Masking bit for Tx output power High Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
221	DD	0	8	RW	Media Lane Power Low Warning flag mask M-Tx	Masking bit for Tx output power Low Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
222	DE	0	8	RW	Media Lane M-LDI Bias High Alarm flag mask M-TX	Masking bit for Tx bias High Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
223	DF	0	8	RW	Media Lane M-LDI Bias Low Alarm flag mask M-Tx	Media Lane Bias Low Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
224	E0	0	8	RW	Media Lane M-LDI Bias High Warning flag mask M-Tx	Media Lane Bias High Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
225	E1	0	8	RW	Media Lane M-LDI Bias Low Warning flag mask M-Tx	Media Lane Bias Low Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
226	E2	0	8	RW	Media Lane LOS flag mask M-Rx	Media Lane RX LOS Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
227	E3	0	8	RW	Media Lane CDR LOL flag mask M-Rx	Media Lane RX CDR LOL Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
228	E4	0	8	RW	Media Lane Power High Alarm flag mask M-Rx	Media Lane RX Power High Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
229	E5	0	8	RW	Media Lane RX Power Low Alarm flag mask M-Rx	Media Lane RX Power Low Alarm Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
230	E6	0	8	RW	Media Lane RX Power High Warning flag mask M-Rx	Media Lane RX Power High Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
231	E7	0	8	RW	Media Lane RX Power Low Warning flag mask M-Rx	Media Lane RX Power Low Warning Bits 7 to 0: Correspond to lane 8 to 1. 0b = not masked; 1b = masked	FALSE	00	FALSE	00
232-239	E8-EF	0	64	RO	Reserved	Reserved	0000000000000000	00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00
240-255	F0-FF	0	128	RW	Custom	Custom	00000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

TABLE 7: UPPER PAGE 11H (LANE STATUS)

The upper memory map page 11h is a banked page that contains lane dynamic status bytes. The presence of Page 11h is conditional on the state of bit 7 in Page 00h byte 2. All fields on Page 11h are read-only.

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	4	4	RO	Data Path State host lane 2	Data path state encoding, as observed Host Lane See Table 8-58, CMIS4.0 for Data Path State Indicator Encodings	0	00	0	00
		0	4		Data Path State host lane 1		0		0	
129	81	4	4	RO	Data Path State host lane 4		0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Data Path State host lane 3		0		0	
130	82	4	4	RO	Data Path State host lane 6		0	00	0	00
		0	4		Data Path State host lane 5		0		0	
131	83	4	4	RO	Data Path State host lane 8		0	00	0	00
		0	4		Data Path State host lane 7		0		0	
132-133	84-85	0	16	RO	Reserved					
134	86	0	8	RO	Host Lane L-Lane Data Path State Changed Flag	Latched Data path state changed flag for host lane Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
135	87	0	8	RO	Media Lane L-Tx Fault Flag	Media Lane latched TX fault Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
136	88	0	8	RO	L-TX LOS Flag	Latched TX LOS flag Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
137	89	0	8	RO	L-TX CDR LOL Flag	Latch TX CDR LOL flag Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
138	8A	0	8	RO	Media Lane L-TX Adaptive input EQ fault Flag	Latched TX Adaptive input EQ fault Flag Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
139	8B	0	8	RO	Media Lane L-TX Power High Alarm Flag	Media Lane Latched TX Power High Alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
140	8C	0	8	RO	Media Lane L-TX Power Low Alarm Flag	Media Lane Latched power low alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
141	8D	0	8	RO	Media Lane L-TX Power High Warning Flag	Media Lane Latched TX Power High Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
142	8E	0	8	RO	Media Lane L-TX Power Low Warning Flag	Media Lane Latched TX Power Low Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
143	8F	0	8	RO	Media Lane L-TX Power High Alarm Flag	Media Lane Latched TX Power High Alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
144	90	0	8	RO	Media Lane L-TX Power Low Alarm Flag	Media Lane Latched TX Power Low Alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
145	91	0	8	RO	Media Lane L-TX Bias High Warning Flag	Media Lane Latched TX Bias High Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
146	92	0	8	RO	Media Lane L-TX Bias Low Warning Flag	Media Lane Latched TX Bias Low Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
147	93	0	8	RO	Media Lane L-RX LOS Flag	Media Lane Latched RX LOS Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
148	94	0	8	RO	Media Lane L-RX CDR LOL Flag	Media Lane Latched RX CDR LOL Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
149	95	0	8	RO	Media Lane L-RX Power High Alarm Flag	Media Lane Latched RX Power High Alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
150	96	0	8	RO	Media Lane L-RX Power Low Alarm Flag	Media Lane Latched RX Power Low Alarm Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
151	97	0	8	RO	Media Lane L-RX Power High Warning Flag	Media Lane Latched RX Power High Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
152	98	0	8	RO	Media Lane L-RX Power Low Warning Flag	Media Lane Latched RX Power Low Warning Bits 7 to 0: correspond to Lane 8 to Lane 1 1b = Flag latched; 0b= No flag	0	00	0	00
153	99	0	8	RO	Reserved			0		0
154	9A	0	8	RO	Tx 1 Power MSB	Internally measured Tx output Optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	0.0000	00 00	0.0000	00 00
155	9B	0	8	RO	Tx 1 Power LSB					
156	9C	0	8	RO	Tx 2 Power MSB		0.0000	00 00	0.0000	00 00
157	9D	0	8	RO	Tx 2 Power LSB					
158	9E	0	8	RO	Tx 3 Power MSB		0.0000	00 00	0.0000	00 00
159	9F	0	8	RO	Tx 3 Power LSB					
160	A0	0	8	RO	Tx 4 Power MSB		0.0000	00 00	0.0000	00 00
161	A1	0	8	RO	Tx 4 Power LSB					
162	A2	0	8	RO	Tx 5 Power MSB		0.0000	00 00	0.0000	00 00
163	A3	0	8	RO	Tx 5 Power LSB					
164	A4	0	8	RO	Tx 6 Power MSB		0.0000	00 00	0.0000	00 00
165	A5	0	8	RO	Tx 6 Power LSB					
166	A6	0	8	RO	Tx 7 Power MSB		0.0000	00 00	0.0000	00 00
167	A7	0	8	RO	Tx 7 Power LSB					
168	A8	0	8	RO	Tx 8 Power MSB		0.0000	00 00	0.0000	00 00
169	A9	0	8	RO	Tx 8 Power LSB					
170	AA	0	8	RO	Tx 1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA increments. CMIS Table 8-33	0.0	00 00	0.0	00 00
171	AB	0	8	RO	Tx 1 Bias LSB					
172	AC	0	8	RO	Tx 2 Bias MSB		0.0	00 00	0.0	00 00
173	AD	0	8	RO	Tx 2 Bias LSB					
174	AE	0	8	RO	Tx 3 Bias MSB		0.0	00 00	0.0	00 00
175	AF	0	8	RO	Tx 3 Bias LSB					
176	B0	0	8	RO	Tx 4 Bias MSB		0.0	00 00	0.0	00 00
177	B1	0	8	RO	Tx 4 Bias LSB					
178	B2	0	8	RO	Tx 5 Bias MSB		0.0	00 00	0.0	00 00
179	B3	0	8	RO	Tx 5 Bias LSB					
180	B4	0	8	RO	Tx 6 Bias MSB		0.0	00 00	0.0	00 00
181	B5	0	8	RO	Tx 6 Bias LSB					
182	B6	0	8	RO	Tx 7 Bias MSB		0.0	00 00	0.0	00 00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
183	B7	0	8	RO	Tx 7 Bias LSB					
184	B8	0	8	RO	Tx 8 Bias MSB		0.0	00 00	0.0	00 00
185	B9	0	8	RO	Tx 8 Bias LSB					
186	BA	0	8	RO	Rx 1 Power MSB	Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	0.0000	00 00	0.0000	00 00
187	BB	0	8	RO	Rx 1 Power LSB					
188	BC	0	8	RO	Rx 2 Power MSB		0.0000	00 00	0.0000	00 00
189	BD	0	8	RO	Rx 2 Power LSB					
190	BE	0	8	RO	Rx 3 Power MSB		0.0000	00 00	0.0000	00 00
191	BF	0	8	RO	Rx 3 Power LSB					
192	C0	0	8	RO	Rx 4 Power MSB		0.0000	00 00	0.0000	00 00
193	C1	0	8	RO	Rx 4 Power LSB					
194	C2	0	8	RO	Rx 5 Power MSB		0.0000	00 00	0.0000	00 00
195	C3	0	8	RO	Rx 5 Power LSB					
196	C4	0	8	RO	Rx 6 Power MSB		0.0000	00 00	0.0000	00 00
197	C5	0	8	RO	Rx 6 Power LSB					
198	C6	0	8	RO	Rx 7 Power MSB		0.0000	00 00	0.0000	00 00
199	C7	0	8	RO	Rx 7 Power LSB					
200	C8	0	8	RO	Rx 8 Power MSB		0.0000	00 00	0.0000	00 00
201	C9	0	8	RO	Rx 8 Power LSB					
202	CA	4	4	RO	Lane 2 Config Error Code	0h = No status 1h = Config accepted 2h = Config rejected due to unknown. 3h = Config rejected due to invalid Code. 4h = Config rejected due to invalid lane comb. 5h = Config rejected due to Invalid SI 6h = Config rejected due to currently in use. 7h =Config rejected due to incomplete lane info. 8h to Ch = Reserved. Dh to Fh = Config rejected for custom reason	0	00 00 00 00	0	00 00 00 00
		0	4		Lane 1 Config Error Code		0		0	
203	CB	4	4	RO	Lane 4 Config Error Code		0		0	
		0	4		Lane 3 Config Error Code		0		0	
204	CC	4	4	RO	Lane 6 Config Error Code		0		0	
		0	4		Lane 5 Config Error Code		0		0	
205	CD	4	4	RO	Lane 8 Config Error Code		0		0	
		0	4		Lane 7 Config Error Code		0		0	
206	CE	4	4	RO	Active Set Lane 1 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 1	0	00	0	00
		1	3		Active Set Lane 1 Data Path ID	First lane in the data path containing lane 1 000b=Lane 1	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	1		Active Set Lane 1 Explicit Control	0b=Lane 1 settings are Application-defined 1b=Lane 1 settings are host-specified	0		0	
207	CF	4	4	RO	Active Set Lane 2 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 2	0	00	0	00
		1	3		Active Set Lane 2 Data Path ID	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	0		0	
		0	1		Active Set Lane 2 Explicit Control	0b=Lane 2 settings are Application-defined 1b=Lane 2 settings are host-specified	0		0	
208	D0	4	4	RO	Active Set Lane 3 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 3	0	00	0	00
		1	3		Active Set Lane 3 Data Path ID	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Active Set Lane 3 Explicit Control	0b=Lane 3 settings are Application-defined 1b=Lane 3 settings are host-specified	0		0	
209	D1	4	4	RO	Active Set Lane 4 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 4	0	00	0	00
		1	3		Active Set Lane 4 Data Path ID	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Active Set Lane 4 Explicit Control	0b=Lane 4 settings are Application-defined 1b=Lane 4 settings are host-specified	0		0	
210	D2	4	4	RO	Active Set Lane 5 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 5	0	00	0	00
		1	3		Active Set Lane 5 Data Path ID	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Active Set Lane 5 Explicit Control	0b=Lane 5 settings are Application-defined 1b=Lane 5 settings are host-specified	0		0	
211	D3	4	4	RO	Active Set Lane 6 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 6	0	00	0	00
		1	3		Active Set Lane 6 Data Path ID	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Active Set Lane 6 Explicit Control	0b=Lane 6 settings are Application-defined 1b=Lane 6 settings are host-specified	0		0	
212	D4	4	4	RO	Active Set Lane 7 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 7	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		1	3		Active Set Lane 7 Data Path ID	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	0		0	
		0	1		Active Set Lane 7 Explicit Control	0b=Lane 7 settings are Application-defined 1b=Lane 7 settings are host-specified	0		0	
213	D5	4	4	RO	Active Set Lane 8 ApSel code	ApSel Code from CMIS Table 8-13 or Table 8-39, lane 8	0		0	
		1	3		Active Set Lane 8 Data Path ID	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	0	00	0	00
		0	1		Active Set Lane 8 Explicit Control	0b=Lane 8 settings are Application-defined 1b=Lane 8 settings are host-specified	0		0	
214	D6	0	8	RO	Active Application Control Set: Tx Adaptive Input EQ enable	Adaptive Input EQ EN (Channel 1-8) Bit 7 to 0: correspond to Tx 8 to Tx 1 1b = Enable 0b = Disable (use manual fixed EQ)	0	00	0	00
215	D7	6	2	RO	Active Set Tx4 Adaptive Input Eq Recall	Adaptive Input EQ Recall (Channel 1-8) Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See CMIS Table 8-49 and Table 8-53	0000	00 00	0000	00 00
		4	3		Active Set Tx3 Adaptive Input Eq Recall					
		2	2		Active Set Tx2 Adaptive Input Eq Recall					
		0	2		Active Set Tx1 Adaptive Input Eq Recall					
216	D8	6	2	RO	Active Set Tx8 Adaptive Input Eq Recall		0000	00 00	0000	00 00
		4	3		Active Set Tx7 Adaptive Input Eq Recall					
		2	2		Active Set Tx6 Adaptive Input Eq Recall					
		0	2		Active Set Tx5 Adaptive Input Eq Recall					
217	D9	4	4	RO	Active Set Tx2 Input Eq control	Manual fixed Tx input eq control. Refer to Table 6-4. CMIS 4.0	00000000	00 00 00 00	00000000	00 00 00 00
		0	4		Active Set Tx1 Input Eq control					
218	DA	4	4	RO	Active Set Tx4 Input					

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
					Eq control					
		0	4		Active Set Tx3 Input Eq control					
219	DB	4	4	RO	Active Set Tx6 Input Eq control					
		0	4		Active Set Tx5 Input Eq control					
220	DC	4	4	RO	Active Set Tx8 Input Eq control					
		0	4		Active Set Tx7 Input Eq control					
221	DD	0	8	RO	Application Control Set Indicator: Tx CDR Controls	Bits 7 to 0: correspond to Tx 8 to Tx 1 1b = CDR enabled, 0b = CDR bypassed	00	00	00	00
222	DE	0	8	RO	Application Control Set Indicator: Rx CDR Controls	Bits 7 to 0: correspond to Rx 8 to Rx 1 1b = CDR enabled, 0b = CDR bypassed	00	00	00	00
223	DF	4	4	RO	Active Set Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor Refer to Table 6-5, CMIS 4.0	00000000	00 00 00 00	00000000	00 00 00 00
		0	4		Active Set Rx1 Output Eq control, pre-cursor					
224	E0	4	4	RO	Active Set Rx4 Output Eq control, pre-cursor					
		0	4		Active Set Rx3 Output Eq control, pre-cursor					
225	E1	4	4	RO	Active Set Rx6 Output Eq control, pre-cursor					
		0	4		Active Set Rx5 Output Eq control, pre-cursor					
226	E2	4	4	RO	Active Set Rx8 Output Eq control, pre-cursor					
		0	4		Active Set Rx7 Output Eq control, pre-cursor					
227	E3	4	4	RO	Active Set Rx2 Output		00000000	00 00 00 00	00000000	00 00 00 00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
					Eq control, post-cursor	Rx output equalization post-cursor Refer to Table 6-5, CMIS 4.0				
		0	4		Active Set Rx1 Output Eq control, post-cursor					
228	E4	4	4	RO	Active Set Rx4 Output Eq control, post-cursor					
		0	4		Active Set Rx3 Output Eq control, post-cursor					
229	E5	4	4	RO	Active Set Rx6 Output Eq control, post-cursor					
		0	4		Active Set Rx5 Output Eq control, post-cursor					
230	E6	4	4	RO	Active Set Rx8 Output Eq control, post-cursor					
		0	4		Active Set Rx7 Output Eq control, post-cursor					
231	E7	4	4	RO	Active Set Rx2 Output Amplitude control	Rx output amplitude encoding Refer to Table 6-6, CMIS 4.0	00000000	00 00 00 00	00000000	00 00 00 00
		0	4		Active Set Rx1 Output Amplitude control					
232	E8	4	4	RO	Active Set Rx4 Output Amplitude control					
		0	4		Active Set Rx3 Output Amplitude control					
233	E9	4	4	RO	Active Set Rx6 Output Amplitude control					
		0	4		Active Set Rx5 Output Amplitude control					
234	EA	4	4	RO	Active Set Rx8 Output Amplitude control					
		0	4		Active Set Rx7 Output Amplitude control					
235-239	EB-EF	0	40	RO	Reserved			0		0
240	F0	4	4	RO	Module Tx media lane 1 wavelength mapping	TX Media Wavelength Mapping 0000 = Mapping unknown or undefined	1	11	1	11

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	4		Module Tx media lane 1 fiber mapping	0001= media wavelength 1 0010= media wavelength 2 0011= media wavelength 3 0100= media wavelength 4 0101= media wavelength 5 0110= media wavelength 6 0111= media wavelength 7 1000= media wavelength 8 1001-1111= Reserved 3 to 0: TX media fiber mapping 0000 = Mapping unknown or undefined 0001= media fiber 1 or TR1 0010= media fiber 2 or RT1 0011= media fiber 3 or TR2 0100= media fiber 4 or RT2 0101= media fiber 5 or TR3 0110= media fiber 6 or RT3 0111= media fiber 7 or TR4 1000= media fiber 8 or RT4 1001-1111= Reserved	1		1	
241	F1	4	4	RO	Module Tx media lane 2 wavelength mapping		1	12	1	12
		0	4		Module Tx media lane 2 fiber mapping		2		2	
242	F2	4	4	RO	Module Tx media lane 3 wavelength mapping		1	13	1	13
		0	4		Module Tx media lane 3 fiber mapping		3		3	
243	F3	4	4	RO	Module Tx media lane 4 wavelength mapping		1	14	1	14
		0	4		Module Tx media lane 4 fiber mapping		4		4	
244	F4	4	4	RO	Module Tx media lane 5 wavelength mapping		0	00	0	00
		0	4		Module Tx media lane 5 fiber mapping		0		0	
245	F5	4	4	RO	Module Tx media lane 6 wavelength mapping		0	00	0	00
		0	4		Module Tx media lane 6 fiber mapping		0		0	
246	F6	4	4	RO	Module Tx media lane 7 wavelength		0	00	0	00
		0	4		Module Tx media lane 7 fiber mapping		0		0	
247	F7	4	4	RO	Module Tx media lane 8 wavelength mapping		0	00	0	00
		0	4		Module Tx media lane 8 fiber mapping		0		0	
248	F8	4	4	RO	Module Rx media lane 1 wavelength mapping	RX Media Wavelength Mapping 0000 = Mapping unknown or undefined 0001= media wavelength 1 0010= media wavelength 2	1	11	1	11
		0	4		Module Rx media lane 1 fiber mapping		1		1	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
249	F9	4	4	RO	Module Rx media lane 2 wavelength mapping	0011= media wavelength 3 0100= media wavelength 4 0101= media wavelength 5 0110= media wavelength 6 0111= media wavelength 7 1000= media wavelength 8 1001-1111= Reserved 3 to 0: RX media fiber mapping 0000 = Mapping unknown or undefined 0001= media fiber 1 or RT1 0010= media fiber 2 or TR1 0011= media fiber 3 or RT2 0100= media fiber 4 or TR2 0101= media fiber 5 or RT3 0110= media fiber 6 or TR3 0111= media fiber 7 or RT4 1000= media fiber 8 or TR4 1001-1111= Reserved	1	12	2	12
		0	4		Module Rx media lane 2 fiber mapping		2		1	
250	FA	4	4	RO	Module Rx media lane 3 wavelength mapping		1	13	3	13
		0	4		Module Rx media lane 3 fiber mapping		3		1	
251	FB	4	4	RO	Module Rx media lane 4 wavelength mapping		1	14	4	14
		0	4		Module Rx media lane 4 fiber mapping		4		1	
252	FC	4	4	RO	Module Rx media lane 5 wavelength mapping		0	00	0	00
		0	4		Module Rx media lane 5 fiber mapping		0		0	
253	FD	4	4	RO	Module Rx media lane 6 wavelength mapping		0	00	0	00
		0	4		Module Rx media lane 6 fiber mapping		0		0	
254	FE	4	4	RO	Module Rx media lane 7 wavelength mapping		0	00	0	00
		0	4		Module Rx media lane 7 fiber mapping		0		0	
255	FF	4	4	RO	Module Rx media lane 8 wavelength mapping		0	00	0	00
		0	4		Module Rx media lane 8 fiber mapping		0		0	

TABLE 8: UPPER PAGE 13H (MODULE DIAGNOSTICS 1)

Upper memory map pages 13h and 14h are banked pages that contain module diagnostic control and status fields. The presence of Page 13h is conditional on the state of bit 5 in Page 01h byte 142 (Refer to Table 8-28, CMIS 4.0). Host and Media side Generator Patterns are coded per Table 8-72, CMIS 4.0. (CMIS-4.0 Table 8-66 to Table 8-90)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	7	1	RO	Loopback Capabilities	Reserved		0A		0A
		6	1		Simultaneous Host and Media Loopback Supported	0b=loopback Not supported 1b=loopback supported	FALSE		FALSE	
		5	1		Per-lane Media Side Loopback Supported		FALSE		FALSE	
		4	1		Per-lane Host Side Loopback Supported		FALSE		FALSE	
		3	1		Host Side Input Loopback Supported		TRUE		TRUE	
		2	1		Host Side Output Loopback Supported		FALSE		FALSE	
		1	1		Media Side Input Loopback Supported		TRUE		TRUE	
		0	1		Media Side Output Loopback Supported		FALSE		FALSE	
129	81	6	2	RO	Gating Supported	00b=Not Supported 01b=Supported with time accuracy <= 2 ms 10b=Supported with time accuracy <= 20 ms 11b=Supported with time accuracy > 20 ms	Supported with time accuracy >2ms	FC	Supported with time accuracy >2ms	FC
		5	1		Latched Error Info Supported	0b=Not Supported 1b=Supported.	TRUE		TRUE	
		4	1		Real-Time BER Error Count Polling by Module	This flag controls if the module polls and updates the error information BER or Total Error Counters. (CMIS Table 8-70)	Poll Error Info		Poll Error Info	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		3	1		Per Lane Gating Timer	1b=Per lane gating timer supported.	Per-Lane Gating Time Supported		Per-Lane Gating Time Supported	
		2	1		Auto Restart Implemented	0b=Auto Restart not implemented 1b=Auto Restart implemented.	TRUE		TRUE	
		0	2		Reserved	Reserved				
130	82	7	1	RO	Media Side FEC Supported	1b=Supported 0b=Not supported	FALSE	2B	FALSE	2B
		6	1		Host Side FEC Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
		5	1		Media Side Input SNR Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		4	1		Host Side Input SNR Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
		3	1		Media Side Input Peak Detector Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		2	1		Host Side Input Peak Detector Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
		1	1		BER Error Count/Total Bits Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		0	1		BER Register Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
131	83	7	1	RO	Media Side Pre-FEC PRBS Generator Supported	1b=Supported 0b=Not supported	FALSE	66	FALSE	66
		6	1		Media Side Post-FEC PRBS Generator Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		5	1		Media Side Pre-FEC PRBS Checker Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		4	1		Media Side Post-FEC PRBS Checker Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
		3	1		Host Side Pre-FEC PRBS Generator Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
		2	1		Host Side Post-FEC PRBS Generator Supported	1b=Supported 0b=Not supported	TRUE		TRUE	
		1	1		Host Side Pre-FEC PRBS Checker Supported	1b=Supported 0b=Not supported	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		0	1		Host Side Post-FEC PRBS Checker Supported	1b=Supported 0b=Not supported	FALSE		FALSE	
132	84	7	1	RO	Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-13 Supported	TRUE	FF	TRUE	FF
		6	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-13Q Supported	TRUE		TRUE	
		5	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-15 Supported	TRUE		TRUE	
		4	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-15Q Supported	TRUE		TRUE	
		3	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-23 Supported	TRUE		TRUE	
		2	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-23Q Supported	TRUE		TRUE	
		1	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-31 Supported	TRUE		TRUE	
		0	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-31Q Supported	TRUE		TRUE	
133	85	7	1	RO	Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side User Pattern Supported	FALSE	5F	FALSE	5F
		6	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side Vendor Pattern Supported	TRUE		TRUE	
		5	1		Host PRBS Pattern Generation Capabilities	Reserved				
		4	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side SSPRQ Supported	TRUE		TRUE	
		3	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-7 Supported	TRUE		TRUE	
		2	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-7Q Supported	TRUE		TRUE	
		1	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-9 Supported	TRUE		TRUE	
		0	1		Host PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Host Side PRBS-9Q Supported	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
134	86	7	1	RO	Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-13 Supported	TRUE	FF	TRUE	FF
		6	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-13Q Supported	TRUE		TRUE	
		5	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-15 Supported	TRUE		TRUE	
		4	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-15Q Supported	TRUE		TRUE	
		3	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-23 Supported	TRUE		TRUE	
		2	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-23Q Supported	TRUE		TRUE	
		1	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-31 Supported	TRUE		TRUE	
		0	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-31Q Supported	TRUE		TRUE	
135	87	7	1	RO	Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side User Pattern Supported	FALSE	5F	FALSE	5F
		6	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side Custom (Vendor Pattern) Supported	TRUE		TRUE	
		5	1		Media PRBS Pattern Generation Capabilities	Reserved				
		4	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side SSPRQ Supported	TRUE		TRUE	
		3	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-7 Supported	TRUE		TRUE	
		2	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-7Q Supported	TRUE		TRUE	
		1	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-9 Supported	TRUE		TRUE	
		0	1		Media PRBS Pattern Generation Capabilities	1b=Supported 0b=Not supported Media Side PRBS-9Q Supported	TRUE		TRUE	
136	88	7	1	RO	Host PRBS Pattern Checker Capabilities	Host Side PRBS-13 Supported	TRUE	FF	TRUE	FF

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		6	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-13Q Supported	TRUE		TRUE	
		5	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-15 Supported	TRUE		TRUE	
		4	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-15Q Supported	TRUE		TRUE	
		3	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-23 Supported	TRUE		TRUE	
		2	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-23Q Supported	TRUE		TRUE	
		1	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-31 Supported	TRUE		TRUE	
		0	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-31Q Supported	TRUE		TRUE	
137	89	7	1	RO	Host PRBS Pattern Checker Capabilities	Host Side User Pattern Supported	FALSE	0F	FALSE	0F
		6	1		Host PRBS Pattern Checker Capabilities	Host Side Custom (Vendor Pattern) Supported	FALSE		FALSE	
		5	1		Host PRBS Pattern Checker Capabilities	Reserved				
		4	1		Host PRBS Pattern Checker Capabilities	Host Side SSPRQ Supported	FALSE		FALSE	
		3	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-7 Supported	TRUE		TRUE	
		2	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-7Q Supported	TRUE		TRUE	
		1	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-9 Supported	TRUE		TRUE	
		0	1		Host PRBS Pattern Checker Capabilities	Host Side PRBS-9Q Supported	TRUE		TRUE	
138	8A	7	1	RO	Media PRBS Pattern Checker Capabilities	Media Side PRBS-13 Supported	TRUE	FF	TRUE	FF
		6	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-13Q Supported	TRUE		TRUE	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		5	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-15 Supported	TRUE		TRUE	
		4	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-15Q Supported	TRUE		TRUE	
		3	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-23 Supported	TRUE		TRUE	
		2	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-23Q Supported	TRUE		TRUE	
		1	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-31 Supported	TRUE		TRUE	
		0	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-31Q Supported	TRUE		TRUE	
139	8B	7	1	RO	Media PRBS Pattern Checker Capabilities	Media Side User Pattern Supported	FALSE	0F	FALSE	0F
		6	1		Media PRBS Pattern Checker Capabilities	Media Side Custom (Vendor Pattern) Supported	FALSE		FALSE	
		5	1		Media PRBS Pattern Checker Capabilities	Reserved				
		4	1		Media PRBS Pattern Checker Capabilities	Media Side SSPRQ Supported	FALSE		FALSE	
		3	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-7 Supported	TRUE		TRUE	
		2	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-7Q Supported	TRUE		TRUE	
		1	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-9 Supported	TRUE		TRUE	
		0	1		Media PRBS Pattern Checker Capabilities	Media Side PRBS-9Q Supported	TRUE		TRUE	
140	8C	6	2	RO	PG and Checker Swap/Invert Capabilities	Recovered clock can be used for pattern generation	Not supported	00	Not supported	00
		5	1		PG and Checker Swap/Invert Capabilities	Reference clock available for patterns	FALSE		FALSE	
		0	5		PG and Checker Swap/Invert Capabilities	User pattern supported length in 2-byte increments, 0000b = 2 bytes, 1111b = 32 bytes	0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
141	8D	7	1	RD	PG and Checker Swap/Invert Capabilities	Media Side Checker Data Swap	FALSE	11	FALSE	11
		6	1		PG and Checker Swap/Invert Capabilities	Media Side Checker Data Invert	FALSE		FALSE	
		5	1		PG and Checker Swap/Invert Capabilities	Media Side Generator Data Swap	FALSE		FALSE	
		4	1		PG and Checker Swap/Invert Capabilities	Media Side Generator Data Invert	TRUE		TRUE	
		3	1		PG and Checker Swap/Invert Capabilities	Host Side Checker Data Swap	FALSE		FALSE	
		2	1		PG and Checker Swap/Invert Capabilities	Host Side Checker Data Invert	FALSE		FALSE	
		1	1		PG and Checker Swap/Invert Capabilities	Host Side Generator Data Swap	FALSE		FALSE	
		0	1		PG and Checker Swap/Invert Capabilities	Host Side Generator Data Invert	TRUE		TRUE	
142	8E	7	1	RD	PG and Checker Swap/Invert Capabilities	Media Checker Per Lane Enable	TRUE	FF	TRUE	FF
		6	1		PG and Checker Swap/Invert Capabilities	Media Checker Per Lane Pattern Type Selection	TRUE		TRUE	
		5	1		PG and Checker Swap/Invert Capabilities	Media Generator Per Lane Enable	TRUE		TRUE	
		4	1		PG and Checker Swap/Invert Capabilities	Media Generator Per Lane Pattern Type Selection	TRUE		TRUE	
		3	1		PG and Checker Swap/Invert Capabilities	Host Checker Per Lane Enable	TRUE		TRUE	
		2	1		PG and Checker Swap/Invert Capabilities	Host Checker Per Lane Pattern Type Selection	TRUE		TRUE	
		1	1		PG and Checker Swap/Invert Capabilities	Host Generator Per Lane Enable	TRUE		TRUE	
		0	1		PG and Checker Swap/Invert Capabilities	Host Generator Per Lane Pattern Type Selection	TRUE		TRUE	
143	8F	0	8	RO	Reserved	Reserved				

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
144	90	0	64	RW	Host Controls	Pattern Generator, Host Side	0000000000000000	00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00
145	91	0	8	RW	Host Side Generator Data Invert	1b= invert, 0b= do not invert, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
146	92	0	8	RW	Host Side Generator Byte Swap	1b= swap MSB and LSB for PAM4, 0b= do not swap, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
147	93	0	8	RW	Host Side Generator pre-FEC Enable	1b= generate the pattern at the input to the internal FEC block, 0b= generate the pattern at the output from the internal FEC block per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
148	94	4	4	RW	Host Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane CMIS Table 8-72 for pattern codings.	0	00	0	00
		0	4		Host Side Generator Lane 1 pattern select		0		0	
149	95	4	4	RW	Host Side Generator Lane 4 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 3 pattern select		0		0	
150	96	4	4	RW	Host Side Generator Lane 6 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 5 pattern select		0		0	
151	97	4	4	RW	Host Side Generator Lane 8 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 7 pattern select		0		0	
152	98	0	64	RW	Host Controls Media Side Generator Enable	Using the config defined in bytes 153-159 0b=Disable 1b= enable, pattern generator, per lane, bit 0 = lane 1, bit7= lane 8	0000000000000000	00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00
153	99	0	8	RW	Media Side Generator Data Invert	1b= invert, 0b= do not invert, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
154	9A	0	8	RW	Media Side Generator Byte Swap	1b= swap MSB and LSB for PAM4, 0b= do not swap, per lane, bit 0 = lane 1, bit7= lane 8 This control inverts the pattern and does not swap the P and N signals	0	00	0	00
155	9B	0	8	RW	Media Side Generator pre-FEC Enable	1b= generate the pattern at the input to the internal FEC block, 0b= generate the pattern at the output from the internal FEC block per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
156	9C	4	4	RW	Host Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane CMIS Table 8-72 for pattern codings.	0	00	0	00
		0	4		Host Side Generator Lane 1 pattern select		0		0	
157	9D	4	4	RW	Host Side Generator Lane 4 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 3 pattern select		0		0	
158	9E	4	4	RW	Host Side Generator Lane 6 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 5 pattern select		0		0	
159	9F	4	4	RW	Host Side Generator Lane 8 pattern select		0	00	0	00
		0	4		Host Side Generator Lane 7 pattern select		0		0	
160	A0	0	64	RW	Host Controls Host Side Checker Enable	1b=Enable checker, using the configuration defined in bytes 161-167 0b=Disable pattern checker bit 0 = lane 1, bit7= lane 8	0000000000000000	00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00
161	A1	0	8	RW	Host Side Checker Data Invert	1b= invert, 0b= do not invert, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
162	A2	0	8	RW	Host Side Checker Byte Swap	1b= swap MSB and LSB for PAM4, 0b= do not swap, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
163	A3	0	8	RW	Host Side Checker post-FEC Enable	1b= check the pattern at the output from the internal FEC block, 0b= check the pattern at the input to the internal FEC block per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
164	A4	4	4	RW	Host Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane CMIS Table 8-72 for pattern codings.	0	00	0	00
		0	4		Host Side Checker Lane 1 pattern select		0		0	
165	A5	4	4	RW	Host Side Checker Lane 4 pattern select		0	00	0	00
		0	4		Host Side Checker Lane 3 pattern select		0		0	
166	A6	4	4	RW	Host Side Checker Lane 6 pattern select		0	00	0	00
		0	4		Host Side Checker Lane 5 pattern select		0		0	
167	A7	4	4	RW	Host Side Checker Lane 8 pattern select		0	00	0	00
		0	4		Host Side Checker Lane 7 pattern select		0		0	
168	A8	0	64	RW	Host Controls Media Side Checker Enable	1b= enable, 0b= disable, per lane, bit 0 = lane 1, bit7= lane 8	0000000000000000	00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00
169	A9	0	8	RW	Media Side Checker Data Invert	1b= invert, 0b= do not invert, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
170	AA	0	8	RW	Media Side Checker Byte Swap	1b= swap MSB and LSB for PAM4, 0b= do not swap, per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
171	AB	0	8	RW	Media Side Checker post-FEC Enable	1b= check the pattern at the output from the internal FEC block, 0b= check the pattern at the input to the internal FEC block per lane, bit 0 = lane 1, bit7= lane 8	0	00	0	00
172	AC	4	4	RW	Media Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane CMIS Table 8-72 for pattern codings.	0	00	0	00
		0	4		Media Side Checker Lane 1 pattern select		0		0	

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
173	AD	4	4	RW	Media Side Checker Lane 4 pattern select		0	00	0	00
		0	4		Media Side Checker Lane 3 pattern select		0		0	
174	AE	4	4	RW	Media Side Checker Lane 6 pattern select		0	00	0	00
		0	4		Media Side Checker Lane 5 pattern select		0		0	
175	AF	4	4	RW	Media Side Checker Lane 8 pattern select		0	00	0	00
		0	4		Media Side Checker Lane 7 pattern select		0		0	
176	B0	4	4	RW	Host PRBS Generator Clock Source	The source of the clock used for Host PRBS Pattern Gen can be configured using this control register (CMIS-4.0 Table 8-84)	0	00	0	00
		0	4		Media PRBS Generator Clock Source	The source of the clock used for Media PRBS Pattern Gen can be configured using this control register (CMIS-4.0 Table 8-84)	0		0	
177	B1	7	1	RW	Reset All Lanes	0b= individual lane, 1b= all lanes	0	00	0	00
		6	1		Reserved	Reserved				
		5	1		Reset Error Information	1b = the Error Information in Selector 01h to 05h are frozen 0b=Error Information in Selectors 01h-05h will be reset to 0.	0		0	
		4	1		Auto Restart Gate Time	CMIS Table 8-84	0		0	
		1	3		Gate Time	000b= not gated; 001b = 5s; 010b= 10s; 011b= 30s; 100b= 60s; 101b = 120s ; 110b = 300s ; 111b= custom	0		0	
		0	1		BER/Error Count Update Time	0b= 1s; 1b= 5s	0		0	
178	B2	4	4	RW	Reserved	Reserved	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
		2	2		Host PRBS Checker Clock Source	0h= recovered clock; 1h= internal clock; 2h= reference clock; 3h= reserved	0		0	
		0	2		Media PRBS Checker Clock Source	0h= recovered clock; 1h= internal clock; 2h= reference clock; 3h= reserved	0		0	
179	B3	0	8	RW	Reserved	Reserved	0	00	0	00
180	B4	0	8	RW	Media Side Output Loopback	0b= no loopback per lane 8-1 1b= loopback per lane 8-1	0	00	0	00
181	B5	0	8	RW	Media Side Input Loopback	0b= no loopback per lane 8-1 1b= loopback per lane 8-1	0	00	0	00
182	B6	0	8	RW	Host Side Output Loopback	0b= no loopback per lane 8-1 1b= loopback per lane 8-1	0	00	0	00
183	B7	0	8	RW	Host Side Input Loopback	0b= no loopback per lane 8-1 1b= loopback per lane 8-1	0	00	0	00
184-195	B8-C3	0	96	RW	Reserved	Reserved				
196-205	C4-CD	0	80	RW	Custom	Custom	0000000000000000	00 00 00 00 00 00 00 00 00 00	0000000000000000	00 00 00 00 00 00 00 00 00 00
206	CE	7	1	RW	M-Loss of Reference Clock	Loss of reference clock flag mask For the module	0	00	0	00
		0	6		Reserved	Reserved				
207	CF	0	8		Reserved	Reserved		00		00
208	D0	0	8	RW	M-Host Lane Pattern Checker Gating complete	Per-host lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable. M-Host Lane 8-1 to Bit 7-0	0	00	0	00
209	D1	0	8	RW	M-Media Lane Pattern Checker Gating complete	Per-media lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable. M-Media Lane 8-1 to Bit 7-0	0	00	0	00
210	D2	0	8	RW	M-Host Lane Pattern Generator LOL	Per-host lane pattern generator loss of lock flag mask M-Host Lane 8-1 to Bit 7-0	0	00	0	00

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
211	D3	0	8	RW	M-Media Lane Pattern Generator LOL	Per-media lane pattern generator loss of lock flag mask M-Media Lane 8-1 to Bit 7-0	0	00	0	00
212	D4	0	8	RW	M-Host Lane Pattern Checker LOL	Per-host lane pattern checker loss of lock flag mask M-Host Lane 8-1 to Bit 7-0	0	00	0	00
213	D5	0	8	RW	M-Media Lane Pattern Checker LOL	Latched per-media lane pattern checker loss of lock flag M-Media Lane 8-1 to Bit 7-0	0	00	0	00
214-223	D6-DF	0	80	RW	Reserved	Reserved		00		00
224-255	E0-FF	0	256	RW	User Pattern	Host defined user pattern	0000000000000000000000000000000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	0000000000000000000000000000000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

TABLE 9: UPPER PAGE 14H (MODULE DIAGNOSTICS 2)

The presence of Page 14h is conditional on the state of bit 5 in Page 01h byte 142 (8Eh). (CMIS-4.0 Table 8-91 to Table 8-94)

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128	80	0	8	RW	Diagnostic Selector	This Byte selects the content of the data in bytes 192-255, CMIS Table 8-92	00	00	00	00
129	81	0	8		Reserved	Reserved				
130	82	0	16		Custom	Custom	0000	00 00	0000	00 00
132	84	7	1	RO	Latched Diagnostics Flags L-Loss of Ref Clock	Latched loss of reference clock flag for the module. Clear on Read	0	00 00 00 00 00 00 00 00	0	00 00 00 00 00 00 00 00
		0	6		Reserved	Reserved				

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
133	85	0	8	RO	Reserved	Reserved		00		00
134	86	0	8	RO	L-Host Pattern Checker Gating Complete	Latched per-host lane gating complete flag. Set to 1 on complete, cleared on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
135	87	0	8	RO	L-Media Pattern Checker Gating Complete	Latched per-media lane gating complete flag. Set to 1 on complete, cleared on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
136	88	0	8	RO	L-Host Pattern Generator LOL	Latched per-host lane pattern generator loss of lock flag. Clear on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
137	89	0	8	RO	L-Media Pattern Generator LOL	Latched per-media lane pattern generator loss of lock flag. Clear on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
138	8A	0	8	RO	L-Host Pattern Checker LOL	Latched per-host lane pattern checker loss of lock flag. Clear on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
139	8B	0	8	RO	L-Media Pattern Checker LOL	Latched per-media lane pattern checker loss of lock flag. Clear on read. bit 0 = lane 1, bit7= lane 8	0	00	0	00
140	8C	0	80		Reserved	Reserved				
192-255	C0-FF	0	512	RO	Error Information Registers	Contents defined by Diagnostic Select in Byte 128 CMIS Table 8-94 Bytes 192-255 Contents per Diagnostics Selector	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

TABLE 10: UPPER PAGE 15H TIMINING CHARACTERISTICS FOR PTP (CMIS-5.0 PROVISION)

Page 15h may age 15h is an optional Page containing per-lane timing characteristics. The module advertises support of Page 15h in Bit 01h:145.3 (see Table 8-43). Page 15h may optionally be Banked. Each Bank of Page 15h refers to 8 lanes. All fields in Page 15h are read-only reporting registers (not necessarily static).

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
128-223	80-DF	0	96		Reserved	Reserved	00	00	00	00
224	E0	0	8	RO	DataPathRxLatencyHostLane1	DataPathRxLatencyHostLane<i> U16 lane <i> Rx delay in ns	25	25	25	25
225	E1	0	8				25	25	25	25
226	E2	0	8		DataPathRxLatencyHostLane2		25	25	25	25
227	E3	0	8				25	25	25	25
228	E4	0	8		DataPathRxLatencyHostLane3		25	25	25	25
229	E5	0	8				25	25	25	25
230	E6	0	8		DataPathRxLatencyHostLane4		25	25	25	25
231	E7	0	8				25	25	25	25
232	E8	0	8		DataPathRxLatencyHostLane5		25	25	25	25
233	E9	0	8				25	25	25	25
234	EA	0	8		DataPathRxLatencyHostLane6		25	25	25	25
235	EB	0	8				25	25	25	25
236	EC	0	8		DataPathRxLatencyHostLane7		25	25	25	25
237	ED	0	8				25	25	25	25
238	EE	0	8		DataPathRxLatencyHostLane8		25	25	25	25
239	EF	0	8				25	25	25	25
240	F0	0	8	RO	DataPathTxLatencyHostLane1	DataPathTxLatencyHostLane<i> U16 lane <i> Tx delay in ns U16 lane <i> Rx delay in ns	1D	1D	1D	1D
241	F1	0	8				1D	1D	1D	1D
242	F2	0	8		DataPathTxLatencyHostLane2		1D	1D	1D	1D
243	F3	0	8				1D	1D	1D	1D
244	F4	0	8		DataPathTxLatencyHostLane3		1D	1D	1D	1D
245	F5	0	8				1D	1D	1D	1D
246	F6	0	8		DataPathTxLatencyHostLane4		1D	1D	1D	1D
247	F7	0	8				1D	1D	1D	1D
248	F8	0	8		DataPathTxLatencyHostLane5		1D	1D	1D	1D

Byte Address Decimal	Byte HEX	LSB	Bit Size	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
							Spec Value	HEX Value	Spec Value	HEX Value
249	F9	0	8				1D	1D	1D	1D
250	FA	0	8		DataPathTxLatencyHostLane6		1D	1D	1D	1D
251	FB	0	8				1D	1D	1D	1D
252	FC	0	8		DataPathTxLatencyHostLane7		1D	1D	1D	1D
253	FD	0	8				1D	1D	1D	1D
254	FE	0	8		DataPathTxLatencyHostLane8		1D	1D	1D	1D
255	FF	0	8				1D	1D	1D	1D

APPENDIX A: INTERFACE AND LANE COUNT DIFFERENCES

Comparison of lower Page 00h byte 86 to byte 92 host and media interface and lane count between FTCD45x3E2PCM-4A and FTCD45x3E2PCM. See CMIS-4.0 Table 8-12, Table 8-13 and SFF-8024 Host Electrical Interfaces Table 4-5, Table 4-6, and Table 4-7.

Byte Address Decimal	Byte HEX	Type	Name	Description	FTCD4523E2PCM-4A FTCD4533E2PCM-4A		FTCD4523E2PCM FTCD4533E2PCM	
					Spec Value	HEX Value	Spec Value	HEX Value
86	56	RO	ApSel 1 Advertising	Host Interface Code SFF-8024 Table 4-5	11h: 400GAUI-8 C2M (Annex 120E)	11	0Dh: 100GAUI-2 C2M (Annex 135G)	0D
87	57	RO		Media Interface Code SFF-8024 Table 4-7	1Ch: 400GBASE-DR4	1C	14h: 10GFC-MM, 100GBASE-DR	14
88	58	RO		Host Lane Count	8	84	2	21
				Media Lane Count	4		1	
89	59	RO		Host Lane Assignment Options (See Table 8-38 for Media Lane Assignment Options)	Permitted to start on Host Lane 8-1	1	Permitted to start on Host Lane 8-1	55
90	5A	RO	ApSel 2 Advertising	Host Interface Code	0Dh: 100GAUI-2 C2M (Annex 135G)	0D	11h: 400GAUI-8 C2M (Annex 120E)	11
91	5B	RO		Media Interface Code	14h: 10GFC-MM,	14	1Ch: 400GBASE-DR4	1C
92	5C	RO		Host Lane Count	2	21	8	84
				Media Lane Count	1		4	
93	5D	RO		Host Lane Assignment Options (See Table 8-38 for Media Lane Assignment Options)	Permitted to start on Host Lane 8-1	55	Permitted to start on Host Lane 8-1	01

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