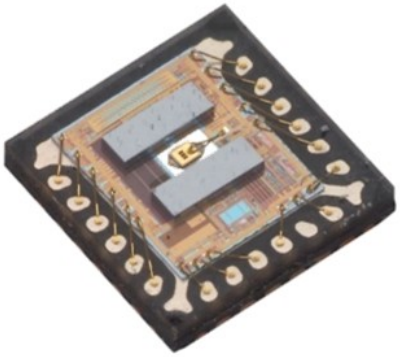
Data Sheet

AEDR-9940A/9940ERA

Three-Channel Reflective Incremental Encoder with Analog or Digital Output (198.4 LPI) AEC-Q100 Qualified



Description

The Broadcom® AEDR-9940A/9940ERA is a three-channel reflective optical encoder. The selectable and programmable options available are three-channel digital or analog differential A, B, and I outputs.

The AEDR-9940A/9940ERA in analog encoder modes, with three channels differential analog outputs (Sine+, Sine–, Cos+, Cos–; I+, I–), can be interfaced directly with external interpolators.

The AEDR-9940A/9940ERA digital encoder mode offers two-channel (AB) quadrature digital outputs and a third channel digital index output. Being TTL compatible, the outputs of the AEDR-9940A/9940ERA encoder can be interfaced with most of the signal processing circuitries. Therefore, the encoder provides easy integration and flexible design-in into existing systems.

The AEDR-9940A/9940ERA encoder is designed to operate over a –40°C to +125°C temperature range and is suitable for commercial, industrial and automotive end applications.

The encoder houses an LED light source and photo-detecting circuitry in a single package. The small size of 4.0 mm (L) × 4.0 mm (W) × 0.7 mm (H) allows it to be used in a wide range of miniature commercial applications, where size and space are primary concerns.

Features

- Analog output option: Single-ended or differential sine-cosine with analog output or digital index output
- Digital output option: Three-channel differential or TTL compatible; two-channel quadrature (AB) outputs for direction sensing and a third channel, index (I) digital output
- SPI programmable interpolator from 1X to 1024X
- Wide-selection built-in interpolator with 1X to 6X, 8X, 9X, 10X, 12X, 16X, 20X, 25X, 32X, 50X, 64X, 80X,100X, 128X, 160X, 256X, 320X, and 640X to 1000X
- Surface-mount leadless package: 4.0 mm (L) × 4.0 mm (W) × 0.7 mm (H)
- Operating supply voltages of 3.3V and 5.0V
- Built-in LED current regulation
- Wide operating temperature range: –40°C to 125°C
- High encoding resolution: 198.4375 LPI (lines per in.) or 7.8125 LP mm (lines per mm) or 0.128 mm (pitch)
- Translucent protection compound
- Auto-calibration options:
  - Off-scale to on-scale triggering
  - Pin-triggering
- Grade 1 AEC-Q100 qualified

Applications

- Closed-loop stepper motors
- Small motors, actuators
- Industrial printers
- Robotics
- Card readers
- Pan-tilt-zoom (PTZ) camera
- Portable medical equipment
- Optometric equipment
- Linear stages

NOTE: Except as expressly indicated in writing, this product is not designed or warranted to be suitable for use in safety-related applications where its failure or malfunction can reasonably be expected to result in injury, death, or severe equipment damage. Customers are solely responsible for determining the suitability of this product for its intended application and solely liable for all loss, damage, expense, or liability in connection with such use.

Output Waveform

Figure 1: Sample of Output Waveforms

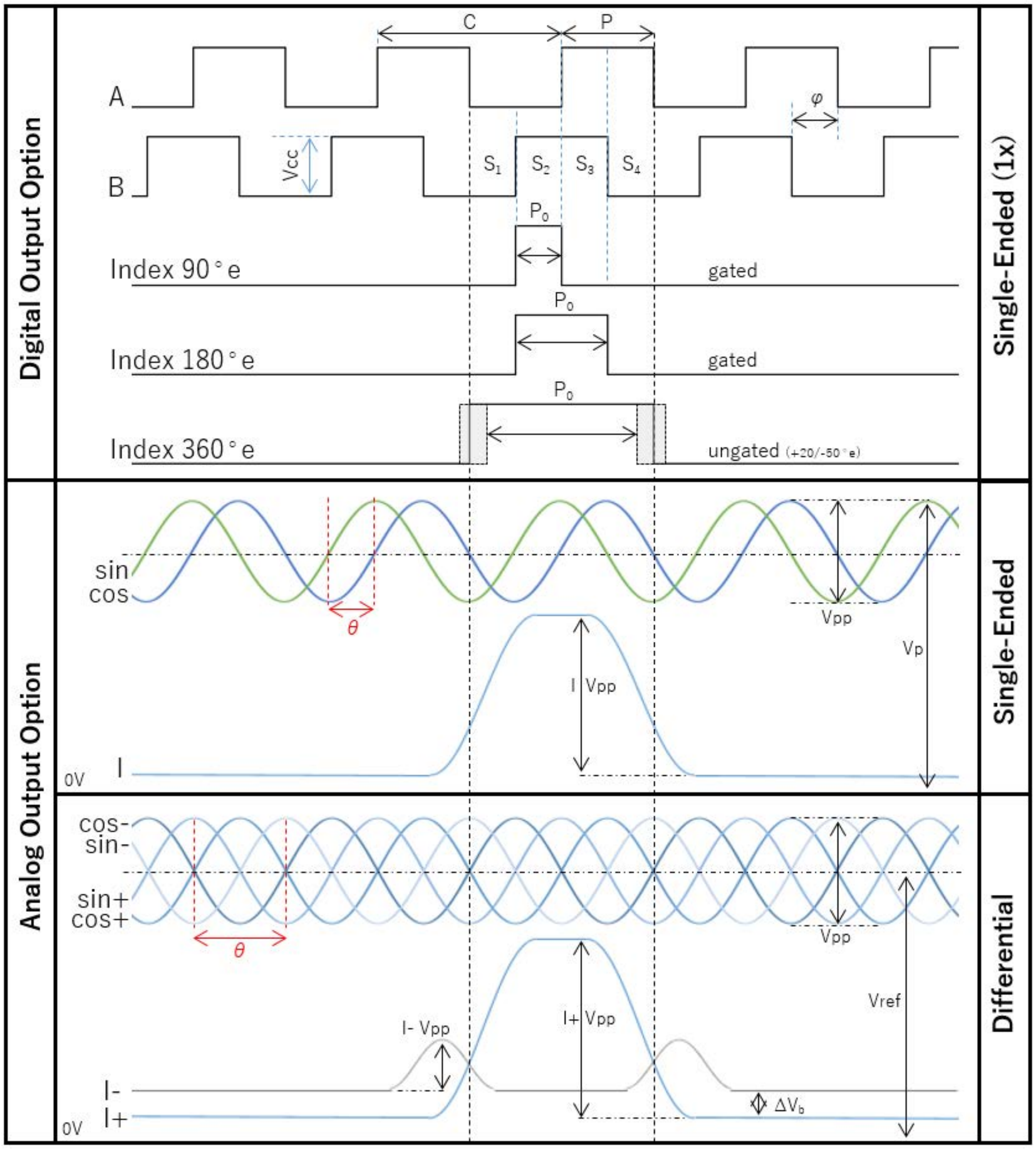
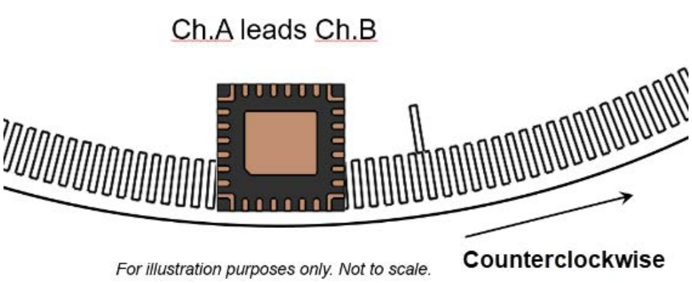


Figure 2: Top View: Code Wheel Movement Direction versus Output Signals



Digital Parameter Definitions

Test	Parameter	Definition
Count	N	The number of bar and window pairs or counts per revolution (CPR) of the code wheel.
Cycle	C	360 electrical degrees (°e), 1 bar and window pair. One Shaft Rotation: 360 mechanical degrees, N cycles.
Cycle Error	ΔC	An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.
Pulse Width (Duty) Error	ΔP	The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e
State	S	The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are four states per cycle, each nominally 90°e.
Phase	φ	The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.
Optical Radius	R_{OP}	The distance from the code wheel's center of rotation to the optical center (O.C.) of the encoder module.
Index Pulse Width	P_O	The number of electrical degrees that an index is high during one full shaft rotation.

Analog Parameter Definitions

Test	Parameter	Definition
Analog Peak-to-Peak	Vpp	The peak-to-peak signal magnitude in V of the analog signals.
Reference Voltage	Vref	The offset in V of the mid-point of the analog signal peak-to-peak to zero voltage point. Vref = Vcc/2
Analog Peak Voltage/Valley Voltage	Vp	The value in V of the peak/valley of the analog signals (one-sided reading).
Analog Minimum Voltage	Vmin	The value in V of the depth of the analog signals (minimum reading in V). Vmin = Vp – Vpp
Analog Index Vbias (delta)	ΔV_b	The absolute difference of the indexes Vbias = I + Vmin – I –Vmin. The minimum value of ΔV_b is 200 mV.
Phase Shift	θ	The value in °e of the phase between two analog signals. Single-ended mode; Cosine leads Sine by 90°e. Differential mode; Cosine+ leads Cosine– by 180°e, or Sine– lags by 180°e from Sine+

Absolute Maximum Ratings

Parameter	Symbol	Range
Storage Temperature	T_S	–40°C to 125°C
Operating Temperature	T_A	–40°C to 125°C
Supply Voltage	V_{CC}	5.5V

NOTE:

- Proper operation of the encoder no longer guaranteed if exceeded maximum ratings.
- Exposure to extreme light intensity (such as from flashbulbs or spotlights) may cause permanent damage to the device.
- Some particles may be present on the surface of the encoder surface after SMT reflow or handling during assembly. Clean the encoder surface gently if some particles are present.

CAUTION! Take anti-static discharge precautions when handling the encoder to avoid damage, degradation or both, induced by ESD.

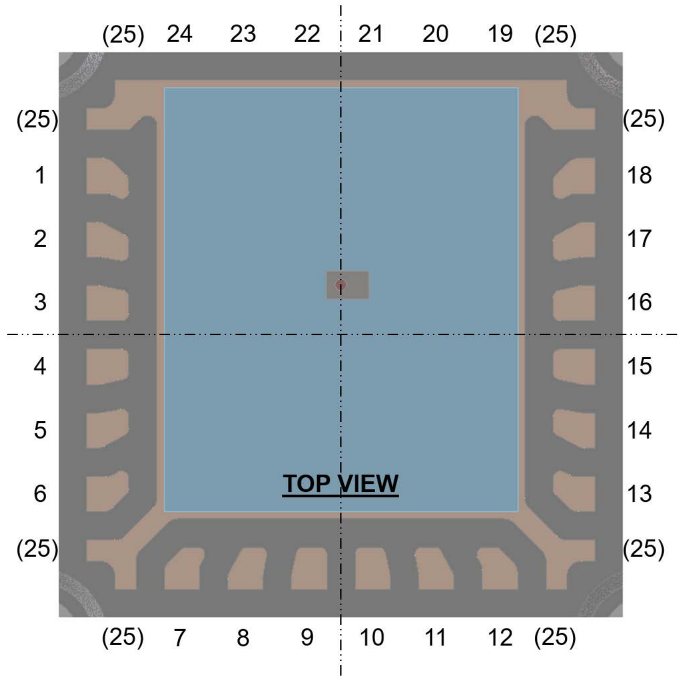
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	Ripple < 100 mVpp, $V_{CC} = V_{DD}$
		4.5	5.0	5.5	V	
Current Consumption	I_{CC}	—	45	—	mA	Dependent on spatial position and rotational speed
Pin Current (All I/O Outputs)	I	–20	—	20	mA	—
Maximum Output Frequency (External Mode Selection)	f	—	—	0.25	MHz	Interpolation: 1X
		—	—	0.50	MHz	Interpolation: 2X
		—	—	1.00	MHz	Interpolation: 4X
		—	—	2.00	MHz	Interpolation: 8X
		—	—	4.00	MHz	Interpolation: 16X
		—	—	4.00	MHz	Interpolation: 32X
		—	—	4.00	MHz	Interpolation: 64X
		—	—	4.00	MHz	Interpolation: 128X
Maximum Output Frequency (SPI programmable)	F	—	—	4.00	MHz	Interpolation: ≥ 32X
Tangential Misalignment	E_T	—	—	±0.35	mm	CPR dependent. With AutoCal: 128 CPR = ±0.25 mm 625 CPR = ±0.35 mm 1000 CPR = ±0.35 mm Without AutoCal: > 512 CPR = ±0.25 mm
Radial Misalignment	E_R	—	—	±0.35	mm	
Code Wheel Gap	G	0.85	1.35	2.35	mm	For typical 625 CPR
		0.85	1.35	1.85	mm	For ≤ 128 CPR
Specular Reflectance	R_f	60%	—	—	—	Reflective area
		—	—	5%	—	Non-reflective area
Tri-state Voltage Threshold	High	90	—	—	%V_{CC}	—
	Low	—	—	10	%V_{CC}	—
	Open	30	—	70	%V_{CC}	—

Power-Up Behavior

When the AEDR-9940A/9940ERA is powered on, the A, B, and I digital outputs will be in an idle state until the first toggle of either the A or B digital signal. This duration is also called as startup phase, where the encoder is in recognition mode to verify the logic and the code wheel position.

Encoder Pinout



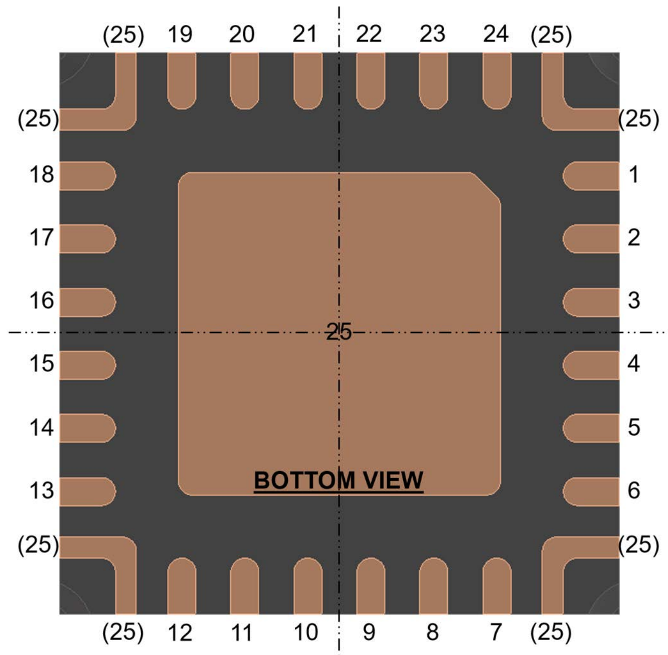


Table 1: AEDR-9940A/9940ERA Pinout

Pin	Name	Function	Pin	Name	Function
1	CH_A+	Digital A+ or Analog Sine+	14	SEL1	Mode Selection 1
2	CH_A– / SPI_DIN	Digital A– or Analog Sine– / SPI Data In	15	VSSA	Analog Ground
3	VDD 5V	Digital Supply Voltage	16	VDDA	Analog Supply Voltage
4	VSSD	Digital Ground	17	CH_B– / SPI_CLK	Digital B+ or Analog Cosine– / SPI Clock
5	CAL	Auto Calibration	18	CH_B+	Digital B– or Analog Cosine+
6	CAL_STAT	Calibration Status	19	No Connect	—
7	LEDERR	LED error indicator	20	No Connect	—
8	INDEXSEL	Index Selection	21	No Connect	—
9	CH_I– / 100k_CLK	Digital or Analog Index– / 100k Clock	22	No Connect	—
10	CH_I+ / SPI_DOUT	Digital or Analog Index+ / SPI Data Out	23	No Connect	—
11	No Connect	—	24	No Connect	—
12	SEL3	Mode Selection 3	25	VSSA	Analog Ground
13	SEL2	Mode Selection 2	(25)	No connect	—

NOTE: No connection to all corner pads indicated as (25).

Select Options – AEDR-9940A/9940ERA Built-In Interpolation Factor

By configuring the selection pins, the user can select an interpolation factor from 1X to 1000X without accessing through SPI communication.

Table 2: Interpolation Factor and Index Option Selections

No.	SEL1	SEL2	SEL3	Interpolation Factor	IndexSEL	Index
1	Low	Low	Low	1X	Low	Interpolation 1X - Index Gated 90 degrees
					High	Interpolation 1X - Index Gated 180 degrees
					Open	Interpolation 1X - Index Raw (Ungated)
2	High	Low	Low	2X	Low	Interpolation 2X - Index Gated 90 degrees
					High	Interpolation 2X - Index Gated 180 degrees
					Open	Interpolation 2X - Index Gated 360 degrees
3	Open[a]	Low	Low	3X	Low	Interpolation 3X - Index Gated 90 degrees
					High	Interpolation 3X - Index Gated 180 degrees
					Open	Interpolation 3X - Index Gated 360 degrees
4	Low	High	Low	4X	Low	Interpolation 4X - Index Gated 90 degrees
					High	Interpolation 4X - Index Gated 180 degrees
					Open	Interpolation 4X - Index Gated 360 degrees

Table 2: Interpolation Factor and Index Option Selections (Continued)

No.	SEL1	SEL2	SEL3	Interpolation Factor	IndexSEL	Index
5	High	High	Low	5X	Low	Interpolation 5X - Index Gated 90 degrees
					High	Interpolation 5X - Index Gated 180 degrees
					Open	Interpolation 5X - Index Gated 360 degrees
6	Open[a]	High	Low	6X	Low	Interpolation 6X - Index Gated 90 degrees
					High	Interpolation 6X - Index Gated 180 degrees
					Open	Interpolation 6X - Index Gated 360 degrees
7	Low	Open[a]	Low	8X	Low	Interpolation 8X - Index Gated 90 degrees
					High	Interpolation 8X - Index Gated 180 degrees
					Open	Interpolation 8X - Index Gated 360 degrees
8	High	Open[a]	Low	9X	Low	Interpolation 9X - Index Gated 90 degrees
					High	Interpolation 9X - Index Gated 180 degrees
					Open	Interpolation 9X - Index Gated 360 degrees
9	Open[a]	Open[a]	Low	10X	Low	Interpolation 10X - Index Gated 90 degrees
					High	Interpolation 10X - Index Gated 180 degrees
					Open	Interpolation 10X - Index Gated 360 degrees
10	Low	Low	High	12X	Low	Interpolation 12X - Index Gated 90 degrees
					High	Interpolation 12X - Index Gated 180 degrees
					Open	Interpolation 12X - Index Gated 360 degrees
11	High	Low	High	16X	Low	Interpolation 16X - Index Gated 90 degrees
					High	Interpolation 16X - Index Gated 180 degrees
					Open	Interpolation 16X - Index Gated 360 degrees
12	Open[a]	Low	High	20X	Low	Interpolation 20X - Index Gated 90 degrees
					High	Interpolation 20X - Index Gated 180 degrees
					Open	Interpolation 20X - Index Gated 360 degrees
13	Low	High	High	25X	Low	Interpolation 25X - Index Gated 90 degrees
					High	Interpolation 25X - Index Gated 180 degrees
					Open	Interpolation 25X - Index Gated 360 degrees
14	High	High	High	32X	Low	Interpolation 32X - Index Gated 90 degrees
					High	Interpolation 32X - Index Gated 180 degrees
					Open	Interpolation 32X - Index Gated 360 degrees
15	Open[a]	High	High	50X	Low	Interpolation 50X - Index Gated 90 degrees
					High	Interpolation 50X - Index Gated 180 degrees
					Open	Interpolation 50X - Index Gated 360 degrees
16	Low	Open[a]	High	64X	Low	Interpolation 64X - Index Gated 90 degrees
					High	Interpolation 64X - Index Gated 180 degrees
					Open	Interpolation 64X - Index Gated 360 degrees
17	High	Open[a]	High	80X	Low	Interpolation80X - Index Gated 90 degrees
					High	Interpolation80X - Index Gated 180 degrees
					Open	Interpolation80X - Index Gated 360 degrees

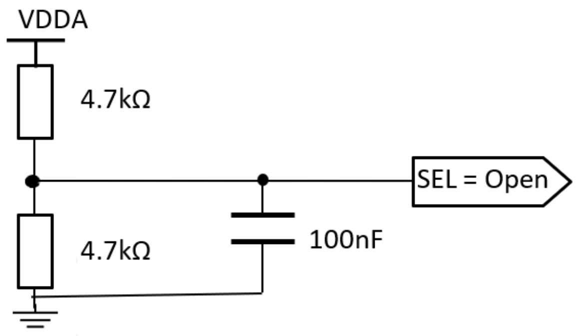
Table 2: Interpolation Factor and Index Option Selections (Continued)

No.	SEL1	SEL2	SEL3	Interpolation Factor	IndexSEL	Index
18	Open[a]	Open[a]	High	100X	Low	Interpolation 100X - Index Gated 90 degrees
					High	Interpolation 100X - Index Gated 180 degrees
					Open	Interpolation 100X - Index Gated 360 degrees
19	Low	Low	Open[a]	128X	Low	Interpolation 128X - Index Gated 90 degrees
					High	Interpolation 128X - Index Gated 180 degrees
					Open	Interpolation 128X - Index Gated 360 degrees
20	High	Low	Open[a]	160X	Low	Interpolation 160X - Index Gated 90 degrees
					High	Interpolation 160X - Index Gated 180 degrees
					Open	Interpolation 160X - Index Gated 360 degrees
21	Open[a]	Low	Open[a]	256X	Low	Interpolation 256X - Index Gated 90 degrees
					High	Interpolation 256X - Index Gated 180 degrees
					Open	Interpolation 256X - Index Gated 360 degrees
22	Low	High	Open[a]	320X	Low	Interpolation 320X - Index Gated 90 degrees
					High	Interpolation 320X - Index Gated 180 degrees
					Open	Interpolation 320X - Index Gated 360 degrees
23	High	High	Open[a]	640X	Low	Interpolation 640X - Index Gated 90 degrees
					High	Interpolation 640X - Index Gated 180 degrees
					Open	Interpolation 640X - Index Gated 360 degrees
24	Open[a]	High	Open[a]	1000X	Low	Interpolation 1000X - Index Gated 90 degrees
					High	Interpolation 1000X - Index Gated 180 degrees
					Open	Interpolation 1000X - Index Gated 360 degrees
25	Low	Open[a]	Open[a]	Ungated Digital	Low	Analog SIN/COS (500 mVpp), Digital Index (Ungated)
					High	Analog SIN/COS (500 mVpp), Digital Index (Ungated)
					Open	Analog SIN/COS (500 mVpp), Digital Index (Ungated)
26	High	Open[a]	Open[a]	Analog	Low	Analog SIN/COS (500 mVpp), Analog Index (1 Vpp)
				Ungated Digital	High	Analog SIN/COS (1 Vpp), Digital Index (Ungated)
				Analog	Open	Analog SIN/COS (1 Vpp), Analog Index (1 Vpp)
27	Open[a]	Open[a]	Open[a]	SPI Mode	Low	SPI Mode: Program Selection
					High	SPI Mode: Output Enabled
					Open	SSI 3W Mode[b]

a. Open selection must be connected to the middle of a voltage divider circuit.

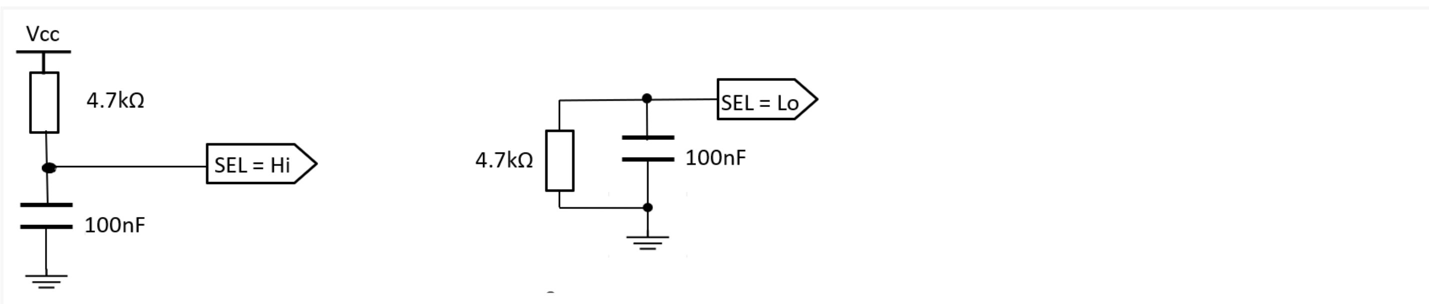
b. SSI 3W mode is for monitoring purposes only.

Figure 3: Example of a Voltage Divider Circuit



It is recommended to use 2 x 4.7-kΩ resistors (VDDA-GND).

Figure 4: Example of a Hi and Lo Selection Circuit



NOTE: It is recommended to include capacitors at the SEL pins to prevent or eliminate any unwanted disturbance or signal coupling that could potentially impact the mode of AEDR-9940A/9940ERA selection and lead to unwanted behavior of the device.

IO Pins Considerations

IO Contention

There should be no voltage or current applied to the IOs of the AEDR-9940A/9940ERA encoder before the encoder is powered up. There are ESD diodes and IO multiplexing in the device pads. Any undue voltage or current going into the device can partially power up the device and bring it to an unknown state or cause an undue collection of charges prior to a proper power up. A proper power sequencing will ensure proper operation of the encoder.

Output Load

The AEDR-9940A/9940ERA encoder is designed for a diverse set of applications. The device provides different modes of functional selection. Careful consideration of external loads is required to prevent unwanted overshoot, ringing, and even instability of the device. Select a proper resistor capacitor load at the output for the mode selected in the application. It is generally not recommended to drive directly a capacitive or inductive load.

Interpolation Factor

The digital interpolation factor shown in the previous table is used in conjunction with the following equations to cater for various rotational speeds (RPM) and counts per revolution (CPR).

RPM = (Count Frequency × 60) / CPR

The CPR (at 1X interpolation) is based on the following equation that is dependent on radius of operation (R_{OP}).

CPR = LPI × 2π × R_{OP} (inch) or CPR = LP mm × 2π × R_{OP} (mm)

NOTE: LP mm (lines per mm) = LPI / 25.4

Programmable Interpolation Factor (Select Options)

The encoder is programmable through SPI with an interpolation factor from 1X to 1024X.

1. Configure external selection to SPI Mode: Program Selection.
2. For signals output after configuration, set external selection to SPI Mode: Output Enabled.

SPI Communication Pinout (For Interpolation and Index Width Selection)

Table 3: Encoder Calibration-Related Pinout

Pin	Name	Function
10	SPI_DOUT	SPI Data Output
2	SPI_DIN	SPI Data Input
17	SPI_CLK	SPI Clock

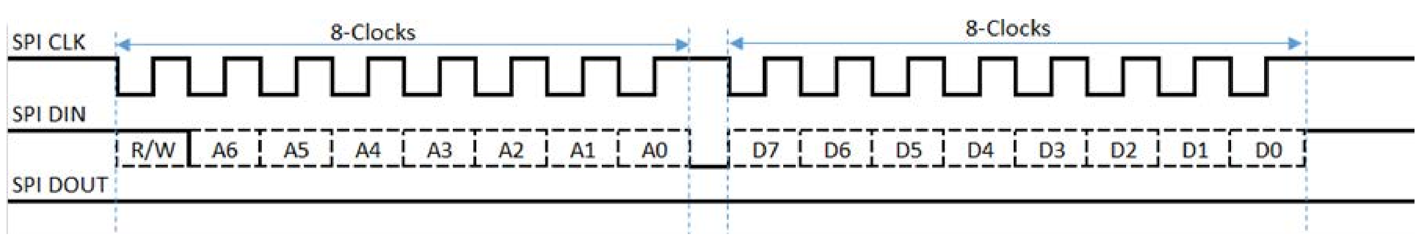
SPI Read and Write Timing Diagram (Maximum Clock Frequency 1 MHz)

Table 4: SPI Read and Write Memory Map

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	Address[6:0]							Data[7:0]							
Write	1	Address[6:0]							Data[7:0]							

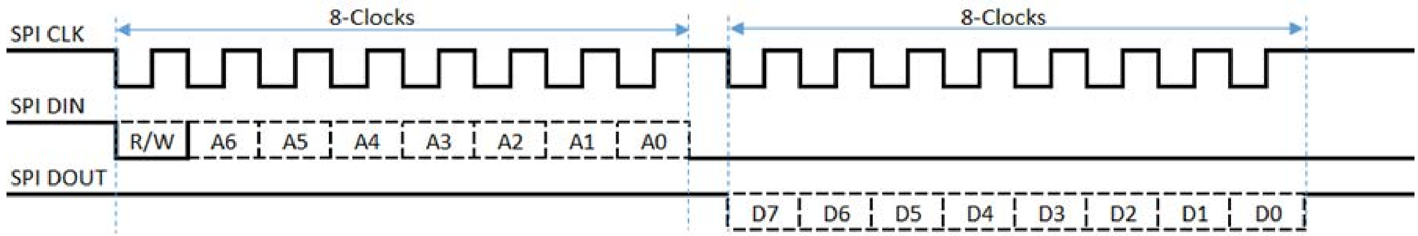
SPI Write: <Write Command = 1><7bits address><8bits data>

Figure 5: SPI Write Timing Diagram



SPI Read: <Read Command = 0><7bits address>

Figure 6: SPI Read Timing Diagram



Unlock Sequence

1. Write to SPI Address 0x00 with value AB (Hex) to unlock Level 1.
2. Write to SPI Address 0x14 with value 00 (Hex) to go to Page 0.

Program Memory

Write to SPI Address 0x01 with value A1 (Hex) to program memory.

Interpolation Settings and Programming

1. Write to SPI Address 0x0B and 0x0C with the appropriate value per the following figure.
2. After finalizing CPR settings, write to SPI Address 0x01 (Hex) with a value A1 (Hex) before continuing to program the AEDR-9940A/9940ERA.

Figure 7: Available Interpolation and Index Values in the AEDR-9940A/9940ERA Encoder

Byte Address	page	Bit								Note
[hex]		7	6	5	4	3	2	1	0	
0x0B				Iwidth_digital[1:0]		CPR[11:8]				CPR: 0-1024
0x0C		CPR[7:0]								

Interpolation CPR	0x0B (Hex)	0x0C (Hex)
1	Bit 0 = 0	01
2	–	02
–	–	–
–	–	–
10	–	0A
11	–	0B
–	–	–
–	–	–
255	Bit 0 = 0	FF
256	Bit 0 = 1	00
257	Bit 0 = 1	01
–	–	–
–	–	–
512	Bit 1 = 1	00
–	–	–
–	–	–
1024	Bit 2 = 1	00

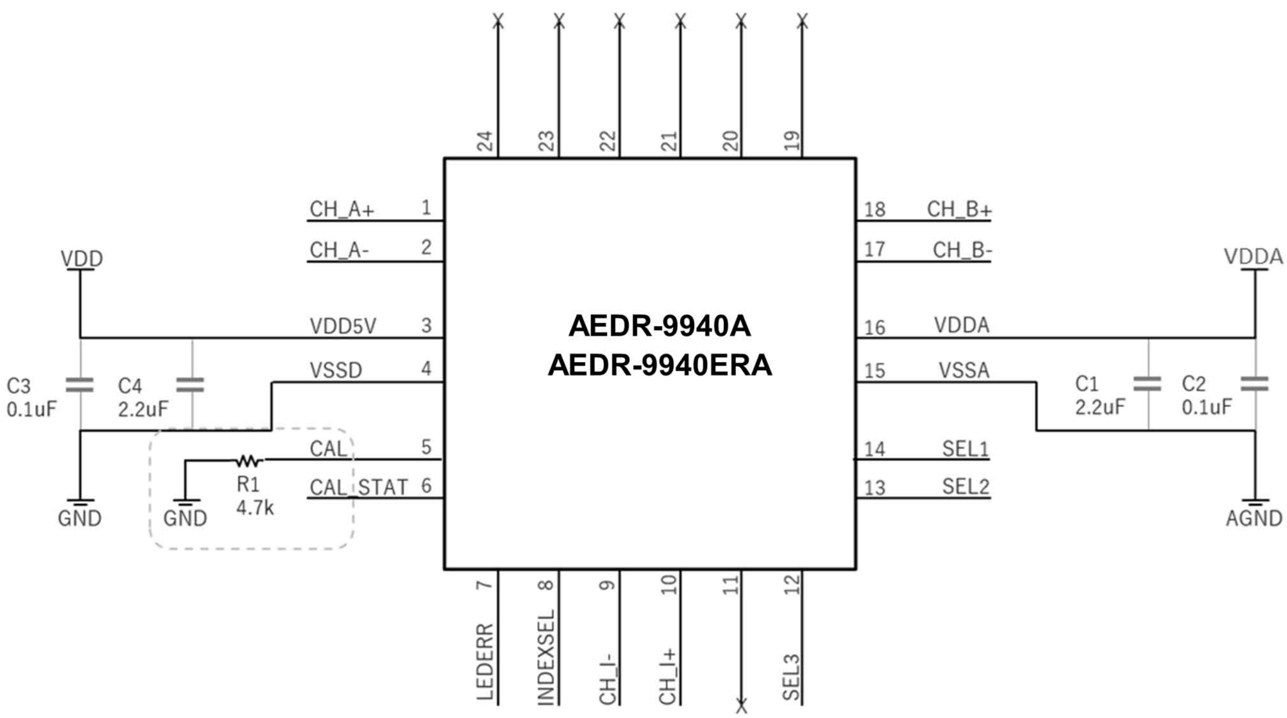
Iwidth_ Digital	Index Width
00	90deg
01	180deg
10	270deg
11	360deg

Recommended Setup for the Power Supply Pins and General Routing

Both VDDA and VDD supplies, and the respective grounds (VSSA and VSSD) must be connected separately as shown in the following figure. Follow these schematic design rules:

- Use a pair of 2.2-uF and 0.1-uF capacitors as a bypass on the VDD and VDDA trace. Place them in parallel as close as possible to the encoder ASIC package, in between the power and ground pins.
- Design separate VDD and VDDA traces.
- Minimize trace or cable length where possible.

Figure 8: Reference Schematic Diagram



NOTE:

1. Refer to the Select Options – AEDR-9940A/9940ERA Built-In Interpolation Factor table for SEL1, SEL2, SEL3, and IND_SEL.
2. VDDA and VDD must be same voltage level.
3. VSSA and VSS must be connected together.
4. The LEDERR and CAL_STAT are encoder status outputs. Do not use the outputs to directly drive an LED. Do not connect the pins if they will not be used.
5. Place a weak pull-low onto the CAL pin (for example, 4.7-kΩ resistor).

Autocalibration Steps (Off-Scale to On-Scale Trigger)

The AEDR-9940A has a built-in autocalibration algorithm that can be triggered by moving the encoder from an off-scale condition (no window bar) to an on-scale condition (window bar). Alternatively, use a paper or opaque material and place it in front of the encoder and remove it to trigger the auto calibration process. The purpose of the calibration process is to align the center of the Index signal to the center of the Channel B signal. The misalignment of the Index signal is due to potential spatial misalignment of the encoder to the code strip after assembly

1. Ensure the encoder is *not* positioned over the code strip or the window bar pattern (off-scale). Power on the encoder. Alternatively, place a piece of opaque (not transparent) material in front of the encoder and then remove it
2. Move the encoder PCBA/read head so it is positioned over the code strip and within the specified spatial tolerance (on-scale).
3. Move the encoder PCBA/read head back and forth over the code strip. Monitor the calibration status by observing the CAL_Stat signal or Ch A+/Ch B+.
4. Move the encoder PCBA/read head continuously for at least 5 seconds to 10 seconds; the total calibration time is dependent on both the speed of movement and the counts of the index pattern crossing the encoder ASIC. The Ch B+ state will change to high if the autocalibration process is successful. The states of both Ch A+ and Ch B+ will change to high if the auto calibration process is unsuccessful. If auto-calibration is unsuccessful, verify the gap between the encoder and the code strip is correct, and repeat steps 1 through 4 as needed.
5. Perform a power cycle and the encoder ASIC will function as normal.

NOTE:

1. After calibration is complete, a power cycle is required for the new encoder settings to be effective.
2. The AEDR-9940ERA option is without this off-scale to on-scale trigger feature.

Autocalibration Steps (By Pin Trigger)

The AEDR-9940A/9940ERA has a built-in auto calibration process that can be triggered on power-up by shorting the CAL pad (pin 5) to VDDA (or VDD). The purpose of the calibration process is to align the center of the Index signal to the center of the channel B signal. The misalignment of the Index signal is due to potential spatial misalignment of the encoder ASIC to the code wheel after assembly. Perform the auto calibration process even if the A, B, and I signals appear normal at the first power-on after the encoder assembly. The auto calibration process helps to optimize the internal encoder ASIC settings, hence enhancing the reliability and performance.

1. Spin the motor at a rotation speed between 1000 rpm and 2000 rpm.
2. Short the CAL pad to VDDA or VDD line. Use a high value resistor such as 4.7 kΩ or 5.6 kΩ to do the shorting.
3. Turn on power to the encoder. This will trigger the encoder ASIC to start the auto calibration process.
4. Wait for at least 5 seconds. Observe CAL_STAT pin, which will start pulsing as the calibration begins. Once the calibration is completed, CAL_STAT will remain high. CAL_STAT will remain pulsing if the calibration attempt fails.
5. 5.Remove the short between CAL to VDDA or VDD.
6. Perform a power cycle and the encoder ASIC will function as normal.

NOTE:

1. If autocalibration is unsuccessful, verify that the gap between the encoder and the code wheel is correct. Repeat steps 1 through 6 as needed.

2. After calibration is complete, a power cycle is required for the new encoder settings to be effective.

Table 5: Pad States During Calibration

Pad	CAL (Pin 5)	A+	B+	I+	Status
Pad State	H	L	L	L	Calibration in-progress
	H	H	L	L	Incremental calibration done
	H	L	H	L	Incremental and index calibration done
	H	H	H	L	Calibration fail/error

Table 6: LED Status Pins During Calibration (CAL_STAT and LEDERR Pins)

Pad	CAL_STAT	LEDERR	Status
Pad State	Pulsing (500 ms)	L	Calibration in-progress
	H	L	Calibration done
	L	H	Out of tangential/radial alignment

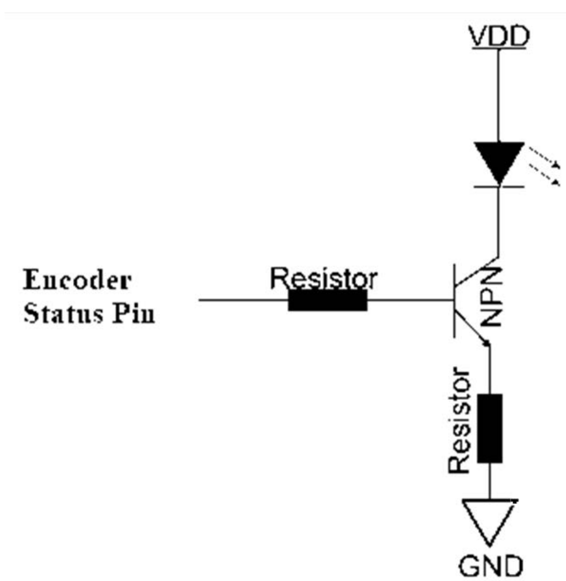
Table 7: Status Pin States (LED Indicators)

PIN	Power Up from t = 0	Encoder Ready	Calibrating	Calibration Done	Calibration Error	LEDERROR[a]	LEDERROR[b]
CAL_STAT	L	L	Pulsing (500 ms)	H	L	L	L
LEDERR	L	L	L	L	L	H	Pulsing (500ms)

a. No toggling signal indicates a maximum LED current state. (off-scale/no window bar).

b. Early warning on high LED current but signal is normal.

Figure 9: Status Pin Connection



NOTE:

1. H = High (VDD)
2. L = Low (GND)

Digital Signals Characteristics (Code Wheel of R_{OP} at 12.73 mm, 625 CPR)

Figure 10: Typical Channel A and Channel B Signals Dynamic Performance over Different Interpolation Values

Parameter	Symbol	Dynamic Performance								Unit
		Typical								
Interpolation Factor		**1X**	**2X**	**4X**	**8X**	**16X**	**32X**	**64X**	**128X**	
Cycle Error	ΔC	±3	±4	±5	±9	±11	±19	±19	±19	°e
Pulse Width (Duty) Error	ΔP	±3	±3	±5	±8	±10	±16	±16	±16	°e
Phase Error	Δφ	±1	±2	±3	±5	±6	±9	±9	±9	°e
State Error	ΔS	±2	±3	±5	±7	±7	±18	±18	±18	°e
Index Pulse Width (Gated 90°)	P_O	90								°e
Index Pulse Width (Gated 180°)	P_O	180								°e
Index Pulse Width (Gated 360°)	P_O	N/A	360							°e
Index Pulse Width (Raw Ungated)	P_O	330	N/A							°e

NOTE:

1. Typical values represent the average value of encoder performance based on factory setup conditions at maximum output frequency for each interpolation.
2. The optimal performance of encoder depends on the motor and system set up condition of the individual customer.

Electrical Characteristics

Characteristics over recommended operating conditions at 25°C.

Table 8: Typical Channel A and Channel B Signal Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
High Level Output Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –20mA
Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OH} = +20mA
Output Current per Channel, I_{out}	I_O	—	—	20	mA	—
Rise Time	t_r	—	< 50	—	ns	CL ≤ 50 pF
Fall Time	t_f	—	< 50	—	ns	

Code Wheel Characteristics

Characteristics are based on a Broadcom-qualified code wheel supplier. Contact Broadcom for information regarding qualified reflective code wheel suppliers.

Table 9: Code Wheel Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Specular Reflectance	R_f	60%	—	—	—	Reflective area
		—	—	5%	—	Non-reflective area
LED Peak Wavelength	λ_p	—	660	—	nm	—

Code Wheel Design Guideline

- The window tracks are reflective surfaces.
- The bar tracks are opaque surfaces.
- Incremental window and bar tracks are trapezoidal.
- The number of Incremental window and bar tracks depend on the CPR.
- The Incremental window and bar tracks have the same width value.
- There is an offset between the incremental window tracks and the index window track, denoted by F.
- Index window track is rectangular.
- There is only one index window track, and its width is 0.04988 mm.

Figure 11: Code Wheel Design (Not to Scale)

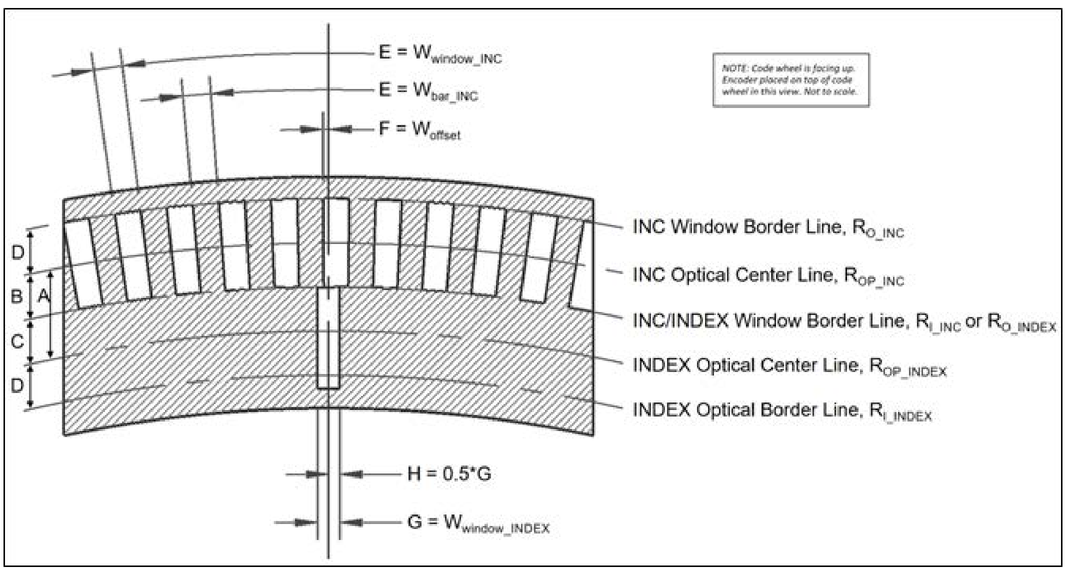


Table 10: Code Wheel Design

Dimension	Formula	AEDR-9940A/9940ERA
Pitch (°)	(360 / CPR)	—
A (mm)	$R_{OP\_INC} – R_{OP\_INDEX}$	1.1504
B (mm)	$R_{OP\_INC} – R_{I\_INC}$	0.5752
C (mm)	$R_{O\_INDEX} - R_{OP\_INDEX}$	0.5752
D (mm)	$R_{O\_INC} – R_{OP\_INC}$ or $R_{OP\_INDEX} – R_{I\_INDEX}$	0.6000
E (°)	(360 / CPR) / 2	—

Table 10: Code Wheel Design (Continued)

Dimension	Formula	AEDR-9940A/9940ERA
F (°)	0.25 × E	—
G (mm)	—	0.04988
H (mm)	G / 2	0.02494

Code Wheel Design Example

The following example shows a code wheel design for 198 LPI at 625 CPR.

Determine R_{OP_INC}	(25.4 / 198.4375) × (625/2π) ≈ 12.7324 mm
Determine R_{OP_INDEX}	12.7324 – 1.1504 = 11.5820 mm
Determine R_{O_INC}	12.7324 + 0.60 = 13.3324 mm
Determine R_{I_INC}	12.7324 – (0.5752) = 12.1572 mm
Determine R_{O_INDEX}	11.5820 + (0.5752) = 12.1572 mm
Determine R_{I_INDEX}	11.5820 – 0.60 = 10.9820 mm
Determine W_{window} and W_{bar}	(360 / 625) / 2 = 0.288°
Determine W_{offset}	0.25 × 0.288 = 0.072°

Code Strip Design Guideline

- The incremental and index window track is a reflective surface, and the incremental bar track is opaque.
- The window width is denoted by W_{window}.
- The bar width is denoted by W_{bar}.
- All windows and bars have the same width value, E.
- There is an offset between the incremental window track and the index window track, denoted by F.

Figure 12: Code Strip Design (Not to Scale

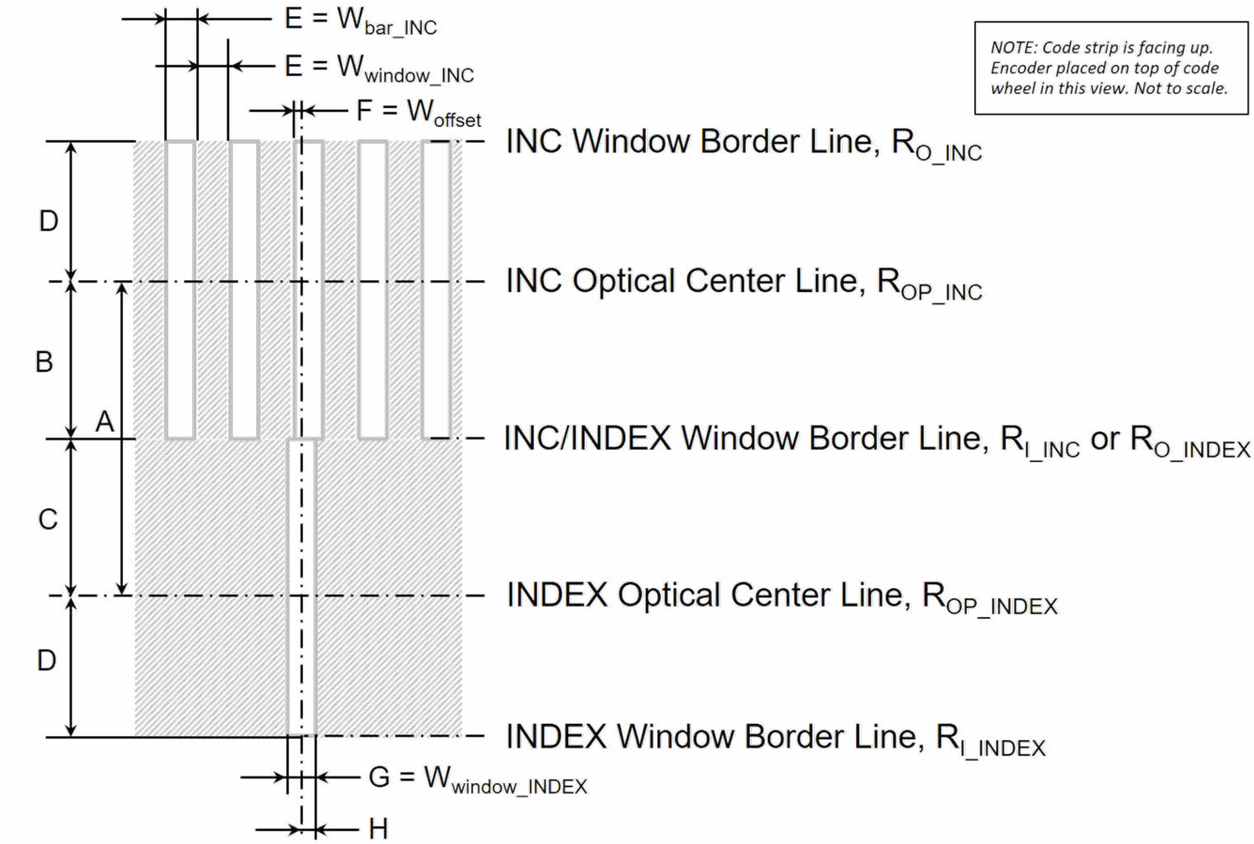


Table 11: Code Strip Design

Dimension	Formula	AEDR-9940A/9940ERA
Pitch (mm)	25.4 / LPI	0.1280
A (mm)	$R_{OP\_INC} – R_{OP\_INDEX}$	1.1504
B (mm)	$R_{OP\_INC} – R_{I\_INC}$	0.5752
C (mm)	$R_{O\_INDEX} – R_{OP\_INDEX}$	0.5752
D (mm)	$R_{O\_INC} – R_{OP\_INC}$ or $R_{OP\_INDEX} – R_{I\_INDEX}$	0.6000
E (mm)	Pitch / 2	0.0640
F (mm)	0.25 × E	0.0160
G (mm)	—	0.04988
H (mm)	G / 2	0.02494

Multiple Index Pulse Code Strip Design Guideline

Multiple Index pulses can be designed into the code wheel or code strip for pseudo absolute encoder application. The code wheel and code strip design is governed by the design guideline on the previous page.

The index pitch must be a multiplier of the incremental pitch. The multiplier must be an integer that is greater than or equal to N, refer to Table 12.

Figure 13: Code Wheel Design for Pseudo Absolute Encoder Application (Not to Scale)

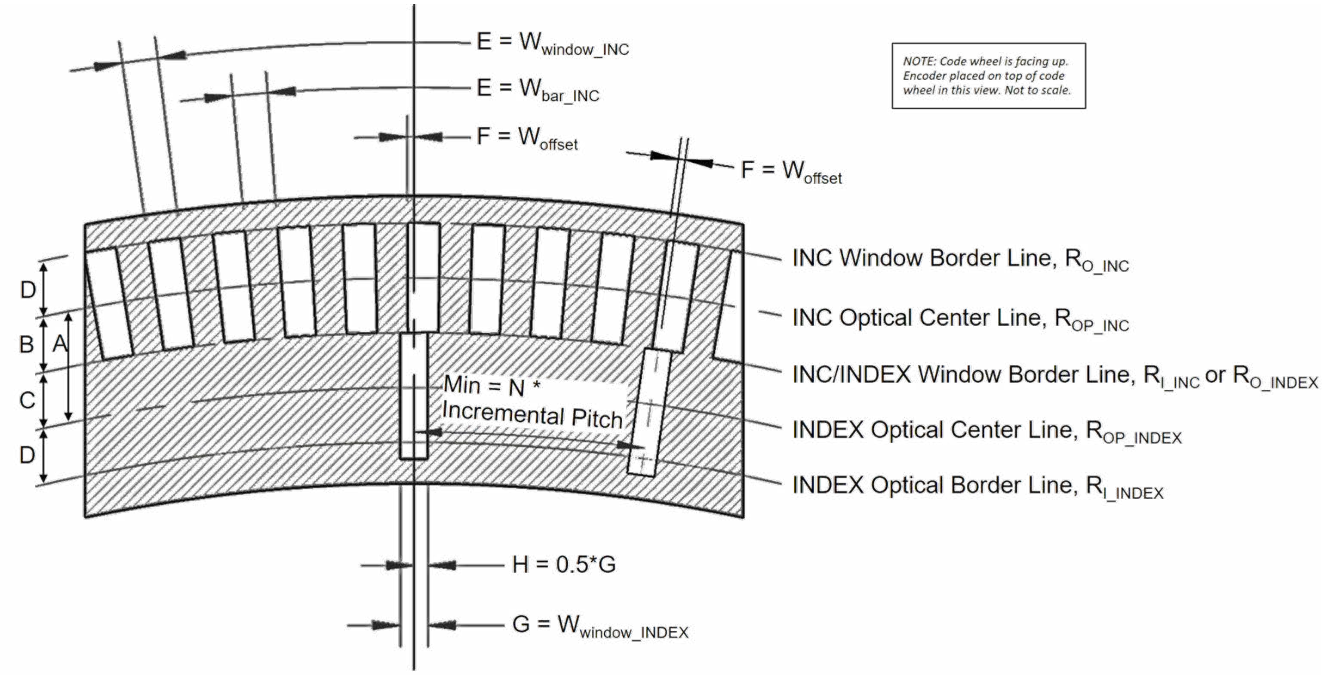


Figure 14: Code Strip Design for Pseudo Absolute Encoder Application (Not to Scale)

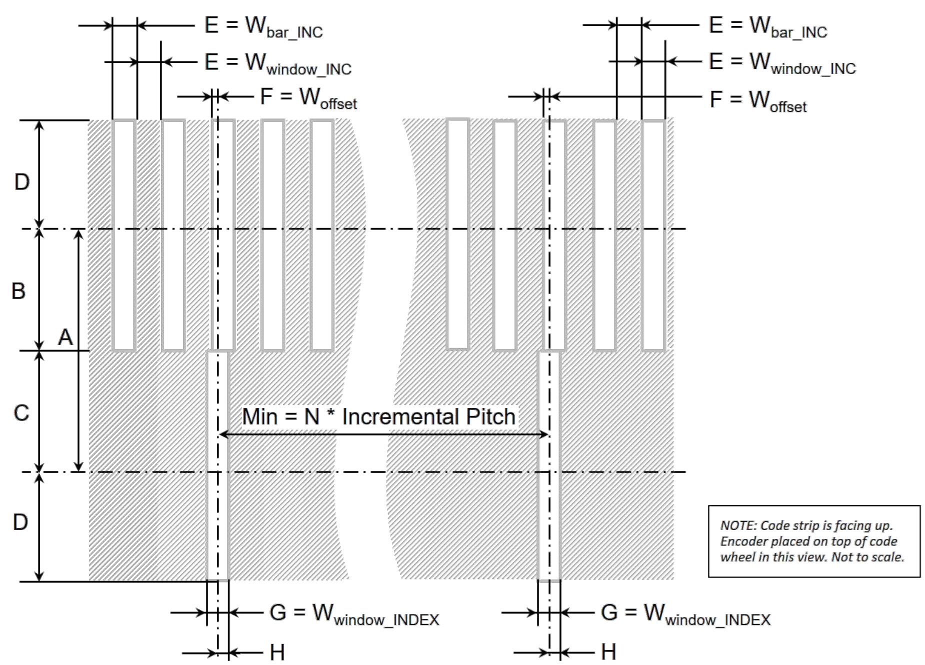


Table 12: Multiplier for Index Pitch in Pseudo Absolute Encoder Application

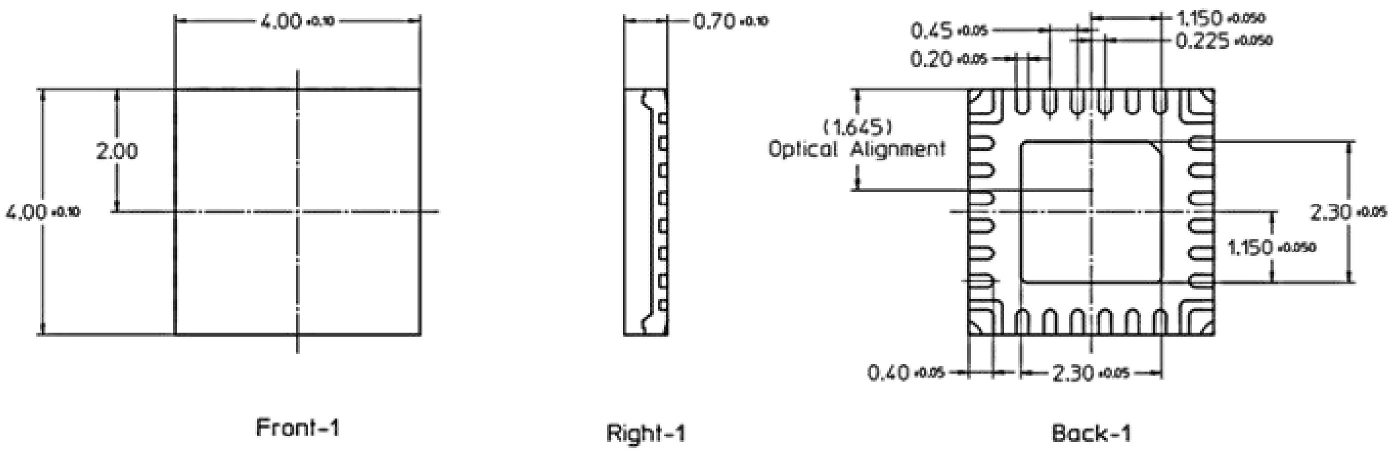
Application	Integer N
Linear application	4
Rotary application, CPR $\geq$ 512	4

Table 12: Multiplier for Index Pitch in Pseudo Absolute Encoder Application (Continued)

Application	Integer N
Rotary application, 200 ≤ CPR < 512	5
Rotary application, 128 ≤ CPR < 00	6

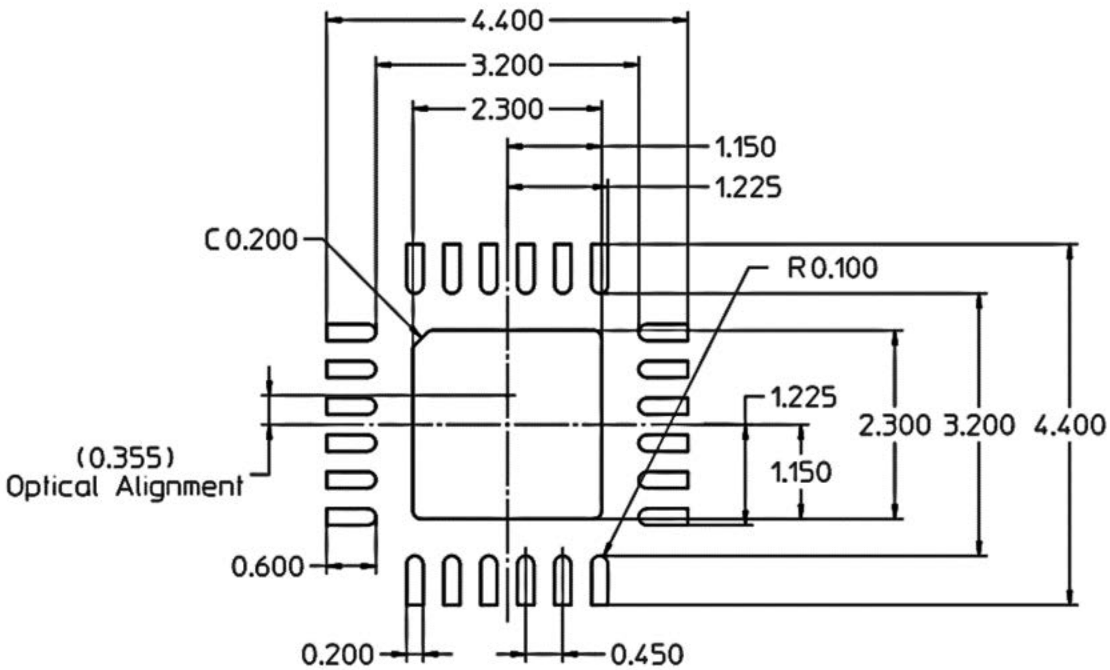
Package Outline Drawing

Figure 15: AEDR-9940A/9940ERA Package Outline



Recommended PCB Land Pattern

Figure 16: PCB Land Pattern for AEDR-9940A/9940ERA



All dimensions are in mm with a tolerance of ±0.05 mm.

Encoder Placement Orientation, Position, and Direction of Movement

The AEDR-9940A/9940ERA is designed with both the emitter and detector die placed in parallel to the code wheel window and bar orientation. The encoder package mounted on top facing down onto code wheel. When properly aligned, the emitter will sit in the middle of the incremental track and the index track.

The optical center of the encoder package must be aligned tangential to the code wheel's R_{OP}. The optimal gap setting recommended is 1.35 mm, with the range of 0.85 mm to 2.35 mm, based on 625 CPR.

Channel A leads Channel B when the code wheel rotates counterclockwise, and Channel B leads Channel A when the code wheel rotates clockwise.

Figure 17: Top View of the AEDR-9940A/9940ERA with Respect to Code Wheel Positioning

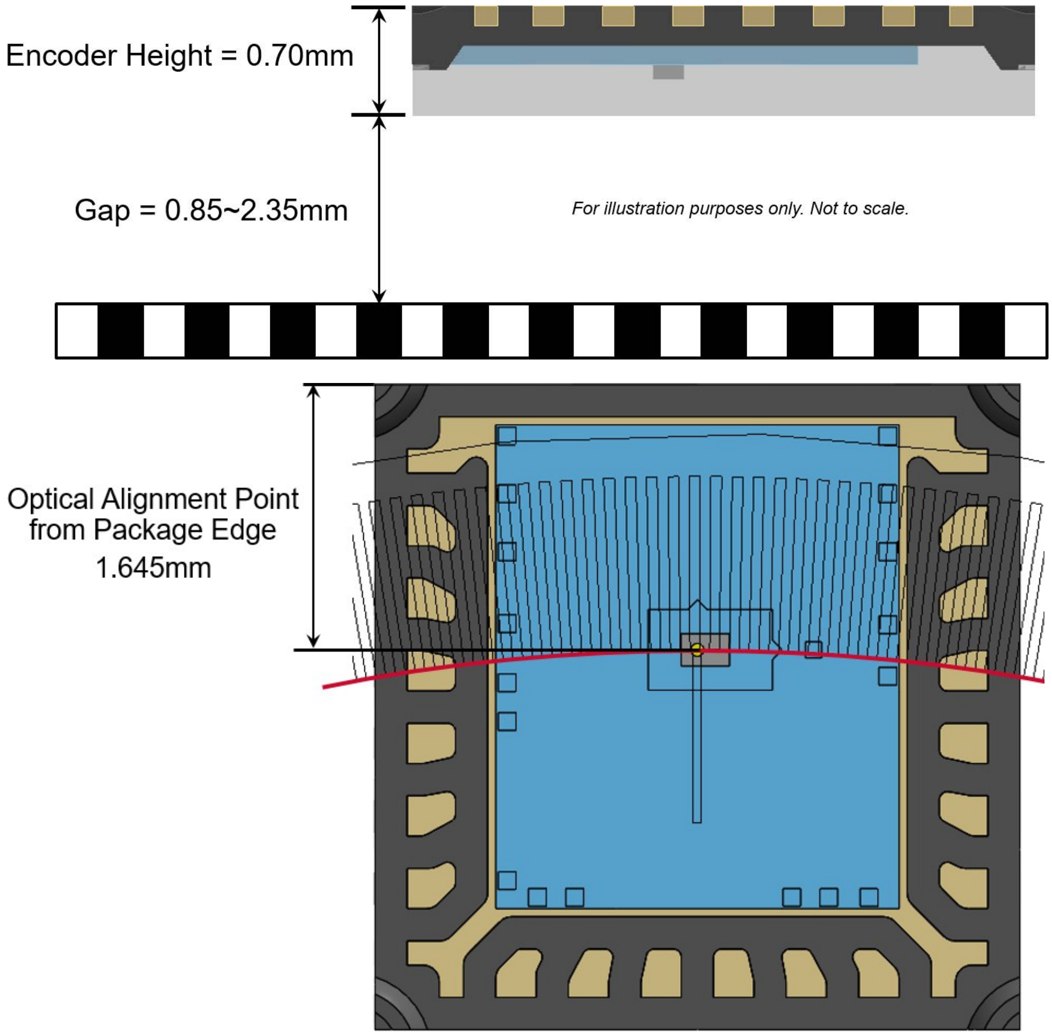
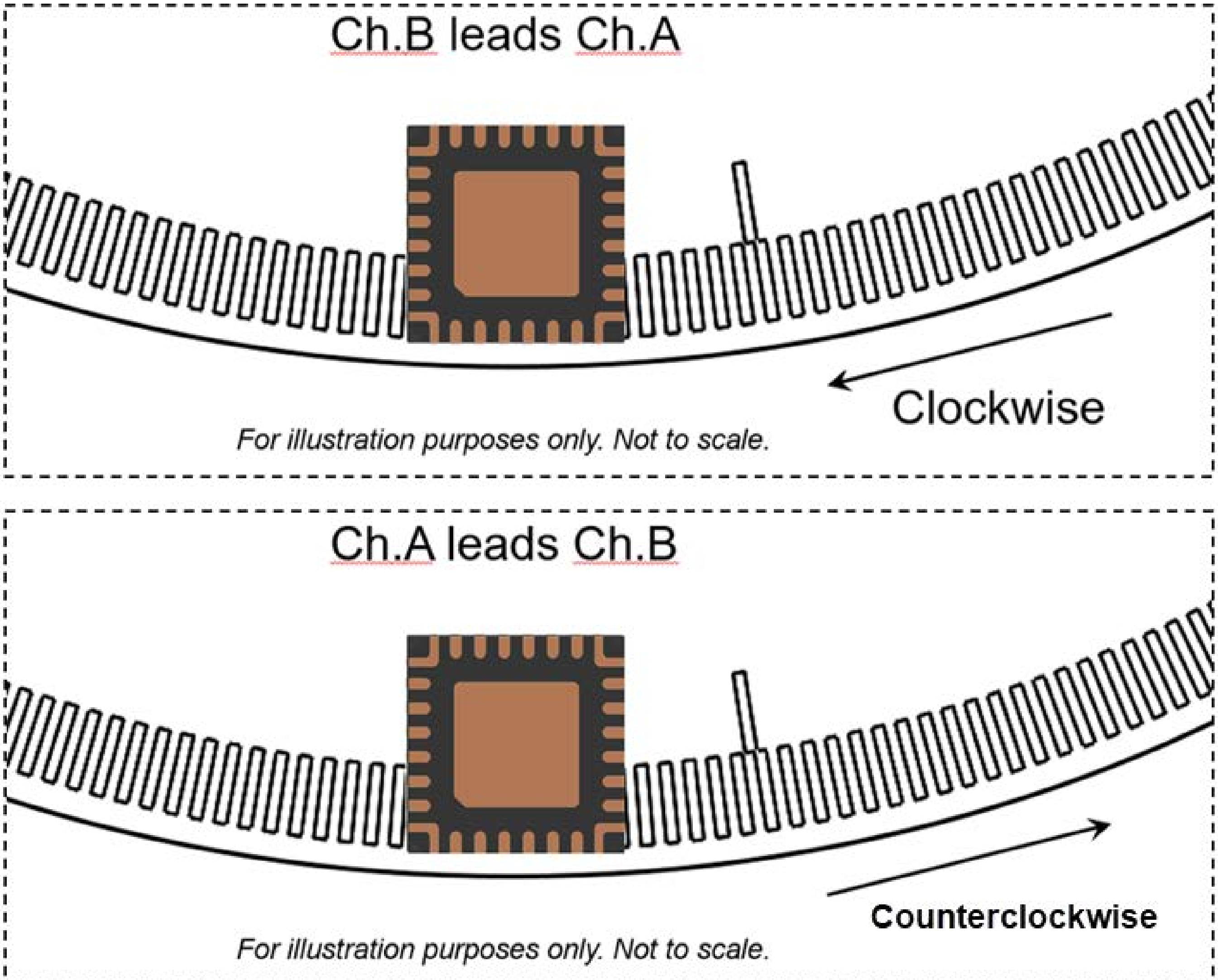


Figure 18: Channel A and Channel B Signal Output Sequence with Respect to Code Wheel Rotational Direction



Moisture Sensitivity Level

The AEDR-9940A/9940ERA package is qualified for moisture sensitive level 3 (MSL 3). Precaution is required to handle this moisture sensitive product to ensure the reliability of the product.

Storage before Use

- The unopened moisture barrier bag (MBB) can be stored at < 40°C and < 90% RH for 12 months.
- Open the MBB just prior to assembly.

Control after Opening the MBB

The encoder ASIC that will be subjected to reflow solder must mounted within 168 hours of exposure to factory conditions of < 30°C and < 60% RH.

Control for the Unfinished Reel

Stored and sealed MBB with desiccant or desiccators at < 5% RH condition.

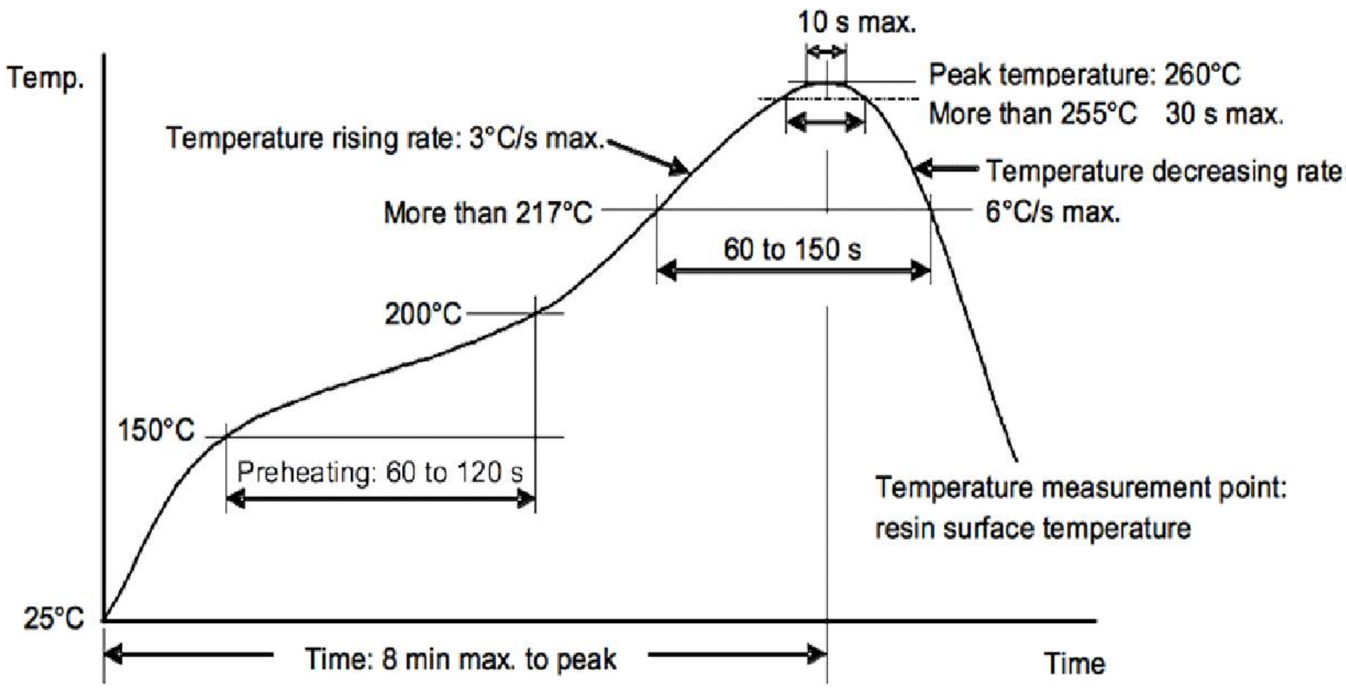
Requirements for Baking

- The humidity indicator card (HIC) is > 10% when read at 23°C ±5°C.
- The encoder floor life exceeded 168 hours after opening the moisture barrier bag.

Recommended Baking Condition

- 60°C ±5°C for 20 hours (in tape and reel) or 125°C ±5°C for 8 hours (loose units).

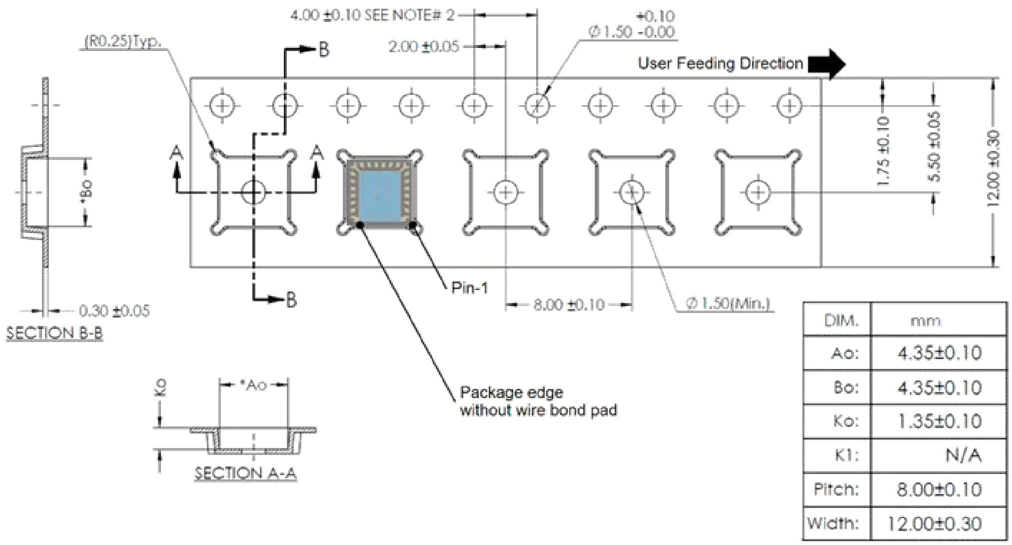
Figure 19: Typical Lead-Free Solder Reflow Profile



CAUTION! Use care when handling the encoder ASIC. It is a sensitive optical device.

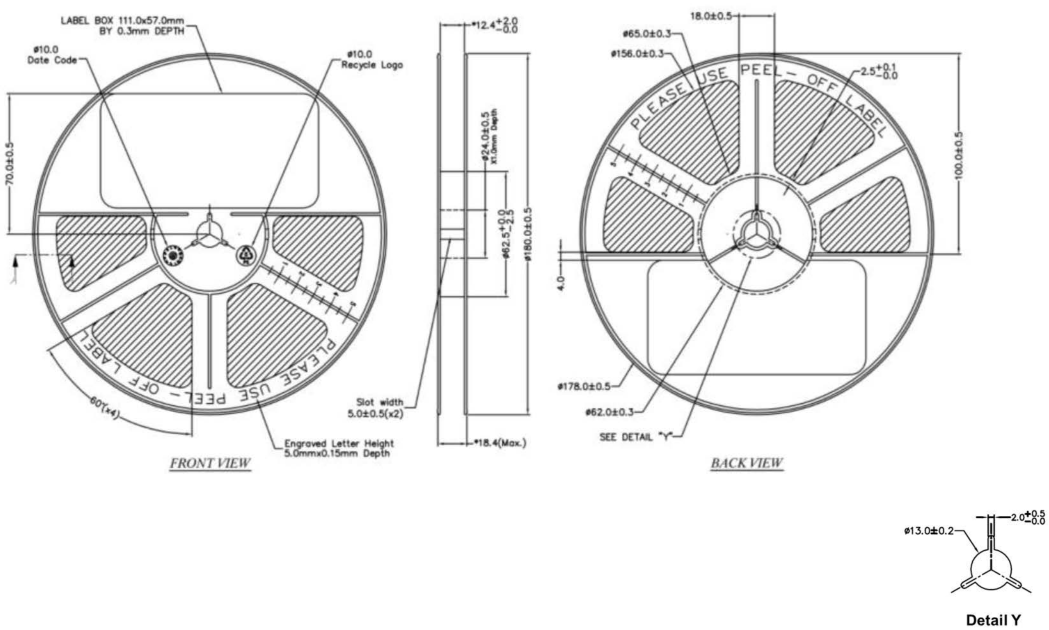
Tape and Reel Information

Figure 20: AEDR-9940A/9940ERA Carrier Tape Dimensions



DIM.	mm
Ao:	4.35±0.10
Bo:	4.35±0.10
Ko:	1.35±0.10
K1:	N/A
Pitch:	8.00±0.10
Width:	12.00±0.30

Figure 21: AEDR-9940A/9940ERA Reel Dimensions and Orientation



Ordering Information

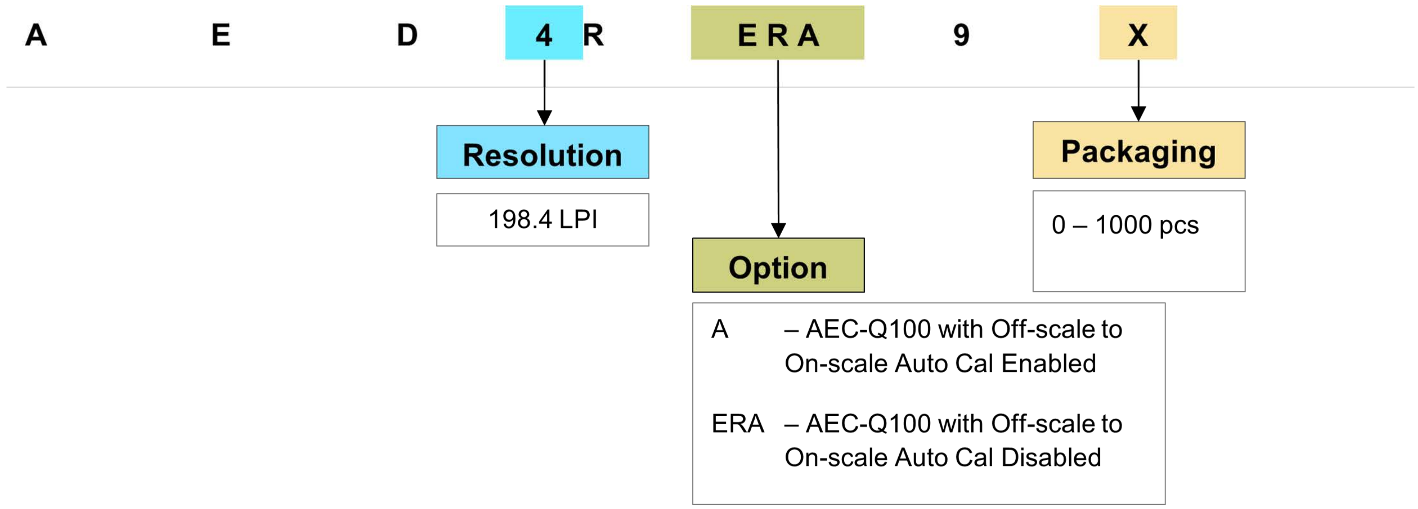


Table 13: Relevant Part Numbers Ordering Information

Ordering information	Type
AEDR-9940A-100	198.4 LPI rotary incremental encoder, 1000 pcs, AEC-Q100
AEDR-9940A-102	198.4 LPI rotary incremental encoder, 100 pcs, AEC-Q100
AEDR-9940ERA-100	198.4 LPI incremental encoder autocal with off-scale to on-scale auto cal disabled, 1000pcs, AEC-Q100
AEDR-9940ERA-102	198.4 LPI incremental encoder autocal with off-scale to on-scale auto cal disabled, 100pcs, AEC-Q100
HEDS-9940EVB	AEDR-9940 evaluation board with two units of code wheel multiple optical radius 256, 400, 512, 720 CPR base
HEDS-9940EVB1	AEDR-9940 evaluation board with two units of code wheel multiple optical radius 200, 360, 500, 625 CPR base
HEDS-9940EVBL	AEDR-9940 evaluation board with two units of code strip, 128 μm pitch
HEDS-9940EREVB	AEDR-9940ER evaluation board with two units of code wheel, multiple optical radius 200, 360, 500, 625 CPR base
HEDS-9940ER1EVB	AEDR-9940ER evaluation board with two units of code wheel, multiple optical radius 256, 400, 512, 720 CPR base
HEDS-9940ERLEVB	AEDR-9940ER evaluation board with two units of code strip, 128 μm pitch
HEDS-9940PRGEVB1	SPI programming kit with evaluation board bundling with two units of code wheel multiple optical radius 200, 360, 500, 625 CPR base
HEDS-9940PRGEVB	SPI programming kit with evaluation board bundling, two units of code wheel multiple optical radius 256, 400, 512, 720 CPR base
HEDS-9940PRGEVBL	SPI programming kit with evaluation board bundling, two units of code strip 128 μm pitch

NOTE: Select part number AEDR-9940ERA if the application does not need the off-scale to on-scale autocalibration.