Application Note

AEAT-9988M

Magnetic Encoder IC: High-Resolution 23-Bit Absolute Incremental Encoder

Description

The Broadcom® AEAT-9988M is an angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation. It is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

This sophisticated system uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A dual-track magnet generates the necessary magnetic fields by rotating perpendicularly. A wide range of selection is available on the magnet ring sizes, from 20-mm to 50-mm inner diameter.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and reprogrammable resolution from 16 bits to 23 bits. When selected, its absolute positioning data is then represented in its digital form to be assessed through a standard SSI, SPI, BiSS-C, or RS-485 communication protocol.

The AEAT-9988M also has a built-in multi-turn counter with battery backup power-off mode operation. The multi-turn resolution is programmable from 10 bits to 16 bits.

Users can choose to receive the absolute angle position in PWM-encoded output signals. The incremental positions are transmitted on ABI and UVW signals with wide user-configurable resolution from 1 CPR to 65,536 CPR of ABI signals and pole pairs from 1 to 64 pole pairs (2 to 128 poles) for UVW commutation signals.

Operation Mode

The AEAT-9988M features two types of operational modes: normal operation mode and configuration mode.

Normal Operation Mode

Normal mode is the normal operating mode of the chip. The absolute output (16-bit to 23-bit absolute position data) is available through the serial protocol pin (Port A).

The incremental positions are indicated on ABI and UVW signals with user-configurable CPR from 1 to 65,536 of ABI signals and pole pairs from 1 to 64 (2 to 128 poles) for UVW commutation signals.

Configuration Mode

The AEAT-9988M has a built-in memory for multiple-time programming (MTP).

Programming of the AEAT-9988M can be performed with the HEDS-9988PRGEVB programming kit or any tester or programmer device using the guidelines provided.

Absolute and Incremental Programming

The absolute resolution can be set to 16, 17, 18, 19, 20, 21, 22, or 23 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI, BiSS-C, and RS-485 protocols. Writing specific commands to specific addresses of the internal registers will program values of shadow registers to memory. The memory can be programmed multiple times.

Memory Map

The AEAT-9988M uses nonvolatile EEPROM as shown in the tables that follow. The memory is separated into 12 pages with 8 bits per address.

Nonvolatile Register (EEPROM)

MTP shadow registers are volatile registers that are loaded with corresponding MTP values after power-on.

All bits are in LOCK mode by default after power-on. To enter UNLOCK mode, write 0xAB to address 0x00.

In UNLOCK mode, you may write to any registers. Values written will remain until power-off.

The UNLOCK state is maintained until the power supply is turned off or any value (except 0xAB) is written to address 0x00.

MTP Shadow Registers

MTP shadow registers are volatile (upon power-up, the value are reloaded from EEPROM) and are not automatically written to EEPROM.

To write MTP shadow registers values to EEPROM (nonvolatile) memory, see EEPROM Programming.

The MTP shadow registers will be from address 0x00 to address 0x7E.

Customer Configuration Registers

The following registers are available for users to store information and configure the encoder as required.

Table 1: Customer Configuration Registers

Addr (Hex)	Bit							
	7	6	5	4	3	2	1	0
0x00	track_cnt[7:0]							
0x01	DIR	MT_Select[2:0]				ST_Select[2:0]		
0x02	Temp Max Limit Offset[7:0]							
0x03	Temp Offset[7:0]							
0x04	Temperature Limit[7:0]							
0x05	Temperature output[7:0]							
0x06	ST_ZR[23:16]							
0x07	ST_ZR[15:8]							
0x08	ST_ZR[7:0]							
0x09	index_mult[7:0]							
0x0A		I_Polarity	Iwidth_Select[1:0]		Iphase_Select[1:0]		abi_ini	ABI_CPR[16]
0x0B	ABI_CPR[15:8]							
0x0C	ABI_CPR[7:0]							
0x0D	uvw_ini	UVW_Select[6:0]						
0x0E	pwm_ini				pwm_select[3:0]			
0x0F	SE_Slew_SEL[1:0]				LD_Slew_SEL[1:0]		LD_Drive_SEL[1:0]	
0x10	GPIO0_cfg[7:0]							
0x11	GPIO1_cfg[7:0]							
0x12	GPIO2_cfg[7:0]							
0x13	gpio_abi_stat	eep_srst	eep_size [2:0]			eep_psize[2:0]		
0x14	Lissajous Upper Limit1[7:0]							

Table 1: Customer Configuration Registers

Addr (Hex)	Bit 7	6	5	4	3	2	1	0
0x15	Lissajous Lower Limit1[7:0]							
0x16	Lissajous Upper Limit2[7:0]							
0x17	Lissajous Lower Limit2[7:0]							
0x18	digital filter[7:0]							
0x19	cal filter[7:0]							
0x1A	hys2_on	arc_en	acc2.1_en	acc2.2_en	sleep[3:0]			
0x1B	RS485 encoder ID[7:0]							
0x1C	RS485 Setting[7:0]							
0x1D	RS485 Setting[7:0]							
0x1E	ssi2_ring	ssi3_config	ssi_temp	ssi_alm	ssi_crc	ssi2_to_flex	alm_sel	
0x1F	spi4_cfg		spi4_crc_init[1:0]					
0x20	Alarm Enable[31:0]							
0x21								
0x22								
0x23								
0x24	Alarm Latch Enable[31:0]							
0x25								
0x26								
0x27								
0x28	Warning Mask[31:0]							
0x29								
0x2A								
0x2B								
0x2C	Error Mask[31:0]							
0x2D								
0x2E								
0x2F								
0x30	sync_offset							
0x31		H3_H2_H1			h1_sign	sync_dir	dpc2_dir	
0x32					hysterisis_setting[3:0]			
0x35	zero_latency					fixed_delay[10:8]		
0x36	fixed_delay[7:0]							

Table 2: Customer Configuration Registers Descriptions

Registers	Description
track_cnt	Magnet multi-pole pair (PP) count
DIR	Counting direction selection
MT_Select	Multi-turn output resolution
ST_Select	Absolute output resolution selection
Temp Max Limit Offset	Temperature maximum limit offset
Temp Offset	Temperature offset setting

Table 2: Customer Configuration Registers Descriptions

Registers	Description
ST_ZR	Single-turn zero rest value via register: ■ ST_ZR [23:16] - MSB bit-23 to bit-16 of absolute single-turn ■ ST_ZR [15:8] - Bit-15 to bit-8 of absolute single-turn ■ ST_ZR [7:0] - LSB bit-7 to bit-0 of absolute single-turn
index_mult	Index-multi setting
I_Polarity	Index-polarity setting
Iwidth_Select	Index-width setting
Iphase_Select	Index-phase setting
abi_ini	ABI output off state
ABI_CPR	ABI count per revolution (CPR) setting
uvw_ini	UVW output off state
UVW_Select	UVW number of pole pair setting
pwm_ini	PWM output off state
pwm_select	PWM output mode
SE_Slew_SEL	Single-ended slew rate
LD_Slew_SEL	Line driver slew rate
LD_Drive_SEL	Differential line driver driveability control
GPIO0_cfg	GPI Input/Output configuration
GPIO1_cfg	GPI Input/Output configuration
GPIO2_cfg	GPI Input/Output configuration
gpio_abi_stat	Programmable GPIO - ABI output function
eep_srst	External EEPROM - soft reset
eep_size	External EEPROM - memory size
eep_psize	External EEPROM - page size
Lissajous Upper Limit1	Lissajous upper limit for single-pole track
Lissajous Lower Limit1	Lissajous lower limit for single-pole track
Lissajous Upper Limit2	Lissajous upper limit for multi-pole track
Lissajous Lower Limit2	Lissajous lower limit for multi-pole track
digital filter	Filter / averaging setting
cal filter	Calibration filter setting
hys2_on	Absolute hysteresis
arc_en	Accuracy correction enable - single-pole + multi-pole
acc2.1_en	Accuracy correction enable - single-pole
acc2.2_en	Accuracy correction enable - multi-pole
sleep	Wake-up time selection
RS485 encoder ID	Encoder ID for RS-485
RS485 Setting	Setting for RS-485
ssi2_ring	SSI2 mode selection
ssi3_config	SSI3 mode selection
ssi_temp	SSI temperature output enable
ssi_alm	SSI alarm format / size
ssi_crc	SSI check type selection
ssi2_to_flex	SSI2 monoflop time

Table 2: Customer Configuration Registers Descriptions

Registers	Description
alm_sel	SSI 8-bit alarm format
spi4_cfg	SPI4 format/mode configuration
spi4_crc_init	SPI4 CRC init
Alarm Enable	Alarm bit enable
Alarm Latch Enable	Alarm latch enable
Warning Mask	Warning bit masking
Error Mask	Error bit masking
sync_offset	single-pole-multi-pole offset synchronization
Pole_length	Pole length selection
h1_sign	First harmonic sign multi-pole from single-pole
sync_dir	Direction of synchronization
dpc2_dir	Direction of dynamic phase correction of multi-pole
hysterisis_setting	Incremental hysteresis setting
zero_latency	Zero latency / prediction enable
fixed_delay	Static latency delay to be compensated

Table 3: Customer Command Registers

Address	bit							
[hex]	7	6	5	4	3	2	1	0
00	EEPROM Unlock L1 [AB'h]							
01	EEPROM Program [C0'h]							
02					ZR Clear	Alarm Clear	ZR Calibrate	MT Clear
04						Auto-All Clear		Auto-All Calibrate
0E						GPO2_EXT	GPO1_EXT	GPO0_EXT
21	Chip Ready	EEPROM Err	CRC Err					
24	Alarm[31:24]							
25	Alarm[23:16]							
26	Alarm[15:8]							
27	Alarm[7:0]							
28		PCode Status			ZR Status [1:0]		Auto-All Status [1:0]	
2B	Chip ID [42'h]							
2C	temp_data[7:0]							
70	Pcode [55:0]							
71								
72								
73								
74								
75								
76								
77	Pcode OTP [BA'h]							
7F	EEPROM Page							

Table 4: Customer Command Registers Descriptions

Registers	Description
EEPROM Unlock L1	EERPOM unlock level 1
EEPROM Program	Program the EEPROM page
ZR Clear	Single-turn zero reset clear
Alarm Clear	Clear all alarms
ZR Calibrate	Single-turn zero reset calibrate
MT Clear	Multi-turn clear
Auto-All Clear	Auto-all clear for signal conditioning and linearization offset
Auto-All Calibrate	Auto-all calibration for signal conditioning and linearization offset
GPO2_EXT	State control for GPIO2 [when GPIO2 set as GPO_EXT]
GPO1_EXT	State control for GPIO1 [when GPIO1 set as GPO_EXT]
GPO0_EXT	State control for GPIO0 [when GPIO0 set as GPO_EXT]
Chip Ready	Status of chip [ready when is 1]
EEPROM Err	EEPROM error status
CRC Err	CRC error for EEPROM
Alarm [31:0]	Alarm status
Pcode Status	EERPOM user passcode status
ZR Status [1:0]	Zero reset status [1=Done, 0=Error]
Auto-All Status [1:0]	Auto-all status [1=Done, 0=Error]
Chip ID	ID of the chip
Pcode [55:0]	EEPROM user passcode
Pcode OTP	EEPROM user passcode one-time programming
EEPROM Page	EEPROM page no selection

EEPROM Passcode (Level 2 Memory Access)

Perform the following steps to set a memory passcode:

1. Write the value 8'h09 to address 0x7F to access the Customer Command registers.
2. Write the value 8'hAB to address 0x00 to unlock Level 1 memory access.
3. Write the desired passcode 7x8 bits to the memory address from 0x70 to 0x76.
4. Write 8'hBA to address 0x77 to set the passcode.

NOTE: The factory default passcode is h00-h00-h00-h00-h00-h00-h00.

EEPROM Unlock

Perform the following steps to unlock the MTP register:

1. Write the value 8'h09 to address 0x7F to access the Customer Command registers.
2. Write the value 8'hAB to address 0x00 to unlock Level 1 memory access.
3. Write the correct user passcode 7x8 bits to the memory address from 0x70 to 0x76 to unlock Level 2 memory access.
4. Read address 0x28 bit-6, Pcode Status, in Customer Command registers.
5. Read and write MTP registers are now accessible.

EEPROM Page

Perform the following steps to load the EEPROM page to the MTP register:

1. Perform the steps in EEPROM Unlock to unlock the EEPROM.
2. Write one of the following values to address 0x7F to load the selected EEPROM page to the MTP register:
   - 8h'07 to load the Customer Configuration register.
   - 8h'09 to load the Customer Command register.

NOTE: Upon power-up, the MTP register is loaded with the Customer Command register.

EEPROM Programming

Perform the following steps to program the MTP shadow register to EEPROM:

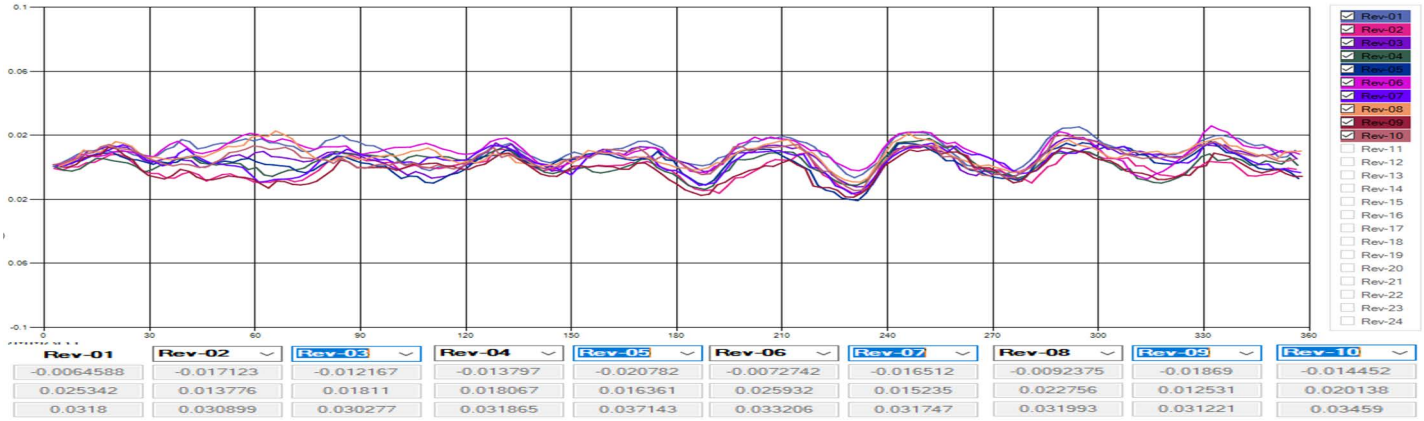
1. Write the desired values to the current MTP register (Customer Configuration / Command Shadow register).
2. Verify the written values by reading back all registers.
3. Write the value 8'h09 to address 0x7F to access the Customer Command registers.
4. Write value 8'hC0 to address 0x01 to program the current MTP registers to EEPROM.

NOTE: EEPROM programming is required if the EEPROM changes need to be retained.

Encoder Calibration

Accuracy Angle Calibration

To achieve a high degree of angle accuracy, the AEAT-9988M comes with a built-in correction algorithm. This algorithm corrects the errors upon installation of the encoder to the motor. The following figure shows the corrected accuracy after multiple rotations.



NOTE:

1. The magnet is set up with 8-pole pair with 3.34-mm pole length.
2. The motor jitter during calibration will impact the accuracy.

The calibration procedures are as follows.

Customer Command Register

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at a constant speed ranging from 100 RPM to 2000 RPM; a higher speed is recommended.
3. Once the speed stabilizes, write the value 8'h1 to address 0x04 to initiate the calibration sequence.
4. Read the calibration status on bit [1:0], address 0x28.
   - 10: Calibration pass
   - 11: Calibration fail
5. Write the value 8'h0 to address 0x04 to exit the calibration sequence.
6. The calibration value is automatically stored in memory; no further programming is required.
   - To erase the calibration value, write the value 8'h4 to address 0x04.
   - To return the operation mode, write the value 8'h0 to address 0x04.

Zero Reset Calibration

The AEAT-9988M allows users to configure a zero reset position. The following is the calibration procedure.

Customer Command Register

1. Stop the encoder to the motor system at the desired location.
2. Once it is stationary, write the value 8'h2 to address 0x02 to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2], address 0x28.
   - 10: Calibration pass
   - 11: Calibration fail
4. Write the value 8'h0 to address 0x02 to exit the calibration sequence.
5. The offset value is automatically stored in memory; no further programming is required.
   - To erase the calibration value, write the value 8'h8 to address 0x02.
   - To return to operation mode, write the value 8'h0 to address 0x02.

Magnet Design and IC Placement

Below is the recommended magnet design specification for AEAT-9988M.

Inner Ring

Properties	Details
Number of Pole Pair	1, 2, 3, 4…., 63, 64
Magnetization	Axial
Magnet Width ($Inner_{OR}$[a] – $Inner_{IR}$[b])	3.00 mm
Magnet Thickness	3.00 mm[c]
Pole Length	[~3.34, 2.60, 1.90] mm

a. The outer radius of the inner ring.

b. The inner radius of the inner ring.

c. The magnet thickness and magnet grade can be adjusted to fulfill the magnetic input field magnitude strength requirement.

Outer Ring

Properties	Details
Number of Pole Pair	1
Magnetization	Diametrical / Axial
Magnet Width ($Outer_{OR}$[a] – $Outer_{IR}$[b])	4.00 mm[c]
Magnet Thickness	3.00 mm[c]
Pole Length	n/a

a. The outer radius of the outer ring.

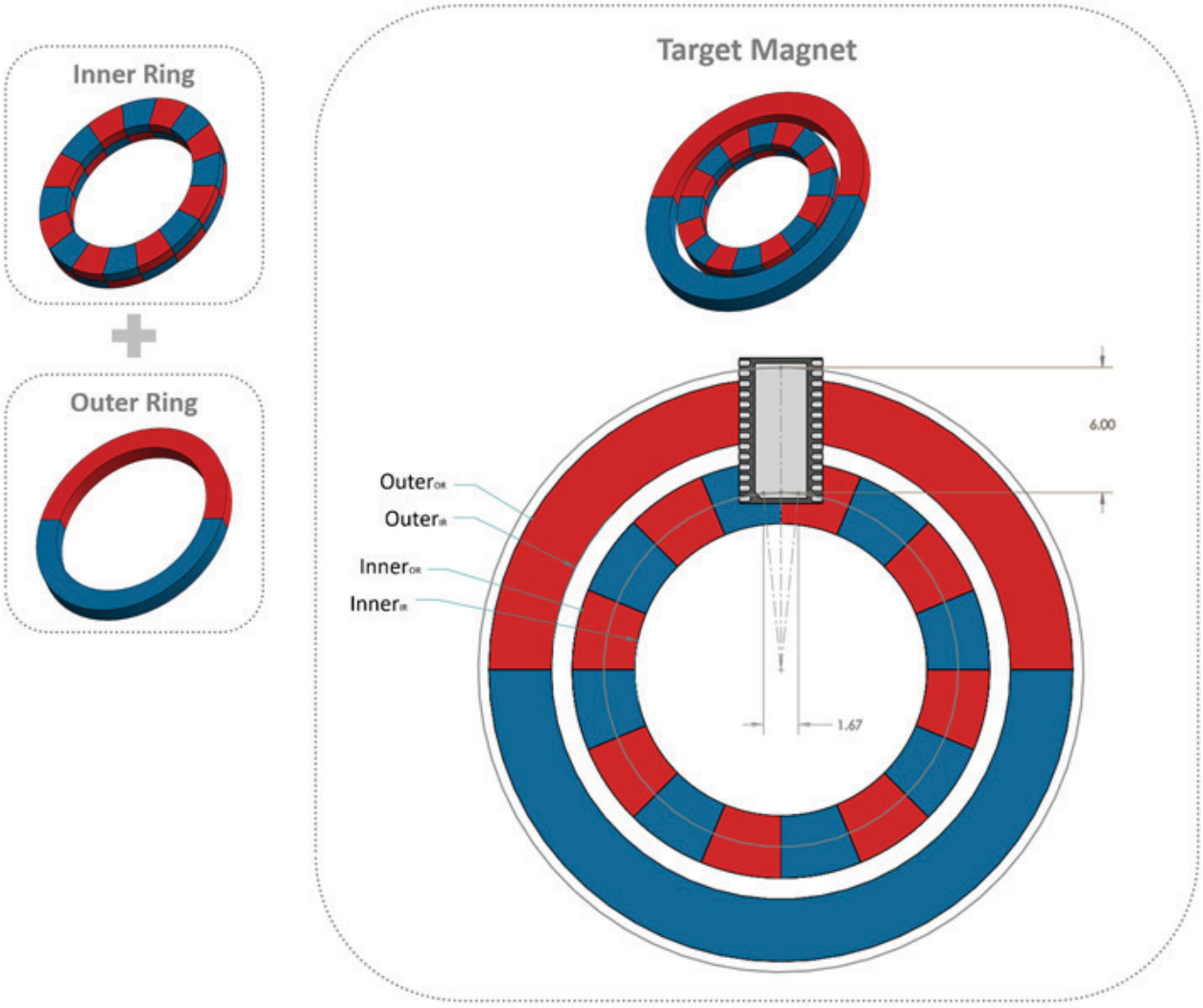
b. The inner radius of the outer ring.

c. The magnet width and thickness and magnet grade can be adjusted to fulfill the magnetic input field magnitude strength requirement.

Ring Air Gap

Air separation ($Outer_{IR}$ – $Inner_{OR}$) = 1.5 mm

Figure 1: Magnet Design and IC Placement



Battery Backup Multi-Turn Operation

The AEAT-9988M series has an integrated function to track multi-turn revolutions by employing battery backup technology.

Table 5: Operating Considerations with Battery Mode

Parameters	Conditions	Min.	Typ.	Max.	Units
Electrically Permissible Speed	In battery mode (VDDA = 0V)	—	—	3000	rpm
External Battery Supply Voltage	V_{CC} > 4.5V	—	3.6	4.5	V
	V_{CC} > 4.75V	—	3.6	4.75	V
Battery Mode Current Consumption	Tamb = 25°C	—	85	—	µA

NOTE:

1. Normal mode: Encoder operates on encoder main power supply.
2. Battery mode: Encoder operates in OFF State, while multi-turn data is tracked by battery circuitry.

External Battery

Figure 2: Recommended External Battery

Table 6: Recommended External Battery Specifications

Parameters	Specifications
Product Name	Toshiba ER6V/3.6V ER6VP
Manufacturer Part Number	ER6VP
Brand	Toshiba Ultra Lithium
Nominal Voltage	3.6V
Nominal Capacity	2000 mAh
Operating Temperature Range	–55°C ~ +85°C
Size	AA

CAUTION!

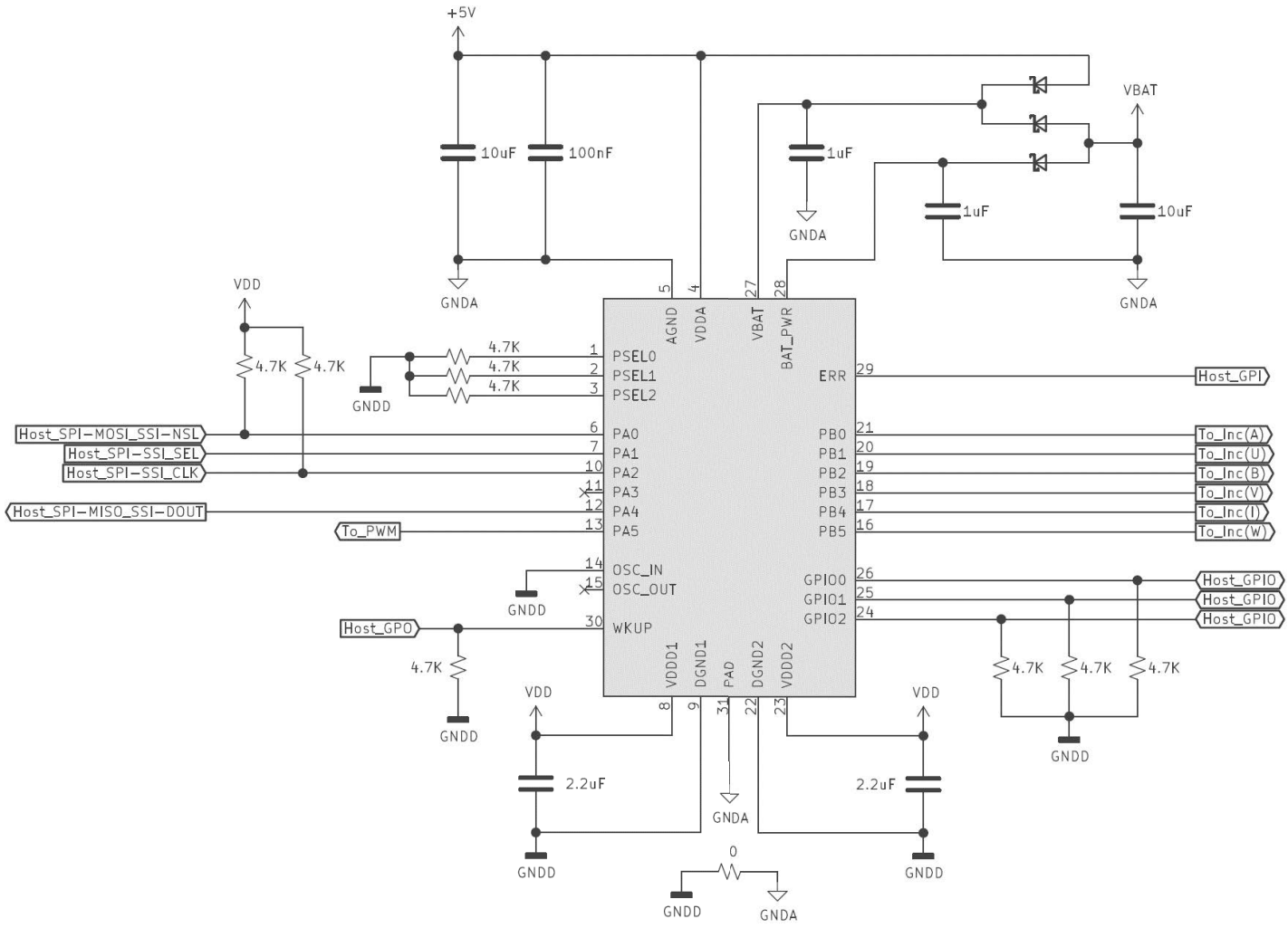
1. The multi-turn data position is maintained with battery power during battery mode. The battery replacement process will cause data loss, therefore the multi-turn counter must be reset after every battery change.
2. The battery life calculation depends on user application conditions.

Recommended Operation Circuit

Absolute and Incremental (PSEL = 000’b)

Absolute: SPI3 and SSI, Single-Ended

Incremental: ABI and UVW, Single-Ended



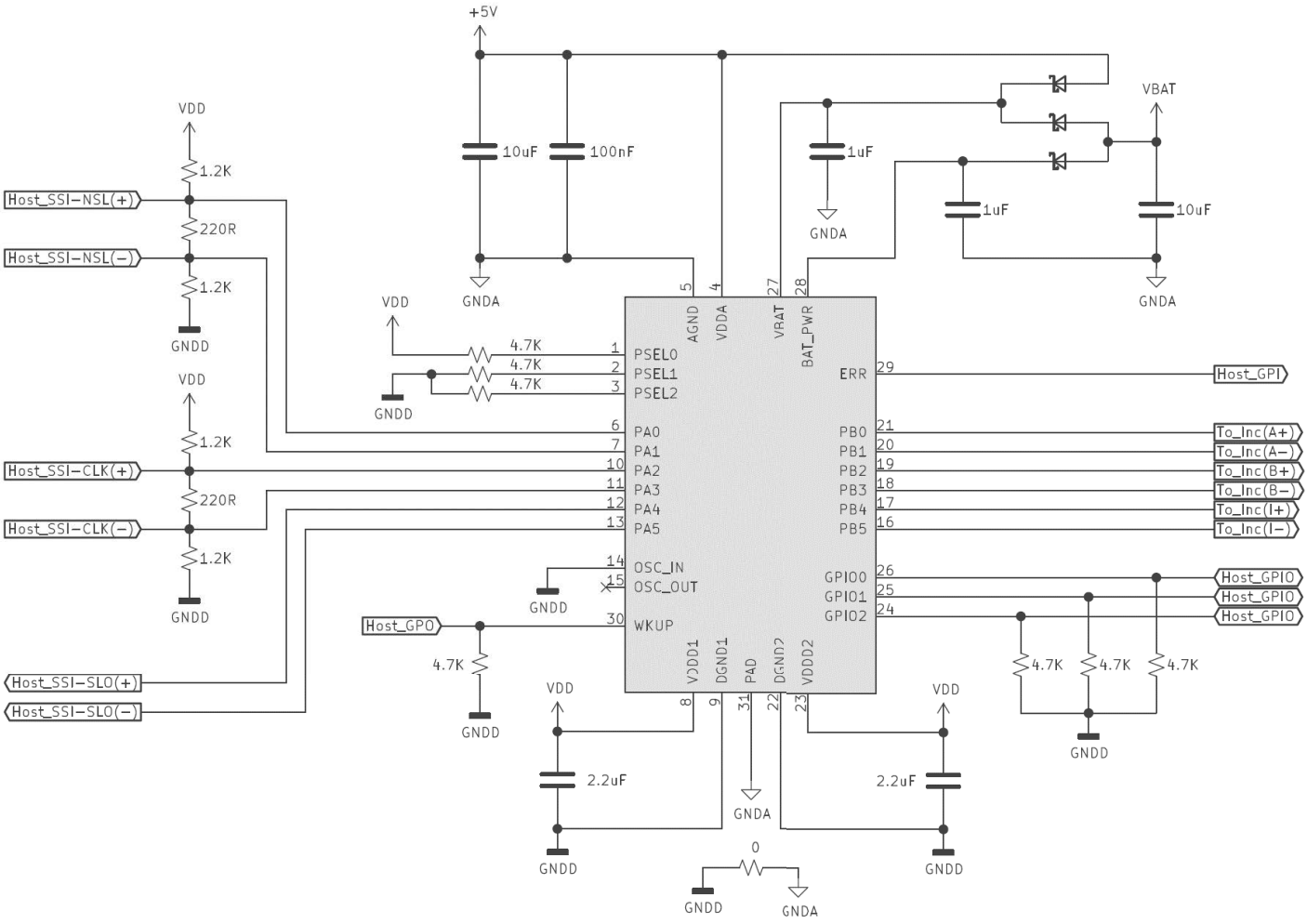
NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G

Absolute and Incremental (PSEL = 001’b)

Absolute: SSI3 Differential with Line Driver

Incremental: ABI Differential with Line Driver



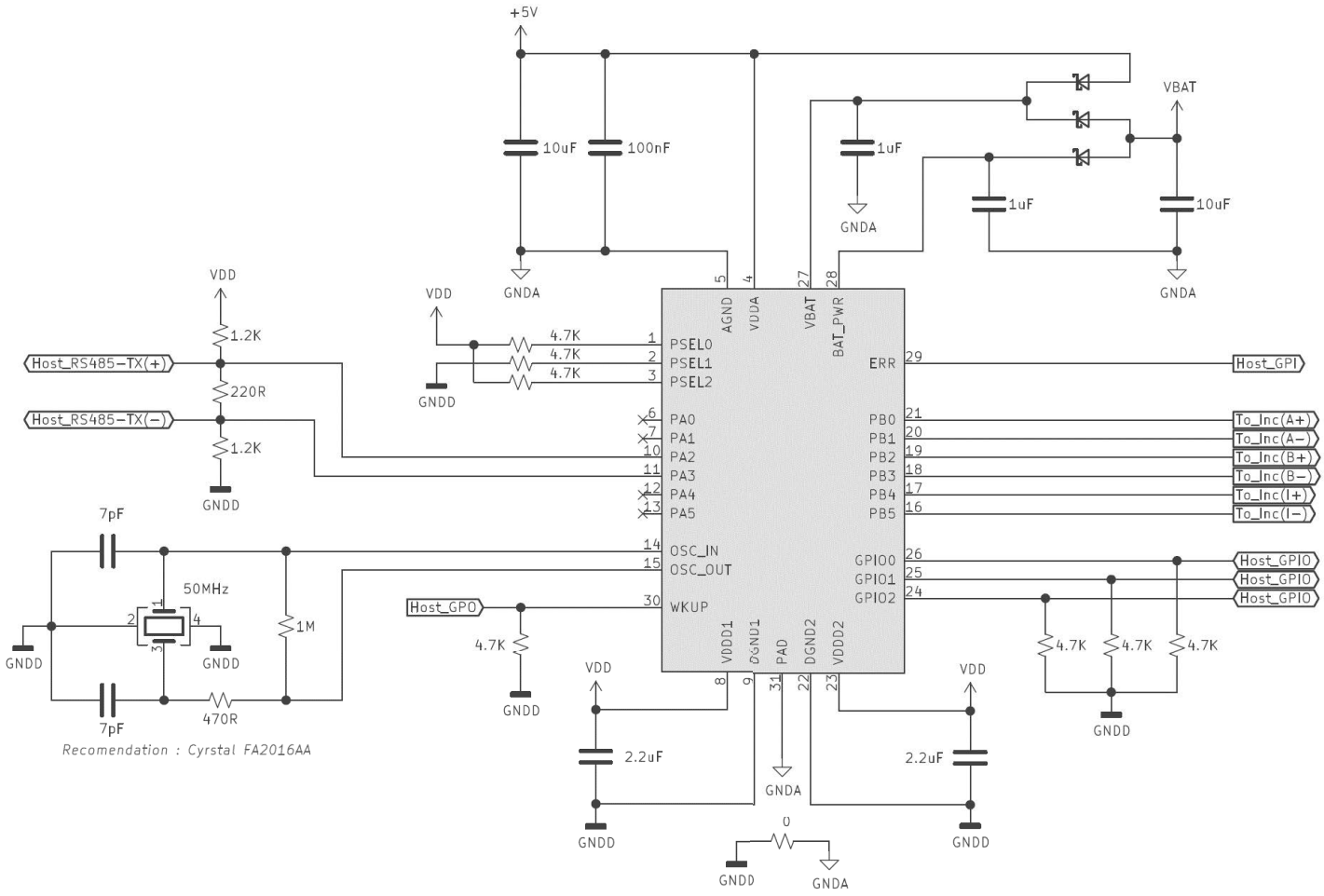
NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G

Absolute and Incremental (PSEL = 101’b)

Absolute: RS-485 Differential with Line Driver

Incremental: ABI Differential with Line Driver



NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G
- Crystal Clock: Manufacturer: Epson, Part Number: FA2016AA 50.000000MHz

Communication Protocol

Serial Interface Format

The AEAT-9988M serial interface hosts up to 10 different communication interfaces for position output and memory access. The protocol is configurable with the PSEL pin (2 to 0). The output pin can be configured to high impedance mode for multi-client connection or bus connection.

The AEAT-9988M has two communications ports, Port A and Port B:

- Port A communication supports both Single Ended (SE) and Differential with Line Driver (LD) modes, ensuring compatibility across various systems. This versatility extends to its SPI capabilities accommodating SPI3 and SPI4 (16-bit parity and 8-bit Operation Command [OC]) functionalities. Additionally, it facilitates SSI via SSI3 and SSI2. Beyond these standard interfaces, Port-Com in Port A configuration integrates seamlessly with other protocols including BiSS-C, RS-485, PWM, and UVW.
- Port B configuration is for incremental configuration. When operating in Single Ended mode, it is able to support simultaneous ABI and UVW output. Transitioning to Differential with Line Driver mode, Port B ensures ABI output in a differential format.

All protocol selections can be switched during operation.

Table 7: MATS Table

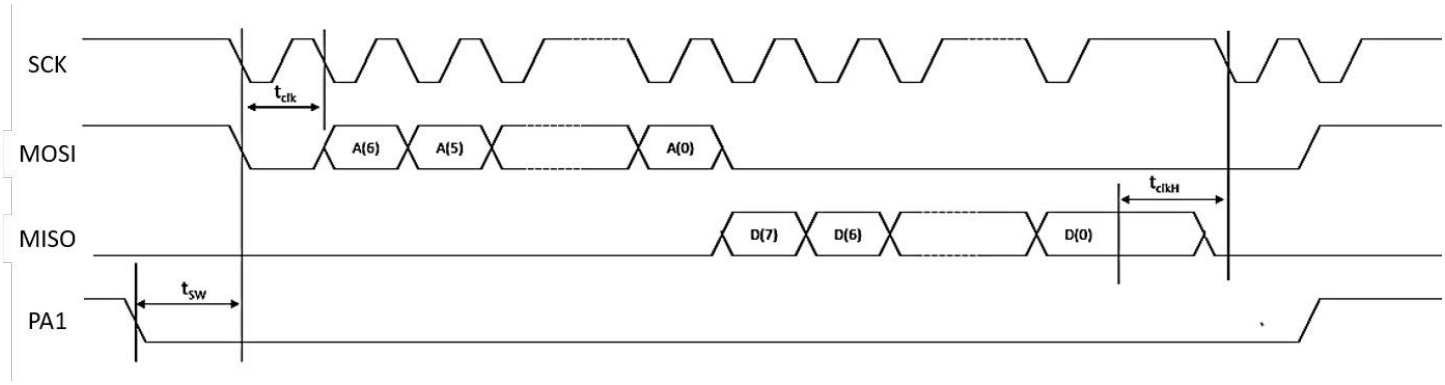
Port Configurator									
PSEL2	0	0	0	0	0	1	1	1	1
PSEL1	0	0	0	1	1	0	0	1	1
PSEL0	0	0	1	0	1	0	1	0	1
Port Assignment									
	SPI3	**SSI**	**SSI**	**BiSS-C**	**BiSS-C**	**RS-485**	**RS-485**	**SPI4**	**UVW/PWM**
	SE	**SE**	**LD**	**SE**	**LD**	**SE**	**LD**	**SE**	**LD**
PA0	MOSI	NSL	NSL+	SLI	SLI+	RX		MOSI	U+
PA1	0	1	NSL–		SLI–			NCS	U–
PA2	SCK	SCK	SCL+	MA	MA+	TX	D+	SCK	V+
PA3			SCL–		MA–		D–		V–
PA4	MISO	SOUT	SLO+	SLO	SLO+	CTS		MISO	W+
PA5	PWM	PWM	SLO–		SLO–	PWM		PWM	W–
PB0	A	A	A+	A	A+	A	A+	A	A+
PB1	U	U	A–	U	A–	U	A–	U	A–
PB2	B	B	B+	B	B+	B	B+	B	B+
PB3	V	V	B–	V	B–	V	B–	V	B–
PB4	I	I	I+	I	I+	I	I+	I	I+
PB5	W	W	I–	W	I–	W	I–	W	I–

NOTE:

- To activate the SPI3 SE protocol, assert 0 on the PA1.
- To activate the SSI SE protocol, assert 1 on the PA1.
- The protocol switch wait time is 2 ms.

Serial Peripheral Interface (SPI3)

Figure 3: SPI3 Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between PA1 falling edge and CLK rising edge	2	—	—	ms
t_{clk}	Serial clock period	1000	—	—	ns
t_{clkH}	CLK high time after end of last clock period	300	—	—	ns

NOTE: Read back the data to confirm it has been written successfully.

Figure 4: SPI3 Read

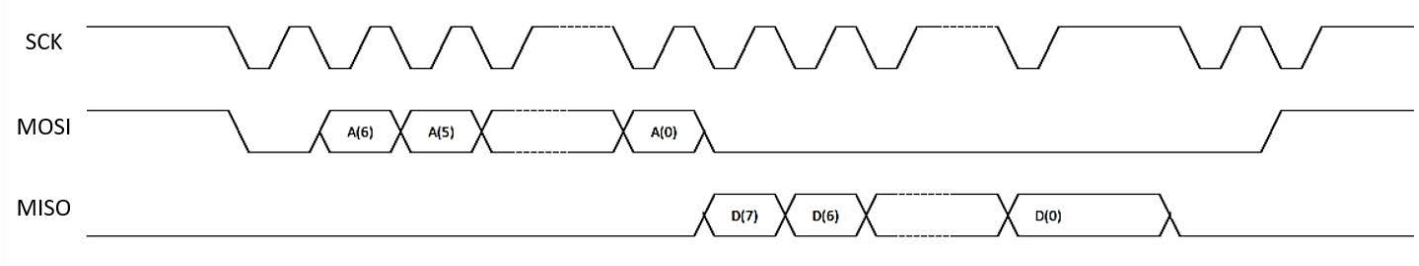
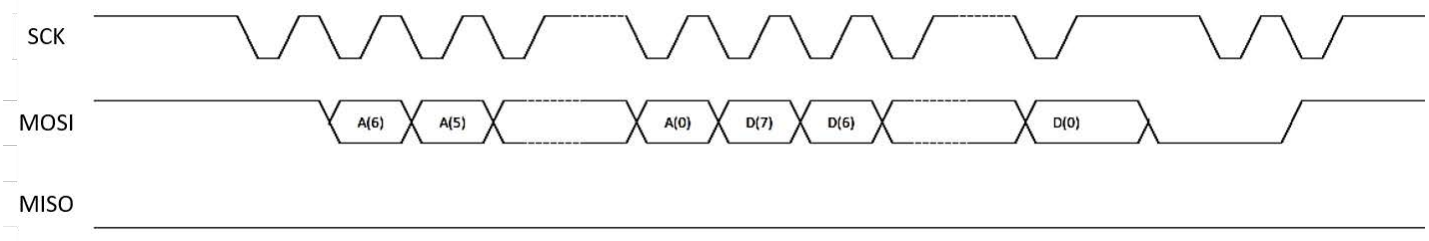
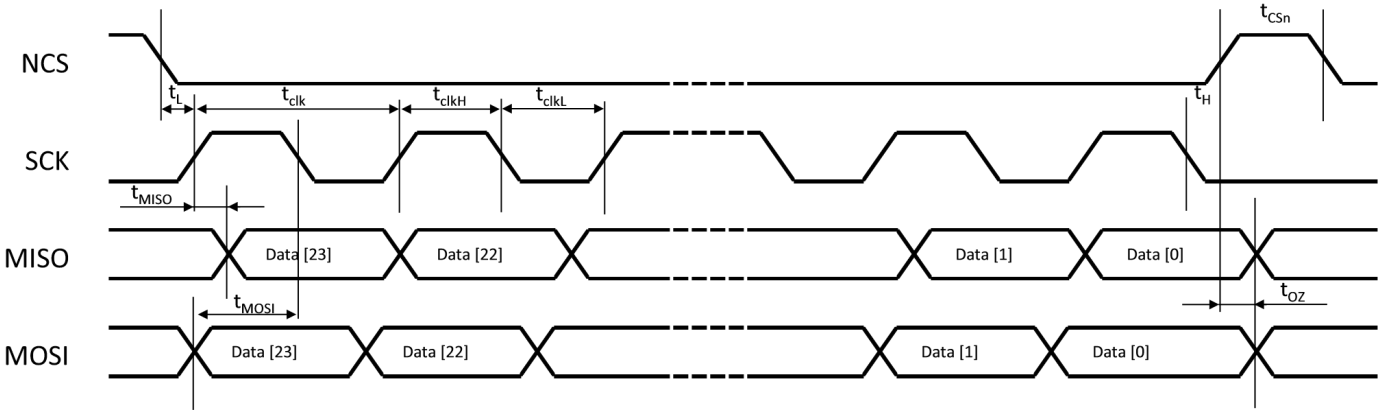


Figure 5: SPI3 Write



Serial Peripheral Interface (SPI4)

Figure 6: SPI4 Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between the SCn falling edge and the CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	50	—	—	ns
t_{clkL}	Low period of the serial clock	25	—	—	ns
t_{clkH}	High period of the serial clock	25	—	—	ns
t_H	Time between the last falling edge of CLK and the rising edge of CSn	$t_{clk}/2$	—	—	ns
t_{CSn}	High time of CS between two transmission	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	CLK edge to data output valid	—	—	51	ns
t_{OZ}	Time between CSn rising edge and MISO HiZ	—	—	10	ns

NOTE: Read back the data to confirm it has been written successfully.

SPI4 Command and Data Frame

Figure 7: SPI4 Read Sequence

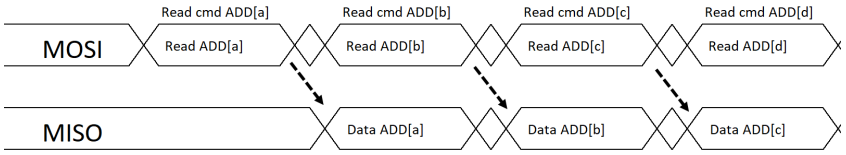
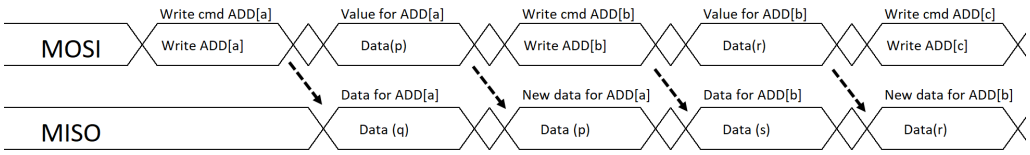
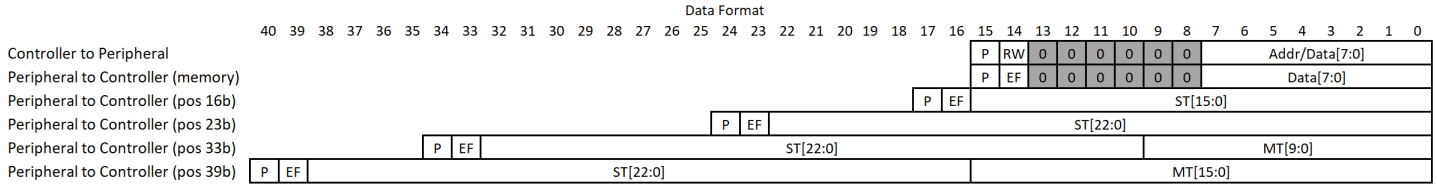


Figure 8: SPI4 Write Sequence



SPI4 16-bit (Parity)

To configure the chip to the SPI4 16-bit selection, set spi4_cfg = 0 in the register setting (Customer Configuration register address 0x1F, bit 7).

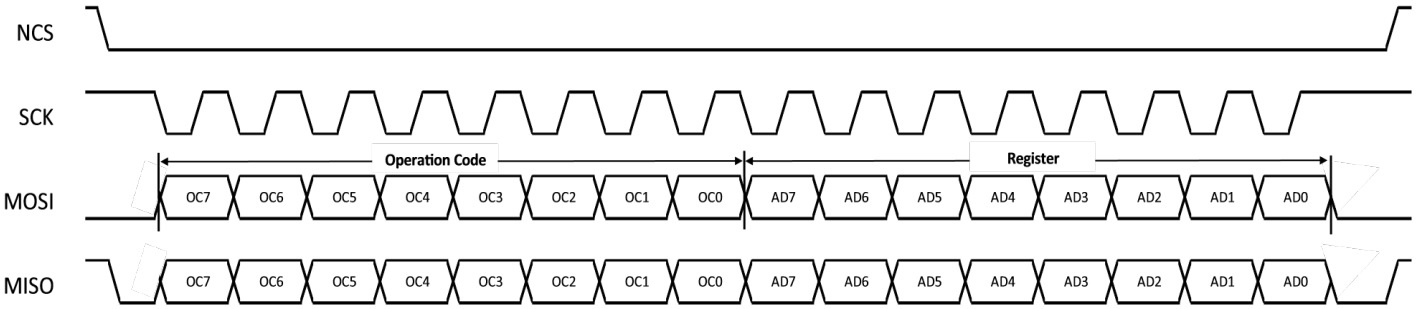


NOTE:

- P: Parity
- EF: Error Flag
- RW: Read = 1, Write = 0

SPI4 8-bit

By default, the chip is configured to the SPI4 8-bit selection, set spi4_cfg = 1 in the register setting (Customer Configuration register address 0x1F, bit 7).

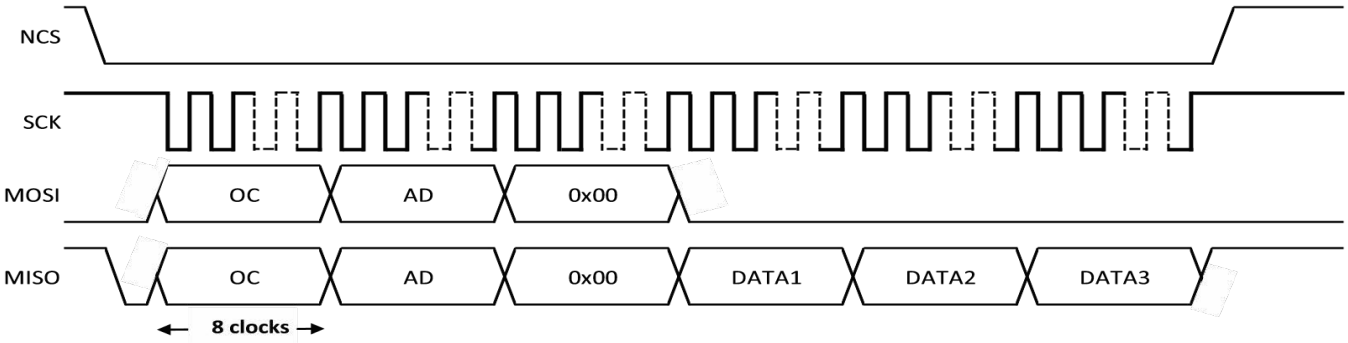


NOTE:

- When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.
- The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over a specific operation command (OC).

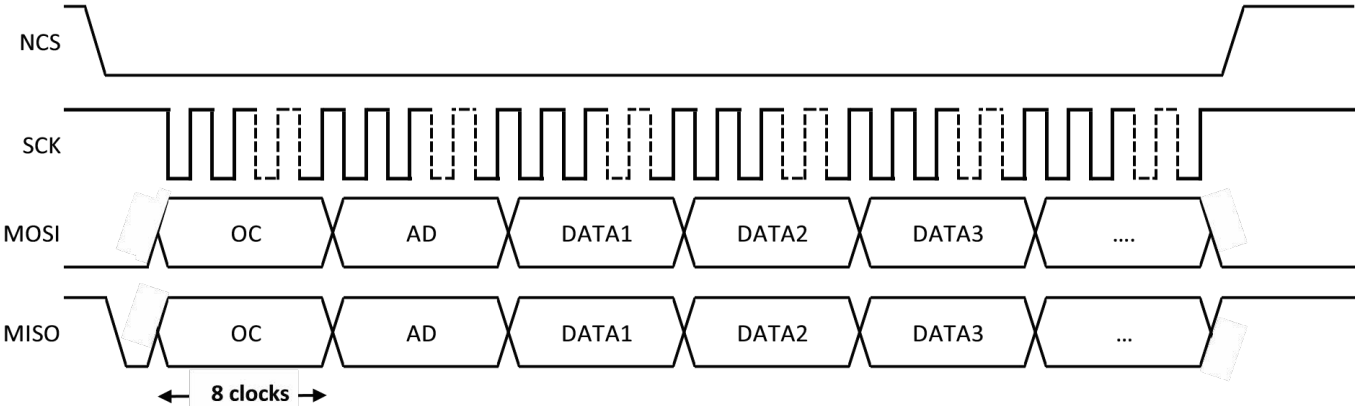
Register Read (OC = 0x81'h)

This operation is used to read data from the internal register of the chip. It can be performed consecutively starting from any register address. The data continues to be transmitted as long the clock (SCK) is sent and the chip select (NCS) remains active.



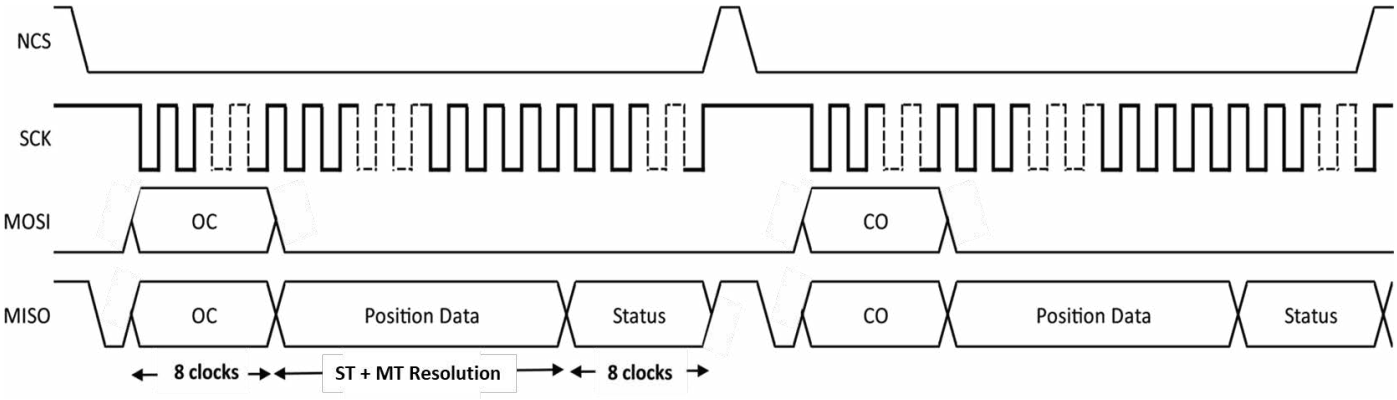
Register Write (OC = 0xCF'h)

This operation is used to write data into the internal register of the chip. It can be performed consecutively starting from any register address. The subsequent data byte is written into the next register address (AD+1), while the NCS signal stays active. Complete written data is transmitted back via MISO.



Position Read (OC = 0xA6'h)

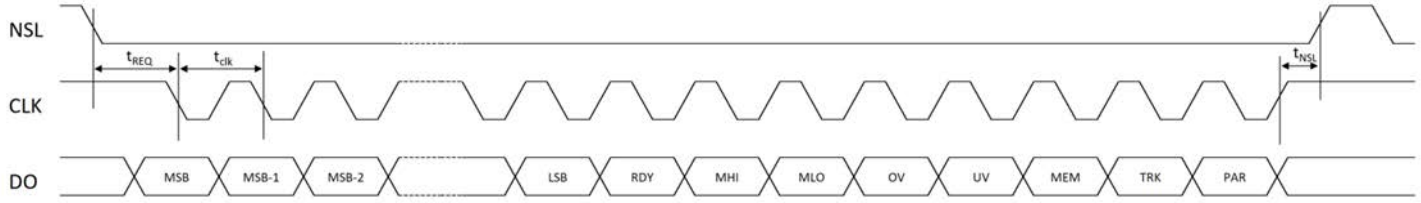
Read the absolute position by sending the operation command, and the data will be transmitted on the MISO line. The position data consists of the multi-turn and single-turn position data length and status byte. The position data length follows the multi-turn and single-turn resolution setting.



Serial Synchronous Interface 3-Wire (SSI3)

It is available in two options per ssi3_config register setting.

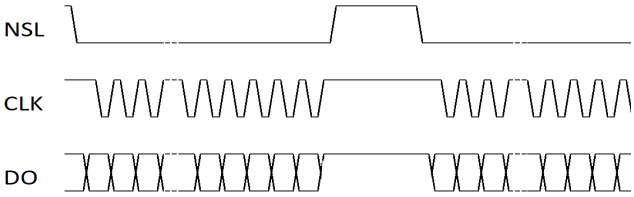
Figure 9: SSI Protocol Timing. Default: Data Output with 3-Wire SSI to 10-MHz Clock Rates



Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	SSI_SPI_SEL switch time	100	—	—	ns
t_{REQ}	SCL high time between the NLS falling edge and the first SCL falling edge	300	—	—	ns
t_{NSLH}	NSL high time between two successive SSI reads	200	—	—	ns

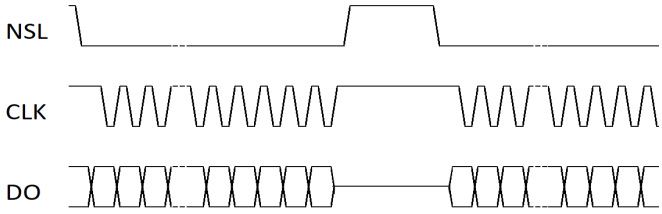
SSI-3(A)

By default, the chip is configured to the SSI-3(A) selection, ssi3_config = 0 in the register setting (Customer Configuration register address 0x1E, bit 6). The D0 pin is held at a high state once the NSL pin is high.

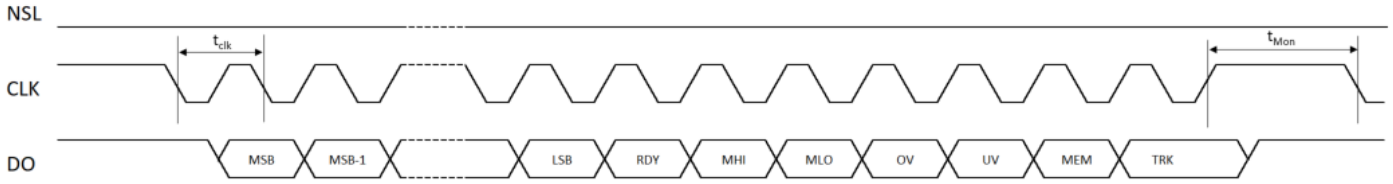


SSI-3(B)

To configure the chip to the SSI-3(B) selection, set ssi3_config = 1 in the register setting (Customer Configuration register address 0x1E, bit 6). The D0 pin is at a tristate (high-impedance) state once the NSL pin is high.



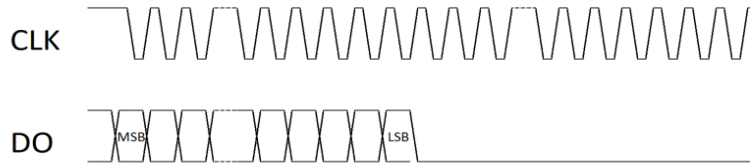
Serial Synchronous Interface 2-Wire (SSI2)



Symbol	Description	Min.	Typ.	Max.	Unit
t_{Clk}	NSL low time after the rising edge of the last clock period for an SSI read	250	—	$t_M/2$	ns
t_M	NSL high time between two successive SSI reads	—	16.5	18.0	µs

SSI-2(A)

By default, the chip is configured to the SSI-2(A) selection, ssi2_ring = 0 in the register setting (Customer Configuration register address 0x1E, bit 7). Output is a single data position and remains low after LSB until the next monoflop (t_M) expires.

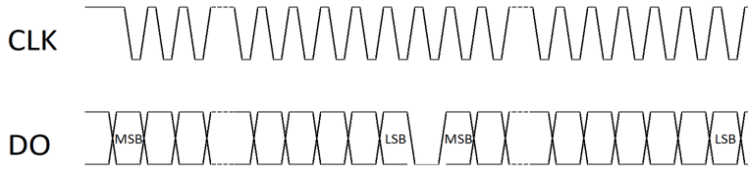


SSI-2(B)

To configure the chip to the SSI-2(B) selection, set ssi2_ring = 1 in the register setting (Customer Configuration register address 0x1E, bit 7).

The same position data can be continuously output by sending clock train, and the data is separated by a single low pulse.

Data will be refreshed when the next monoflop (t_M) expires.



SSI READ Data Format

Protocol	Type			Frame Structure				
	Temp.	Alarm	Check					
SSI	0	0	0	MT[0:16]	ST[16:23]	(nERR+nWRN)[2]	CRC[6]	
	0	0	1	MT[0:16]	ST[16:23]	(nERR+nWRN)[2]	PAR[1]	
	0	1	0	MT[0:16]	ST[16:23]	nALARM[8]	CRC[6]	
	0	1	1	MT[0:16]	ST[16:23]	nALARM[8]	PAR[1]	
	1	0	0	MT[0:16]	ST[16:23]	TEMP[8]	(nERR+nWRN)[2]	CRC[6]
	1	0	1	MT[0:16]	ST[16:23]	TEMP[8]	(nERR+nWRN)[2]	PAR[1]
	1	1	0	MT[0:16]	ST[16:23]	TEMP[8]	nALARM[8]	CRC[6]
	1	1	1	MT[0:16]	ST[16:23]	TEMP[8]	nALARM[8]	PAR[1]

Table 8: Alarm 8-bit Selection (Use by nALRM for SSI)

ALARM Selection	bit							
	7	6	5	4	3	2	1	0
ST Only	MHI	MLO	TRACK	TEMP	MEM	OV	UV	0
Full (MT + ST)	BA	BE	MT_Track XC	TEMP	OV UV	Track MHI MLO	MEM BB_Cfg	OVS OVF

BiSS-C Full Duplex Serial Communication Protocol

Table 9: General Specification of BiSS-C Serial Communication

Interface	Symbol	Recommended Circuit
Serial Clock	MA or SCLK	Transmitter (P/N: ISL3295E) or equivalent
Serial Data Output	SLO or DAT	Receiver (P/N: ISL3283E) or equivalent

Table 10: BiSS-C Timing Characteristics

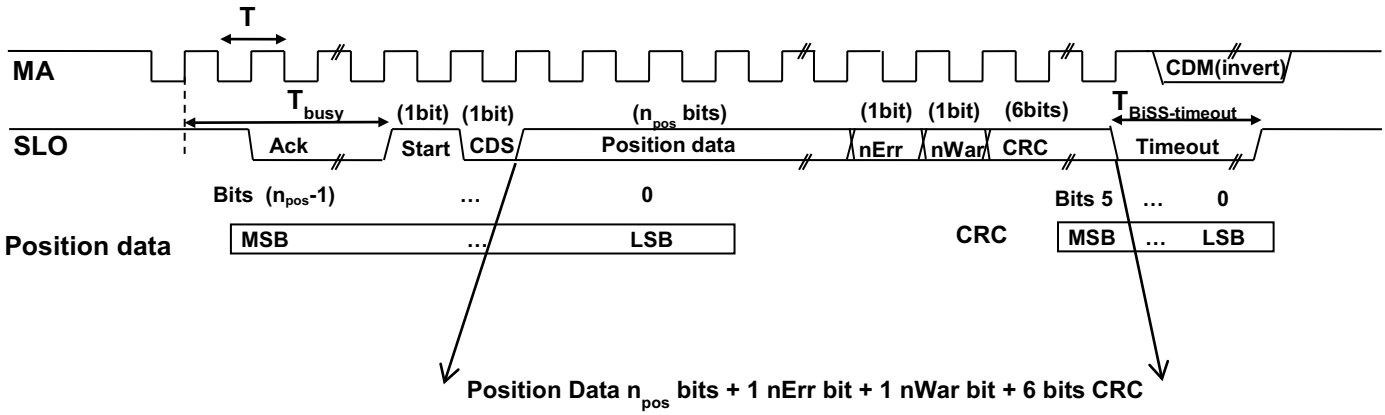
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units	Notes
MA Frequency	f_{MA}	—	0.08	—	10	MHz	
MA Duty	DUT_{CLK}	—	—	50	—	%	
Busy	T_{busy}	5 MHz < f_{MA} ≤ 10 MHz	—	$3/f_{MA}$	—	µs	a
		100 kHz ≤ f_{MA} ≤ 5 MHz	—	$2/f_{MA}$	—		
Timeout	$t_{BiSS\text{-}timeout}$	—	$1.5/f_{MA}$		5	µs	a
Frame to Frame	—	—	—	—	1	µs	
Encoder Initialization Time	—	—		20		ms	

a. Refer to Figure 10 for the timing description.

Table 11: BiSS-C Data Field

MT[15:0]	ST[22:0]	Error[0]	Warning[0]	CRC[5:0]

Figure 10: BiSS-C Interface Timing Diagram



NOTE:

1. CRC Polynomial = Invert of ($X^6 + X^1 + X^0$)
2. nErr bit is active low. Combine all the Error Status and reflect in nErr bit.
3. nWar bit is active low. Combine all the Warning Status and reflect in nWar bit.
4. Position data varies depending on Single-turn and Multi-turn resolution.
5. Position data is latched at the first rising edge of MA.

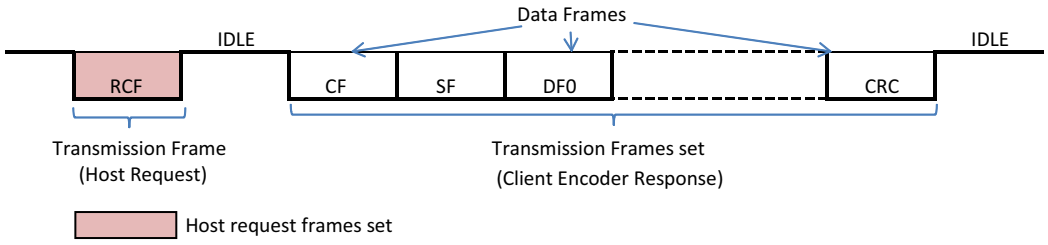
RS-485 Half-Duplex Serial Communication Protocol

Table 12: General Specification of RS-485 Serial Communication

Item	Specification	Note
Transmission Type	Differential transceiver	
Communication Type	Half duplex	Recommended transceiver: ISL8485E or equivalent
Transmission Code Type	Binary, non-zero return (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5 Mb/s, 5.0 Mb/s, and 10.0 Mb/s	
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC	CRC equation G(X) = X^8 + 1 X = CRC0 ~ CRC7

A one-to-one half-duplex serial communication is established between the host (e.g. a servo driver) and the client encoder. The communications are in a differential transmission format. The encoder will carry out specific operations based on the command requests made by the host. An acknowledgment of the command request is necessary before the encoder executes the requested operation by checking the Start Bit, Information Data Field, and Stop Bit. If this check fails, the encoder will not acknowledge and execute the received command request.

Figure 11: General Transmission Frames Format on Half-Duplex Line



NOTE:

- **Start of the Transmission Frames Set:** Upon detecting the first logic of low state 0 on the transmission line after an idling state, and if the following 3 bits conform to the sync code, the encoder will acknowledge it as a valid request control field (RCF) and indicates the start of a transmission frame set. Otherwise, the encoder will continue to search for the next available logic of low state 0.
- **End of the Transmission Frames Set:** After the command frame is detected, if there is no start bit after the end bit of the last frame read and no subsequent frame is detected, the end of transmission frame set is concluded.
- **Idle State:** Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, the logic of output in transmission line is kept to high state 1.

RS-485 Encoder Read Out Frame Sets Format and Timing

Figure 12: Encoder Position RS-485 Data Read Out Frames Set

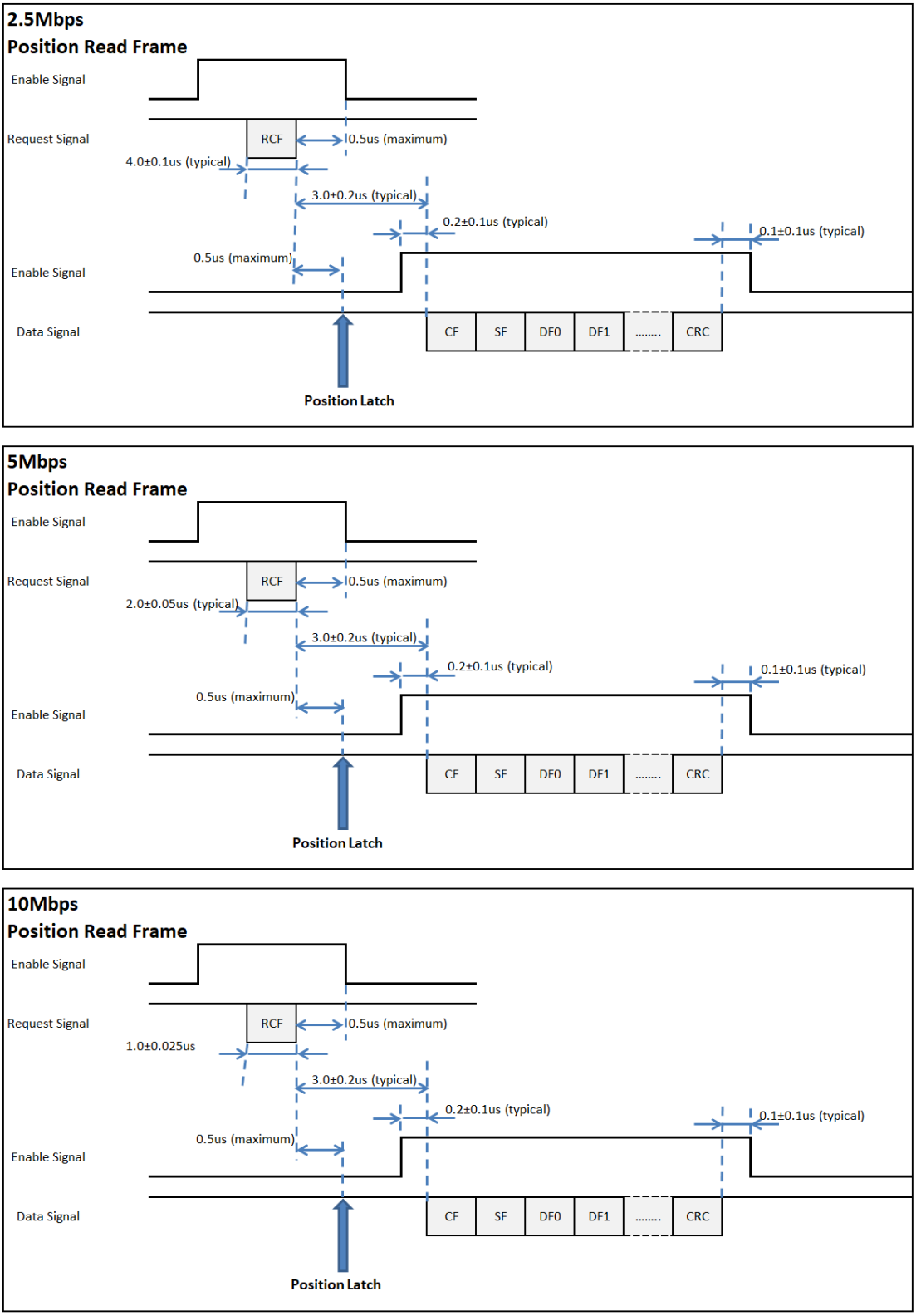
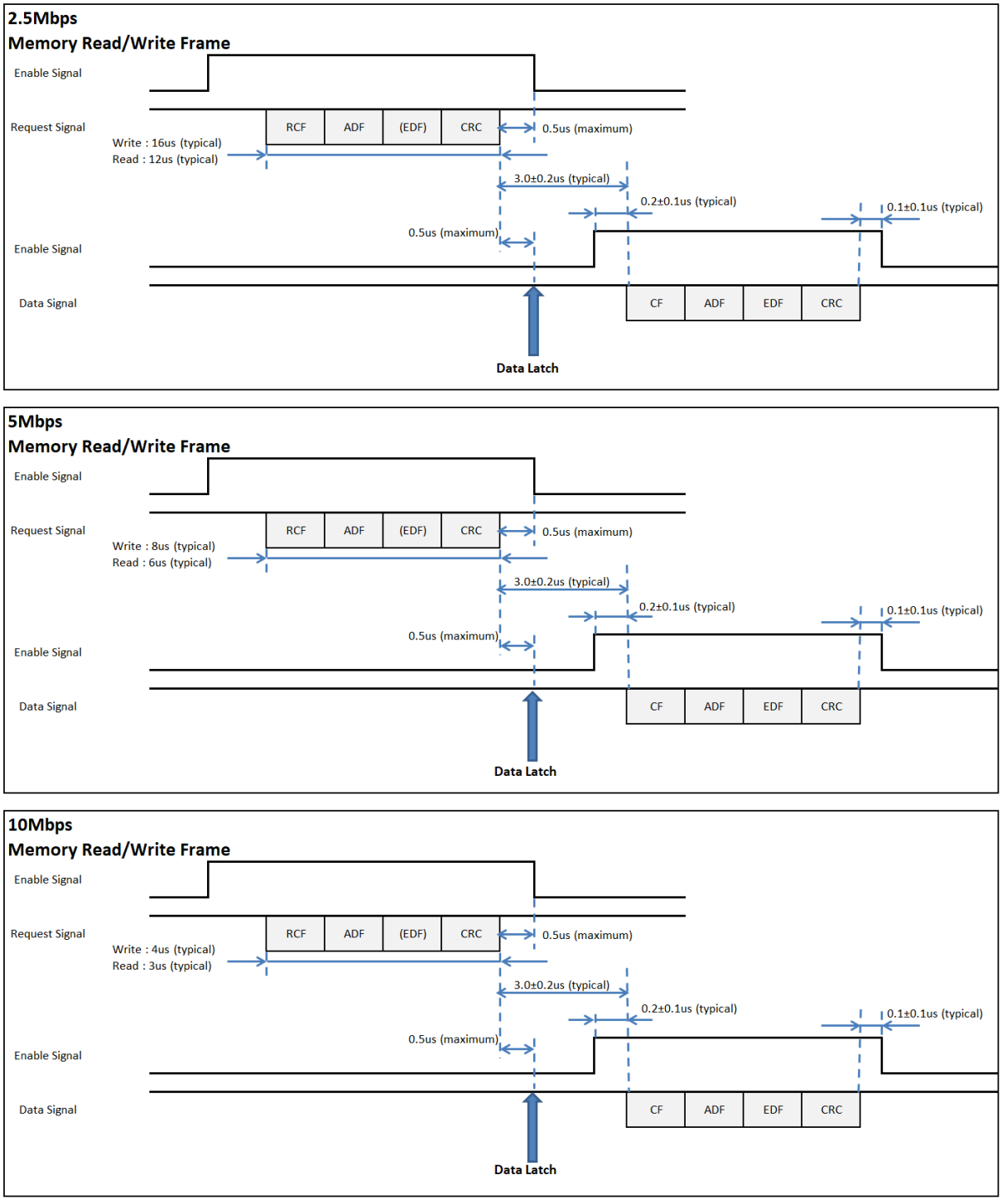


Figure 13: Encoder Memory Data Read and Write Frames Set



Encoder Position Data Read Out Frame Sets

When the host issues a RCF frame request, the encoder shall respond after 3.0 µs (typical) with an encoder data frames set with the following contents:

1. CF: Control Field; corresponds to the command frame issued by the Host
2. SF: Status Field
3. DF0~DF7: Encoder Data Field
4. CRC: Cyclic Redundancy Check frame

The encoder response data frame sets are dependent on the requested operation by the host; refer to Table 16.

Memory Data Read Out Frames Set

Content of transmission frames:

1. CF: Control Field; same for both host command and encoder response
2. ADF: Address Data Field; indicates the memory location to read
3. EDF: Memory Data Field; contains the data read from memory
4. CRC: Cyclic Redundancy Check check

Memory Data Write Frames Set

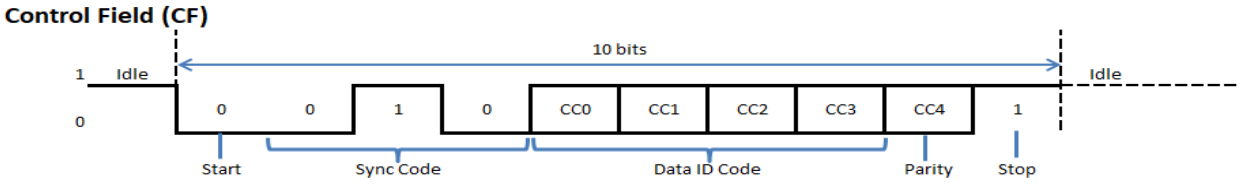
Content of transmission frames:

1. CF: Control Field; same for both host command and encoder response
2. ADF: Address Data Field; indicates the memory location to write
3. EDF: Memory Data Field; contains the written data to memory
4. CRC: Cyclic Redundancy Check check

Detailed Description of Data Frames

Control Field (CF)

Figure 14: Control Field Format



The contents of the CF frame are as follows:

1. Start Bit: Indicates the start of a frame, always 0
2. Sync Code: Indicates a valid sync code has been issued, defined as 010
3. Data ID: A combination of bits defining command instructions, refer to Table 13 and Table 14.
4. Parity Bit: Parity check bit for the data ID, refer to Table 13.
5. Stop Bit: Indicates the end of a frame, always 1.

Data ID and Client Encoder Operation Definition

Table 13: Encoder Operation Command Code Definition and Parity Bit

Encoder Operation	Data ID	Encoder Sync Code			Data ID Bits				Parity	HEX
		BIT 0	BIT 1	BIT 2	CC0	CC1	CC2	CC3	CC4	
Position or Encoder Information Read Command	0	0	1	0	0	0	0	0	0	02
	1	0	1	0	1	0	0	0	1	8A
	2	0	1	0	0	1	0	0	1	92
	3	0	1	0	1	1	0	0	0	1A
	4	0	1	0	0	0	1	0	1	A2
Memory Write Command	6	0	1	0	0	1	1	0	0	32
Alarm Clear Command	7	0	1	0	1	1	1	0	1	BA
Position Zero Reset Command	8	0	1	0	0	0	0	1	1	C2
Multi-turn and Alarm Clear Command	C	0	1	0	0	0	1	1	0	62
Memory Read Command	D	0	1	0	1	0	1	1	1	EA

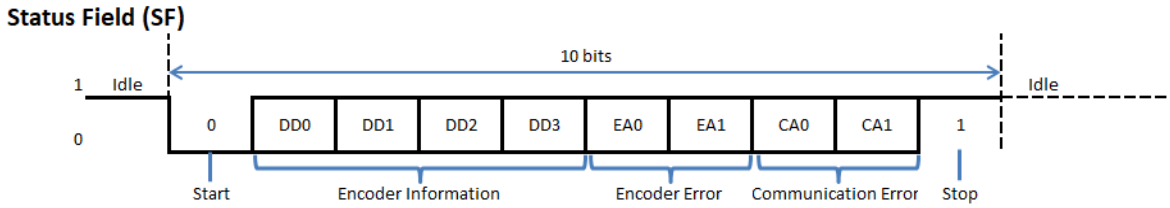
Table 14: Description of Encoder Operation

Operation	Data ID	Description of Operation
Position Read Command	0, 1, 2, 3, 4	Transmit Data ID code (Table 13) according to the List of Data field to the Encoder.
Memory Write Command	6	8 bits of data to be written into a designated memory address of the user accessible area.
Alarm Clear Command	7	Consecutive sending to perform Alarm Clear command.
Position Zero Reset Command	8	Consecutive sending to perform Position Zero Reset command
Multi-turn and Alarm Clear Command	C	Consecutive sending to perform Multi-turn and Alarm Clear command
Memory Read Command	D	8 bits of data to be read from a designated memory address of the user-accessible area.

NOTE: Refer to Table 16 for the requirements of consecutive sending for the clear or reset commands.

Status Field (SF)

Figure 15: SF Frame Format



The contents of the SF frame are as follows:

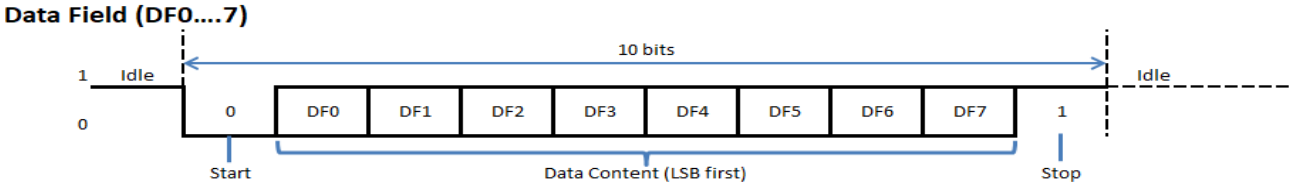
1. Start Bit: Indicates the start of a frame, always 0
2. Encoder Information: Defined as 0000
3. Encoder Error: Returns with state of 1 if an encoder error is detected
4. Stop Bit: Indicates the end of a frame, always 1

Table 15: Status Field Description of Error Flags

Logic When Error Is Detected	Error Flag	Error Description
Encoder Error Bit 1	EA0	Encoder counting error
	EA1	Multi-turn counting error
Communication Error Bit 1	CA0	Parity error detected in Host Request Frames set
	CA1	End bit error detected in Host Request Frames set

Data Field (DF_n)

Figure 16: DF_n Frame Format



The contents of the DF_n frame are as follows:

1. Start Bit: Indicates the start of frame, always 0
2. DF0~DF7: 8 bits data set, with LSB first in the sequence
3. End bit: Indicates the end of frame, always 1

Description of Data Frames with Respective Data ID

Table 16: Data Frames Content with Respective Data ID for up to 24-bit Multi-turn

Data ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
0	CF	SF	ABS0	ABS1	ABS2						Include CRC	Position Read Command	6
1	CF	SF	ABM0	ABM1	ABM2								6
2	CF	SF	ENID									Encoder Identification	4
3	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	ALMC		Position Read Command	11
4	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	TEMP			11
6	CF	ADF	EDF									Memory or Register Write Command	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform Alarm Clear Command	6
8	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform ST Zero Reset Command	6
C	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform MT & Alarm Clear Command	6
D	CF	ADF	EDF									Memory or Register Read Command	4

NOTE:

- **ABSn:** Single-turn counts; LSB of the single-turn counts is located in ABS0 and MSB of the counts, data is located in ABS2.
- **ABMn:** Multi-turn counts; LSB of the multi-turn counts is located in ABM0 and MSB of the counts, data is located in ABM2.
- **ENID:** Encoder single-turn bits identification in 8-bit format; for example, 23-bit output is set to 17h.
- **ALMC:** Encoder alarm data in 8-bit format.
- **TEMP:** Encoder temperature readout data in 8-bit format.

Status and Alarm

Details of the error bit are available in the following register address.

	Bit							
Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x24	0	0	0	OVS	MT_Track	0	0	0
0x25	0	0	XC	0	0	0	BB_cfg	OVF
0x26	0	0	0	Temp	Mem	0	ST_Track	0
0x27	OV	UV	MHI	MLO	BE	BA	0	0

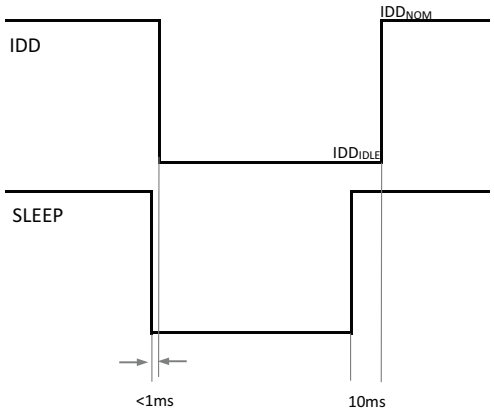
- **Multi-Turn Over Speed (OVS) Alarm:** This indicates the over-speed detection during the multi-turn counting in battery mode.
- **Multi-Turn Tracker (MT_Track) Error:** This indicates that the multi-turn position is potentially wrong due to the single-turn position count.
- **Multi-Turn Counter Comparison (XC) Alarm:** This indicates that the raw multi-turn position is not a match with the software multi-turn position count.
- **Multi-Turn Battery Backup Configuration (BB_cfg) Alarm:** This indicates that corruption of the multi-turn battery backup configuration has occurred.
- **Multi-Turn Overflow (OVF) Alarm:** This indicates overflow of the multi-turn counting.
- **Temperature (Temp) Alarm:** This indicates that the temperature has exceeded the temperature limit setting.
- **Memory (Mem) Error:** This indicates that memory corruption has occurred. When this is set high, perform a power cycle to reload the memory. The value for this alarm is represented as 1.
- **Single-Turn Tracker (ST_Track) Error:** This indicates that the angular error has exceeded 5° within 5 ms. When this is set high consistently, perform a power cycle to reinitialize the sensor. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is set high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is set low consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Battery-Backup Multi-Turn Battery Error (BE):** This indicates that the battery level is below 3.0V. When this is set high consistently, the battery must be replaced and the multi-turn counter will be reset. The multi-turn counter will not function during battery mode.
- **Battery-Backup Multi-Turn Battery Alarm (BA):** This indicates that the battery level is below 3.2V. Replacing the battery is recommended. The multi-turn counter is functioning during battery mode.

Power Modes

The AEAT-9988M is designed with two power modes:

- **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}.
- **Sleep Mode** powers down the chip front-end and digital processing blocks, leaving only the detection block to track on user input with low current consumption, IDD_{IDLE}.
- The SLEEP pin is an active low, tied to VDDA if unused.

Figure 17: Sleep Mode Timing



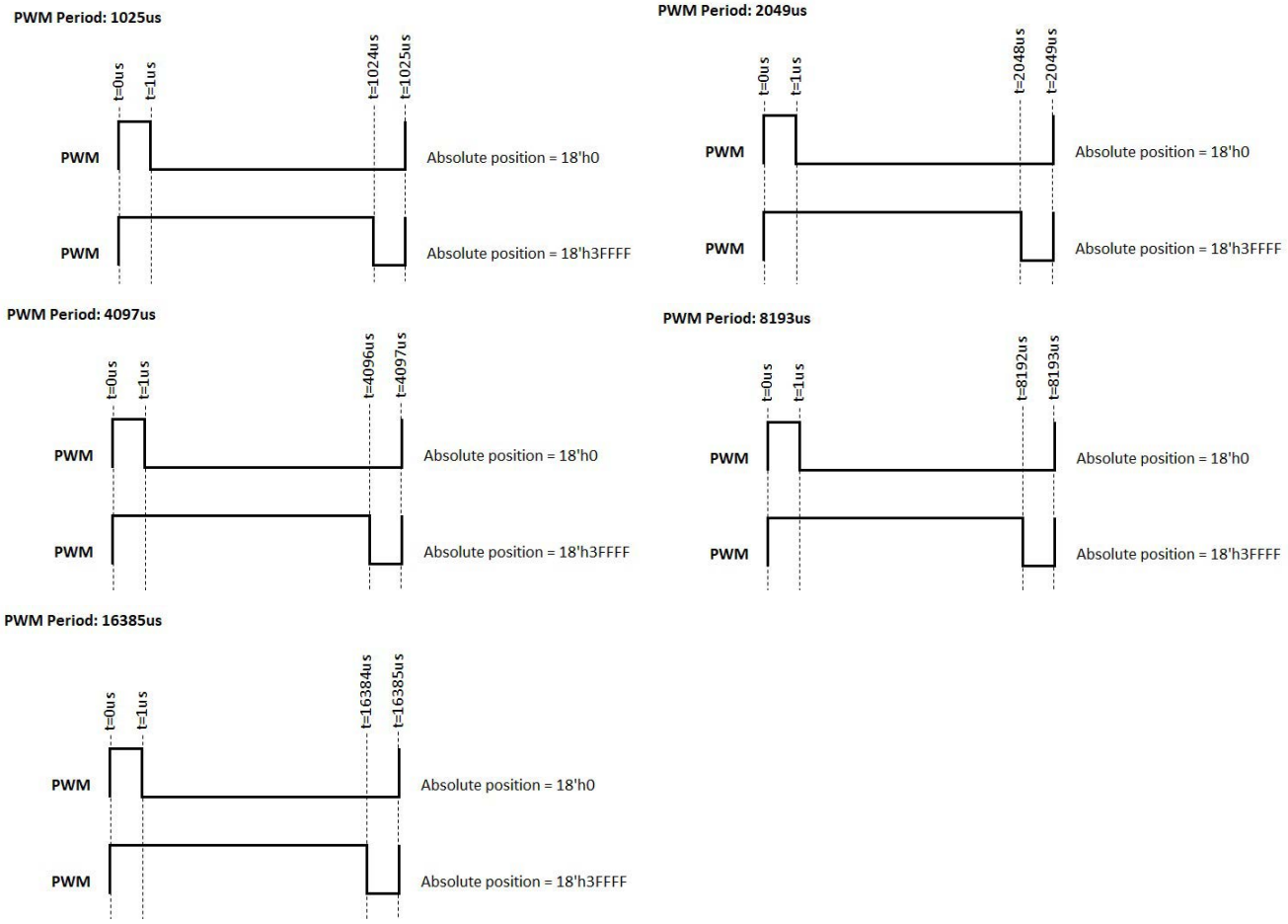
PWM

The PWM protocol uses one output pin (PA5) from the AEAT-9988M. The PWM signals are configurable to have a period of 1025, 2049, 4097, 8193 or 16385 µs.

During power-up, the PWM signal is 0 before the chip is ready.

PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

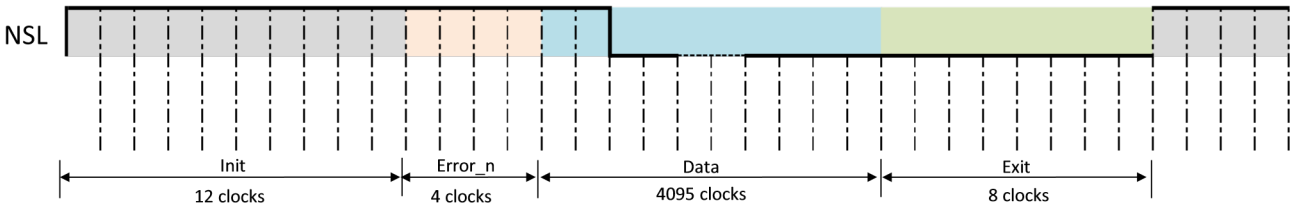
PWM Period: 1025, 2049, 4097, 8193, 16385 µs



The PWM protocol is also available with Init, Error_n, and Exit, along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PWM Period: 4119 µs



Incremental Output Format

The AEAT-9988M provides ABI and UVW signals to indicate the incremental position of the motor.

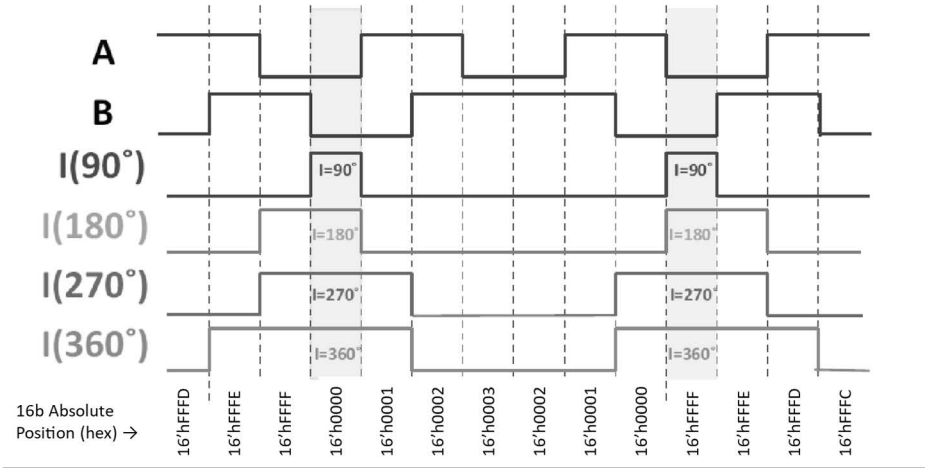
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

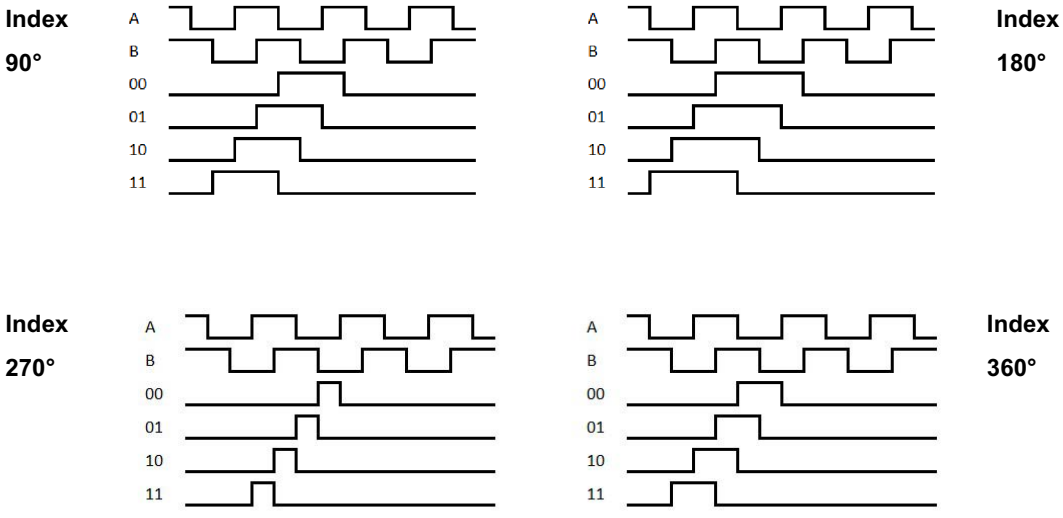
- Programmable CPR: 0 to 65,536 CPR
- Programmable I-width: 90, 180, 270 or 360 electrical degrees (edeg)
- Programmable I-state: 90, 180, 270 or 360 electrical degrees (edeg)

Figure 18: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming Hysteresis is Set at 0.02 Mechanical Degrees



The index position is configurable among the incremental states.

The index signal rises high once per turn at the absolute zero position.



The number of indexes per revolution is configurable from 1 pulse up to 256 pulses.

Figure 19: 1 Index per Revolution

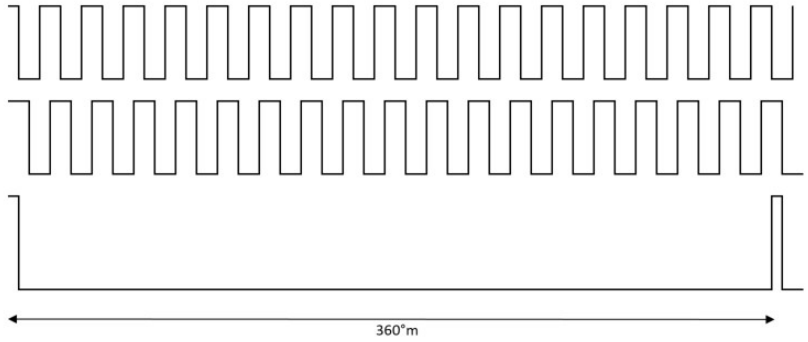
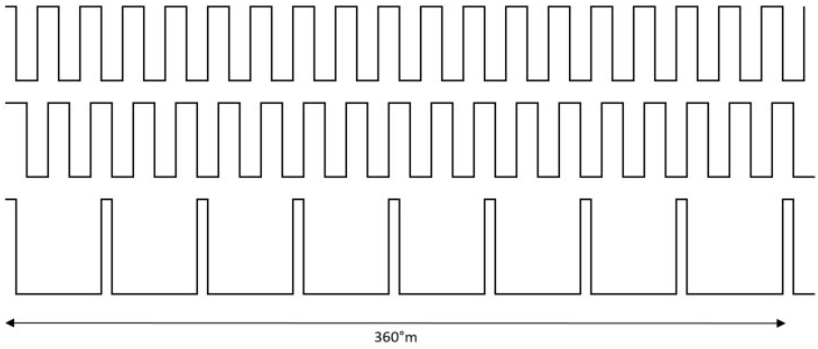


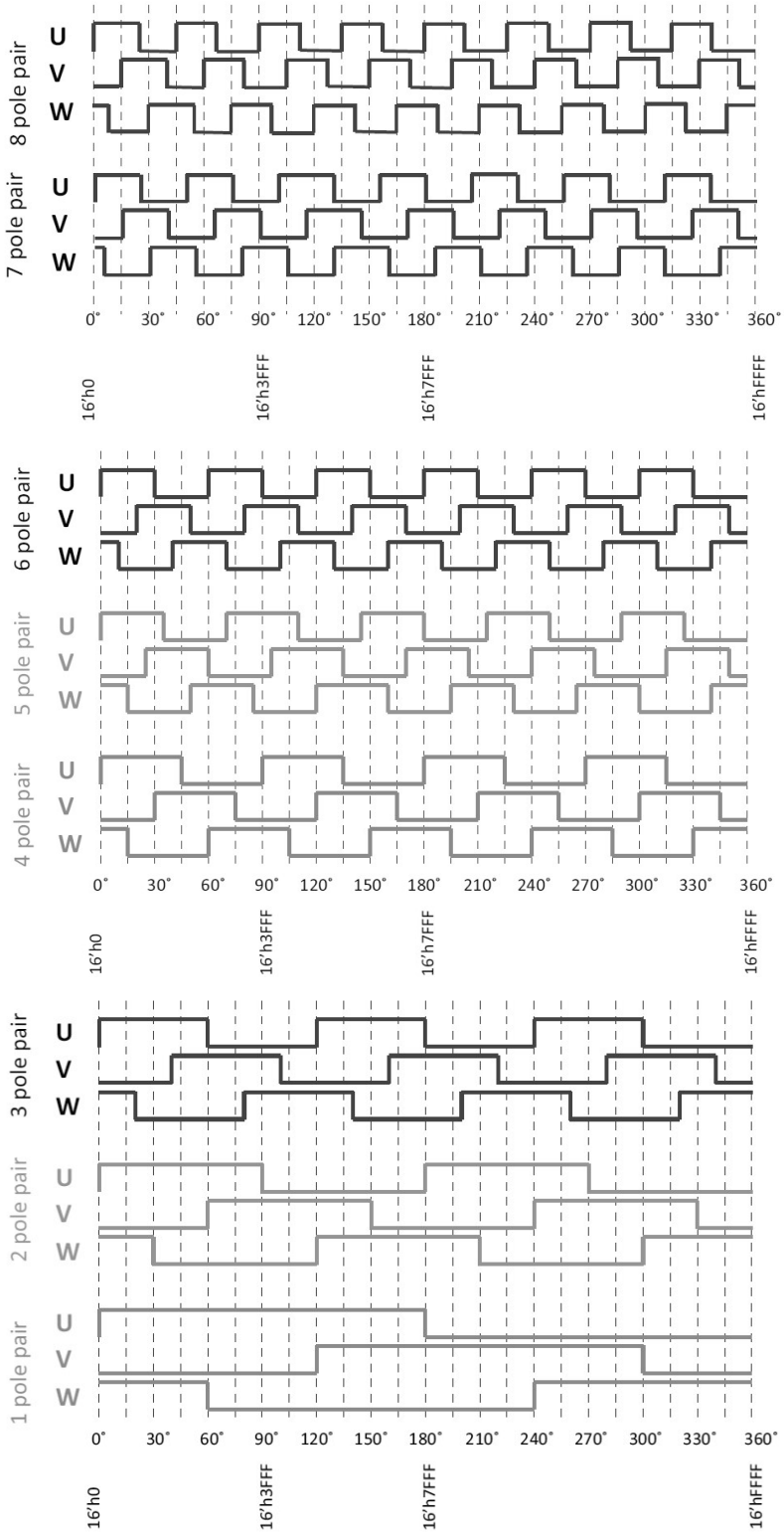
Figure 20: 8 Indexes per Revolution



UVW

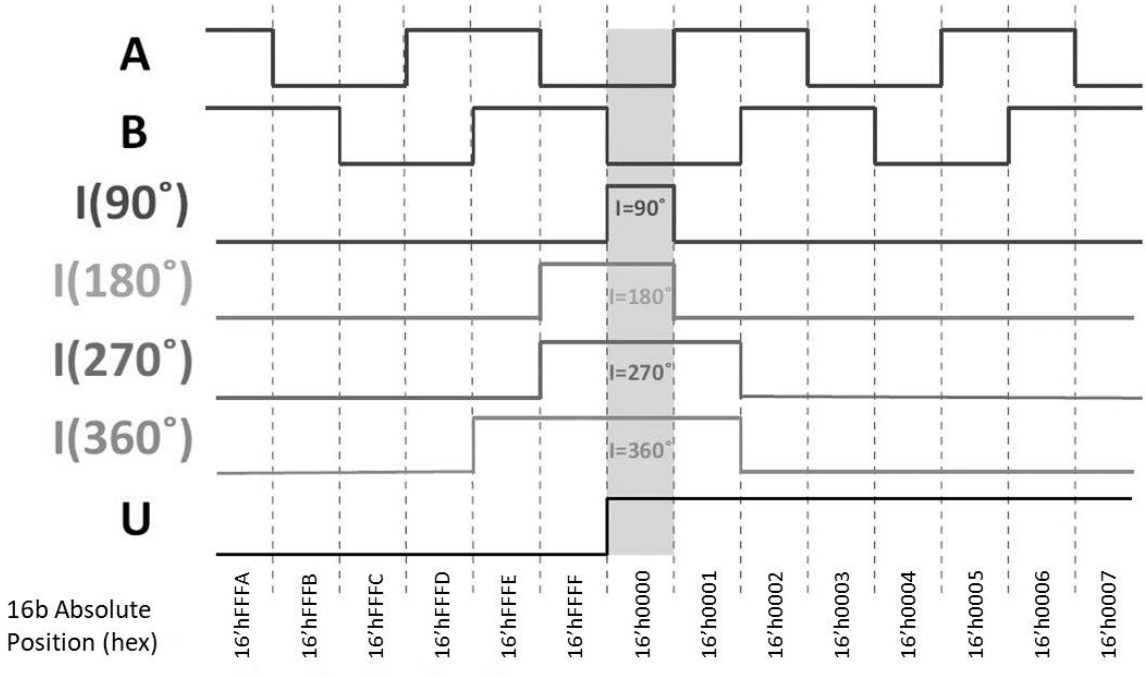
Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback.

The AEAT-9988M can configure pole pairs from 1 to 64 (equivalent to 2 to 128 poles).



NOTE: Signal U from the UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 21: U-to-I Tagging



Recommended PCB Land Pattern (in mm)

Figure 22: Recommended PCB Land Pattern Details

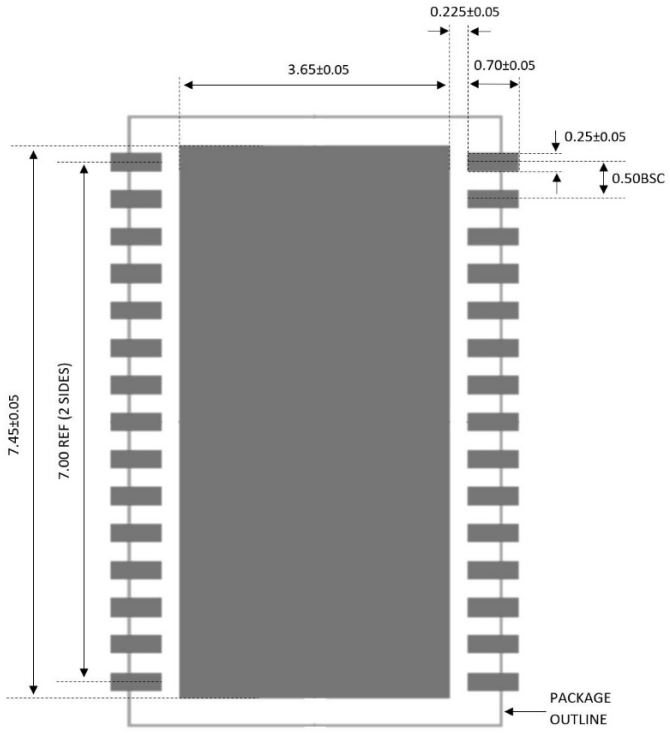


Figure 23: Recommended Lead-Free Solder Reflow Temperature Profile