11 GHz to 20 GHz, Tunable Band-Pass Filter

Data Sheet

ADMV8420

FEATURES

Amplitude settling time: 200 ns
Wideband rejection: ≥20 dB
Single-chip implementation
24-lead, 4 mm × 4 mm, RoHS-compliant LFCSP

APPLICATIONS

Test and measurement equipment
Military radar and electronic warfare systems
Very small aperture terminal (VSAT) communications

FUNCTIONAL BLOCK DIAGRAM

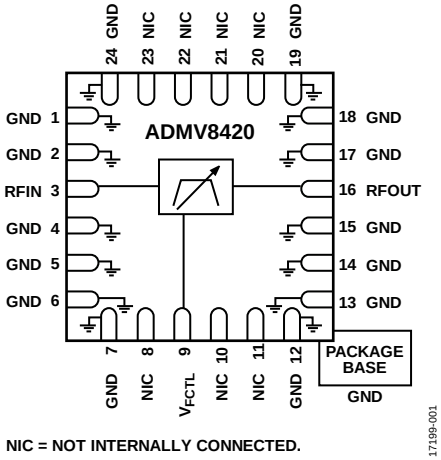

Figure 1.

GENERAL DESCRIPTION

The ADMV8420 is a monolithic microwave integrated circuit (MMIC), tunable band-pass filter that features a user-selectable pass band frequency. The 3 dB filter bandwidth is approximately 20%, and the 20 dB filter bandwidth is approximately 40%. Additionally, the center frequency (f_{CENTER}) varies between 11 GHz to 20 GHz by applying a center frequency control voltage between 0 V to 15 V. This tunable filter is a smaller alternative to switched filter banks and cavity tuned filters. The ADMV8420 has minimal microphonics due to the monolithic design and provides a dynamically adjustable solution in advanced communications applications.

Rev. 0 **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

6/2019—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, center frequency control voltage (V_{FCTL}) is swept from 0 V to 15 V.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
f_{CENTER}	11		20	GHz	
BANDWIDTH					
3 dB		20		%	
REJECTION					
Low-Side		0.8 × f_{CENTER}		GHz	≥20 dB
High-Side		1.2 × f_{CENTER}		GHz	≥20 dB
Reentry		2.3 × f_{CENTER}		GHz	≤30 dB
LOSS					
Insertion Loss		5		dB	
Return Loss		8.5		dB	
DYNAMIC PERFORMANCE					
Input Power at 5° Shift in Insertion Phase (V_{FCTL} = 0 V)		10		dBm	
Input Third-Order Intercept (IP3)		31		dBm	
Group Delay		0.5		ns	
Phase Sensitivity		1.33		Rad/V	
Amplitude Settling		200		ns	Time to settle to minimum insertion loss, within ≤0.5 dB of static insertion loss
Drift Rate		−1.07		MHz/°C	
RESIDUAL PHASE NOISE					
1 MHz Offset		−161		dBc/Hz	
TUNING					
V_{FCTL}	0		15	V	
Center Frequency Control Current (I_{FCTL})			±1	mA	

ABSOLUTE MAXIMUM RATINGS

Table 2.

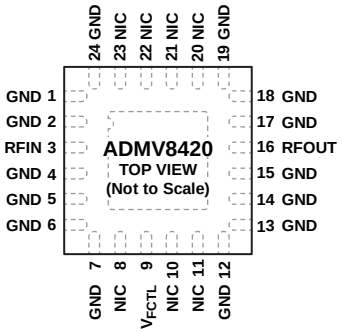
Parameter	Rating
Tuning	
V_{FCTL}	−0.5 V to +15 V
I_{FCTL}	±1 mA
Radio Frequency (RF) Input Power	27 dBm
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature for 1 Million Mean Time to Failure (MTTF)	150°C
Nominal Junction Temperature (Temperature at Ground Pad = 85°C, Input Power (P_{IN}) = 27 dBm)	108°C
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	1000 V
Field Induced Charge Device Model (FICDM)	1250 V
Moisture Sensitivity Level (MSL) Rating	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA SHOWN HEREIN WAS MEASURED WITH THESE CONNECTED TO RF AND DC GROUND.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

17199-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 12 to 15, 17 to 19, 24	GND	Ground. These pins must be connected to the radio frequency (RF) and dc ground.
3	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. Do not apply an external voltage to this pin.
8, 10, 11, 20 to 23	NIC	Not Internally Connected. These pins are not connected internally. However, all data shown is measured with these pins connected to the RF and dc ground.
9	V_{FCTL}	Center Frequency Control Voltage. This pin controls the f_{CENTER} of the device.
16	RFOUT	RF Output. This pin is dc-coupled and matched to 50 Ω. Do not apply an external voltage to this pin.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc gound.

INTERFACE SCHEMATICS

Figure 3. V_{FCTL} Interface Schematic

Figure 4. GND Interface Schematic

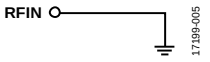


Figure 5. RFIN Interface Schematic

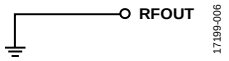


Figure 6. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

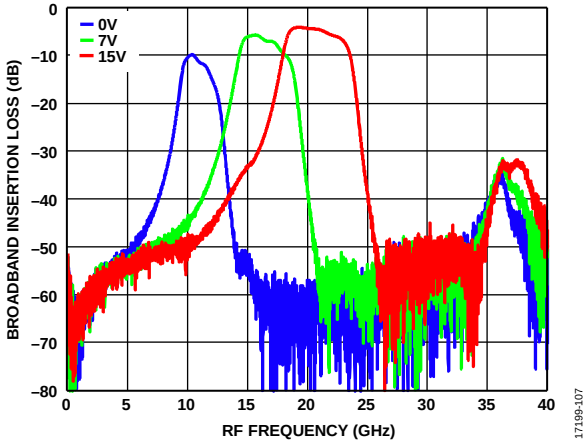


Figure 7. Broadband Insertion Loss vs. RF Frequency at Various Voltages

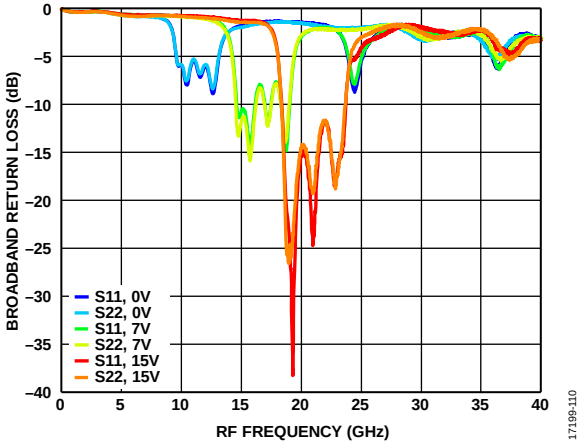


Figure 10. Broadband Return Loss vs. RF Frequency at Various Voltages

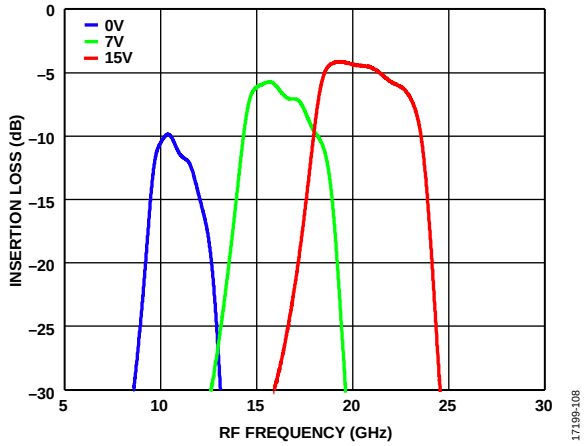


Figure 8. Insertion Loss vs. RF Frequency at Various Voltages

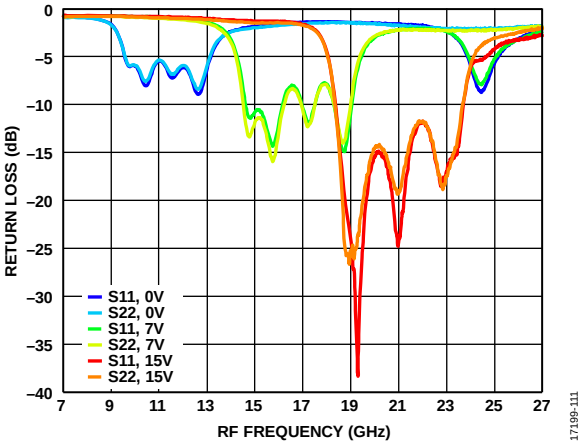


Figure 11. Return Loss vs. RF Frequency at Various Voltages

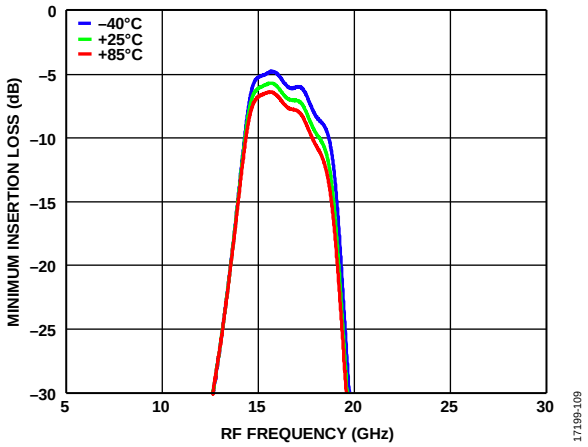


Figure 9. Minimum Insertion Loss vs. RF Frequency at Various Temperatures, V_{FCTL} = 7 V

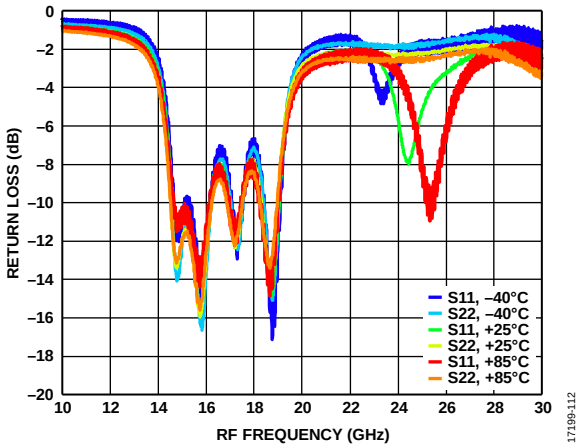


Figure 12. Return Loss vs. RF Frequency at Various Temperatures, V_{FCTL} = 7 V

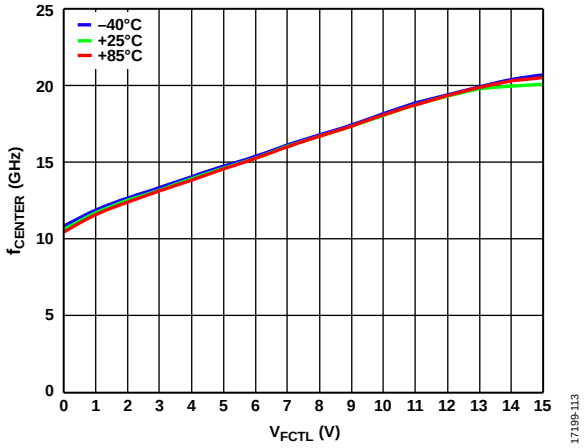


Figure 13. f_{CENTER} vs. V_{FCTL} at Various Temperatures

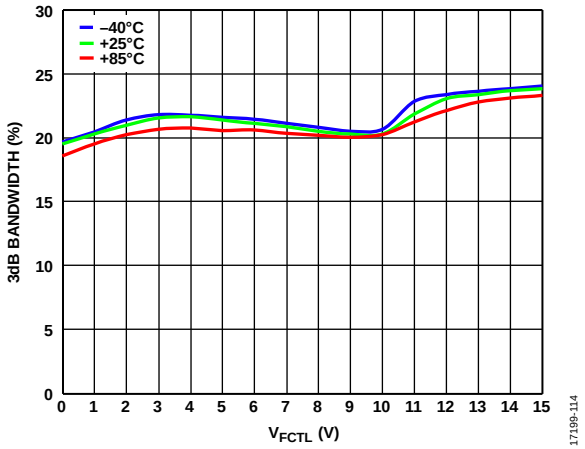


Figure 14. 3 dB Bandwidth vs. V_{FCTL} at Various Temperatures

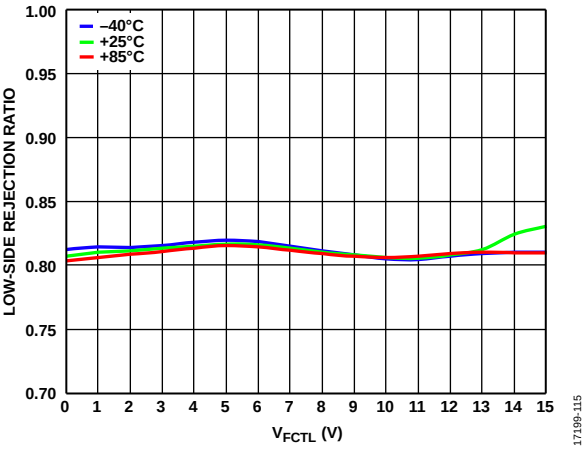


Figure 15. Low-Side Rejection Ratio vs. V_{FCTL} at Various Temperatures

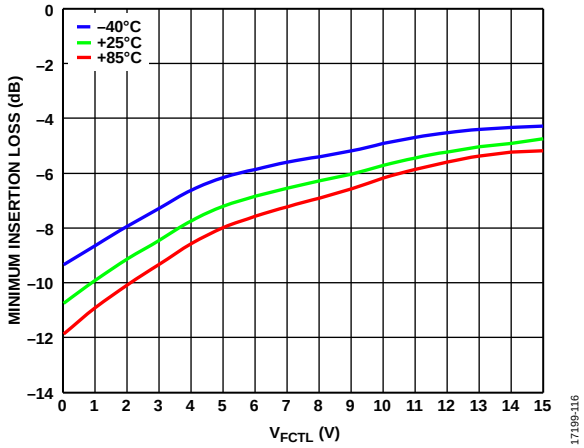


Figure 16. Minimum Insertion Loss vs. V_{FCTL} at Various Temperatures

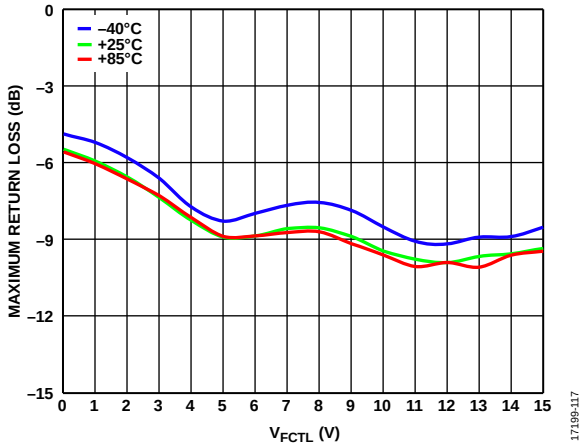


Figure 17. Maximum Return Loss in a 2 dB Bandwidth vs. V_{FCTL} at Various Temperatures

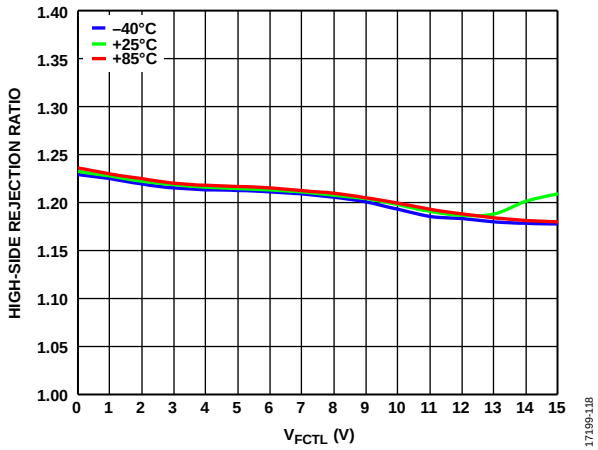


Figure 18. High-Side Rejection Ratio vs. V_{FCTL} at Various Temperatures

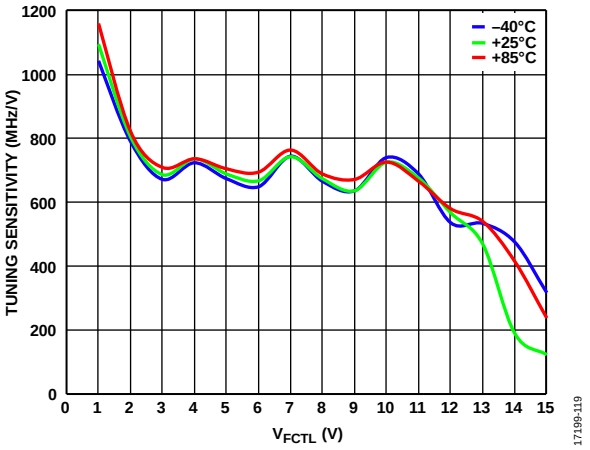


Figure 19. Tuning Sensitivity vs. V_{FCTL} at Various Temperatures

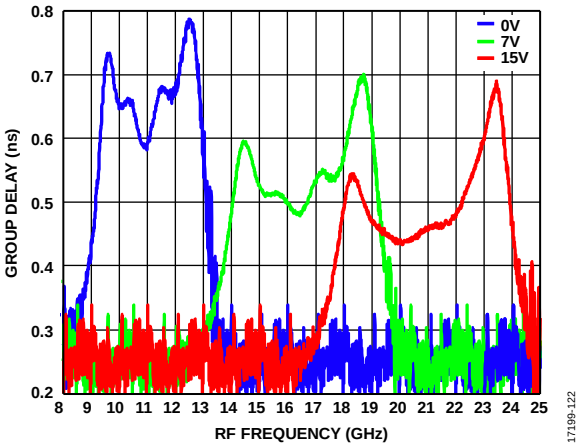


Figure 22. Group Delay vs. RF Frequency at Various Voltages

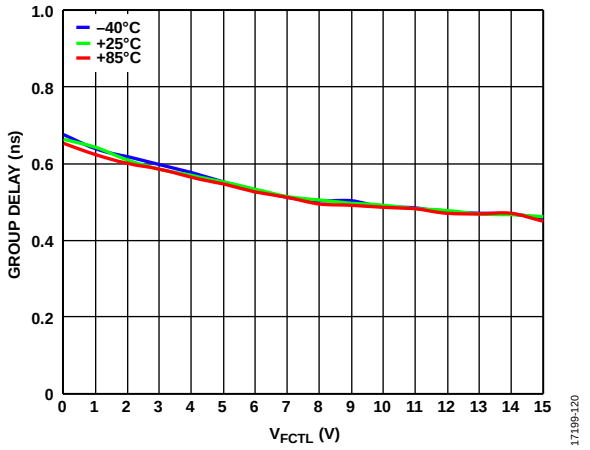


Figure 20. Group Delay vs. V_{FCTL} at Various Temperatures

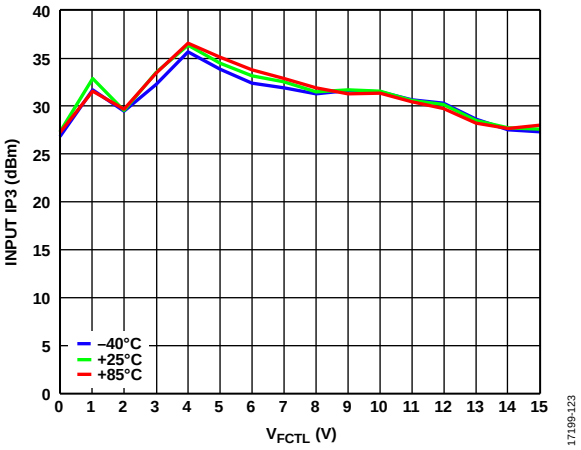


Figure 23. Input IP3 vs. V_{FCTL} at Various Temperatures, P_{IN} = 20 dBm

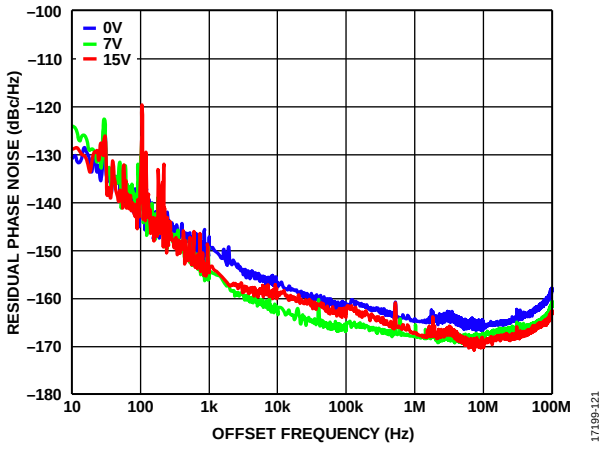


Figure 21. Residual Phase Noise vs. Offset Frequency at Various V_{FCTL} Voltages

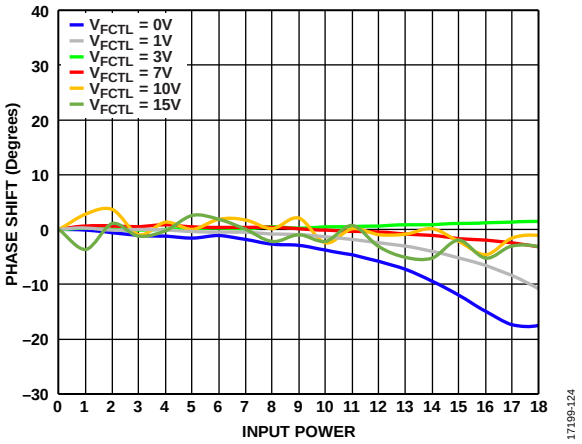


Figure 24. Phase Shift vs. Input Power (dBm)

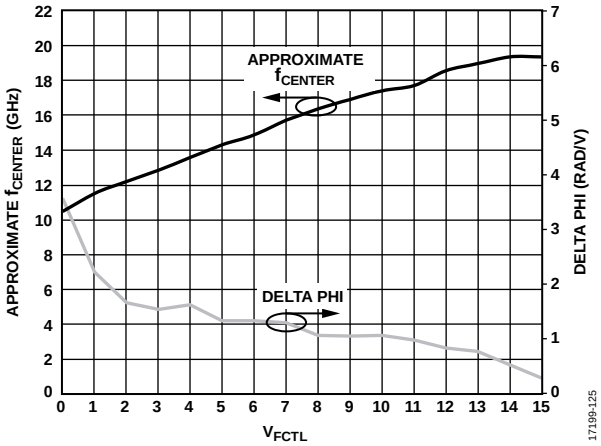


Figure 25. Phase Sensitivity vs. V_{FCTL} Voltages

THEORY OF OPERATION

The ADMV8420 is a MMIC band-pass filter that features a user-selectable pass band frequency. Varying the applied analog tuning voltage between 0 V and 15 V at V_{FCTL} varies the f_{CENTER} between 11 GHz and 20 GHz.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 26 shows the typical application circuit for the ADMV8420. The RFIN and RFOUT pins are dc-coupled and require external 100 pF series capacitors (C1 and C2).

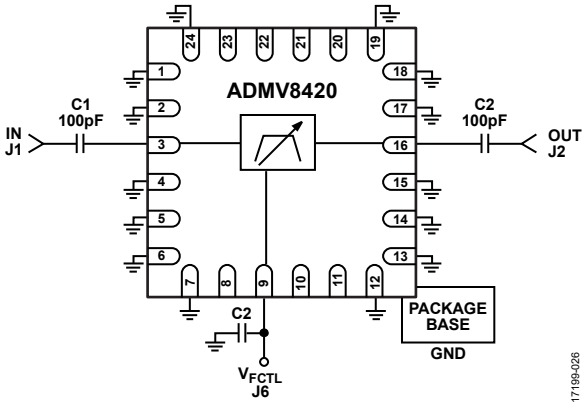


Figure 26. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

All RF traces are routed on Layer 1 (primary side). The remaining three layers are ground planes that provide a solid ground for RF transmission lines, as shown in Figure 27. The top dielectric material is Rogers 4350, which offers low loss performance. The prepreg material in Layer 2 attaches the Isola 370HR core layer to copper traces layers. Both the prepreg material and the Isola 370HR core layer achieve the required board finish thickness.

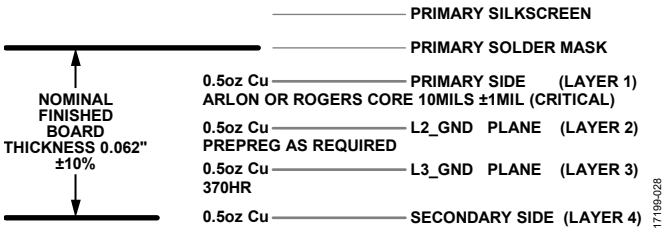


Figure 27. The Cross-Sectional View of the ADMV8420-EVALZ PCB Layers

The circuit board in this application uses RF circuit design techniques. Signal lines must have 50 Ω impedance. The package ground leads and exposed pad must connect directly to the ground plane (see Figure 27). A sufficient number of via holes connect the top and bottom ground planes. The evaluation circuit board shown in Figure 28 is available from Analog Devices, Inc. upon request.

Table 4. Bill of Materials for the ADMV8420-EVALZ

Item	Description
J1 to J2	PCB mount, Southwest 2.4 mm connector
J6 to J7	Test points
C2	Capacitor, 100 pF, 0402
U1	ADMV8420
PCB[1]	08-051298[2] evaluation PCB

[1] Circuit board material is Arlon 25FR or Rogers 25FR. Rogers 4350 is the laminate on top of Arlon 25FR or Rogers 25FR.
[2] The raw, bare PCB identifier is 08-051298. Reference the ADMV8420 when ordering the complete evaluation PCB.

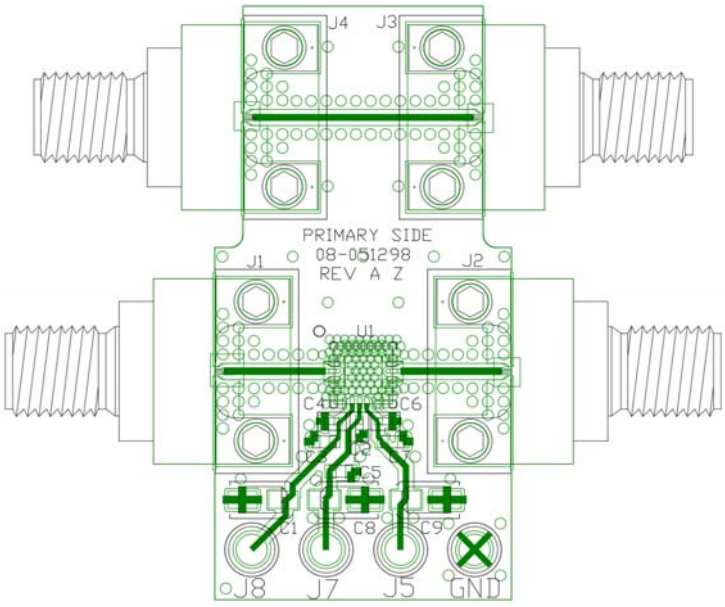


Figure 28. Evaluation PCB, Top Layer Outline Dimensions

OUTLINE DIMENSIONS

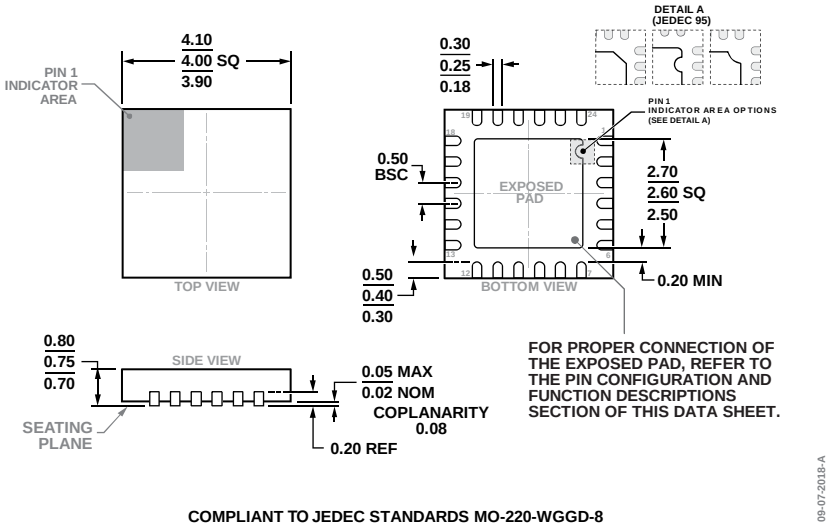


Figure 29. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV8420ACPZ	–40°C to +85°C	24-Lead LFCSP	CP-24-15
ADMV8420ACPZ-R5	–40°C to +85°C	24-Lead LFCSP, 7″ Tape and Reel	CP-24-15
ADMV8420-EVAL		Evaluation Board	

[1] All models are RoHS-compliant parts.

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Analog Devices Inc.:

ADMV8420ACPZ ADMV8420ACPZ-R5 ADMV8420-EVALZ