Ultrathin 1.5A µModule Thermoelectric Cooler (TEC) Regulator

FEATURES

- **Built-in Two Zero-Drift, Rail-to-Rail Chopper Amplifiers**
- 2.7V to 5.5V Input Voltage Range
- 1.5A Driving Capability
- **1% Accuracy 2.5V Internal Reference Output**
- TEC Voltage and Current Monitoring
- Independent Programmable Heating and Cooling Current Limit
- Programmable Maximum TEC Voltage
- Default 2MHz Switching Frequency
- Synchronization from 1.85MHz to 3.25MHz
- Capable of NTC, PTC and RTD Thermal Sensors
- **3.5mm × 4mm × 1.3mm LGA Package**

APPLICATIONS

- TEC Temperature Control
- Optical Networking System, Optical Module
- LiDAR System

DESCRIPTION

The LTM®4663 is a complete 1.5A µModule® Thermoelectric Cooler (TEC) regulator in a tiny 3.5mm × 4mm × 1.3mm LGA package. Included in the package are the TEC controller, linear power stage, switching regulator, inductor and all support components.

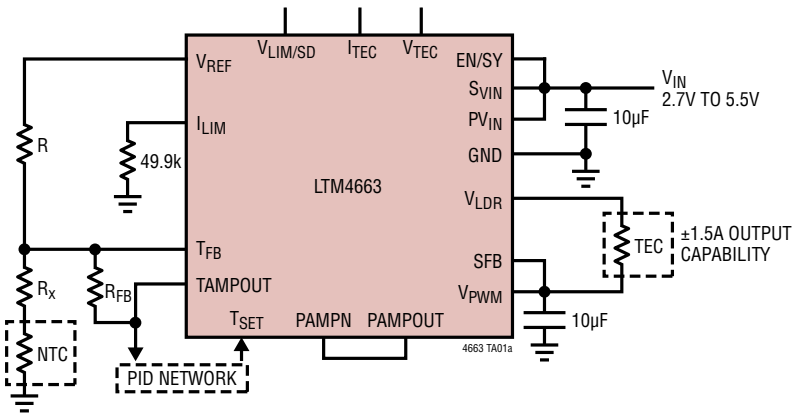
Operating over an input voltage range of 2.7V to 5.5V, the LTM4663 supports a 1.5A continuous sink or source current capability. Only input and output capacitors are needed. The LTM4663 has two zero drift, rail-to-rail chopper amplifiers to serve as the thermistor input amplifier and the temperature feedback control loop.

The LTM4663 supports NTC, PTC thermistors and resistive temperature detectors (RTD). The maximum cooling and heating currents can be programmed independently as well as the maximum TEC voltage.

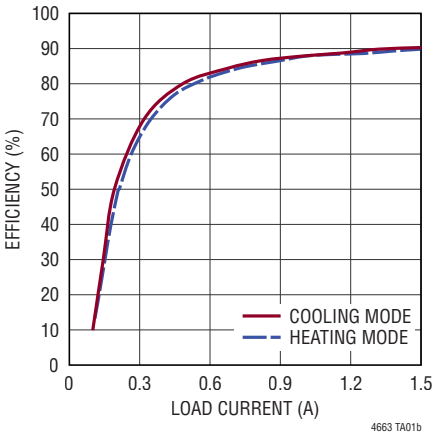
The LTM4663 is available in LGA RoHS compliant terminal finish.

TYPICAL APPLICATION

1.5A TEC Supply µModule Regulator



Efficiency vs TEC Current at V_{IN} = 5V in Cooling/Heating Mode with 2Ω Load

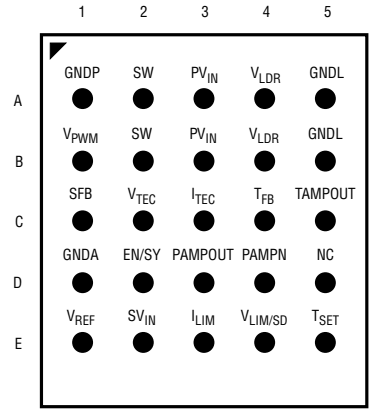


ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN} ..... –0.3V to 5.75V
V_{LDR}, V_{PWM} ..... –0.3V to PV_{IN}
T_{FB}, T_{SET}, PAMPN, SFB,
$V_{LIM/SD}$, I_{LIM}, EN/SY ..... –0.3V to SV_{IN}
TAMPOUT, PAMPOUT, I_{TEC}, V_{TEC} ..... –0.3V to 5.75V
V_{REF} ..... –0.3V to 3V
Operating Junction Temperature
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 260°C

PIN CONFIGURATION



LGA PACKAGE
25-LEAD (3.5mm × 4mm × 1.3mm)

T_{JMAX} = 125°C, θ_{JCtop} = 34°C/W ,
$\theta_{JCbottom}$ = 12°C/W, θ_{JA} = 36°C/W
WEIGHT = 60mg

NOTES:
1) θ_{JC} VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO PAGES 16, 17 FOR LAB MEASUREMENT AND DE-RATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4663EV#PBF	Au (RoHS)	4663V	v	LGA	3	–40°C to 125°C
LTM4663IV#PBF						–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA Assembly and Manufacturing Procedures
- LGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), PV_{IN} = SV_{IN} = 5V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV_{IN}	Power Input Voltage		●	2.7		5.5	V
SV_{IN}	Signal Input Voltage		●	2.7		5.5	V
$I_{Q(SVIN)}$	Input Supply Bias Current	PWM Not Switching Shutdown, EN/SY = GND			3.8 480	5.5 700	mA µA
UVLO	Undervoltage Lockout	SV_{IN} Rising		2.45	2.55	2.65	V
UVLO_HYS	UVLO Hysteresis				80		mV
V_{REF}	Reference Voltage			2.475	2.5	2.525	V
V_{TEC}	Max TEC Differential Voltage	No Load	●	93% • PV_{IN}			V
I_{TEC}	Max TEC Current		●			1.5	A
I_{SFB}	SFB Bias Current	(Note 3)			1		µA
t_{SS}	Soft-Start Time				150		ms
$V_{LIM/SD}$	Shutdown Voltage Threshold					0.07	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), PV_{IN} = SV_{IN} = 5V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FREQ	Oscillator Frequency				2.0		MHz
SYNC	External Sync Frequency Range			1.85		3.25	MHz
$V_{EN/SY}$ Low		EN/SY Input Voltage Low Level				0.8	V
$V_{EN/SY}$ High		EN/SY Input Voltage High Level		2.1			V
Error Amp							
V_{CM}	Input Voltage Range	(Note 3)		0		SV_{IN}	V
V_{OS}	Input Offset Voltage	(Note 3)			10	100	µV
CMRR	Common Mode Rejection Ratio	(Note 3)			120		dB
TEC Current Limit							
V_{ILIM}	I_{LIM} Input Range	Cooling Heating		1.3 0.2		V_{REF} – 0.2 1.2	V V
I_{ILIM}	Current Limit Threshold	Cooling V_{ILIM} = 1.3V V_{ILIM} = 1.8V Heating V_{ILIM} = 1.2V V_{ILIM} = 0.7V		220 1125 220 1125	300 1260 300 1260	360 1375 360 1375	mA mA mA mA
TEC Voltage Limit							
V_{VLIM}	V_{LIM} Input Range			0.2		$SV_{IN/2}$	V
AV_{LIM}	Voltage Limit Gain	$(V_{LDR} – V_{SFB})/V_{VLIM}$			2		V/V
TEC Current Measurement							
R_{CS}	Current Sense Gain	V_{IN} = 5V			0.535		V/A
V_{ITEC}	TEC Current Measurement	Heating I_{LOAD} = –1.5A Heating I_{LOAD} = –0.5A Cooling I_{LOAD} = 0.5A Cooling I_{LOAD} = 1.5A			0.45 0.98 1.52 2.05		V V V V
TEC Voltage Measurement							
AV_{TEC}	Voltage Sense Gain				0.25		V/V
V_{VTEC}	TEC Voltage Measurement	TEC = 4.8V,V_{LIM} = 2.5V TEC = 2.4V,V_{LIM} = 2.5V TEC = 0V,V_{LIM} = 2.5V TEC = –2.4V,V_{LIM} = 2.5V TEC = –4.8V,V_{LIM} = 2.5V			2.45 1.85 1.25 0.625 0.05		V V V V V
V_{VTEC_RANGE}	V_{TEC} Output Range			0.005		2.625	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4663 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4663E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4663I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

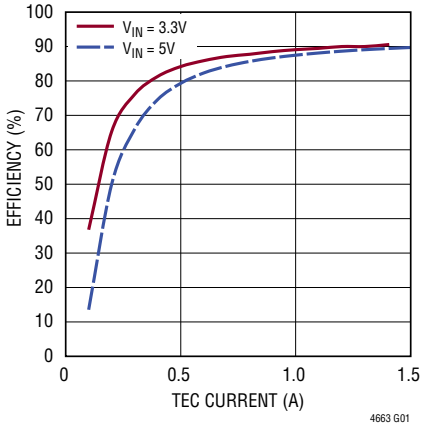
Note 3: 100% tested at wafer level.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

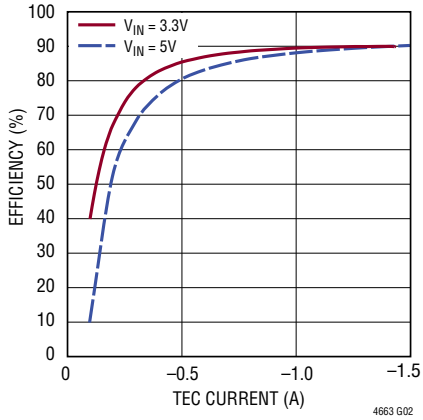
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

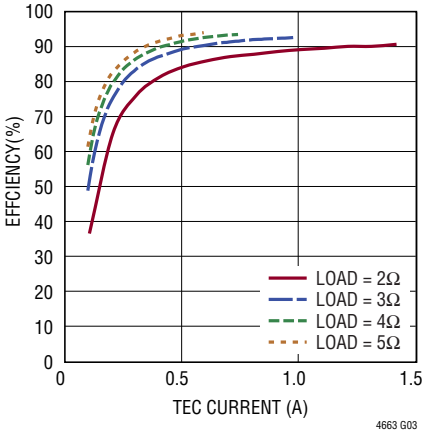
Efficiency vs TEC Current at V_{IN} = 3.3V and 5V in Cooling Mode with 2Ω Load



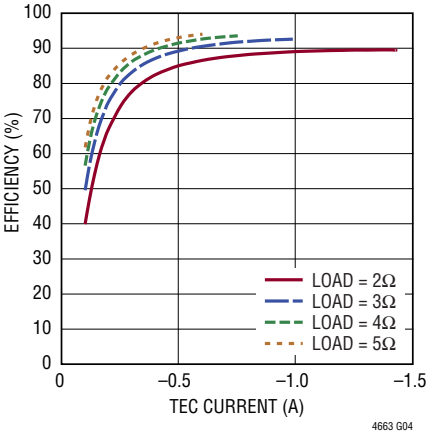
Efficiency vs TEC Current at V_{IN} = 3.3V and 5V in Heating Mode with 2Ω Load



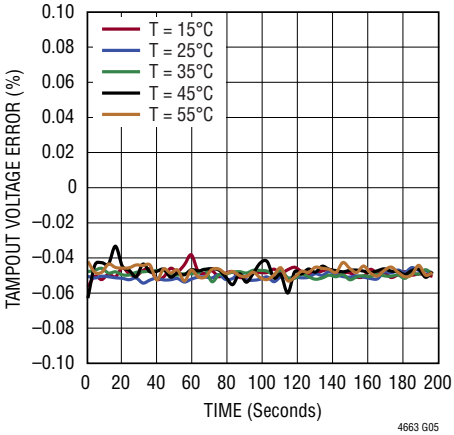
Efficiency vs TEC Current at V_{IN} = 3.3V with Different Loads in Cooling Mode



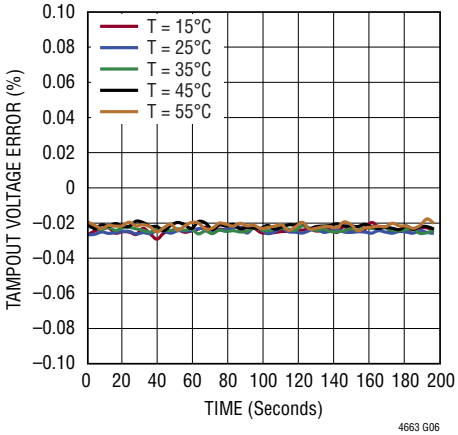
Efficiency vs TEC Current at V_{IN} = 3.3V with Different Loads in Heating Mode



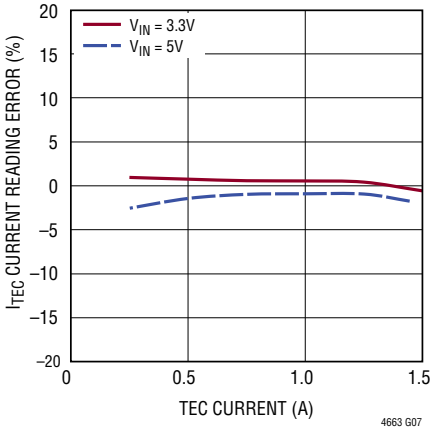
Thermal Stability over Ambient Temperature at V_{IN} = 3.3V, T_{SET} = 1 V



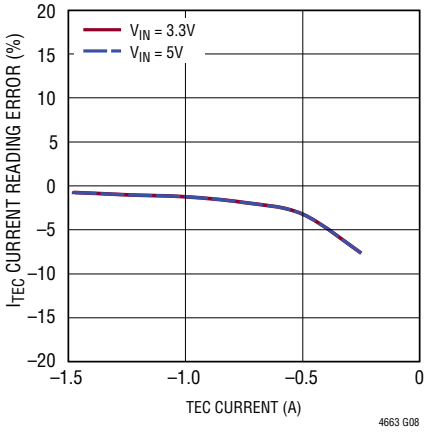
Thermal Stability over Ambient Temperature at V_{IN} = 3.3V, T_{SET} = 1.5 V



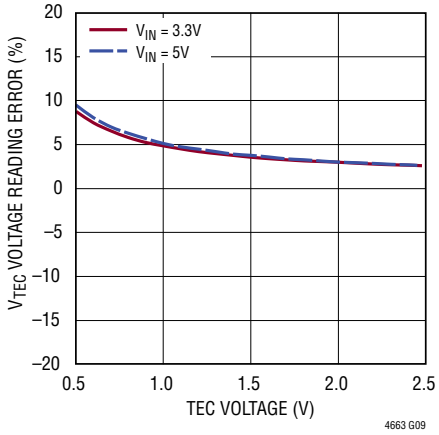
I_{TEC} Current Reading Error vs TEC Current in Cooling Mode



I_{TEC} Current Reading Error vs TEC Current in Heating Mode



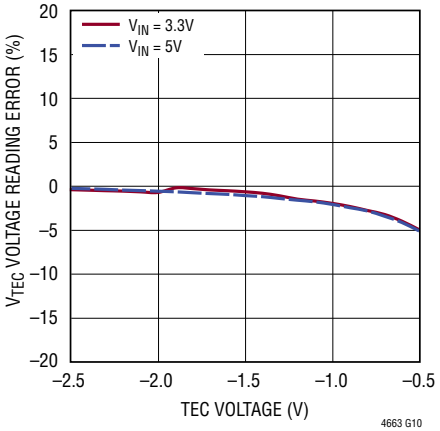
V_{TEC} Voltage Reading Error vs TEC Voltage in Cooling Mode



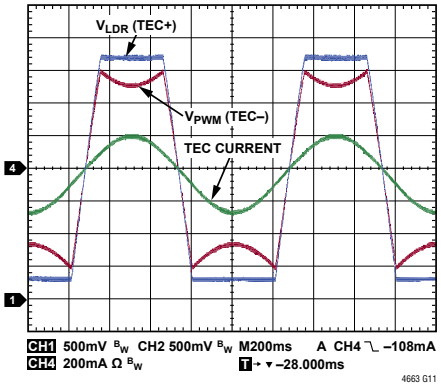
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

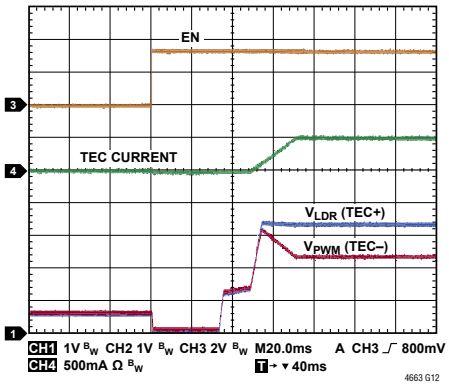
V_{TEC} Voltage Reading Error vs TEC Voltage in Heating Mode



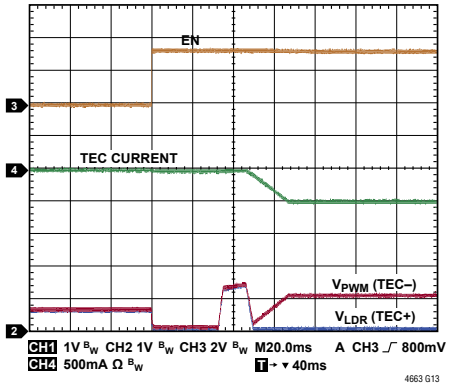
Cooling/Heating Mode Transition



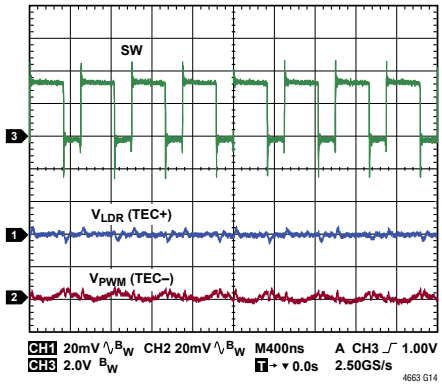
Typical Enable Waveforms in Cooling Mode, V_{IN} = 3.3 V, Load = 2Ω, TEC Current = 0.5A



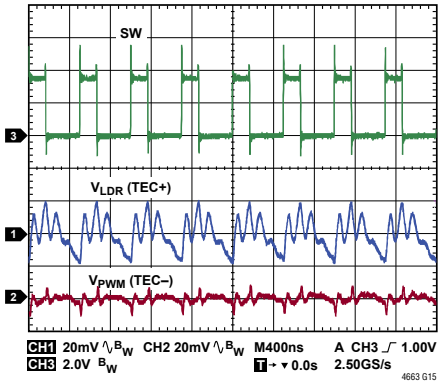
Typical Enable Waveforms in Heating Mode, V_{IN} = 3.3V, Load = 2Ω, TEC Current = –0.5A



Typical Switch and Voltage Ripple Waveforms in Heating Mode, V_{IN} = 3.3V, Load = 2Ω, TEC Current = –1A



Typical Switch and Voltage Ripple Waveforms in Cooling Mode V_{IN} = 3.3V, Load = 2Ω, TEC Current = 1A



PIN FUNCTIONS

GNDP (A1): Power Ground Pin for PWM Switching Mode Regulator. Connect to GNDL with large PCB copper area.

SW (A2, B2): Switching node of the PWM Switching Mode Regulator that is used for testing purposes. R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating.

PV_{IN} (A3, B3): Power Input Pins for Both PWM Switching Mode Regulator and Linear Power Stage. Apply input voltage between these pins and GNDP/GNDL pins. Recommend placing input decoupling capacitance directly between PV_{IN} pins and GNDP pins.

V_{LDR} (A4, B4): Linear Power Output Pin. Apply the TEC device between V_{PWM} pin and V_{LDR} pin.

GNDL (A5, B5): Power Ground Pin for Linear Power Stage. Connect to GNDP with large PCB copper area.

V_{PWM} (B1): PWM Switching Mode Regulator Power Output Pin. Apply the TEC device between V_{PWM} pin and V_{LDR} pin. Recommend placing output decoupling capacitance directly between V_{PWM} pins and GNDP pins.

SFB (C1): PWM Switching Mode Regulator Voltage Feedback Pin. Connect this pin close to the TEC device.

V_{TEC} (C2): Voltage Monitor Pin for the TEC device.

I_{TEC} (C3): Current Monitor Pin for the TEC device.

T_{FB} (C4): Temperature Feedback Pin. Connect this pin to the thermistor input. This is connected to the inverting input of the thermistor temperature error amplifier. See the Applications Information section for details.

TAMPOUT (C5): Output of the Thermistor Temperature Error Amplifier.

GNDA (D1): Signal Ground Pin for the Internal Control Circuits. Return ground path of all analog circuitry. Tie a single connection to the GNDP/GNDL in the application. See layout guidelines in Figure 17.

EN/SY (D2): Enable and External Synchronization Input of the TEC Driver. Set this pin logic high to enable the device. An external synchronization clock input can be applied to this pin.

PAMPOUT (D3): Output of the Compensation Amplifier.

PAMPN (D4): Inverting Input of the Compensation Amplifier.

NC (D5): Pin used for testing purposes. Leave floating. Do not connect.

V_{REF} (E1): 2.5V Internal Reference Output Voltage. This pin is internal decoupled with 0.1µF capacitor. No additional decoupling is required.

SV_{IN} (E2): Signal V_{IN}. Filtered Input Voltage to the Internal Control Circuits. Connect to PV_{IN} directly in most applications.

I_{LIM} (E3): Current Limit Set Pin. An external resistor divider R_{CT}/R_{CB} between V_{REF} and GNDA sets the TEC driver cooling and heating current limits. See the Applications Information section for details.

$V_{LIM/SD}$ (E4): Voltage Limit Set Pin. An external resistor between this pin and GNDA sets the TEC driver cooling and heating voltage limits. See the Applications Information section for details.

T_{SET} (E5): Temperature Set Pin for the TEC Driver. This pin is the non-inverting input of the compensation amplifier. The T_{SET} voltage controls the target temperature of the thermistor, by either sinking or sourcing current from the TEC device.

BLOCK DIAGRAM

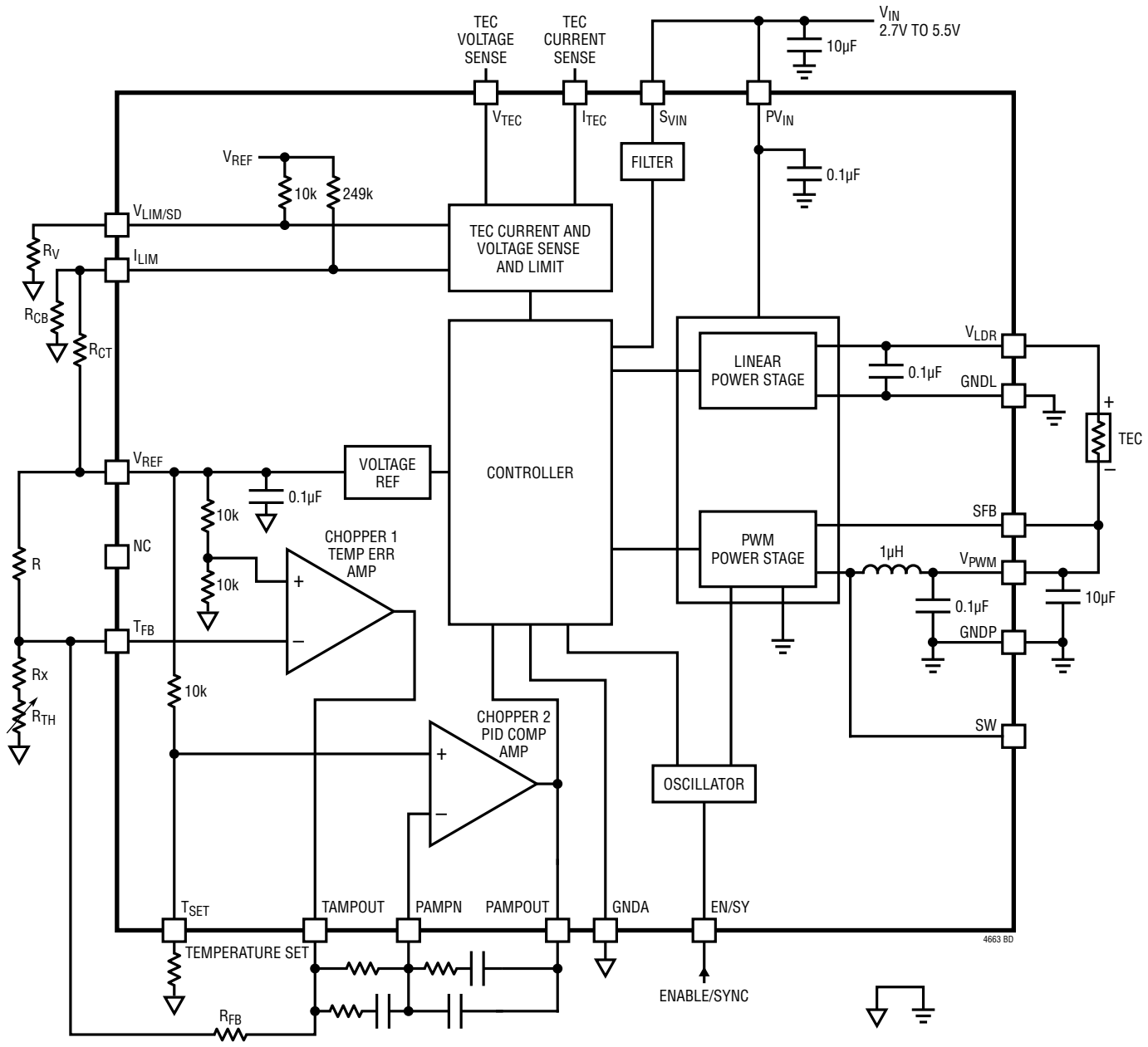


Figure 1. Simplified LTM4663 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement	PV_{IN} to GNDP		10		µF
C_{OUT}	External Output Capacitor Requirement	V_{PWM} to GNDP		10		µF

OPERATION

The LTM4663 is a complete Thermoelectric Cooler (TEC) µModule regulator that sets, stabilizes and monitors TEC temperature. It can deliver up to 1.5A of sinking or sourcing current with external input and output capacitors. Operating over 2.7V to 5.5V input voltage range, the LTM4663 controls an internal FET H-bridge whereby the direction of the current fed through the TEC can be either positive (for cooling mode), or negative (for heating mode).

The LTM4663 has two self-correcting, auto-zeroing amplifiers(Chopper 1 and Chopper 2) to linearize the thermal sensor input and to form an analog temperature feedback control loop. With the zero drift chopper amplifiers, extremely good long-term temperature stability is maintained via an autonomous temperature control loop. See Figure 18 for an overview of how to configure the analog PID control, while see Figure 19 for configuring the digital PID control.

The LTM4663 can also be configured for use in a software controlled PID loop. In this scenario, the Chopper 1 amplifier can configure as a thermistor input amplifier connected to an external temperature measurement analog-to-digital converter (ADC). The Chopper 2 amplifier is used as a buffer for the external digital-to-analog converter (DAC), which controls the temperature setpoint. Connect the DAC to T_{SET} and short the PAMPN and PAMPOUT pins together. See Figure 19 for an overview of how to configure the LTM4463 external circuitry for digital PID control.

To provide good efficiency and small solution size, the LTM4663 utilizes a PWM switching mode power supply on one side of the H-bridge while a linear power stage on the other side. A default 2MHz switching frequency and a 10µF capacitor maintains less than 1% of the worst-case output voltage ripple across the TEC.

The maximum voltage across the TEC and the current flowing through the TEC are set by using the $V_{LIM/SD}$ and I_{LIM} pins. The maximum cooling and heating currents can be set independently to allow asymmetric cooling and heating limits. The real time TEC voltage and current can be monitored using V_{TEC} and I_{TEC} pins.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The LTM4663 has two half-bridge type power stages, a PWM switching mode regulator and a linear power stage, to allow current flow in or out of the TEC device connected in between (see Figure 2).

The object temperature is measured from an external thermal sensor. The sensed temperature (voltage) is fed back to the LTM4663 at T_{FB} pin to complete a closed thermal control loop. The thermistor input amplifier gains the thermistor sensed voltage, then outputs to the PID compensation amplifier. The PID compensation amplifier then compensates a feedback loop response to drive both the PWM switching mode regulator and the linear power stage to drive the TEC to heat up or cool down the object.

INPUT AND OUTPUT DECOUPLING CAPACITORS

Benefiting from the unique topology and the 2MHz default switching frequency, only one ceramic capacitor is required at the input and output of the PWM switching regulator to maintain less than 1% of the worst-case output voltage ripple across the TEC. Additional output filtering may be required by the system designer if further reduction of output ripples or dynamic transient spikes is required.

ENABLE AND SHUTDOWN

To enable the LTM4663, apply a logic high voltage to the EN/SY pin while the voltage at the $V_{LIM/SD}$ pin is above the maximum shutdown threshold of 0.07V. If either the EN/SY pin voltage is set to logic low or the $V_{LIM/SD}$ voltage is

APPLICATIONS INFORMATION

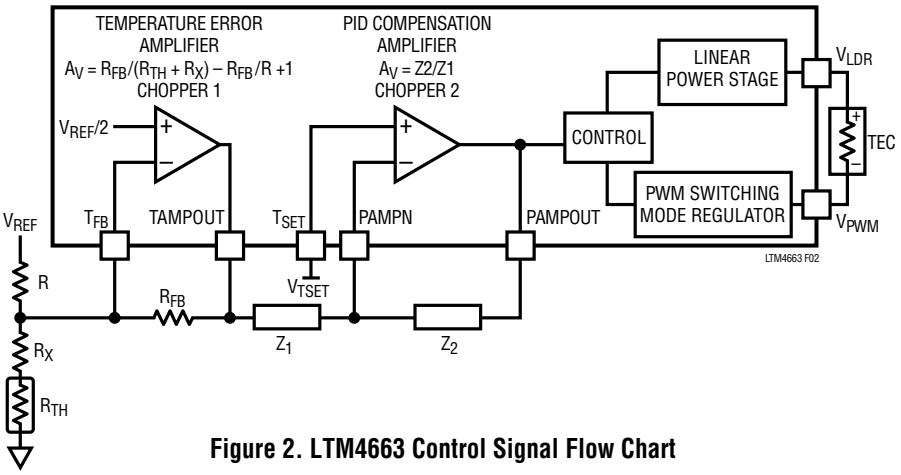


Figure 2. LTM4663 Control Signal Flow Chart

below 0.07V, the controller goes into an ultralow current state. The current drawn in shutdown mode is 480µA typically. Most of the current is consumed by the V_{REF} circuit block, which is always on even when the device is disabled or shut down. The device can also be enabled when an external synchronization clock signal is applied to the EN/SY pin, and the voltage at $V_{LIM/SD}$ input is above 0.07V. Table 1 shows the combinations of the two input signals that are required to enable the LTM4663.

Table 1. Enable Pin Combinations

EN/SY PIN	$V_{LIM/SD}$ PIN	STATUS
>2.1V	>0.07V	Enable
Clock	>0.07V	Enable
<0.8V	No Effect*	Shutdown
No Effect*	<0.07V	Shutdown

*No effect means this signal has no effect in shutting down or in enabling the device.

OPERATING FREQUENCY

The LTM4663 has a default 2MHz switching frequency for the PWM switching regulator output stage. The oscillator is active when the enabled voltage at the EN/SY pin is set to a logic level higher than 2.1V and the $V_{LIM/SD}$ pin voltage is greater than the shutdown threshold of 0.07V.

FREQUENCY SYNCHRONIZATION AND CLOCK IN

The switching frequency of the LTM4663 can be synchronized to an external clock from 1.85MHz to 3.25MHz applied to the EN/SY input pin. The clock high level must be above 2.1V and the clock low level below 0.8V.

SOFT-START

The LTM4663 has an internal soft-start circuit that generates a ramp with a typical 150ms profile to minimize inrush current during power-up. The settling time and the final voltage across the TEC depends on the TEC voltage required by the control voltage of voltage loop. The higher the TEC voltage is, the longer it requires to reach the final output voltage.

When the LTM4663 is first powered up, the linear side discharges the output of any prebias voltage. As soon as the prebias is eliminated, the soft-start cycle begins. During the soft-start cycle, both the PWM and linear outputs track the internal soft-start ramp until they reach mid-scale V_B. From the mid-scale voltage, the PWM and linear outputs are then diverge from each other until the required differential voltage is developed across the TEC or the differential voltage reaches the voltage limit. The voltage developed across the TEC depends on the control point at that moment. Figure 3 shows an example of the soft-start in cooling mode. Note that, as both the V_{LDR} and V_{PWM} voltages increase with the soft-start ramp and approach V_B, the ramp slows down to avoid possible current overshoot at the point where the TEC voltage starts to build up.

APPLICATIONS INFORMATION

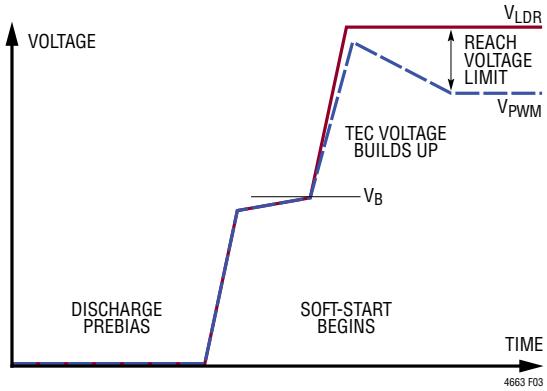


Figure 3. Soft-Start Profile in Cooling Mode

MAXIMUM TEC VOLTAGE LIMIT

The maximum voltage of the TEC driver in the LTM4663 can be programmed individually by applying a resistor (R_V) from $V_{LIM/SD}$ pin to GNDA. The voltage limiter operates bidirectionally and allows the cooling limit to be different from the heating limit.

As shown in Figure 4, the internal current sink circuitry connected to $V_{LIM/SD}$ draws a current when the LTM4663 drives the TEC in a heating direction, which lowers the voltage at $V_{LIM/SD}$. The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

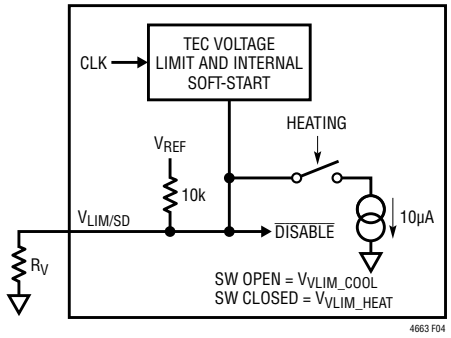


Figure 4. TEC Voltage Limit Setting

The maximum TEC voltage in the cooling mode can be calculated as:

$$V_{LIM\_COOL} = 2 \bullet 2.5V \bullet \frac{R_V}{10k + R_V}$$

The maximum TEC voltage in the heating mode can be calculated as:

$$V_{LIM\_HEAT} = 2 \bullet \left(2.5V \bullet \frac{R_V}{10k + R_V} - 10\mu A \bullet \frac{10k \bullet R_V}{10k + R_V} \right)$$

See Table 2 for the list of Typical TEC Voltage Limit settings.

Table 2. Example of Typical TEC Voltage Limit Setting

BOTTOM RESISTOR R_V (kΩ)	MAX TEC VOLTAGE (COOLING MODE) (V)	MAX TEC VOLTAGE (HEATING MODE) (V)
OPEN	5	–4.8
90.9	4.5	–4.32
40.2	4	–3.84
23.2	3.5	–3.35
15	3	–2.88
10	2.5	–2.4
6.65	2	–1.92
4.22	1.5	–1.42
2.49	1	–0.96

APPLICATIONS INFORMATION

MAXIMUM TEC CURRENT LIMIT

The maximum current of the TEC driver in the LTM4663 can be programmed individually by applying a resistor divider R_{CT}/R_{CB} between V_{REF} and GNDA.

As shown in Figure 5, the internal current sink circuitry connected to I_{LIM} draws a 40µA current when the LTM4663 drives the TEC in a cooling direction, which allows a high cooling current. The current sink is not active when the TEC is driven in a heating direction.

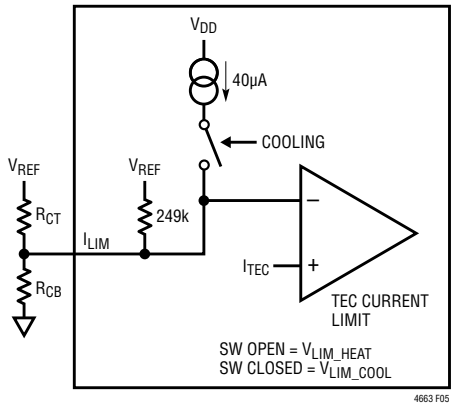


Figure 5. TEC Current Limit Setting

The maximum TEC current limit in the heating mode can be calculated as:

$$I_{LIM\_HEAT} = \frac{1.25V - 2.5V \bullet \frac{R_{CB}}{R_{CT}//249k + R_{CB}}}{0.535}$$

The maximum TEC current limit in the cooling mode can be calculated as:

$$I_{LIM\_COOL} = \frac{2.5V \bullet \frac{R_{CB}}{R_{CT}//249k + R_{CB}} + 40\mu A \bullet \frac{R_{CT}//249k \bullet R_{CB}}{R_{CT}//249k + R_{CB}} - 1.25V}{0.535}$$

See Figure 3 for the list of Typical TEC Current Limit settings.

Table 3. Example of Typical TEC Current Limit Setting

TOP RESISTOR R_{CT} (kΩ)	BOTTOM RESISTOR R_{CB} (kΩ)	TEC CURRENT LIMIT (COOLING MODE) (A)	TEC CURRENT LIMIT (HEATING MODE) (A)
OPEN	49.9	1.5	–1.5
316	43.2	1.2	–1.2
140	37.4	1	–1
63.4	28	0.7	–0.7
38.3	21.5	0.5	–0.5

APPLICATIONS INFORMATION

TEC VOLTAGE MONITOR

V_{TEC} is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center V_{TEC} voltage of 1.25V corresponds to 0V across the TEC. Convert the voltage at V_{TEC} and the voltage across the TEC using the following equation:

$$V_{VTEC} = 1.25V + 0.25 \bullet (V_{LDR} - V_{PWM})$$

TEC CURRENT MONITOR

I_{TEC} is an analog voltage output pin with a voltage proportional to the actual current through TEC. A center I_{TEC} voltage of 1.25V corresponds to 0A through the TEC. Convert the voltage at I_{TEC} and the current through the TEC using the following equations:

$$V_{ITEC\_COOLING} = 1.25V + I_{LDR} \bullet R_{CS}$$

$$V_{ITEC\_HEATING} = 1.25V - I_{LDR} \bullet R_{CS}$$

where the current sense gain R_{CS} is 0.535V/A.

THERMISTOR SETUP

The thermistor has a nonlinear relationship to temperature; near optimal linearity over a specified temperature range can be achieved with the proper value of R_X placed in series with the thermistor.

First, the thermistor resistances at different temperatures must be known, where:

$R_{LOW} = R_{TH}$ at T_{LOW}

$R_{MID} = R_{TH}$ at T_{MID}

$R_{HIGH} = R_{TH}$ at T_{HIGH}

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. In some cases, with only the thermistor material constant β available, calculate R_{TH} using the following equation:

$$R_{TH} = R_R \exp\left[\beta\left(\frac{1}{T} - \frac{1}{T_R}\right)\right]$$

where:

R_{TH} is a thermistor resistance at temperature T (K).

R_R is a nominal thermistor resistance at standard reference temperature T_R (K).

Calculate R_X using the following equation:

$$R_X = \left(\frac{R_{LOW}R_{MID} + R_{MID}R_{HIGH} - 2R_{LOW}R_{HIGH}}{R_{LOW} + R_{HIGH} - 2R_{MID}}\right)$$

THERMISTOR AMPLIFIER

The Chopper 1 amplifier can be used as a thermistor input amplifier. In Figure 6, the output voltage is a function of the thermistor temperature. The voltage at TAMPOUT is expressed as:

$$V_{TAMPOUT} = \left(\frac{R_{FB}}{R_{TH} + R_X} - \frac{R_{FB}}{R} + 1\right) \bullet \frac{V_{REF}}{2}$$

where:

R_{TH} is a thermistor resistance at a certain temperature.

R_X is a compensation resistor.

The Chopper 1 amplifier should be optimized according to the temperature range for each application to gain better voltage-to-temperature linearity and temperature setting resolution. To center the $V_{TAMPOUT}$ vs Temperature curve around TMID, calculate R using the following equation:

$$R = R_X + R_{MID}$$

Figure 6 shows a $V_{TAMPOUT}$ vs Temperature curve, where $V_{TAMPOUT}$ is centered around $V_{REF}/2$ at 25°C. The average temperature-to-voltage coefficient is 25mV/°C at a range of 5°C to 45°C.

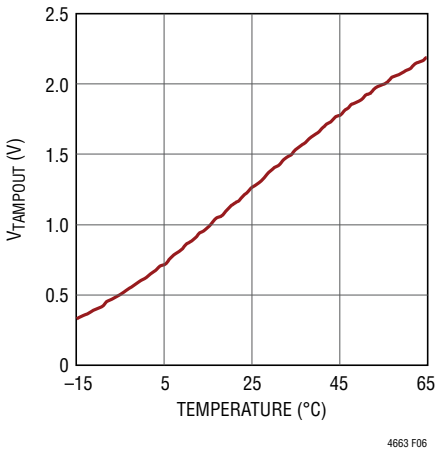


Figure 6. $V_{TAMPOUT}$ vs Temperature

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PID COMPENSATION AMPLIFIER

Use the Chopper 2 amplifier as the PID compensation amplifier. The voltage at TAMPOUT feeds into the PID compensation amplifier. The frequency response is dictated by the compensation network. Apply the temperature set voltage at T_{SET}. In Figure 7, the voltage at PAMPOUT is calculated using the following equation:

$$V_{PAMPOUT} = V_{TSET} - \frac{Z2}{Z1}\left(V_{TAMPOUT} - V_{TSET}\right)$$

where:

V_{TSET} is the control voltage input to the T_{SET} pin. V_{TSET} sets the object target temperature. Take Figure 6 for an example, 1.25V T_{SET} voltage setting maintains a 25°C target temperature for the object; 0.75V T_{SET} voltage setting cools down the object to 5°C; and 1.75V T_{SET} voltage setting heats up the object to 45°C.

Z1 is the impedence of R_I, R_D, and C_D (see Figure 7).

Z2 is the impedence of R_P, C_I, and C_F (see Figure 7).

The user sets the exact compensation network. This network varies from a simple integrator to proportional-integral (PI), PID (proportional-integral-derivative), or any other type of network. The user also determines the type of compensation and component values because they are dependent on the thermal response of the object and the TEC. One method to empirically determine these values is to input a step function to T_{SET}; thus changing the target temperature, and adjust the compensation network to minimize the settling time of the TEC temperature.

A typical compensation network for temperature control of a laser module is a PID loop consisting of a very low frequency pole and two separate zeros at higher frequencies. Figure 7 shows a simple network for implementing PID compensation. To reduce the noise sensitivity of the control loop, an additional pole is added at a higher frequency than that of the zeros. The bode plot of the magnitude is shown in Figure 8.

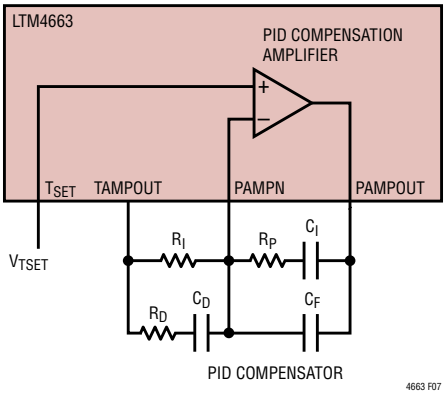

Figure 7. Analog PID Compensation Network

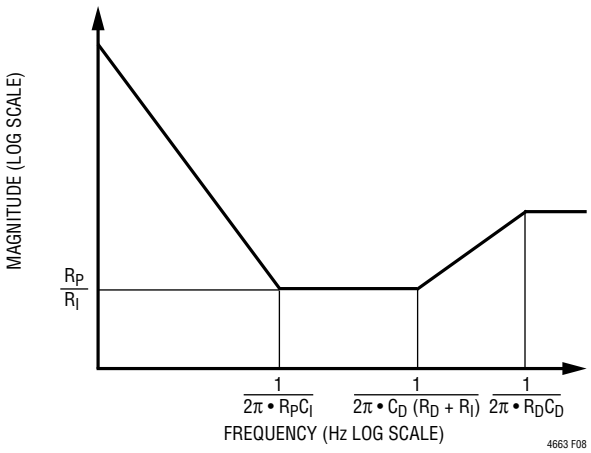

Figure 8. Bode Plot for PID Compensation

To ensure stability, the crossover frequency must be lower than the thermal time constant of the TEC and thermistor. There are many texts written on loop stabilization, and it is beyond the scope of this data sheet to discuss all methods and trade-offs for optimizing compensation networks.

TAMPOUT is a convenient measure to gauge the thermal instability of the system. If the thermal loop is in steady state, the TAMPOUT voltage equals the T_{SET} voltage, meaning that the temperature of the controlled object equals the target temperature.

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Switching Mode and Linear Power Stages

The output of the PID compensation amplifier signal (PAMPOUT) will be used to drive both a switching mode regulator and a linear power stage to form a positive or negative voltage across the TEC device connected in between. Figure 9 shows the relationship between PAMPOUT voltage and the differential voltage of V_{LDR}-V_{PWM} which is the voltage applied at TEC device.

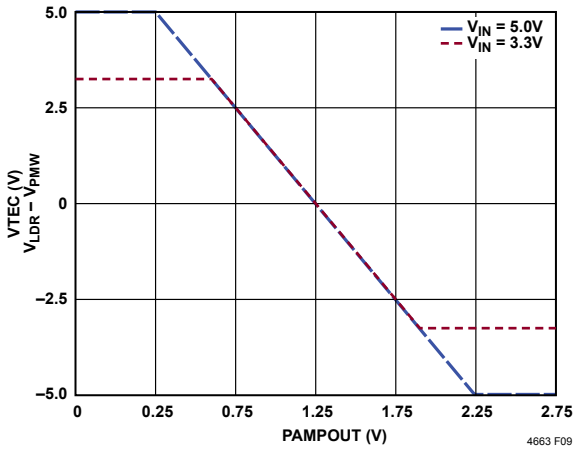

Figure 9. TEC Voltage vs PAMPOUT Voltage

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients in found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal

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resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two-layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 10; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or subgroup of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule regulator—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The power loss curves in Figure 11 and Figure 12 can be used in coordination with the load current derating curves in Figure 13 to Figure 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4663. The power loss

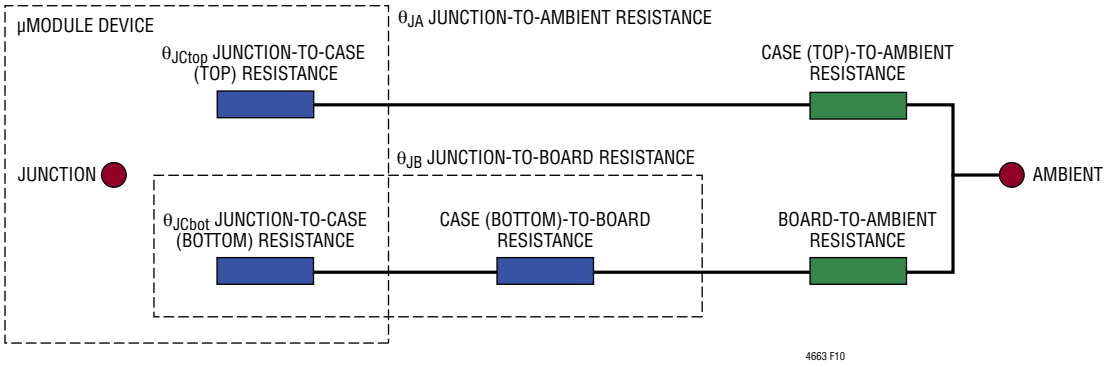

Figure 10. Graphical Representation of JESD 51-12 Thermal Coefficients

APPLICATIONS INFORMATION (R_L = 2Ω Load)

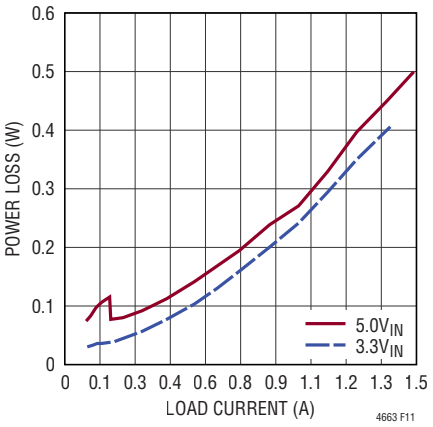

Figure 11. Cooling Mode Power Loss for 3.3V and 5V Input

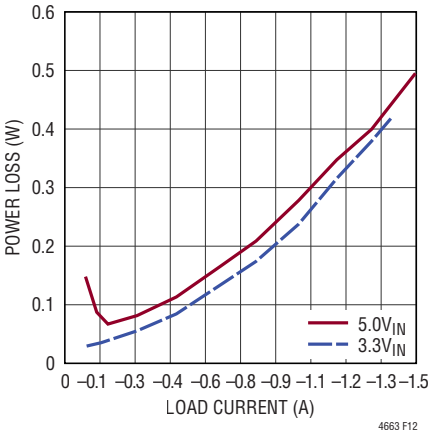

Figure 12. Heating Mode Power Loss for 3.3V and 5V Input

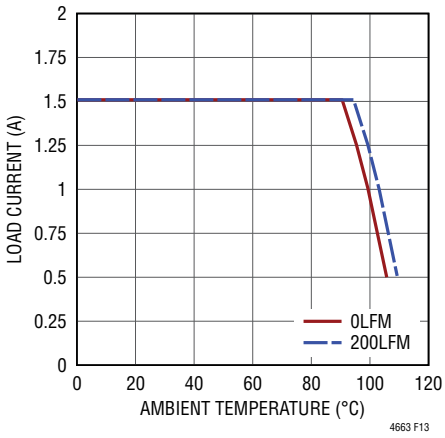

Figure 13. 5V Input, Derating Curve, Cooling Mode

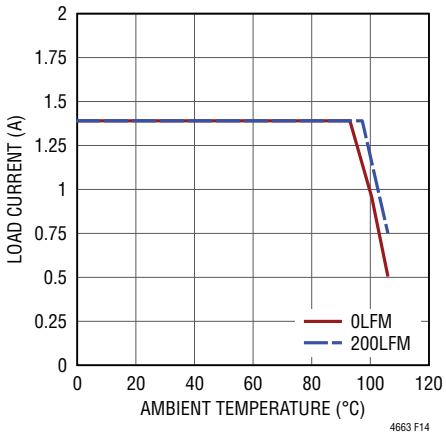

Figure 14. 3.3V Input, Derating Curve, Cooling Mode

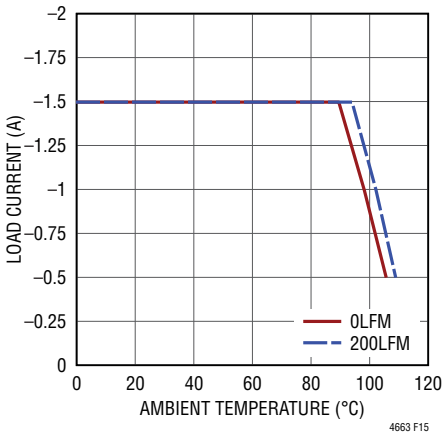

Figure 15. 5V Input, Derating Curve, Heating Mode

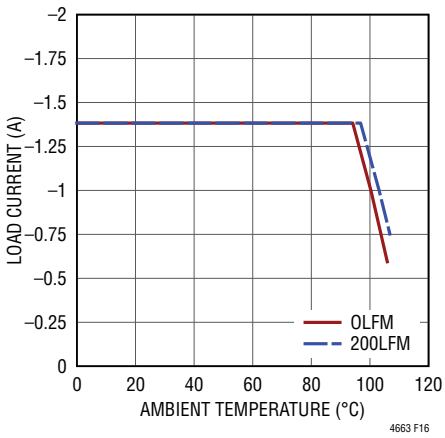

Figure 16. 3.3V Input, Derating Curve, Heating Mode

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curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. These approximate factor is 1.1 assuming at 110°C junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 110°C, which is a 15°C guard band from maximum junction temperature of 125°C. The derating curves are plotted with the output current up to 1.5A and the ambient temperature at 90°C. The resistive load is set to be 2Ω for both cooling and heating modes, and the input voltage is chosen from 3.3V and 5V. These are chosen to include the lower and higher input and load ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 110°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 110°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 13, the ambient temperate is derated to 90°C at 1.5A of load current with no air to prevent the junction temperature exceeding 110°C. Figure 11 shows that the cooling mode power loss for the $5V_{IN}$ to 1.5A is 0.5W, and the 1.1 multiplying factor would make the total power loss to be 0.55W. If the 90°C ambient temperature is subtracted from the 110°C junction temperature, then the difference of 20°C divided by 0.55W equals a 36.3°C/W for θ_{JA} thermal resistance. Table 4 specifies a 36°C/W value which is very close.

Table 4 and Table 5 provide equivalent thermal resistances with and without airflow. The derived thermal resistances for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four-layer board with two-ounce copper for the two outer layers and one-ounce copper for the two inner layers. The PCB dimensions are 90mm × 75mm.

Table 4. 2Ω Cooling Mode

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	θ_{JA} (°C/W)
Figure 13, Figure 14	3.3, 5	Figure 11	0	36
Figure 13, Figure 14	3.3, 5	Figure 11	200	27

Table 5. 2Ω Heating Mode

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	θ_{JA} (°C/W)
Figure 15, Figure 16	3.3, 5	Figure 12	0	36
Figure 15, Figure 16	3.3, 5	Figure 12	200	27

APPLICATIONS INFORMATION

SAFETY CONSIDERATIONS

The LTM4663 module does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4663 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including PV_{IN}, GND, V_{PWM} and V_{LDR}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the PV_{IN}, PGND and V_{PWM} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Use a separated GNDA ground copper area for components connected to signal pins. Connect the GNDA to GNDP and GNDL underneath the unit.

Figure 17 gives a good example of the recommended layout.

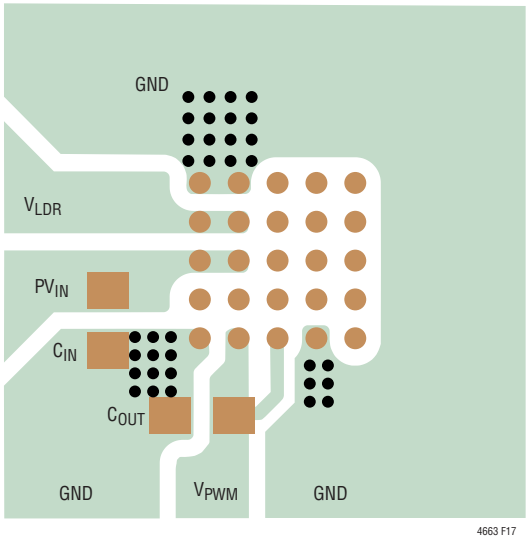


Figure 17. Recommended PCB Layout

TYPICAL APPLICATIONS

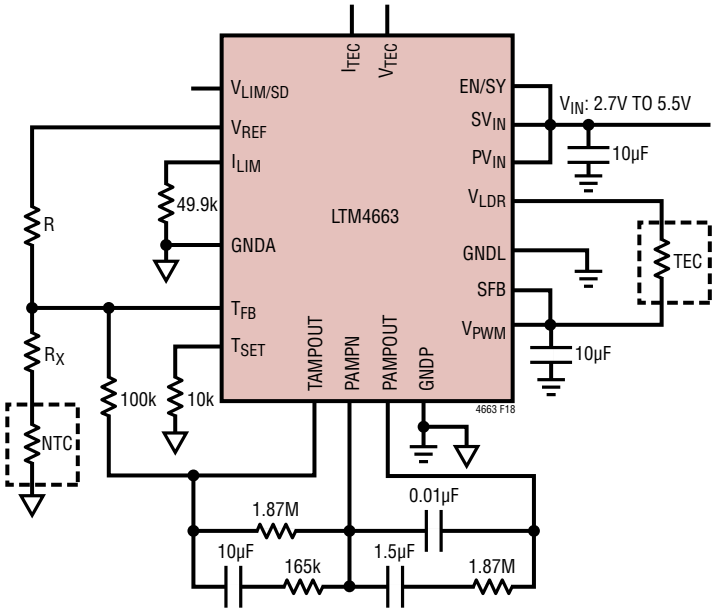


Figure 18. 2.7V to 5.5V Input, ±1.5A TEC Driver Circuit with Analog PID Compensation in a Temperature Control Loop

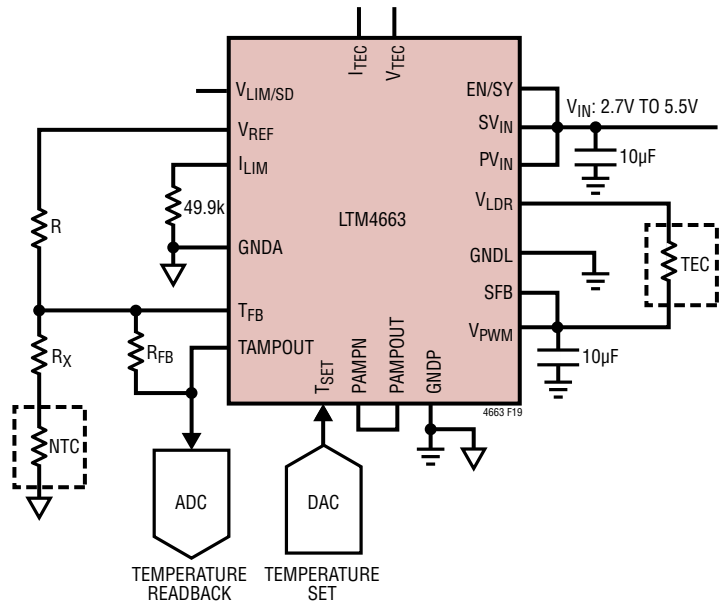


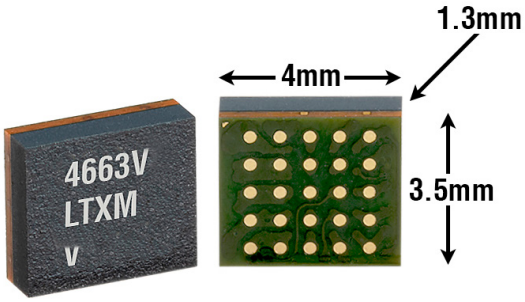
Figure 19. 2.7V to 5.5V Input, ±1.5A TEC Driver Circuit in a Digital Temperature Control Loop

PACKAGE DESCRIPTION

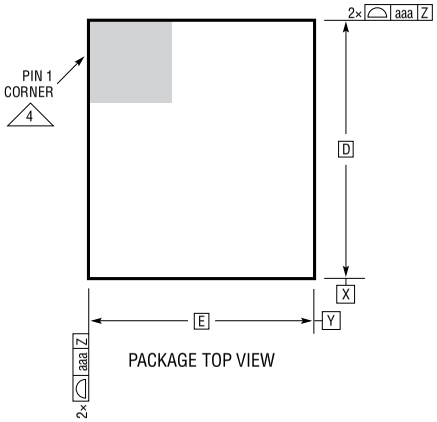
LTM4663 Component LGA Pinout

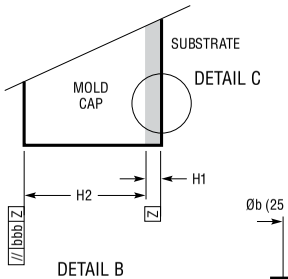
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GNDP	B1	V_{PWM}	C1	SFB	D1	GNDA	E1	V_{REF}
A2	SW	B2	SW	C2	V_{TEC}	D2	EN/SY	E2	SV_{IN}
A3	PV_{IN}	B3	PV_{IN}	C3	I_{TEC}	D3	PAMPOUT	E3	I_{LIM}
A4	V_{LDR}	B4	V_{LDR}	C4	T_{FB}	D4	PAMPN	E4	$V_{LIM/SD}$
A5	GNDL	B5	GNDL	C5	TAMPOUT	D5	NC	E5	T_{SET}

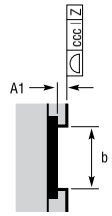
PACKAGE PHOTO

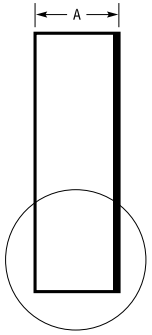


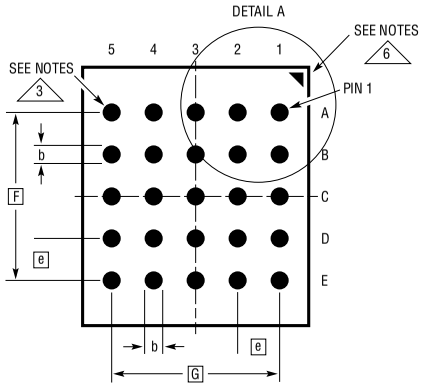
LGA Package
25-Lead (4mm × 3.5mm × 1.3mm)
(Reference LTC DWG# 05-08-1785 Rev Ø)

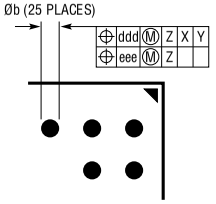




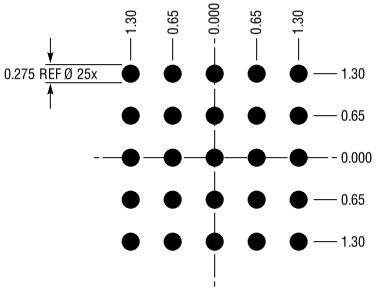




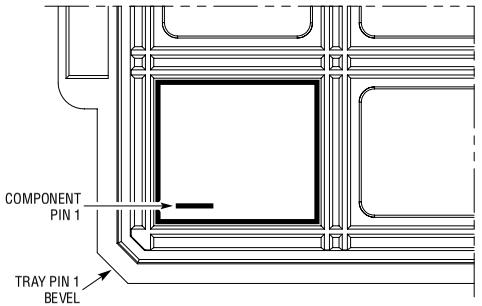




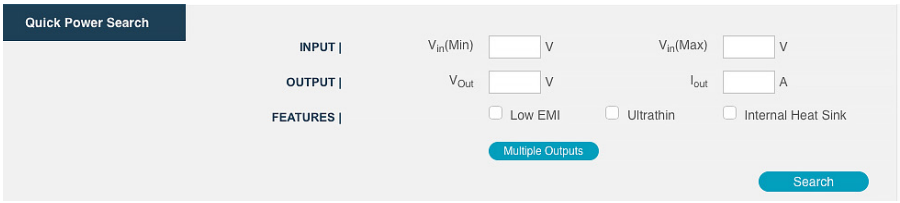
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.28	1.34	1.40	
A1	0.015	0.025	0.035	
b	0.25	0.28	0.31	PAD DIMENSION
D		4.00		
E		3.50		
e		0.65		
F		2.60		
G		2.60		
H1		0.47 REF		SUBSTRATE THK
H2		0.87 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF PADS: 25				



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4691	Ultrathin, Dual 2A Step-Down µModule Regulator	2.25V ≤ V_{IN} ≤ 3.6V, 0.5V ≤ V_{OUT} ≤ 2.5V, 3mm × 4mm × 1.18mm LGA
LTM4668/LTM4668A	Quad 1.2A Step-Down µModule Regulator	2.7V ≤ V_{IN} ≤ 17V, 0.6V ≤ V_{OUT} ≤ 1.8V (LTM4668A: 0.6V ≤ V_{OUT} ≤ 5.5V, 2.25MHz) 6.25mm × 6.25mm × 2.1mm BGA
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4622A	Ultrathin, Dual 2A or Single 4A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 1.5V ≤ V_{OUT} ≤ 12V, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4623	Ultrathin, Single 3A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4625	Single 5A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 5.01mm BG
LTM4664	54V_{IN} Dual 25A, Single 50A µModule Regulator with Digital Power System Management	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA